LM5006 80V, 600 mA Constant On-Time Buck Switching Regulator

Check for Samples: LM5006

FEATURES

- **Operating Input Voltage Range: 6V to 75V**
- **Integrated 80V, N-Channel Buck Switch**
- **Internal Start-Up Regulator**
- **No Loop Compensation Required**
- **Ultra-Fast Transient Response**
- **Operating Frequency Remains Constant with Line and Load Variations**
- **Adjustable Output Voltage from 2.5V**
- **Precision Internal Reference, ±2.5%**
- **Intelligent Current Limit Reduces Foldback**
- **Programmable Input UV Detector with Status Flag Output**
- **Gate Output Driver for Synchronous Rectifier**
- **Pre-Charge Switch Enables Bootstrap Gate Drive with no Load**
- **Thermal Shutdown**

TYPICAL APPLICATIONS

- **Non-Isolated Telecommunication Buck Regulator**
- **Secondary High Voltage Post Regulator**
- **+42V Automotive Systems**

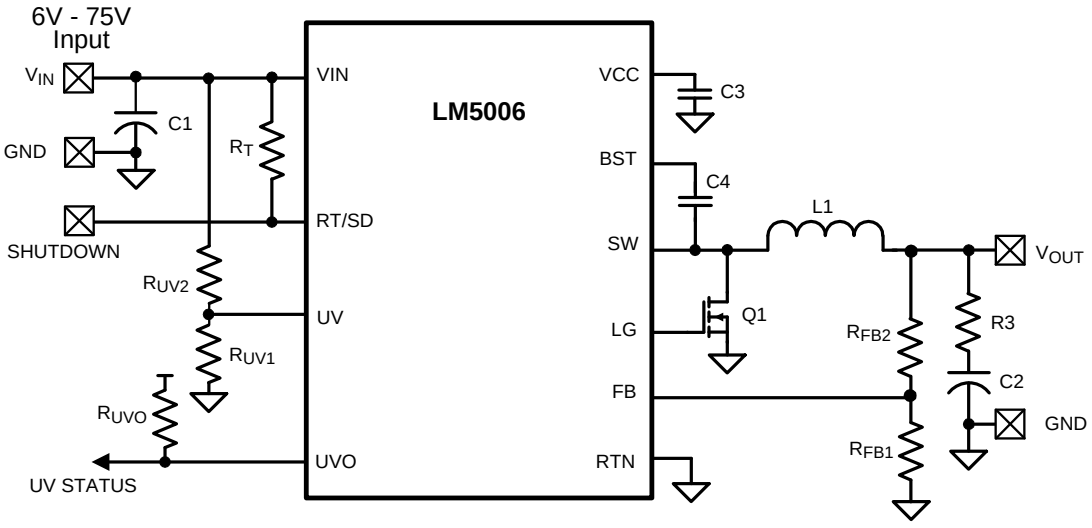
PACKAGE

- **VSSOP - 10**

DESCRIPTION

The LM5006 Step Down Switching Regulator features all of the functions needed to implement a low cost, efficient Buck bias regulator. This high voltage regulator contains an 80V N-Channel MOSFET Switch and a startup regulator. The device is easy to implement and is provided in an VSSOP-10 package. The regulator's control scheme uses an on-time inversely proportional to V_{IN}. This feature results in the operating frequency remaining relatively constant with line and load variations. The control scheme requires no loop compensation, resulting in fast transient response. An intelligent current limit is implemented with a forced off-time which is inversely proportional to V_{OUT}. This scheme ensures short circuit control while providing minimum foldback. Other features include: Thermal Shutdown, VCC Under Voltage Lock-out, Max Duty Cycle Limiter, a Pre-charge Switch, a programmable Under Voltage Detector with a status flag output, and a gate driver output for a synchronous rectifier.

Typical Application, Basic Step-Down Regulator



Connection Diagram

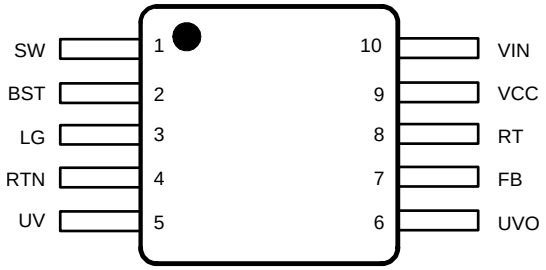


Figure 1. Top View
10–Lead VSSOP

PIN DESCRIPTIONS

Pin	Name	Description	Application Information
1	SW	Switching Node	Power switching node. Connect to the output inductor, re-circulating diode or synchronous FET, and bootstrap capacitor.
2	BST	Boost Pin	An external capacitor is required between the BST and the SW pins (0.01uF or greater ceramic). The BST pin capacitor is charged from Vcc through an internal diode when SW is low.
3	LG	Low side gate driver output for synchronous rectifier MOSFET	This output drives an external N-MOSFET which can replace the free-wheeling diode between SW and GND. Using a FET for synchronous rectification generally improves efficiency.
4	RTN	Ground pin	Ground for the entire circuit.
5	UV	Input pin for the under voltage indicator	A resistor divider from VIN, or some other system voltage, programs the under-voltage detection threshold. An internal current sink is enabled when UV is below 2.5V to provide hysteresis.
6	UVO	Under voltage status indicator	This open drain output is high when the UV pin voltage is below 2.5V, or when the VCC_{UVLO} function or the shutdown function is invoked.
7	FB	Feedback Input from Regulated Output	This pin is connected to the inverting input of the internal regulation comparator. The regulation level is 2.5V.
8	RT/SD	On-time set pin and shutdown input	A resistor between this pin and Vin sets the switch on-time as a function of Vin, and the frequency. The minimum recommended on-time is 200 ns at max input voltage. Taking this pin to ground shuts off the regulator.
9	VCC	Output from the internal high voltage series pass regulator. Regulated at 7.5V.	The internal regulator provides bias supply for the Buck switch gate driver and other internal circuitry. A 1uF ceramic capacitor to ground is required. The regulator is current limited to ≈30 mA.
10	VIN	Input Voltage	The operating input range is 6V to 75V

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

VIN, UV to RTN		-0.3V to 80V
BST to RTN		-0.3V to 88V
SW to RTN (Steady State)		-1V to V_{IN} + 0.3V
BST to VCC		80V
BST to SW		10V
VCC, LG, UVO, to RTN		–0.3V to 10V
FB, RT to RTN		-0.3 to 5V
ESD Rating	Human Body Model (3)	2kV
For soldering specs see: SNOA549C. See (4).		
Junction Temperature		150°C
Storage Temperature Range		-55°C to +150°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For specifications and test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.
(4) For detailed information on soldering plastic VSSOP packages, refer to the Packaging Data Book available from TI.

Operating Ratings (1)

V_{IN}	6V to 75V
Operating Junction Temperature	−40°C to + 125°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For specifications and test conditions, see the Electrical Characteristics.

Electrical Characteristics

Specifications with standard type are for T_J = 25°C only; limits in **boldface type** apply over the full Operating Junction Temperature (T_J) range. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: VIN = 48V (1).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VCC Supply						
Vcc Reg	Vcc Regulator Output	Vin = 48V	**7.1**	7.5	**7.9**	V
	Vin – Vcc	VIN = 6V, I_{CC} = 5mA		240		mV
	Vcc Output Impedance	Vin =6V		45		Ω
	Vcc Current Limit	Vin = 48V (2)	**20**	30		mA
	Vcc UVLO	Vcc Increasing		4	**4.8**	V
	Vcc UVLO hysteresis			450		mV
	Iin Operating current	FB = 3V, Vin = 48V		1	**1.32**	mA
	Iin Shutdown Current	RT/SD = 0V		20	**70**	µA
Switch Characteristics						
	Buckswitch Rds(on)	Itest = 200 mA		0.56	**1.1**	Ω
	Gate Drive UVLO	Vbst – Vsw Rising	**2.15**	3	**3.8**	V
	Gate Drive UVLO hysteresis			250		mV
	Pre-charge switch voltage	At 1 mA		0.8		V
	Pre-charge switch on-time			150		ns
Current Limit						
	Current Limit Threshold		**700**	1175	**1500**	mA

(1) All electrical characteristics having room temperature limits are tested during production with T_A = T_J = 25°C. All hot and cold limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) The V_{CC} output is intended as a self bias for the internal gate drive power and control circuits. Device thermal limitations limit external loading.

Electrical Characteristics (continued)

Specifications with standard type are for T_J = 25°C only; limits in **boldface type** apply over the full Operating Junction Temperature (T_J) range. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: VIN = 48V(1).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Current Limit Response Time	I_{switch} = 1.24A, Time to Switch Off		190		ns
T_{OFF-1}	OFF time generator (test 1)	FB=0V, VIN = 75V		37		µs
T_{OFF-2}	OFF time generator (test 2)	FB=2.3V, VIN = 75V		7.2		µs
T_{OFF-3}	OFF time generator (test 3)	FB=0V, VIN = 10V		5.7		µs
T_{OFF-4}	OFF time generator (test 4)	FB=2.3V, VIN = 10V		1.25		µs
On Time Generator						
T_{ON} - 1	On-Time	Vin = 10V Ron = 250K	**2.2**	3.3	**4.51**	µs
T_{ON} - 2	On-Time	Vin = 75V Ron = 250K	**300**	450	**565**	ns
	Remote Shutdown Threshold	Voltage at RT/SD rising	**0.46**	0.9	**1.4**	V
	Remote Shutdown Hysteresis			60		mV
Minimum Off Time						
	Minimum Off Time	VIN = 6V		260	**347**	ns
Regulation and OV Comparators						
	FB Reference Threshold	Internal reference Trip point for switch ON	**2.4365**	2.5	**2.5625**	V
	FB Over-Voltage Threshold	Trip point for switch OFF		2.85		V
	FB Bias Current			1		nA
Under Voltage Sensing						
UV_{TH}	UV Threshold		**2.4**	2.5	**2.6**	V
UV_{HYS}	UV Hysteresis Current	UV = 2V	**2.7**	5	**7.3**	uA
UV_{BIAS}	UV Bias Current	UV = 3V		1		nA
UVO_{VOL}	UVO Output Low Voltage	UV = 3V, I_{UVO} = 5mA		360	**600**	mV
UVO_{IOH}	UVO Leakage Current	UV = 2V, V_{UVO} = 7.8V		1		nA
LG Output						
$V_{LG(LO)}$	LG Low Voltage	Sink Current = 10mA		0.11	**0.25**	V
$V_{LG(HI)}$	LG High Voltage	Source Current = 10mA	**VCC –0.55**	VCC –0.275		V
t_{SWLG}	SW Low to LG High Deadtime			56		ns
t_{LGSW}	LG Low to SW High Deadtime			58		ns
R_{LG}	Driver Output Resistance	Sink Current =10mA		15		Ω
		Source Current = 10mA		28		
Thermal Shutdown						
Tsd	Thermal Shutdown Temp.			165		°C
	Thermal Shutdown Hysteresis			20		°C
Thermal Resistance						
θ_{JA}	Junction to Ambient	DGS Package		200		°C/W

Typical Performance Characteristics

Efficiency at 300 kHz, 10V

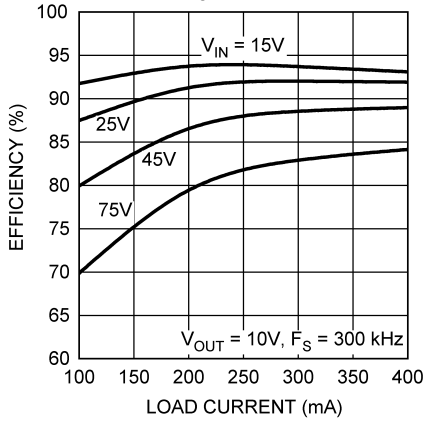


Figure 2.

Efficiency Comparison at 200 kHz

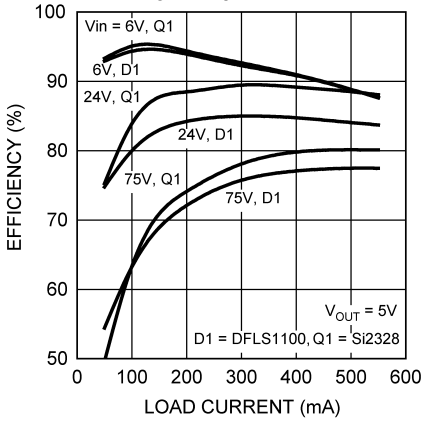


Figure 3.

V_{CC} vs. V_{IN}

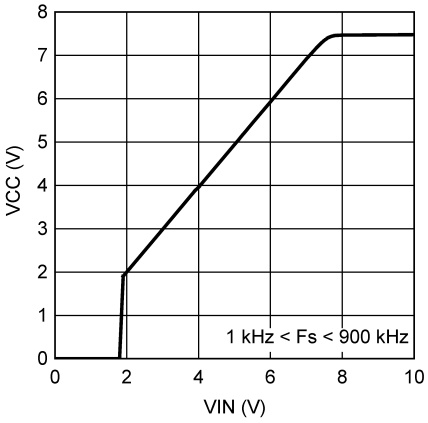


Figure 4.

V_{CC} vs. I_{CC}

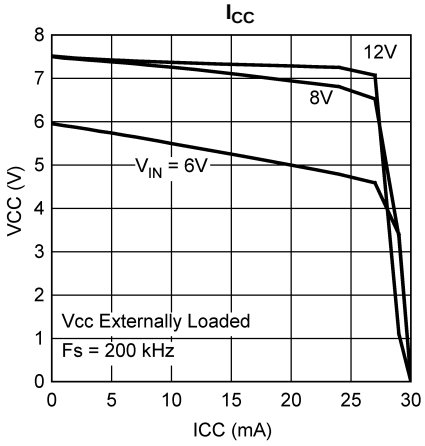


Figure 5.

I_{CC} vs. Externally Applied V_{CC}

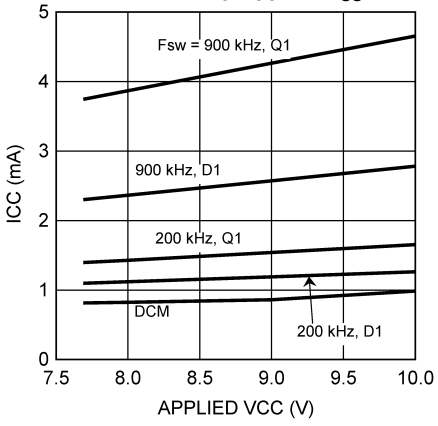


Figure 6.

On-Time vs. V_{IN} and R_T

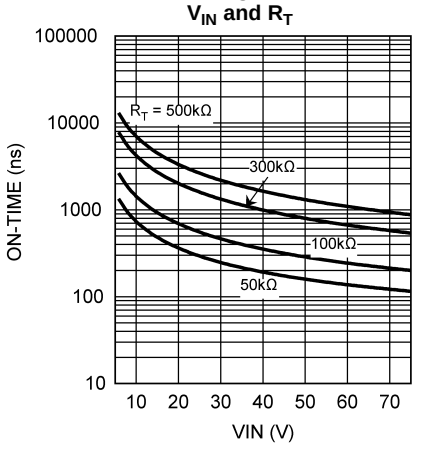


Figure 7.

Typical Performance Characteristics (continued)

Current Limit Off-Time vs. V_{FB}

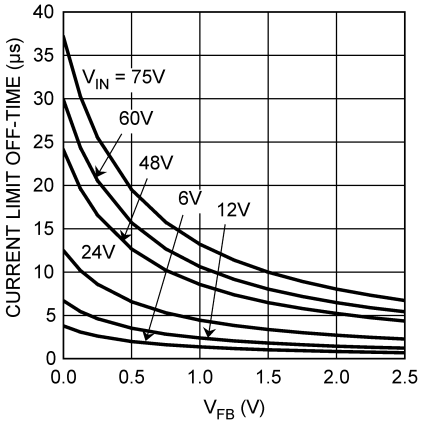


Figure 8.

Maximum Switching Frequency

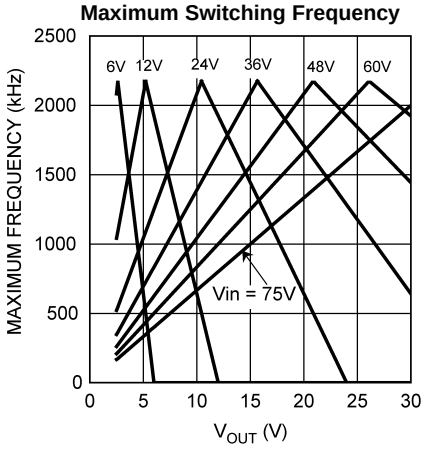


Figure 9.

Voltage at the R_T Pin

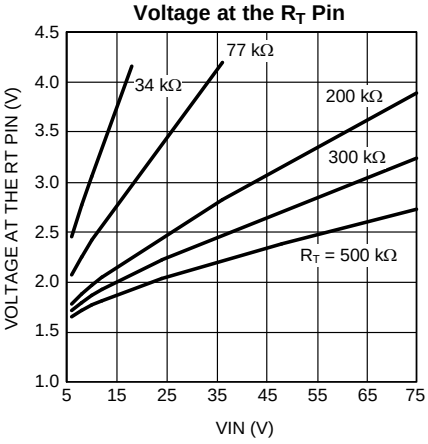


Figure 10.

Operating Current into V_{IN}

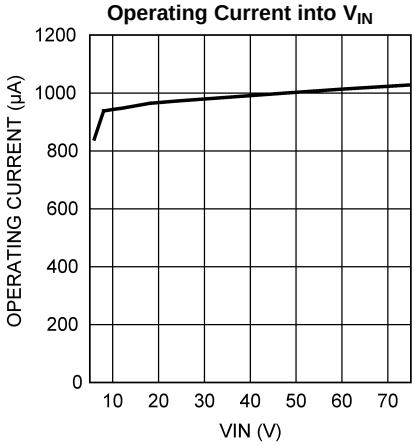


Figure 11.

Shutdown Current into V_{IN}

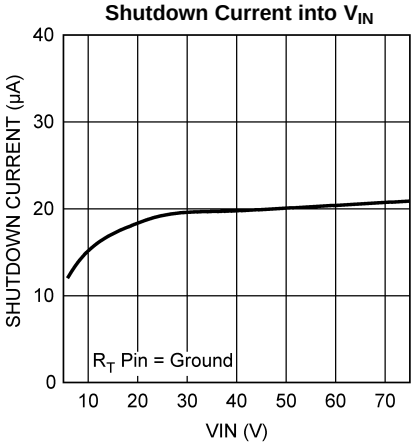


Figure 12.

UVO Pin Low Voltage vs. Sink Current

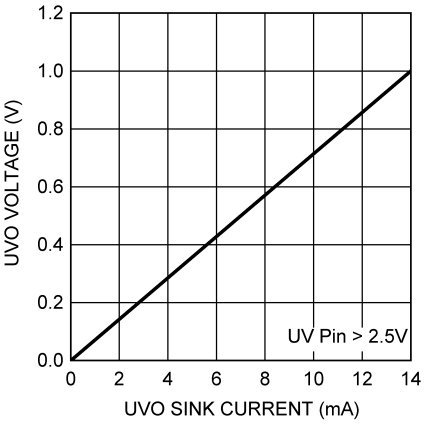


Figure 13.

Typical Performance Characteristics (continued)

LG vs. SW Deadtime

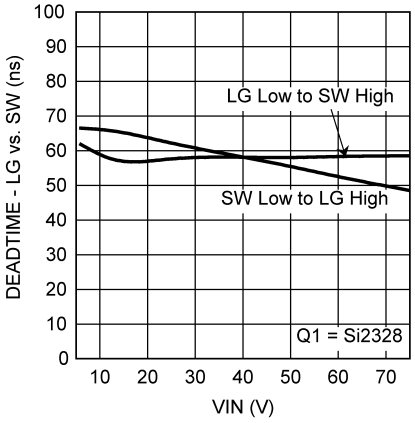


Figure 14.

V_{CC} UVLO vs. Temperature

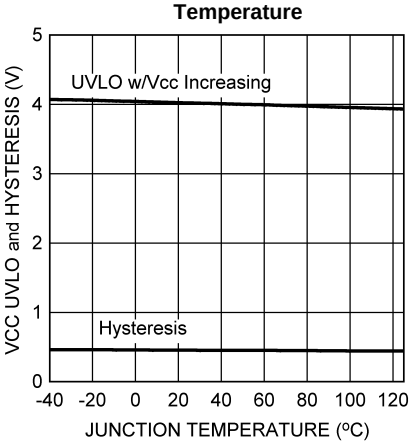


Figure 15.

Gate Drive UVLO vs. Temperature

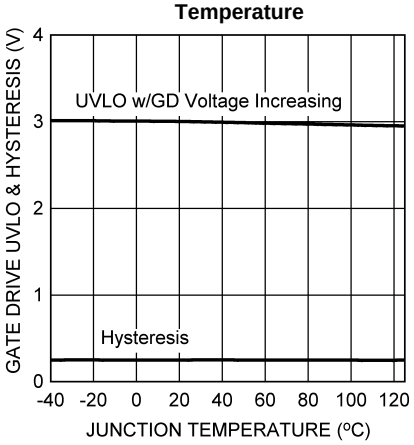


Figure 16.

V_{CC} vs. Temperature

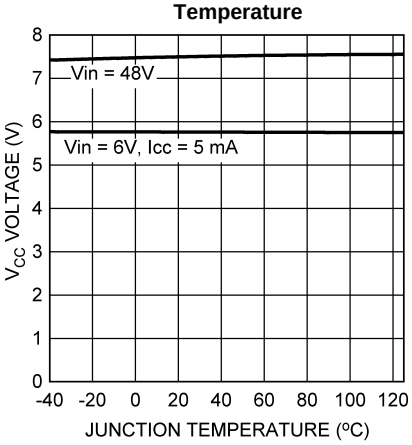


Figure 17.

V_{CC} Dropout vs. Temperature

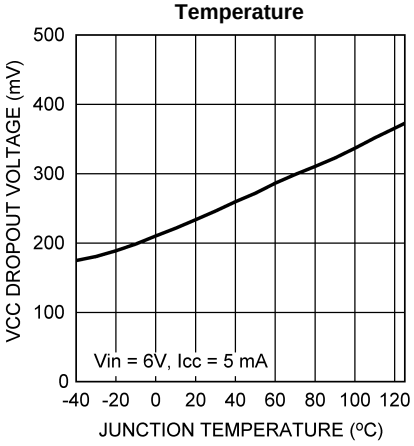


Figure 18.

V_{CC} Output Impedance vs. Temperature

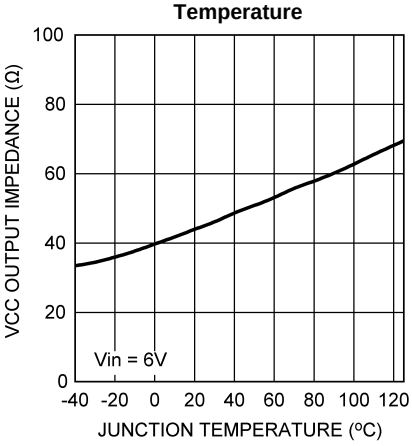


Figure 19.

Typical Performance Characteristics (continued)

V_{CC} Current Limit vs. Temperature

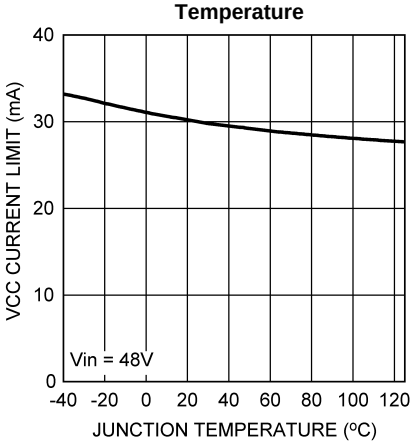


Figure 20.

Reference Voltage vs. Temperature

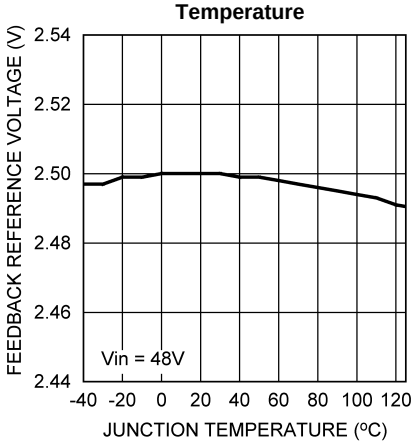


Figure 21.

On-time vs. Temperature

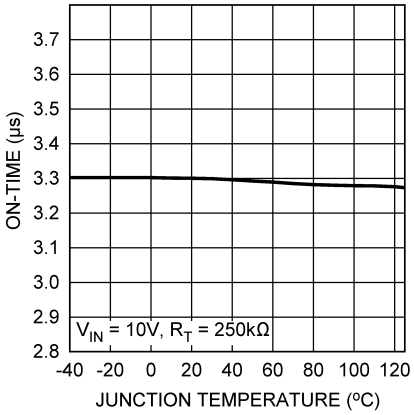


Figure 22.

Minimum Off-time vs. Temperature

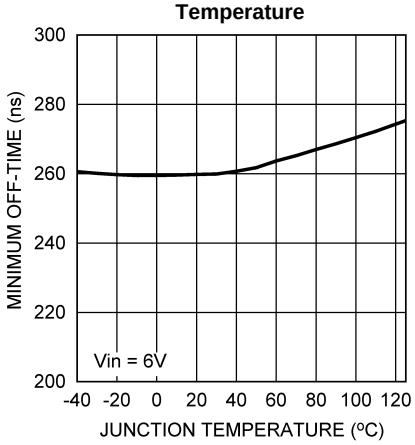


Figure 23.

Current Limit Threshold vs. Temperature

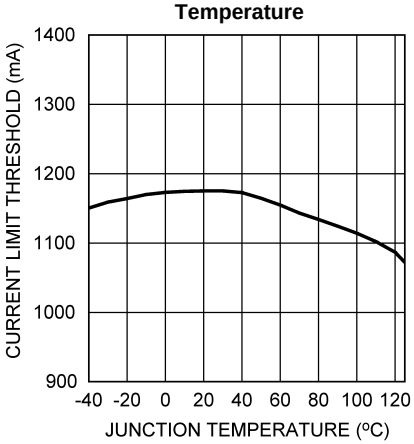


Figure 24.

Current Limit Off-Time vs. Temperature

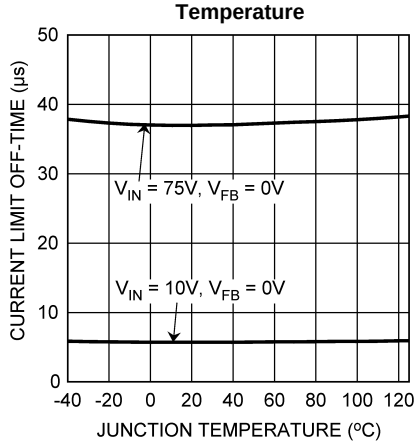


Figure 25.

Typical Performance Characteristics (continued)

Operating Current vs. Temperature

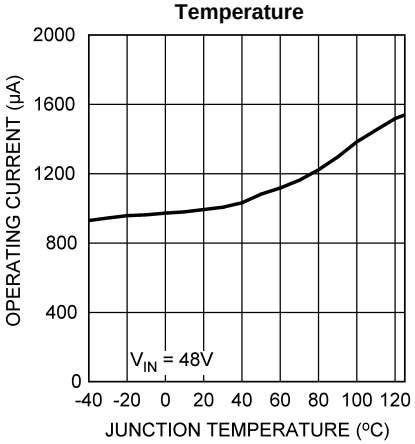


Figure 26.

Shutdown Current vs. Temperature

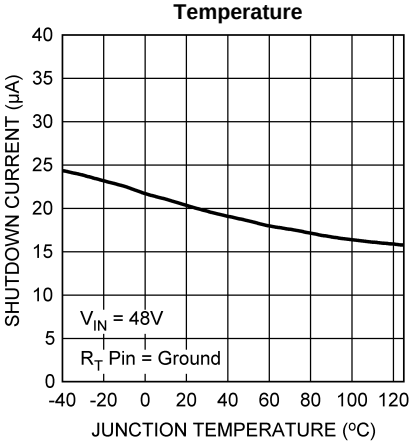


Figure 27.

RT Pin Shutdown Threshold vs. Temperature

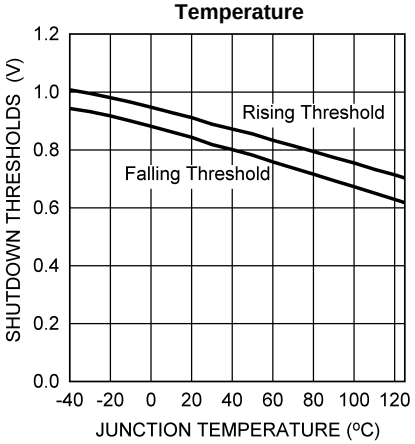


Figure 28.

LG vs. SW Deadtime vs. Temperature

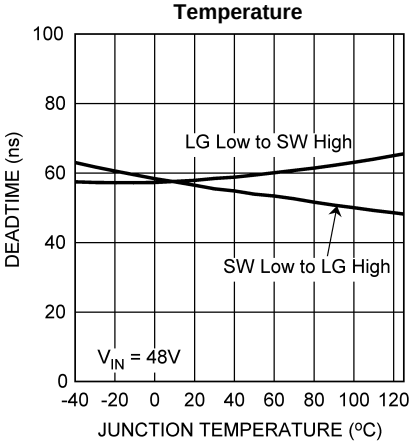


Figure 29.

UV Pin Threshold vs. Temperature

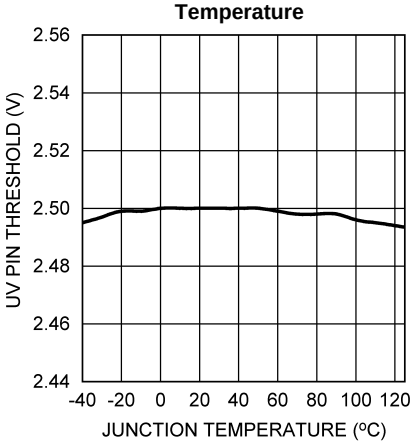


Figure 30.

UV Hysteresis Current vs. Temperature

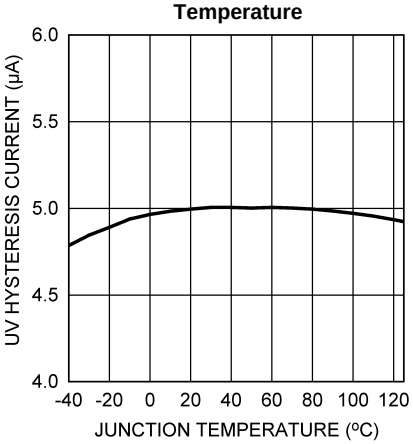
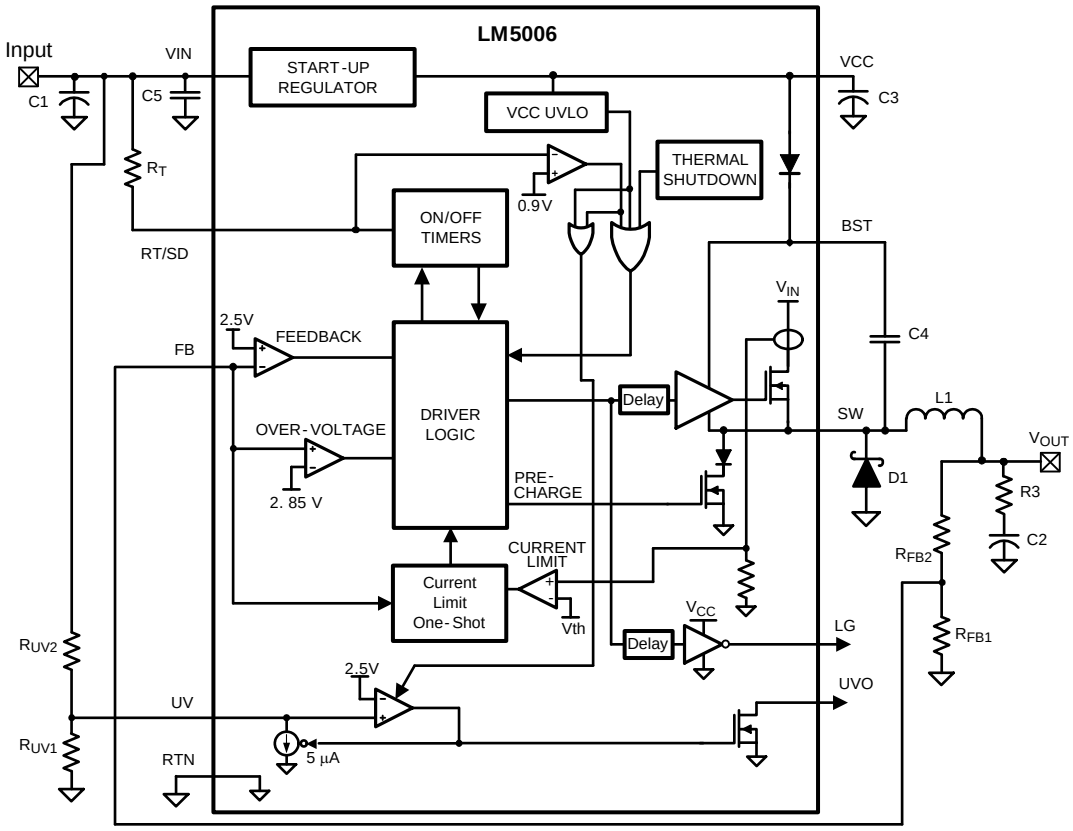


Figure 31.

Block Diagram



FUNCTIONAL DESCRIPTION

The LM5006 Step Down Switching Regulator features all the functions needed to implement a low cost, efficient, Buck bias power converter. This high voltage regulator contains an 80 V N-Channel Buck Switch, is easy to implement and is provided in the VSSOP-10 package. The regulator is based on a control scheme using an on-time inversely proportional to V_{IN}. The control scheme requires no loop compensation. Current limit is implemented with forced off-time, which is inversely proportional to V_{OUT}. This scheme ensures short circuit control while providing minimum foldback.

The LM5006 can be applied in numerous applications to efficiently regulate down higher voltages. This regulator is well suited for 48 Volt Telecom and the new 42V Automotive power bus ranges. Features include: Thermal Shutdown, V_{CC} under-voltage lockout, Gate drive under-voltage lockout, Max Duty Cycle limit timer, intelligent current limit off timer, a pre-charge switch, a programmable under voltage detector with status flag, and a gate driver output for a synchronous rectifier.

Control Circuit Overview

The LM5006 is a Buck DC-DC regulator that uses a control scheme in which the on-time varies inversely with line voltage (V_{IN}). Control is based on a comparator and the on-time one-shot, with the output voltage feedback (FB) compared to an internal reference (2.5V). If the FB level is below the reference the buck switch is turned on for a fixed time determined by the line voltage and a programming resistor (R_T). Following the ON period the switch remains off for at least the minimum off-timer period of 260 ns. If FB is still below the reference at that time the switch turns on again for another on-time period. This continues until regulation is achieved.

If the flyback diode (D1 in the Block Diagram) is used, the LM5006 operates in discontinuous conduction mode at light load currents, and continuous conduction mode at heavy load current. In discontinuous conduction mode, current through the output inductor starts at zero and ramps up to a peak during the on-time, then ramps back to zero before the end of the off-time. The next on-time period starts when the voltage at FB falls below the internal reference - until then the inductor current remains zero. In this mode the operating frequency is lower than in continuous conduction mode, and varies with load current. Therefore at light loads the conversion efficiency is maintained, since the switching losses reduce with the reduction in load and frequency. The discontinuous operating frequency can be calculated as follows:

$$F = \frac{V_{OUT}^2 \times L \times 1.28 \times 10^{20}}{R_L \times (R_T)^2} \quad (1)$$

where

- R_L = the load resistance

In continuous conduction mode, current flows continuously through the inductor and never ramps down to zero. In this mode the operating frequency is greater than the discontinuous mode frequency and remains relatively constant with load and line variations. The approximate continuous mode operating frequency can be calculated as follows:

$$F = \frac{V_{OUT} \times (V_{in} - 0.5V)}{1.25 \times 10^{-10} \times V_{IN} \times (R_T + 500\Omega)} \quad (2)$$

The buck switch duty cycle is approximately equal to:

$$DC = \frac{t_{ON}}{t_{ON} + t_{OFF}} = \frac{V_{OUT}}{V_{IN}} \quad (3)$$

If a synchronous rectifier (Q1 in the Typical Application schematic on the front page) is used instead of a flyback diode, the LM5006 operates in continuous conduction mode for all values of load current. The switching frequency remains relatively constant with load and line variations, and can be calculated using Equation 2.

The output voltage (V_{OUT}) is programmed by two external resistors as shown in the Block Diagram. The regulation point can be calculated as follows:

$$V_{OUT} = 2.5 \times (R_{FB1} + R_{FB2}) / R_{FB1} \quad (4)$$

The LM5006 regulates the output voltage based on ripple voltage at the feedback input, requiring a minimum amount of ESR for the output capacitor C2. A minimum of 25mV to 50mV of ripple voltage at the feedback pin (FB) is required for the LM5006. In cases where the capacitor ESR is too small, additional series resistance may be required (R3 in the Block Diagram).

For applications where lower output voltage ripple is required the output can be taken directly from a low ESR output capacitor, as shown in Figure 32. However, R3 slightly degrades the load regulation.

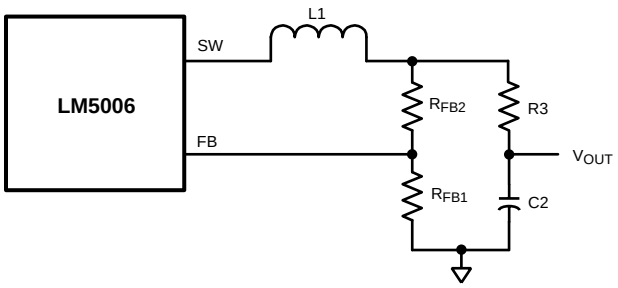


Figure 32. Low Ripple Output Configuration

Start-Up Regulator (V_{CC})

The high voltage bias regulator is integrated within the LM5006. The input pin (VIN) can be connected directly to line voltages between 6V and 75V, with transient capability to 80V. The V_{CC} output is regulated at 7.5V. The V_{CC} regulator output current is limited at approximately 30 mA.

C3 must be located as close as possible to the VCC and RTN pins. In applications with a relatively high input voltage, power dissipation in the bias regulator is a concern. An auxiliary voltage of between 7.5V and 10V can be diode connected to the VCC pin to shut off the V_{CC} regulator, thereby reducing internal power dissipation. The current required into the VCC pin depends on the voltage applied to VCC, the switching frequency, and whether a flyback diode (D1) or a synchronous rectifier (Q1) is used. See Figure 6. Internally a diode connects VCC to VIN requiring that the auxiliary voltage be less than V_{IN}.

The turn-on sequence is shown in Figure 33. During the initial delay (t1) VCC ramps up at a rate determined by its current limit and C3 while internal circuitry stabilizes. When V_{CC} reaches the upper threshold of its under-voltage lock-out, the buckswitch is enabled. The inductor current increases to the current limit threshold (I_{LIM}) and during t2 V_{OUT} increases as the output capacitor charges up. When V_{OUT} reaches the intended voltage the average inductor current decreases (t3) to the nominal load current (I_O).

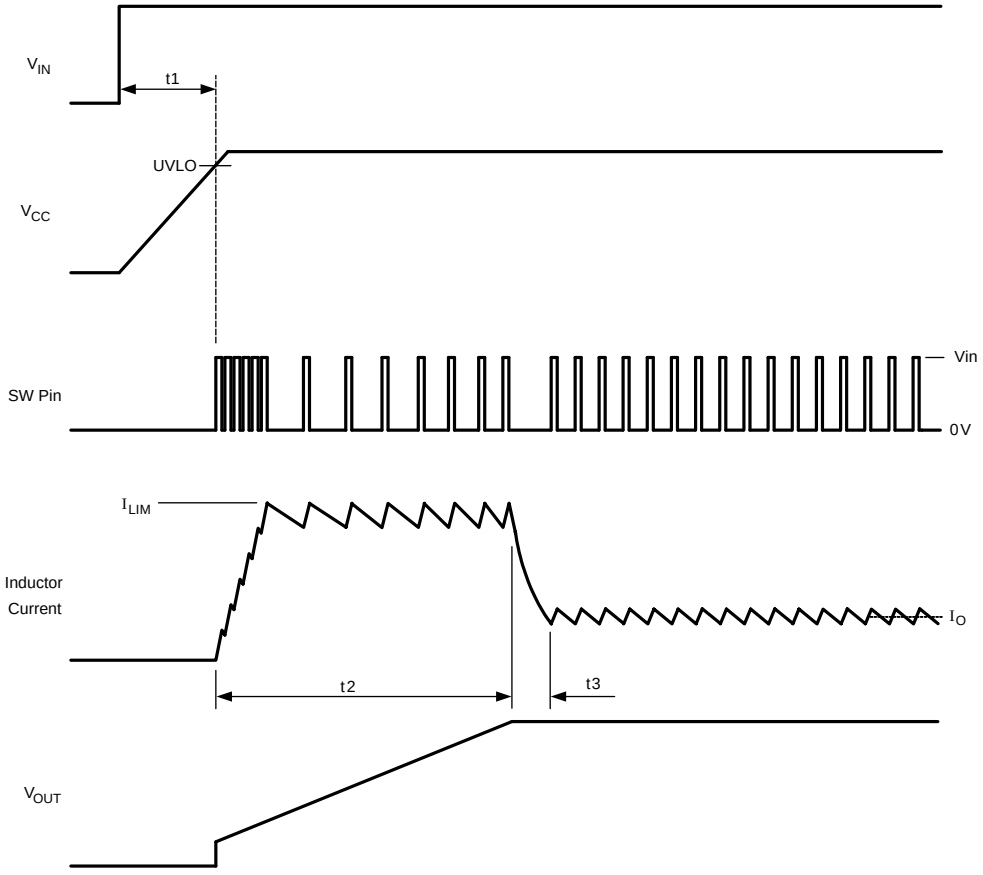


Figure 33. Startup Sequence

Regulation Comparator

The feedback voltage at FB is compared to an internal 2.5V reference. In normal operation (the output voltage is regulated), an on-time period is initiated when the voltage at FB falls below 2.5V. The buck switch stays on for the on-time, causing the FB voltage to rise above 2.5V. After the on-time period, the buck switch stays off until the FB voltage again falls below 2.5V. During start-up, the FB voltage will be below 2.5V at the end of each on-time, resulting in the minimum off-time of 260 ns.

Over-Voltage Comparator

The feedback voltage at FB is compared to an internal 2.85V reference. If the voltage at FB rises above 2.85V the on-time pulse is immediately terminated. This condition can occur if the input voltage, or the output load, change suddenly. The buck switch will not turn on again until the voltage at FB falls below 2.5V.

On-Time Generator and Shutdown

The on-time for the LM5006 is determined by the R_T resistor, and is inversely proportional to the input voltage (Vin), resulting in a nearly constant frequency as Vin is varied over its range. The on-time equation for the LM5006 is:

$$T_{ON} = \frac{1.25 \times 10^{-10} \times (R_T + 500\Omega)}{(V_{IN} - 0.5V)} + 30 \text{ ns} \quad (5)$$

R_T should be selected for a minimum on-time (at maximum V_{IN}) greater than 200 ns, for proper current limit operation. This requirement limits the maximum frequency for each application, depending on V_{IN} and V_{OUT}.

The LM5006 can be remotely disabled by taking the RT/SD pin to ground. See Figure 34. The voltage at the RT/SD pin is between 1.5 and 5.0 volts, depending on Vin and the value of the R_T resistor.

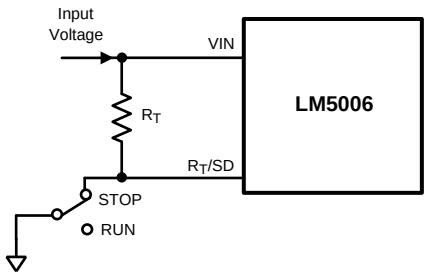


Figure 34. Shutdown Implementation

Current Limit

The LM5006 contains an intelligent current limit OFF timer. If the current in the Buck switch reaches the current limit threshold, the present cycle is immediately terminated, and a non-resetable OFF timer is triggered. The length of off-time is controlled by the FB voltage and V_{IN} (see Figure 8). When FB = 0V, a maximum off-time is required. This condition occurs when the output is shorted, and during the initial part of start-up. This amount of time ensures safe short circuit operation up to the maximum input voltage of 75V. In cases of overload where the FB voltage is above zero volts (not a short circuit) the required current limit off-time is less. Reducing the off-time during less severe overloads reduces the amount of foldback, recovery time, and the start-up time. The off-time in microseconds is calculated from the following equation:

$$T_{OFF} = \frac{(V_{IN} + 1.83V) \times 0.28}{(V_{FB} \times 1.05) + 0.58} \quad (6)$$

See Figure 8.

The current limit sensing circuit is blanked for the first 50-70 ns of each on-time so it is not falsely tripped by the current surge which occurs at turn-on. The current surge is required by the re-circulating diode (D1) for its turn-off recovery.

N - Channel Buck Switch and Driver

The LM5006 integrates an N-Channel Buck switch and associated floating high voltage gate driver. The gate driver circuit works in conjunction with an external bootstrap capacitor and an internal high voltage diode. A 0.01 µF ceramic capacitor (C4) connected between the BST pin and SW pin provides the voltage to the driver during the on-time.

During each off-time, the SW pin is at approximately 0V, and the bootstrap capacitor charges from Vcc through the internal diode. The minimum OFF timer, set to 260 ns, ensures a minimum time each cycle to recharge the bootstrap capacitor.

The internal pre-charge switch at the SW pin is turned on for ≅150 ns during the minimum off-time period, ensuring sufficient voltage exists across the bootstrap capacitor for the on-time. This feature helps prevent operating problems which can occur during very light load conditions, involving a long off-time, during which the voltage across the bootstrap capacitor could otherwise reduce below the Gate Drive UVLO threshold. The pre-charge switch also helps prevent startup problems which can occur if the output voltage is pre-charged prior to turn-on. After current limit detection, the pre-charge switch is turned on for the entire duration of the forced off-time .

LG (Low Side Gate) Output

Synchronous rectification can be implemented by replacing the flyback diode (D1 in the Block Diagram) with an N-Channel MOSFET, and connecting the MOSFET's gate to the LG output pin. See the Typical Application circuit on the front page. The LG output switches high (from ground to VCC) approximately 56 ns after the internal power buck switch turns off, and switches low approximately 58 ns before the internal power buck switch turns on.

The LG output is capable of sourcing 250 mA peak, and sinking 300 mA. An external gate driver is not needed if the selected MOSFET has a total gate charge of less than 10 nC.

The selected external MOSFET must have a V_{DS} rating greater than the maximum input system voltage (V_{IN}), plus ringing and transients which can occur at the SW pin. The MOSFET's current rating should be at least equal to the maximum current limit specification.

Use of a synchronous rectifier generally results in higher circuit efficiency due to the lower voltage drop across the MOSFET as compared to a diode. Use of a synchronous rectifier also results in continuous conduction mode operation, and therefore a constant frequency, for all load conditions. This feature allows the generation of a secondary output using a transformer winding off the main inductor. See the Applications Information section for more information.

Under Voltage Detector

The Under Voltage Detector can be used to monitor the input voltage, or any other system voltage as long as the voltage at the UV pin does not exceed its maximum rating.

The Under Voltage Output indicator pin (UVO) is connected to the drain of an internal N-channel MOSFET capable of sustaining 10V in the off-state. An external pull-up resistor is required at UVO to an appropriate voltage to indicate the status to downstream circuitry. The off-state voltage at the UVO pin can be higher or lower than the voltage at VIN, but must not exceed 10V.

The UVO pin switches low when the voltage at the UV input pin is above its threshold. Typically the monitored voltage threshold is set with a resistor divider (R_{UV1}, R_{UV2}) as shown in the Block Diagram. When the voltage at the UV pin is below its threshold, the internal 5 µA current source at UV is enabled. As the input voltage increases, taking UV above its threshold, the current source is disabled, raising the voltage at UV to provide threshold hysteresis.

The UVO output is high when the VCC voltage is below its UVLO threshold, or when the LM5006 is shutdown using the RT/SD pin (see Figure 34), regardless of the voltage at the UV pin.

Thermal Protection

The LM5006 should be operated so the junction temperature does not exceed 125°C during normal operation. An internal Thermal Shutdown circuit is provided to shutdown the LM5006 in the event of a higher than normal junction temperature. When activated, typically at 165°C, the controller is forced into a low power reset state by disabling the buck switch. This feature prevents catastrophic failures from accidental device overheating. When the junction temperature reduces below 145°C (typical hysteresis = 20°C) normal operation is resumed.

Applications Information

SELECTION OF EXTERNAL COMPONENTS

A guide for determining the component values is illustrated with a design example. Refer to the Block Diagram. The following steps will configure the LM5006 for:

- Input voltage range (Vin): 15V to 75V
- Output voltage (V_{OUT}): 10V
- Load current (for continuous conduction mode): 100 mA to 400 mA
- Switching Frequency: 300 kHz

R_{FB1}, R_{FB2}: $V_{OUT} = V_{FB} \times (R_{FB1} + R_{FB2}) / R_{FB1}$ and since V_{FB} = 2.5V, the ratio of R_{FB2} to R_{FB1} calculates as 3:1. Standard values of 3.01 kΩ and 1.00 kΩ are chosen. Other values could be used as long as the 3:1 ratio is maintained.

F_s and R_T: Unless the application requires a specific frequency, the choice of frequency is generally a compromise. A higher frequency allows for a smaller inductor, input capacitor, and output capacitor (both in value and physical size), while providing a lower conversion efficiency. A lower frequency provides higher efficiency, but generally requires higher values for the inductor, input capacitor and output capacitor. The maximum allowed switching frequency for the LM5006 is limited by the minimum on-time (200 ns) at the maximum input voltage, and by the minimum off-time (260 ns) at the minimum input voltage. The maximum frequency limit for each application is defined by the following two calculations:

$$F_{S(max)1} = \frac{V_{OUT}}{V_{IN(max)} \times 200\ ns} \quad (7)$$

$$F_{S(max)2} = \frac{V_{IN(min)} - V_{OUT}}{V_{IN(min)} \times 260\ ns} \quad (8)$$

The maximum allowed frequency is the lesser of the two above calculations. See the graph " Maximum Switching Frequency". For this exercise, $F_{s(max)1}$ calculates to 667 kHz, and $F_{s(max)2}$ calculates to 1.28 MHz. Therefore the maximum allowed frequency for this example is 667 kHz, which is greater than the 300 kHz specified for this design. Using Equation 2, RT calculates to 258 kΩ. A standard value 261 kΩ resistor is used. The minimum on-time calculates to 469 ns, and the maximum on-time calculates to 2.28 µs.

L1: The main parameter affected by the inductor is the output current ripple amplitude. The choice of inductor value therefore depends on both the minimum and maximum load currents, keeping in mind that the maximum ripple current occurs at maximum Vin.

a) Minimum load current: To maintain continuous conduction at minimum Io (100 mA) if a flyback diode is used, the ripple amplitude (IOR) must be less than 200 mA p-p so the lower peak of the waveform does not reach zero. L1 is calculated using the following equation:

$$L1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{I_{OR} \times F_s \times V_{IN}} \quad (9)$$

At Vin = 75V, L1(min) calculates to 144µH. The next larger standard value (150 µH) is chosen and with this value I_{OR} calculates to 193 mA p-p at Vin = 75V, and 74 mA p-p at Vin = 15V

b) Maximum load current: At a load current of 400 mA, the peak of the ripple waveform must not reach the minimum value of the LM5006's current limit threshold (700 mA). Therefore the ripple amplitude must be less than 600 mA p-p, which is already satisfied in the above calculation. With L1 = 150 µH, at maximum Vin and Io, the peak of the ripple is 498 mA. While L1 must carry this peak current without saturating or exceeding its temperature rating, it also must be capable of carrying the maximum value of the LM5006's current limit threshold without saturating, since the current limit is reached during startup.

The DC resistance of the inductor should be as low as possible. For example, if the inductor's DCR is 0.5 ohm, the power dissipated at maximum load current is 0.08W. While small, it is not insignificant compared to the load power of 4W.

C3: The capacitor on the V_{CC} output provides not only noise filtering and stability, but its primary purpose is to prevent false triggering of the V_{CC} UVLO at the buck switch on/off transitions. C3 should be no smaller than 1 µF.

C2 and R3: When selecting the output filter capacitor C2, the items to consider are ripple voltage due to its ESR, ripple voltage due to its capacitance, and the nature of the load.

A low ESR for C2 is generally desirable so as to minimize power losses and heating within the capacitor. However, the regulator requires a minimum amount of ripple voltage at the feedback input for proper loop operation. For the LM5006 the minimum ripple required at pin 7 is 25 mV p-p, requiring a minimum ripple at V_{OUT} of 100 mV for this example. Since the minimum ripple current (at minimum Vin) is 74 mA p-p, the minimum ESR required at V_{OUT} is 100 mV/74 mA = 1.35Ω. Since quality capacitors for SMPS applications have an ESR considerably less than this, R3 is inserted as shown in the Block Diagram. R3's value, along with C2's ESR, must result in at least 25 mV p-p ripple at pin 7. See the LOW OUTPUT RIPPLE CONFIGURATIONS section for techniques to reduce the output ripple voltage.

D1/Q1: Either a Schottky diode or an N-Channel MOSFET may be used for the free-wheel switch. Use of a MOSFET generally results in higher circuit efficiency. Other factors to consider are component dimensions (PC board space) and cost. If a diode is to be used a power Schottky diode is recommended. Ultra-fast recovery diodes are not recommended as the high speed transitions at the SW pin may inadvertently affect the IC's operation through external or internal EMI. The important parameters are reverse recovery time and forward voltage. The reverse recovery time determines how long the reverse current surge lasts with each turn-on of the internal buck switch. The forward voltage drop affects efficiency. The diode's reverse voltage rating must be at least as great as the maximum input voltage, plus ripple and transients, and its current rating must be at least as great as the maximum current limit specification. The diode's average power dissipation is calculated from:

$$P_{D1} = V_F \times I_{OUT} \times (1–D) \quad (10)$$

Where V_F is the diode's forward voltage drop, and D is the on-time duty cycle. If a MOSFET is to be used for synchronous rectification, an N-Channel device is required. The MOSFET's voltage rating must be at least as great as the maximum input voltage, plus ripple and transients, and its current rating must be at least as great as the maximum current limit specification. The average power dissipation is calculated from:

$$P_{Q1} = I_{OUT}2 \times R_{DS(on)} \times (1–D)$$

where

- $R_{DS(on)}$ is the device's on-resistance
- D is the on-time duty cycle (11)

C1: This capacitor's purpose is to supply most of the switch current during the on-time, and limit the voltage ripple at Vin, on the assumption that the voltage source feeding Vin has an output impedance greater than zero. At maximum load current, when the buck switch turns on, the current into the VIN pin suddenly increases to the lower peak of the output current waveform, ramp up to the peak value, then drop to zero at turn-off. The average input current during this on-time is the load current (400 mA). For a worst case calculation, C1 must supply this average load current during the maximum on-time. To keep the input voltage ripple to less than 1V (for this exercise), C1 calculates to:

$$C1 = \frac{I \times t_{ON}}{\Delta V} = \frac{0.4A \times 2.28\ \mu s}{1V} = 0.91\ \mu F \quad (12)$$

Quality ceramic capacitors in this value have a low ESR which adds only a few millivolts to the ripple. It is the capacitance which is dominant in this case. To allow for the capacitor's tolerance, temperature effects, and voltage effects, a 1.0 µF, 100V, X7R capacitor is used.

C4: The recommended value is 0.01µF for C4, as this is appropriate in the majority of applications. A high quality ceramic capacitor, with low ESR is recommended as C4 supplies the surge current to charge the buck switch gate at turn-on. A low ESR also ensures a quick recharge during each off-time.

C5: This capacitor helps avoid supply voltage transients and ringing due to long lead inductance at V_{IN}. A low ESR, 0.1µF ceramic chip capacitor is recommended, located close to the LM5006.

UV and UVO pins: The Under Voltage Detector function is used to monitor a system voltage, such as the input voltage at VIN, by connecting the UV pin to two resistors (R_{UV1}, R_{UV2}) as shown in the Block Diagram. When the voltage at the UV pin increases above its threshold the UVO pin switches low. The UVO pin is high when the voltage at the UV input pin is below its threshold. Hysteresis is provided by the internal 5µA current source which is enabled when the voltage at the UV pin is below its threshold. The resistor values are calculated using the following procedure:

Choose the upper and lower thresholds (V_{UVH} and V_{UVL}) at V_{IN}.

$$R_{UV2} = \frac{V_{UVH} - V_{UVL}}{5\ \mu A} = \frac{V_{UV(HYS)}}{5\ \mu A} \quad (13)$$

$$R_{UV1} = \frac{R_{UV2} \times 2.5V}{V_{UVL} - 2.5V} \quad (14)$$

As an example, assume the application requires the following thresholds: V_{UVH} = 15V and V_{UVL} = 14V. Therefore $V_{UV(HYS)}$ = 1V. The resistor values calculate to:

(15)

$$R_{UV2} = 200k\Omega,\ R_{UV1} = 43.5k\Omega \quad (16)$$

Capacitor C6 is added to filter noise and ripple, which may be present on the V_{IN} line (see Figure 35). Where the resistor values are known, the threshold voltages and hysteresis are calculated from the following:

$$V_{UVH} = 2.5V + \left[R_{UV2} \times \left(\frac{2.5V}{R_{UV1}} + 5\ \mu A\right)\right] \quad (17)$$

$$V_{UVL} = 2.5V \times \frac{(R_{UV1} + R_{UV2})}{R_{UV1}} \quad (18)$$

$$V_{UV(HYS)} = R_{UV2} \times 5\ \mu A \quad (19)$$

The pull-up voltage for the UVO output can be any voltage under 10V. The maximum continuous current into the UVO output pin should not exceed 5 mA.

FINAL CIRCUIT

The final circuit is shown in Figure 35. The circuit was tested, and the resulting performance is shown in Figure 37 and Figure 36.

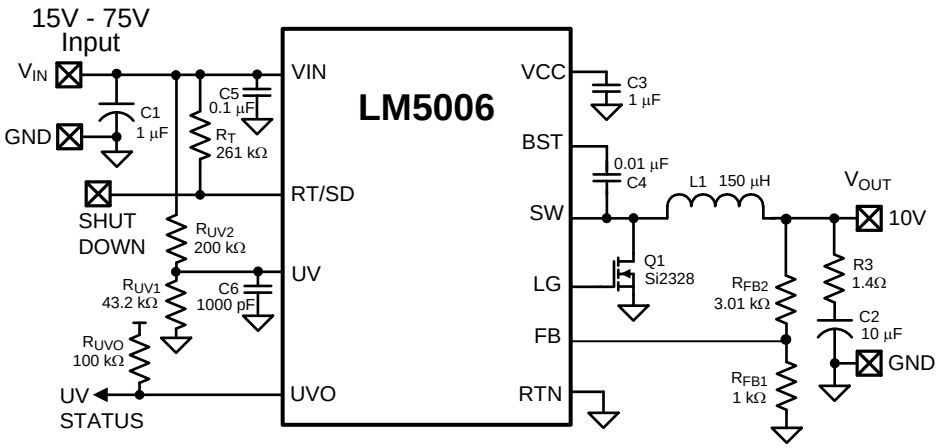


Figure 35. LM5006 Example Circuit

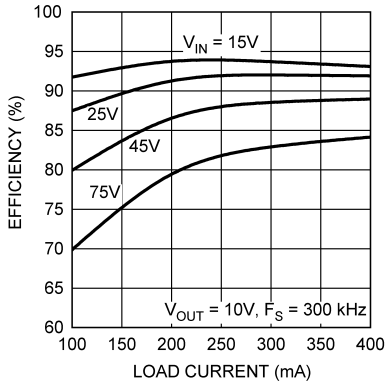


Figure 36. Efficiency vs. Load Current and V_{IN}

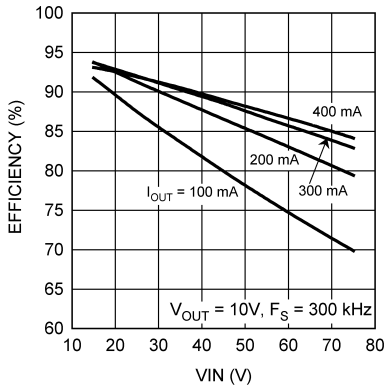


Figure 37. Efficiency vs. V_{IN}

LOW OUTPUT RIPPLE CONFIGURATIONS

For applications where low output ripple is required, the following options can be used to reduce or nearly eliminate the ripple.

a) Reduced ripple configuration: In Figure 38, Cff is added across R_{FB2} to AC-couple the ripple at V_{OUT} directly to the FB pin. This allows the ripple at V_{OUT} to be reduced to a minimum of 25 mVp-p by reducing R3, since the ripple at V_{OUT} is not attenuated by the feedback resistors. The minimum value for Cff is determined from:

$$Cff = \frac{3 \times t_{ON\,(max)}}{(R_{FB1} // R_{FB2})} \quad (20)$$

where

- $t_{ON(max)}$ is the maximum on-time, which occurs at the minimum input voltage

The next larger standard value capacitor should be used for Cff.

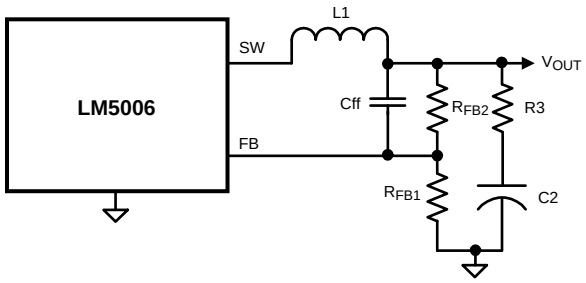


Figure 38. Reduced Ripple Configuration

b) Minimum ripple configuration: If the application requires a lower value of ripple (<10 mVp-p), the circuit of Figure 39 can be used. R3 is removed, and the resulting output ripple voltage is determined by the inductor's ripple current and C2's characteristics. RA and CA are chosen to generate a sawtooth waveform at their junction, and that voltage is AC-coupled to the FB pin via CB. To determine the values for RA, CA and CB, use the following procedure:

Calculate $V_A = V_{OUT} - (V_{SW} \times (1 - (V_{OUT}/V_{IN(min)})))$

where

- V_{SW} is the absolute value of the voltage at the SW pin during the off-time (21)

If a Schottky diode is used for the flyback function, the off-time voltage is in the range of 0.5V to 1V, depending on the specific diode used, and the maximum load current. If a MOSFET is used for synchronous rectification, the off-time voltage is in the range of 50 mV to 200 mV, depending on the $R_{DS(on)}$ of the selected device. V_A is the DC voltage at the RA/CA junction, and is used in the next equation.

- Calculate $RA \times CA = (V_{IN(min)} - V_A) \times t_{ON}/\Delta V$

where

- t_{ON} is the maximum on-time (at minimum input voltage)
- ΔV is the desired ripple amplitude at the RA/CA junction (typically 40-50 mV) (22)

RA and CA are then chosen from standard value components to satisfy the above product. Typically CA is 1000 pF to 5000 pF, and RA is 10 kΩ to 300 kΩ. CB is then chosen large compared to CA, typically 0.1 µF.

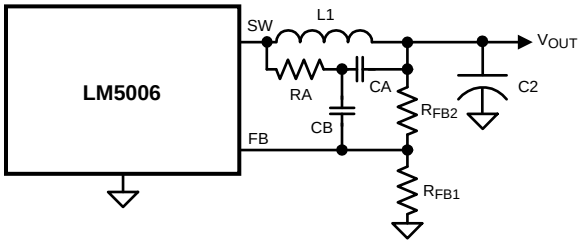


Figure 39. Minimum Output Ripple Using Ripple Injection

c) Alternate minimum ripple configuration: The circuit in Figure 40 is the same as that in the Block Diagram, except the output voltage is taken from the junction of R3 and C2. The ripple at V_{OUT} is determined by the inductor's ripple current and C2's characteristics. However, R3 slightly degrades the load regulation. This circuit may be suitable if the load current is fairly constant.

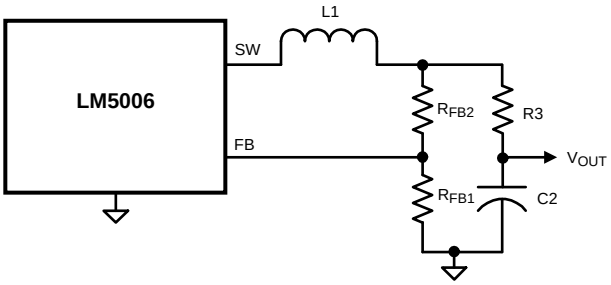


Figure 40. Alternate Minimum Output Ripple

Secondary Output

A secondary slave output voltage can be produced by replacing the inductor (L1) with an inductor which has a second winding, and using a MOSFET for synchronous rectification (Q1) rather than a diode. The synchronous rectification option is required to ensure the circuit is in continuous conduction mode at all values of the main output's load current. This ensures the secondary output voltage is correct for all load conditions. See Figure 41.

The approximate secondary output voltage (V_{OUT2}) is:

$$V_{OUT2} = (V_{OUT1} \times \frac{N_S}{N_P}) - V_{D1} \quad (23)$$

where

- N_P and N_S are the number of primary and secondary turns
- V_{D1} is the drop across D1

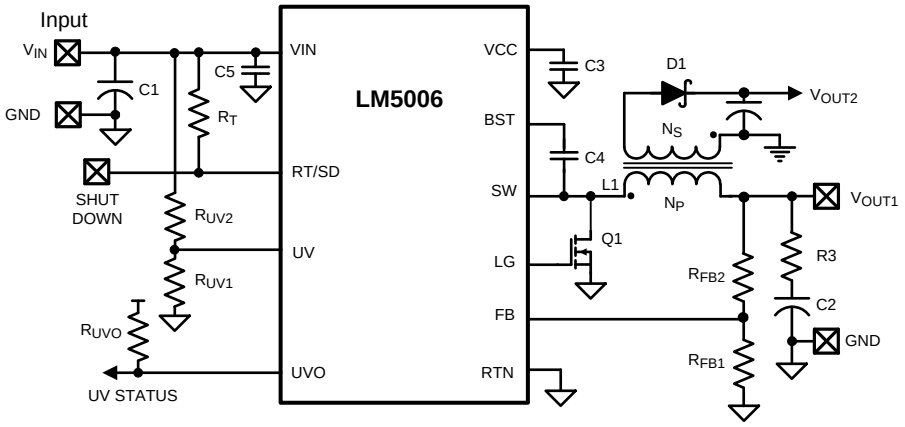


Figure 41. Generate a Secondary Output

PC Board Layout

The LM5006 regulation, over-voltage, and current limit comparators are very fast, and respond to short duration noise pulses. Layout considerations are therefore critical for optimum performance. The layout must be as neat and compact as possible, and all of the components must be as close as possible to the associated pins. The two major current loops have currents which switch very fast, and so the loops should be as small as possible to minimize conducted and radiated EMI. The first loop is formed by C1, through VIN to the SW pin, L1, C2, and back to C1. The second loop is formed by L1, C2, D1 (or Q1), and back to L1. Since a current equal to the load

current switches between these two loops with each transition from on-time to off-time and back to on-time, it is imperative that the ground end of C1 have a short and direct connection to D1's anode (or Q1's source), without going through vias or a lengthy route. The power dissipation in the LM5006 can be approximated by determining the total conversion loss ($P_{IN} – P_{OUT}$), and then subtracting the power losses in D1 (or Q1), and in the inductor. The power loss in the diode is approximately:

$$P_{D1} = I_{OUT} \times V_F \times (1–D)$$

where

- V_F is the diode's forward voltage drop
- D is the on-time duty cycle (24)

The average power dissipation in the synchronous rectifier (Q1) is calculated from:

$$P_{Q1} = I_{OUT}^2 \times R_{DS\ (on)} \times (1–D)$$

where

- $R_{DS(on)}$ is the device's on-resistance
- D is the on-time duty cycle (25)

The power loss in the inductor is approximately:

$$P_{L1} = I_{OUT}^2 \times R_L \times 1.1$$

where

- R_L is the inductor DC resistance
- the 1.1 factor is an approximation for the AC losses (26)

If it is expected that the internal dissipation of the LM5006 will produce excessive junction temperatures during normal operation, good use of the PC board's ground plane can help to dissipate heat. Additionally the use of wide PC board traces, where possible, can help conduct heat away from the IC. Judicious positioning of the PC board within the end product, along with the use of any available air flow (forced or natural convection) can help reduce the junction temperature.

REVISION HISTORY

Changes from Revision A (March 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	21

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM5006MM/NOPB	Active	Production	VSSOP (DGS) | 10	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SZLB
LM5006MM/NOPB.A	Active	Production	VSSOP (DGS) | 10	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SZLB
LM5006MMX/NOPB	Active	Production	VSSOP (DGS) | 10	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SZLB
LM5006MMX/NOPB.A	Active	Production	VSSOP (DGS) | 10	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SZLB

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

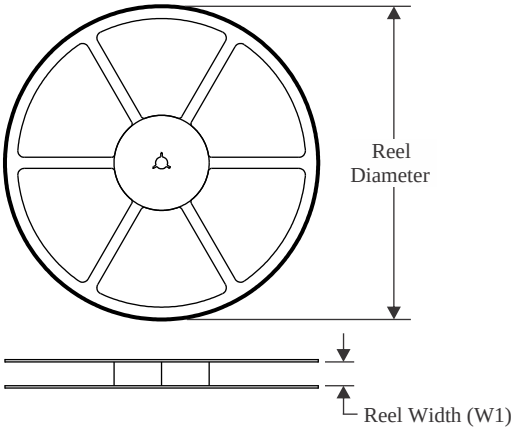
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

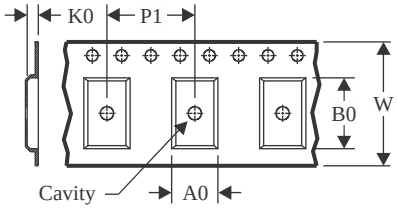
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

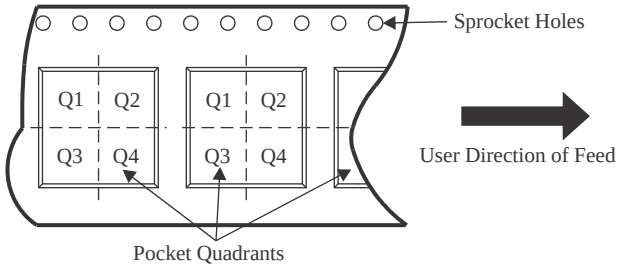


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

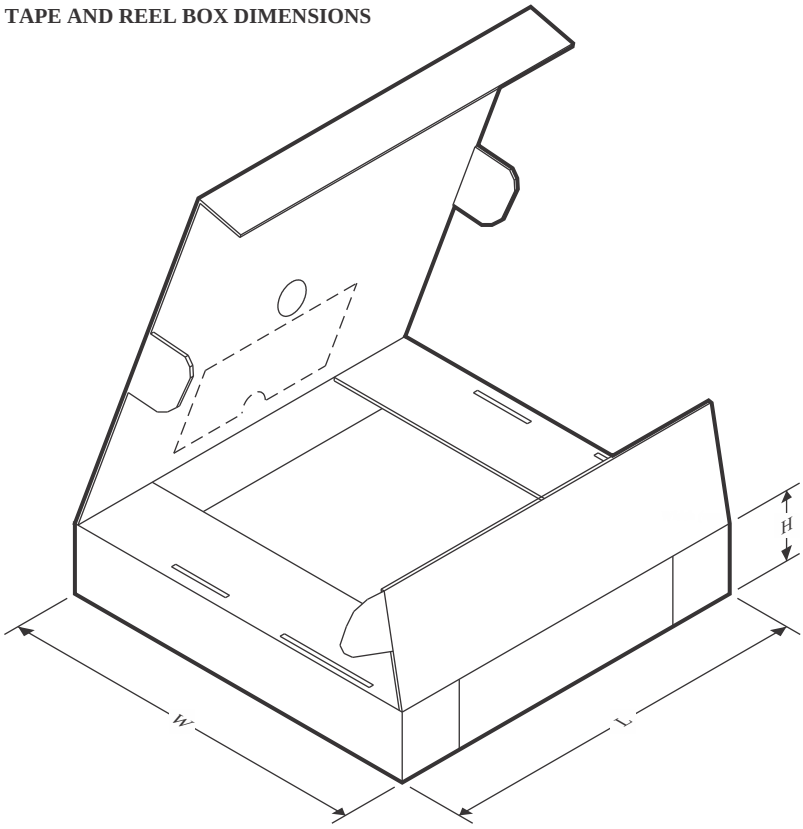
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5006MM/NOPB	VSSOP	DGS	10	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5006MMX/NOPB	VSSOP	DGS	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

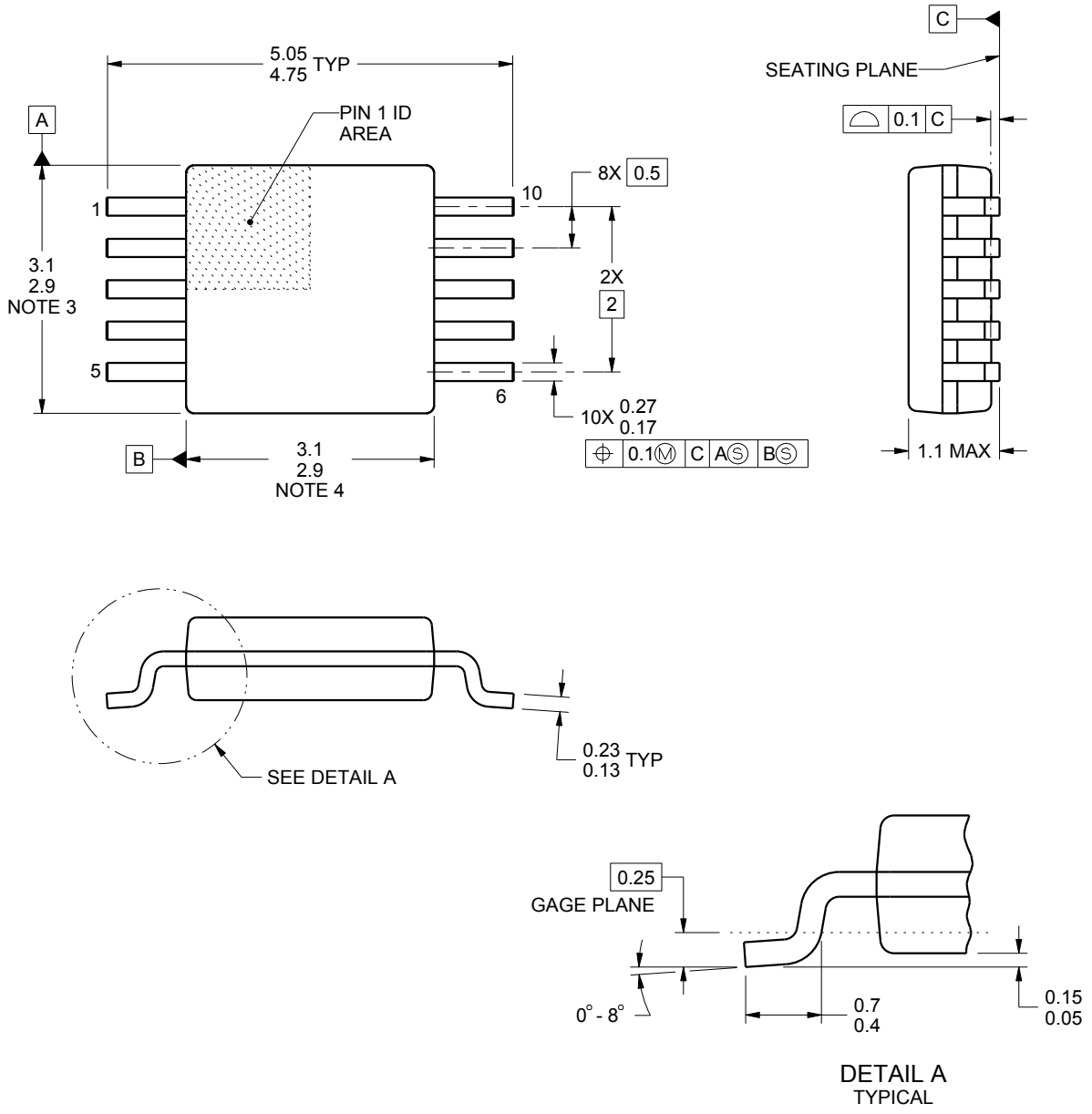
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5006MM/NOPB	VSSOP	DGS	10	1000	208.0	191.0	35.0
LM5006MMX/NOPB	VSSOP	DGS	10	3500	367.0	367.0	35.0

PACKAGE OUTLINE

DGS0010A

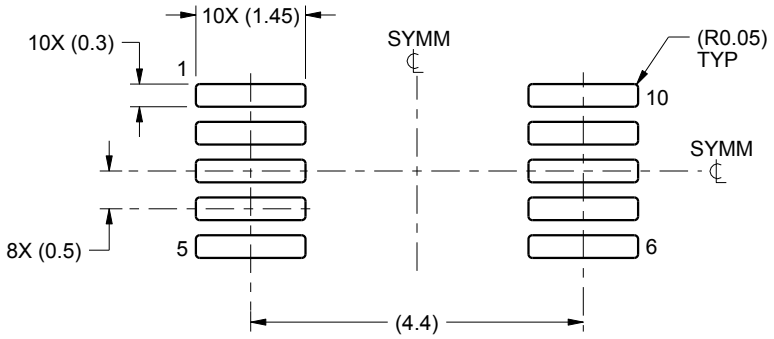
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

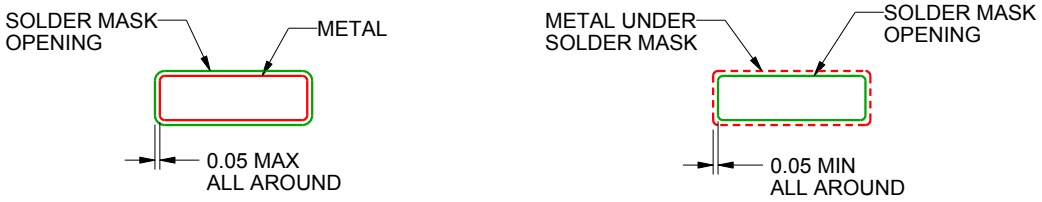


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

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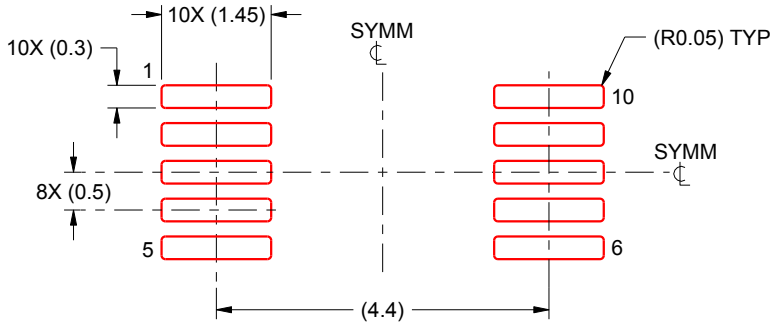
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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