LM5168E 115V, 0.3A, Synchronous Buck Converter

1 Features

- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Designed for reliability in rugged applications
  - 6V to 115V wide input voltage range
  - –55°C to +150°C junction temperature range
  - Fixed 3ms internal soft-start timer
  - Peak and valley current-limit protection
  - Input UVLO and thermal shutdown protection
- Designed for scalable industrial power supplies and battery packs
  - 50ns low minimum on and off times
  - 1MHz adjustable switching frequency
  - Diode emulation for high light-load efficiency
  - 10µA sleep current in auto mode
  - 3µA shutdown quiescent current
  - Pin-to-pin compatible with LM5164, LM5163, and LM5013
  - Similar pinout and functionality to LM5017 and LM34927
- Integration reduces design size and cost
  - COT mode control architecture
  - Integrated 1.9Ω NFET buck switch
  - Integrated 0.71Ω NFET synchronous rectifier
  - 1.2V internal voltage reference
  - No loop compensation components
  - Internal VCC bias regulator and boot diode
  - Open-drain power-good indicator
  - Package: SOIC PowerPAD™-8 integrated circuit package with 1.27mm pin spacing

2 Applications

- Space – solar source, storage
- Aerospace and defense – smart munitions, actuators
- Avionics – sensor imaging, radar

3 Description

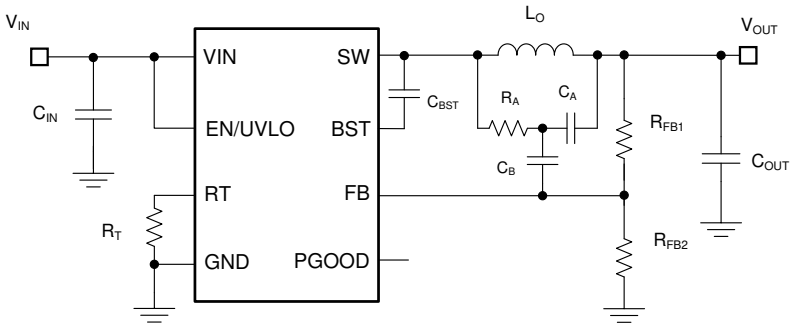
The LM5168E is an extended temperature range, (–55°C to +150°C) synchronous buck converter designed to regulate over a wide input voltage range, minimizing the need for external surge suppression components. A minimum controllable on time of 50ns facilitates large step-down conversion ratios, enabling the direct step-down from a 48V nominal input to low-voltage rails for reduced system complexity and design cost. The LM5168E operates during input voltage dips as low as 6V, at nearly 100% duty cycle if needed, making the device an excellent choice for wide input supply range industrial and high cell count battery pack applications.

With integrated high-side and low-side power MOSFETs, the LM5168E delivers up to 0.3A of output current. A constant on-time (COT) control architecture provides nearly constant switching frequency with excellent load and line transient response. The LM5168E is available in the auto mode version, which enables ultra-low I_Q and diode emulation mode operation for high light-load efficiency.

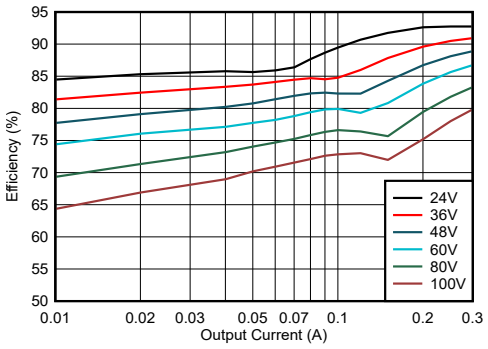
Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LM5168E	DDA (HSOIC, 8)	4.9mm × 6mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Buck Converter Schematic



Buck Converter Efficiency: V_{OUT} = 12V

Table of Contents

4 Device Comparison Table

DEVICE NUMBER	PACKAGE	DESCRIPTION	OUTPUT CURRENT	LIGHT LOAD MODE	CURRENT LIMIT
LM5168PEDDAR	DDA (HSOIC, 8)	0.3A, buck, AUTO, no-hiccup, extended temperature	0.3A	PFM	0.42A, no-hiccup

5 Pin Configuration and Functions

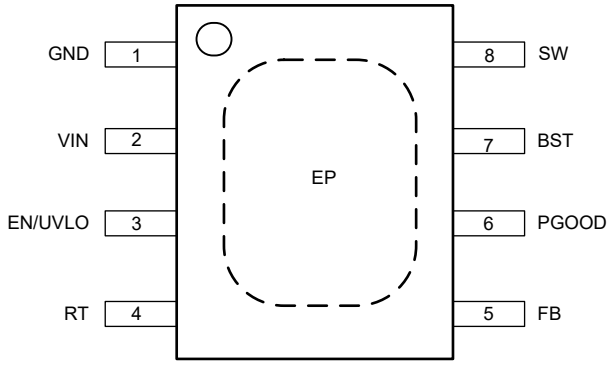


Figure 5-1. 8-Pin SO PowerPAD™ Integrated Circuit Package (Top View)

Table 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	GND	G	Ground connection for internal circuits
2	VIN	P	Regulator supply input pin to the high-side power MOSFET and internal bias regulator. Connect directly to the input supply of the buck converter with short, low impedance paths.
3	EN/UVLO	I	Precision enable and undervoltage lockout (UVLO) programming pin. If the EN/UVLO rising voltage is below 1.1V, the converter is in shutdown mode with all functions disabled. If the UVLO voltage is greater than 1.1V and below 1.5V, the converter is in standby mode with the internal VCC regulator operational and no switching. If the EN/UVLO voltage is above 1.5V, the start-up sequence begins.
4	RT	I	On-time programming pin. A resistor between this pin and GND sets the buck switch on time.
5	FB	I	Feedback input of the voltage regulation comparator
6	PGOOD	O	Power-good indicator. This pin is an open-drain output pin. Connect to a source voltage through an external pullup resistor between 10kΩ to 100kΩ. Connect to GND if the PGOOD feature is not needed.
7	BST	P	Bootstrap gate-drive supply. Required to connect a high-quality 2.2nF X7R ceramic capacitor between BST and SW to bias the internal high-side gate driver.
8	SW	P	Switching node that is internally connected to the source of the high-side NMOS buck switch and the drain of the low-side NMOS synchronous rectifier. Connect to the switching node of the power inductor.
—	EP	—	Exposed pad of the package. No internal electrical connection. Solder the EP to the GND pin and connect to a large copper plane to reduce thermal resistance.

(1) P = Power, G = Ground, I = Input, O = Output

6 Specifications

6.1 Absolute Maximum Ratings

Over the operating junction temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
Pin voltage	VIN	–0.3	118	V
	SW	–1.5	118	
	SW, transient < 20ns	–3		
	BST	–0.3	123.5	
	BST to SW	–0.3	5.5	
	EN	–0.3	118	
	FB	–0.3	5.5	
	RT	–0.3	5.5	
	PGOOD	–0.3	14	
Bootstrap capacitor	External BST to SW capacitance		2.5	nF
Operating junction temperature	T_J	–55	150	°C
Storage temperature	T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) See the Applications section for PCB layout recommendations (*Layout Guidelines*).

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IN}	Pin voltage	VIN	6		115	V
$V_{EN/UVLO}$	Pin voltage	EN/UVLO			115	V
I_{OUT}	Output current range	LM5168E		0.3		A
C_{BST}	External BST to SW capacitance			2.2		nF
F_{SW}	Switching frequency		100		1000	kHz

6.4 Thermal Information

THERMAL METRIC[1]		LM5168E DDA (SOIC) 8 PINS	UNIT
$R_{\theta JA(EVM)}$	Junction-to-ambient thermal resistance for EVM[2]	22	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	38.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	14.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.
(2) This value is obtained on the LM5168PEVM with approximately 49cm^2 of copper area. See *Thermal Considerations* section for more information.

6.5 Electrical Characteristics

T_J = –55°C to +150°C. Typical values are at T_J = 25°C, V_{IN} = 24V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
$I_{Q(VIN)}$	VIN quiescent current	$V_{EN/UVLO}$ = 2.5V, PFM operation		10	25	µA
$I_{Q(STANDBY)}$	VIN standby current	$V_{EN/UVLO}$ = 1.25V		17	35	µA
$I_{SD(VIN)}$	VIN shutdown supply current	$V_{EN/UVLO}$ = 0V, T_J = 25°C		3	6	µA
ENABLE						
$V_{EN(R)}$	EN/UVLO voltage rising threshold	EN/UVLO rising, enable switching	1.45	1.5	1.55	V
$V_{EN(F)}$	EN/UVLO voltage falling threshold	EN/UVLO falling, disable switching	1.35	1.4	1.44	V
$V_{SD(R)}$	EN/UVLO standby rising threshold	EN/UVLO rising, enable internal LDO, no switching.			1.1	V
$V_{SD(F)}$	EN/UVLO standby falling threshold	EN/UVLO falling, disable internal LDO.	0.45			V
REFERENCE VOLTAGE						
V_{FB}	FB voltage	V_{FB} falling	1.181	1.2	1.218	V
START-UP						
t_{SS}	Internal fixed soft-start time		1.75	3	4.75	ms
POWER STAGE						
$R_{DSON(HS)}$	High-side MOSFET on-resistance	I_{SW} = –100mA		1.91		Ω
$R_{DSON(LS)}$	Low-side MOSFET on-resistance	I_{SW} = 100mA		0.74		Ω
$t_{ON(min)}$	Minimum ON pulse width			50		ns
$t_{ON(1)}$	On-time1	V_{VIN} = 6V, R_{RT} = 75kΩ		5000		ns
$t_{ON(2)}$	On-time2	V_{VIN} = 6V, R_{RT} = 25kΩ		1650		ns
$t_{ON(3)}$	On-time3	V_{VIN} = 12V, R_{RT} = 75kΩ		2550		ns
$t_{ON(4)}$	On-time4	V_{VIN} = 12V, R_{RT} = 25kΩ		830		ns
$t_{OFF(min)}$	Minimum OFF pulse width			50		ns
BOOT CIRCUIT						
$V_{BOOT-SW(UV\_R)}$	BOOT-SW UVLO rising threshold	V_{BST-SW} rising		2.6	3.4	V
OVERCURRENT PROTECTION						
$I_{HS\_PK(OC)}$	High-side peak current limit		0.356	0.42	0.484	A
$I_{LS\_PK(OC)}$	Low-side peak current limit		0.356	0.42	0.484	A
$I_{DELTA(OC)}$	Minimum of $I_{HS\_PK(OC)}$ or $I_{LS\_PK(OC)}$ minus $I_{LS\_V(OC)}$			0.084		A
$I_{LS\_V(OC)}$	Low-side valley current limit	Low-side valley current limit on LS FET	0.27	0.336	0.42	A
I_{ZC}	Zero-cross detection current threshold			0		A

6.5 Electrical Characteristics (continued)

T_J = –55°C to +150°C. Typical values are at T_J = 25°C, V_{IN} = 24V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_W	Hiccup time before re-start			64		ms
POWER GOOD						
V_{PGTH}	Power-Good threshold	FB falling, PG high to low	1.055	1.08	1.1	V
		FB rising, PG low to high	1.105	1.14	1.175	V
R_{PG}	Power-Good on-state resistance	VFB = 1V		7		Ω
THERMAL SHUTDOWN						
T_{J-SHD}	Thermal shutdown threshold (1)	Temperature rising		175		°C
$T_{J-SHD-HYS}$	Thermal shutdown hysteresis (1)			10		°C

(1) Specified by design, not product tested

6.6 Typical Characteristics

Unless otherwise specified the following conditions apply: At T_A = 25°C, V_{IN} = 24V.

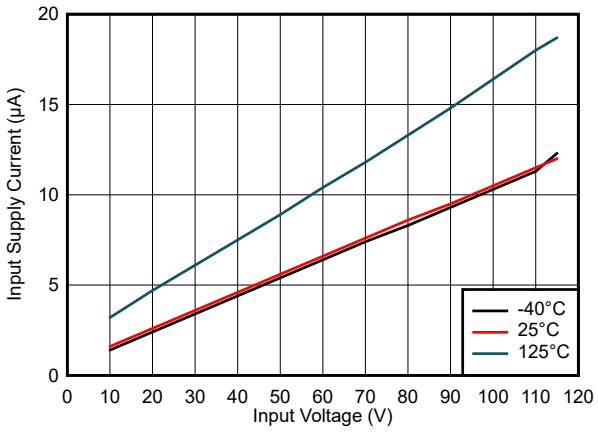


Figure 6-1. Shutdown Supply Current Versus Input Voltage

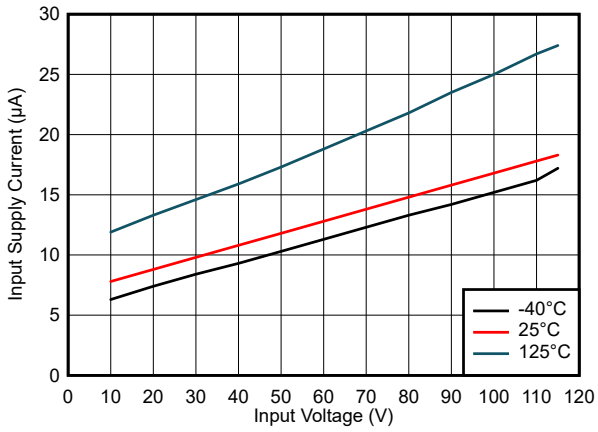


Figure 6-2. Sleep Mode Supply Current Versus Input Voltage (DEM, Non-Switching)

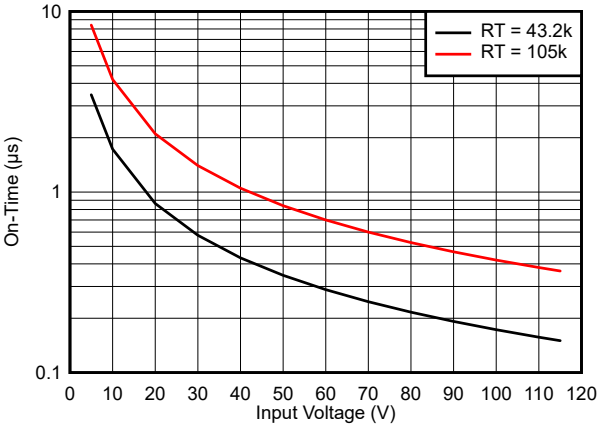


Figure 6-3. COT On Time Versus Input Voltage

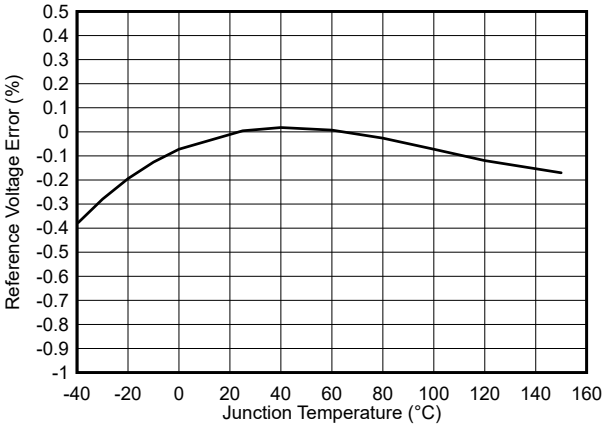


Figure 6-4. Feedback Comparator Threshold Versus Temperature

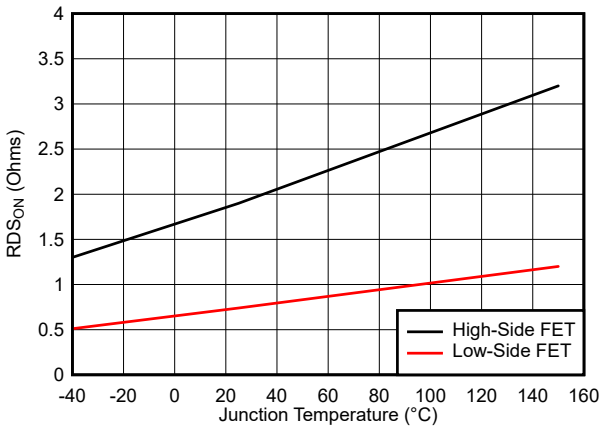


Figure 6-5. MOSFETs On-State Resistance Versus Temperature

7 Detailed Description

7.1 Overview

The LM5168E is an easy-to-use, ultra-low I_Q constant on-time (COT) synchronous buck regulator. With integrated high-side and low-side power MOSFETs, the LM5168E is a low-cost, highly efficient, buck converter that operates from a wide input voltage of 6V to 118V absolute maximum, delivering up to 0.3A DC load current. The LM5168E is available in an 8-pin, SO PowerPAD integrated circuit package with 1.27mm pin pitch for adequate spacing in high-voltage applications. This constant on-time (COT) converter is an excellent choice for low-noise, low-current, and fast load transient requirements, operating with a predictive on-time switching pulse. Over the input voltage range, input voltage feed-forward is employed to achieve a quasi-fixed switching frequency. A controllable on time as low as 50ns permits high step-down ratios and a minimum forced off time of 50ns provides extremely high duty cycles. This feature enables fixed frequency operation as VIN drops close to VOUT. After the forced off time of 50ns is reached, the device enters frequency fold-back operation to maintain a constant output voltage. The LM5168E implements a smart peak and valley current limit detection circuit for robust protection during output short-circuit conditions. Control loop compensation is not required for this regulator, reducing design time and external component count.

The LM5168E is pre-programmed to operate in auto mode. When configured to operate in auto mode, at light loads, the device transitions into an ultra-low I_Q mode to maintain high efficiency and prevent draining battery cells connected to the input when the system is in standby.

The LM5168E incorporates additional features for comprehensive system requirements, including:

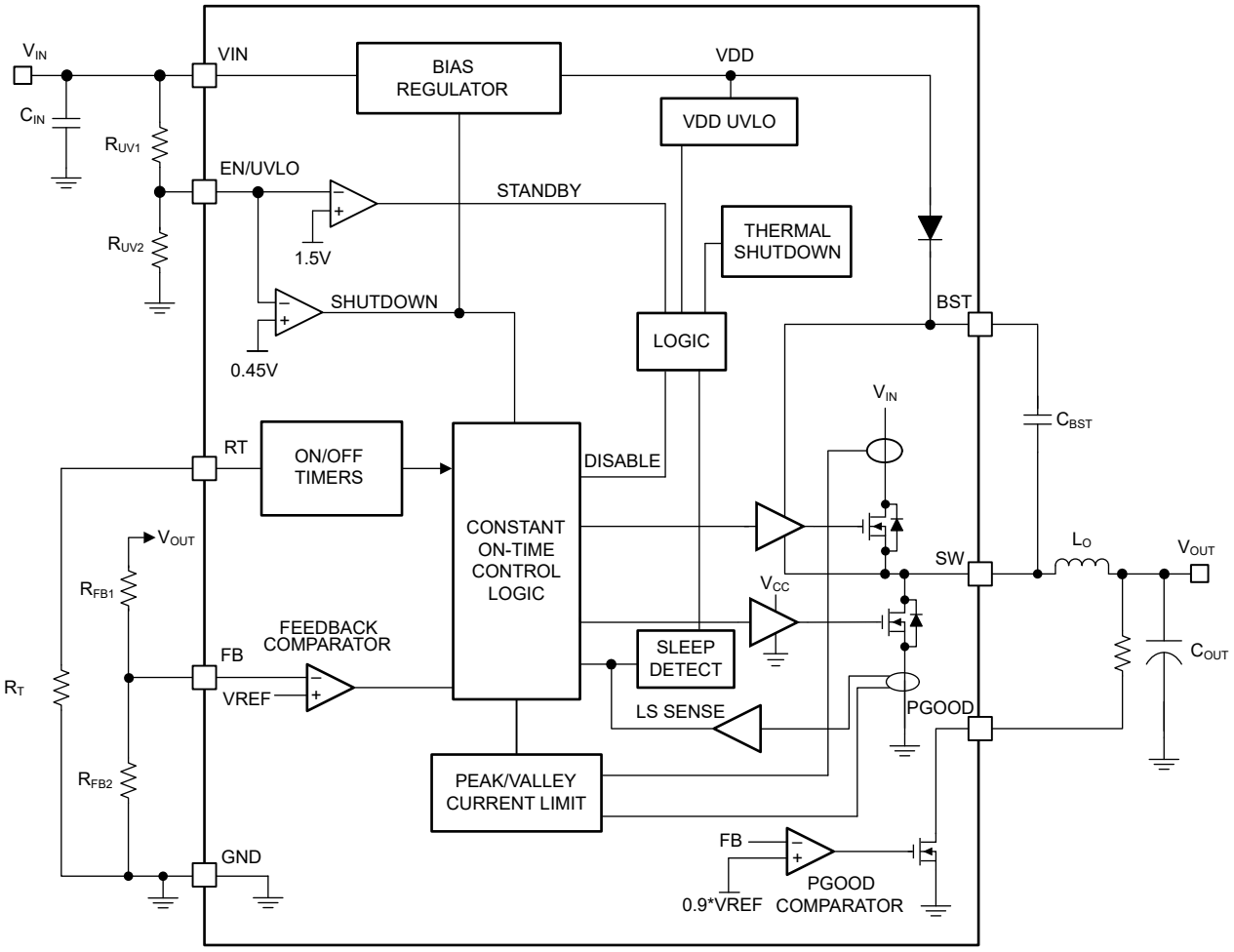
- Power-rail sequencing and fault reporting
- Internally fixed soft start
- Monotonic start-up into prebiased loads
- Precision enable for programmable line undervoltage lockout (UVLO)
- Smart cycle-by-cycle current limit for excellent inductor sizing
- Thermal shutdown with automatic recovery

The LM5168E support a wide range of end equipment requiring a regulated output from a high input supply where the transient voltage deviates from the DC level. Examples of such end equipment systems are the following:

- High cell-count battery-pack systems
- 24V industrial systems
- 48V telecom and PoE voltage ranges

The pin arrangement is designed for a simple layout that requires only a few external components.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Control Architecture

The LM5168E step-down switching converter employs a constant on-time (COT) control scheme. The COT control scheme sets a fixed on time, t_{ON}, of the high-side FET using a timing resistor (R_T). t_{ON} is adjusted as V_{IN} changes and is inversely proportional to the input voltage to maintain a fixed frequency when in continuous conduction mode (CCM). After expiration of t_{ON}, the high-side FET remains off until the FB voltage is equal or below the reference voltage of 1.2V. To maintain stability, the feedback comparator requires a minimal ripple voltage that is in-phase with the inductor current during the off time. Furthermore, this change in feedback voltage during the off time must be large enough to dominate any noise present at the feedback node. The minimum recommended ripple voltage is 20mV. More ripple voltage is used in cases that require robust operation. This action is especially true when there is excessive coupling from the SW pin or the BST pin to the FB pin. See also Table 7-1 for different types of ripple injection schemes that provide stability over the full input voltage range.

During a rapid start-up or a positive load step, the regulator operates with minimum off times until regulation is achieved. This feature enables extremely fast load transient response with minimal output voltage undershoot. When regulating the output in steady-state operation, the off time automatically adjusts to produce the switch-node duty cycle required for output voltage regulation to maintain a fixed switching frequency. In CCM, the switching frequency F_{SW} is programmed by the R_T resistor.

Table 7-1. Ripple Generation Methods

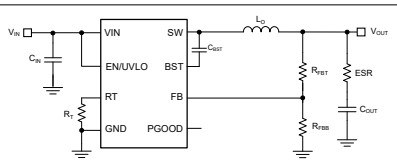
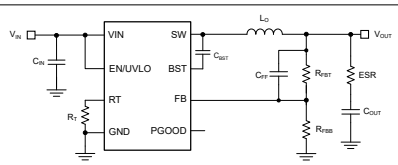
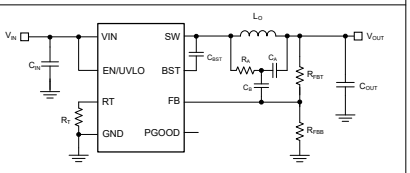
TYPE 1	TYPE 2	TYPE 3
Lowest Cost	Reduced Ripple	Minimum Ripple
		
$RESR \geq \frac{20\ mV \times VOUT}{VFB \times \Delta IL}$ (1) $RESR \geq \frac{VOUT}{2 \times VIN \times FSW \times COUT}$ (2)	$RESR \geq \frac{20\ mV}{\Delta IL}$ (3) $RESR \geq \frac{VOUT}{2 \times VIN \times FSW \times COUT}$ (4) $CFF \geq \frac{1}{2\pi \times FSW \times (RFBB \mid\mid RFBT)}$ (5)	$C_A \geq \frac{10}{F_{SW} \times (R_{FBB} \mid\mid R_{FBT})}$ (6) $R_A \times C_A \leq \frac{(V_{IN} - V_{OUT}) \times T_{ON}}{20mV}$ (7) $C_B \geq \frac{T_{settle}}{3 \times R_{FBT}}$ (8)

Table 7-1 presents three different methods for generating appropriate voltage ripple at the feedback node. The Type 1 ripple generation method uses a single resistor, R_{ESR}, in series with the output capacitor. The generated voltage ripple has two components: capacitive ripple caused by the inductor ripple current charging and discharging the output capacitor and resistive ripple caused by the inductor ripple current flowing into the output capacitor and through series resistance R_{ESR}. The capacitive ripple component is out-of-phase with the inductor current and does not decrease monotonically during the off time. The resistive ripple component is in-phase with the inductor current and decreases monotonically during the off time. The resistive ripple must exceed the capacitive ripple at V_{OUT} for stable operation. If this condition is not satisfied, unstable switching behavior is observed in COT converters, with multiple on-time bursts in close succession followed by a long off time. The equations under Type 1 define the value of the series resistance R_{ESR} to make sure of sufficient in-phase ripple at the feedback node.

Type 2 ripple generation uses a C_{FF} capacitor in addition to the series resistor. As the output voltage ripple is directly AC-coupled by C_{FF} to the feedback node, the R_{ESR} and ultimately the output voltage ripple, are reduced by a factor of V_{OUT} / V_{FB}.

Type 3 ripple generation uses an RC network consisting of R_A and C_A, and the switch node voltage to generate a triangular ramp that is in-phase with the inductor current. This triangular wave is then AC-coupled into the feedback node with capacitor C_B. Because this circuit does not use output voltage ripple, this circuit is an excellent choice for applications where low output voltage ripple is critical. See also *Related Documentation* section for more details about COT control methods.

Light-load mode operation can be set to PFM and DEM operation. Diode emulation mode (DEM) prevents negative inductor current, and pulse skipping maintains the highest efficiency at light load currents by decreasing the effective switching frequency. DEM operation occurs when the synchronous power MOSFET switches off as inductor valley current reaches zero. Here, the load current is less than half of the peak-to-peak inductor current ripple in CCM. Turning off the low-side MOSFET at zero current reduces switching loss, and lowers conduction loss by preventing negative current conduction. Power conversion efficiency is higher in a DEM converter than an equivalent forced-PWM CCM converter. With DEM operation, the duration that both power MOSFETs remain off progressively increases as load current decreases. When this idle duration exceeds 15µs, the converter transitions into an ultra-low I_Q mode, consuming only 10µA quiescent current from the input.

7.3.2 Internal VCC Regulator and Bootstrap Capacitor

The LM5168E contains an internal linear regulator that is powered from VIN with a nominal output of 5V, eliminating the need for an external capacitor to stabilize the VCC subregulator. The VCC subregulator supplies current to internal circuit blocks, including the synchronous FET driver and logic circuits. The input pin (VIN) can be connected directly to line voltages up to 115V. Because the power MOSFET has a low total gate charge, use a low bootstrap capacitor value to reduce the stress on the internal regulator. Select a high-quality 2.2nF X7R

ceramic bootstrap capacitor as specified in the *Absolute Maximum Ratings*. Selecting a higher value capacitance stresses the internal VCC regulator and can damage the device. An internal bootstrap diode connects from VCC to BST to replenish the charge in the high-side gate drive bootstrap capacitor when the switch-node voltage is low.

7.3.3 Internal Soft Start

The LM5168E employs an internal soft-start control ramp that allows the output voltage to gradually reach a steady-state operating point, thereby reducing start-up stresses and current surges. The soft-start feature produces a controlled, monotonic output voltage start-up. The soft-start time is internally set to 3ms.

7.3.4 On-Time Generator

The on time of the LM5168E high-side FET is determined by the R_T resistor and is inversely proportional to the input voltage, V_{IN}. The inverse relationship with V_{IN} results in a nearly constant frequency as V_{IN} is varied. Use Section 7.3.4 to calculate the on time, where R_T is in kΩ.

$$\mathrm{TON} = \frac{\mathrm{R_T}}{2.5 \times \mathrm{VIN}} \tag{9}$$

Use Equation 10 to determine the R_T resistor to set a specific switching frequency in CCM, where F_{SW} is in kHz.

$$\mathrm{R_T} = \frac{2500 \times \mathrm{V_{OUT}}}{\mathrm{F_{SW}}} \ [\mathrm{k\Omega}] \tag{10}$$

Select R_T for a minimum on time (at maximum V_{IN}) greater than 50ns for proper buck operation. In addition to this minimum on time, the maximum frequency for this device is limited to 1MHz.

7.3.5 Current Limit

The LM5168E manages overcurrent conditions with cycle-by-cycle current limiting of the peak inductor current. The current sensed in the high-side MOSFET is compared every switching cycle to the current limit threshold (0.42A typical). To protect the converter from potential current runaway conditions, the LM5168E includes a foldback valley current limit feature, set at 0.34A, that is enabled if a peak current limit is detected. As shown in Figure 7-1, if the peak current in the high-side MOSFET exceeds 0.42A for the LM5168E (typical), the present cycle is immediately terminated regardless of the programmed on time (t_{ON}), the high-side MOSFET is turned off and the fold-back valley current limit is activated. The low-side MOSFET remains on until the inductor current drops below this fold-back valley current limit, after which the next on-pulse is initiated. This method folds back the switching frequency to prevent overheating and limits the average output current to less than 0.3A for LM5168E to provide proper short-circuit and heavy-load protection.

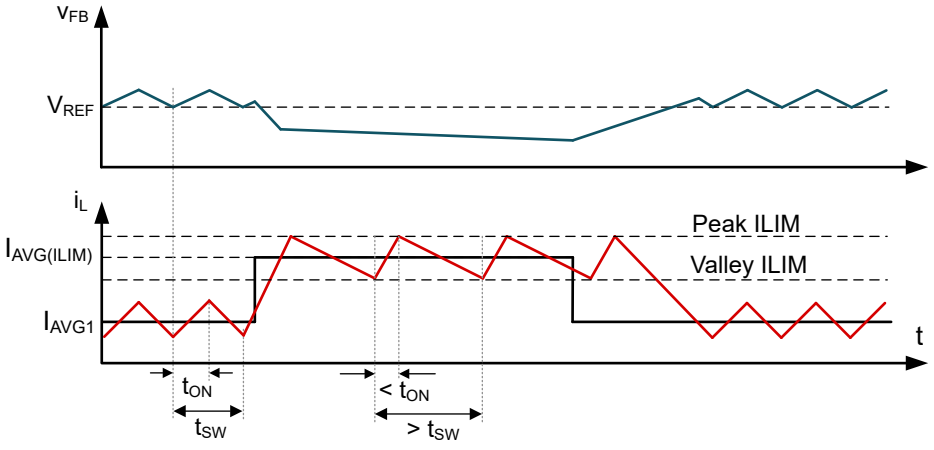


Figure 7-1. Current Limit Timing Diagram

Current is sensed after a leading-edge blanking time following the high-side MOSFET turn-on transition. The propagation delay of the current limit comparator is 100ns. During high step-down conditions when the on time is less than 100ns, a back-up peak current limit comparator in the low-side MOSFET, also set at 0.42A, enables the foldback valley current limit set at 0.34A. This current limit scheme enables ultra-low duty-cycle operation, permitting large step-down voltage conversions while ensuring robust protection of the converter.

The LM5168E implements a current limit off-timer and hiccup protection. If the current in the high-side MOSFET exceeds $I_{HS\_PK(OC)}$, the high-side MOSFET is immediately turned off and a non-resettable off-timer is initiated. The length of the off time is controlled by the FB voltage and the input voltage. In hiccup protection, a soft-start counter enables the output voltage to recover properly after an overcurrent event is detected for 16 consecutive current limit cycles. After four consecutive cycles without current limit detection, the device restarts the hiccup protection counter. The device attempt soft start after a "hiccup period" of 64ms.

7.3.6 N-Channel Buck Switch and Driver

The LM5168E integrates an N-channel buck switch and associated floating high-side gate driver. The gate-driver circuit works in conjunction with an external bootstrap capacitor and an internal high-voltage bootstrap diode. A high-quality ceramic capacitor connected between the BST and SW pins provides the voltage to the high-side driver during the buck switch on time. See also Section 7.3.2 for limitations. During the off time, the SW pin is pulled down to approximately 0V, and the bootstrap capacitor charges from the internal VCC through the internal bootstrap diode. The minimum off-timer, set to 50ns (typical), ensures a minimum time each cycle to recharge the bootstrap capacitor. When the on time is less than 300ns, the minimum off-timer is forced to 250ns to make sure that the BST capacitor is charged in a single cycle. This action is vital during wake-up from sleep mode when the BST capacitor is most likely discharged.

7.3.7 Synchronous Rectifier

The LM5168E integrates an internal low-side synchronous rectifier N-channel MOSFET, which provides a low-resistance path for the inductor current to flow when the high-side MOSFET is turned off.

The synchronous rectifier operates in a diode emulation mode. Diode emulation enables the regulator to operate in a pulse-skipping mode during light-load conditions. This mode leads to a reduction in the average switching frequency at light loads. As a result, efficiency at light loads is improved due to a reduction in switching losses and MOSFET gate driver losses, which are both proportional to switching frequency. This pulse-skipping mode also reduces the circulating inductor current and losses associated with conventional CCM at light loads.

7.3.8 Enable/Undervoltage Lockout (EN/UVLO)

The LM5168E contains a dual-level EN/UVLO circuit. When the EN/UVLO voltage is below 0.45V (typical), the converter is in a low-current shutdown mode and the input quiescent current (I_Q) is dropped down to 3µA. When the voltage is greater than 1.1V but less than 1.5V (typical), the converter is in standby mode. In standby mode, the internal bias regulator is active while the control circuit is disabled. When the voltage exceeds the rising threshold of 1.5V (typical), normal operation begins. Install a resistor divider from VIN to GND to set the minimum operating voltage of the regulator. If the user wishes to implement an input voltage UVLO, refer to Figure 7-2, Equation 11, and Equation 12 for details. Typically, the user chooses a value for R_{UV1} and calculates the value of R_{UV2} using Equation 11 based on a desired V_{ON}. Reasonable values for R_{UV1} are in the 1MΩ range. Equation 12 is then used to calculate the resulting V_{OFF}. V_{ON} and V_{OFF} are the input voltages where the device turns on and off, respectively.

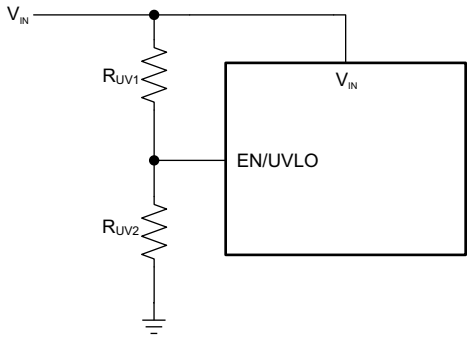


Figure 7-2. Input UVLO Connections

$$R_{UV2} = R_{UV1} \times \left(\frac{V_{EN(R)}}{V_{ON} - V_{EN(R)}} \right) \quad (11)$$

$$V_{OFF} = V_{EN(F)} \times \left(1 + \frac{R_{UV1}}{R_{UV2}} \right) \quad (12)$$

If input UVLO is not required, the user can either drive EN/UVLO as an enable input driven by a logic signal or connect directly to VIN. If EN/UVLO is directly connected to VIN, the regulator begins switching as soon as the internal bias rails are active; approximately 4.5V at VIN.

7.3.9 Power Good (PGOOD)

The LM5168E provides a PGOOD indicator (PG) to indicate when the output voltage is within the regulation level. Use the PGOOD signal for start-up sequencing of downstream converters or for fault protection and output monitoring. PGOOD is an open-drain output that requires a pullup resistor to a DC supply not greater than 14V. The typical range of pullup resistance is 10kΩ to 100kΩ. If necessary, use a resistor divider to decrease the voltage from a higher voltage pullup rail. When the FB voltage exceeds 95% of the internal reference V_{REF}, the internal PGOOD switch turns off and PGOOD can be pulled high by the external pullup. If the FB voltage falls below 90% of V_{REF}, an internal 7Ω PGOOD switch turns on and PGOOD is pulled low to indicate that the output voltage is out of regulation. The rising edge of PGOOD has a built-in deglitch delay of 5µs.

7.3.10 Thermal Protection

The LM5168E includes an internal junction temperature monitor to protect the device in the event of higher than normal junction temperature. If the junction temperature exceeds 175°C (typical), thermal shutdown occurs to prevent further power dissipation and temperature rise. The LM5168E initiates a restart sequence when the junction temperature falls to 165°C, based on a typical thermal shutdown hysteresis of 10°C. This protection is a non-latching protection, so the device cycles into and out of thermal shutdown if the fault persists.

7.4 Device Functional Modes

7.4.1 Shutdown Mode

EN/UVLO provides ON and OFF control for the LM5168E. When $V_{EN/UVLO}$ is below approximately 0.45V, the device is in shutdown mode. Both the internal VCC subregulator and the switching regulator are off. The quiescent current in shutdown mode drops to 3µA at V_{IN} = 24V. The LM5168E also employs internal bias rail undervoltage protection. If the input voltage is below about 4.5V, the regulator remains off.

7.4.2 Active Mode

The LM5168E is in active mode when $V_{EN/UVLO}$ is above the precision enable threshold and the internal bias rail is above the UV threshold. In COT active mode, the LM5168E is in one of the following modes depending on the load current:

1. CCM with fixed switching frequency when load current is above half of the peak-to-peak inductor current ripple
2. Auto mode (P device designator) – light load operation: pulse skipping and diode emulation mode (DEM) when the load current is less than half of the peak-to-peak inductor current ripple in CCM operation.
3. Current limit CCM with peak and valley current limit protection when an overcurrent condition is applied at the output

7.4.3 Sleep Mode

Control Architecture gives a brief introduction to the LM5168E diode emulation (DEM) feature. The converter enters DEM during light-load conditions when the inductor current decays to zero and the synchronous MOSFET is turned off to prevent negative current in the system. In the DEM state, the load current is lower than half of the peak-to-peak inductor current ripple and the switching frequency decreases when the load is further decreased as the device operates in a pulse skipping mode. A switching pulse is set when V_{FB} drops below 1.2V.

As the frequency of operation decreases and V_{FB} remains above 1.2V (V_{REF}) with the output capacitor sourcing the load current for greater than 15µs, the converter enters an ultra-low I_Q sleep mode to prevent draining the input power supply. The input quiescent current (I_Q) required by the LM5168E decreases to 10µA in sleep mode, improving the light-load efficiency of the regulator. In this mode, all internal controller circuits are turned off to make sure of very low current consumption by the device. Such low I_Q renders the LM5168E as the best option to extend operating lifetime for off-battery applications. The FB comparator and internal bias rail are active to detect when the FB voltage drops below the internal reference V_{REF} and the converter transitions out of sleep mode into active mode. There is a 9µs wake-up delay from sleep to active states.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The LM5168E requires only a few external components to create a buck converter to step down from a wide range of supply voltages to a fixed output voltage. Several features are integrated in the device to meet system design requirements, including the following:

- Precision enable
- Input voltage UVLO
- Internal soft start
- Programmable switching frequency
- A PGOOD indicator

To expedite and streamline the process of designing a LM5168E-based converter, a comprehensive LM5168E quick-start calculator tool is available for download to assist the designer with component selection for a given application. This tool is complemented by the availability of an evaluation module and PSPICE models.

8.2 Typical Buck Application

The LM5168E is designed for buck applications by operating in DEM mode, with light load PFM operation. Figure 8-1 shows the schematic for a 5V output buck regulator capable of delivering 300mA of load current, using the LM5168E .

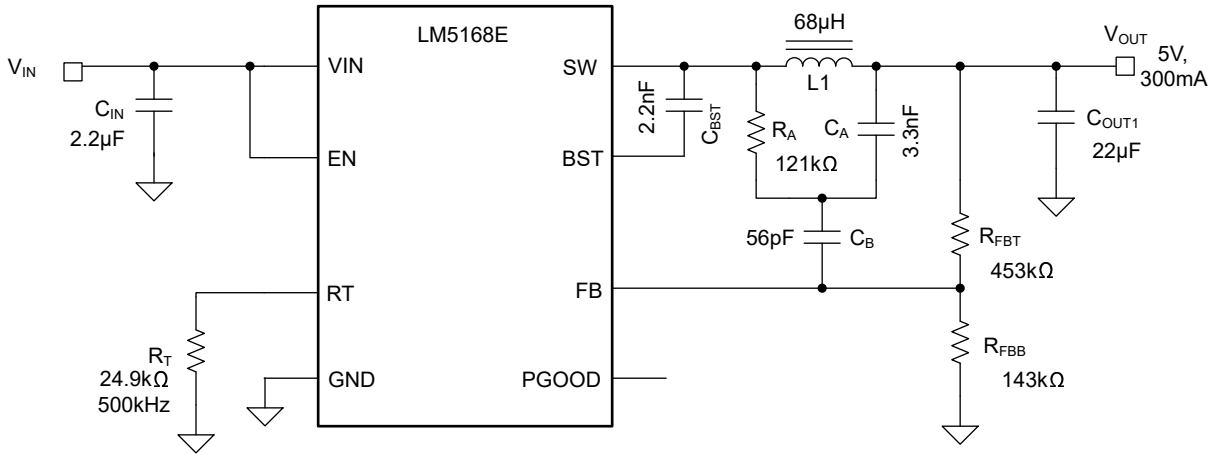


Figure 8-1. Example Buck Converter Schematic

Note

In this data sheet, the *effective* value of capacitance is defined as the actual capacitance under D.C. bias and temperature, not the rated or nameplate values. Use high-quality, low ESR, ceramic capacitors with an X5R or better dielectric throughout. All high value ceramic capacitors have a large voltage coefficient in addition to normal tolerances and temperature effects. Under DC bias, the capacitance drops considerably. Large case sizes and higher voltage ratings are better in this regard. To help mitigate these effects, multiple capacitors can be used in parallel to bring the minimum *effective* capacitance up to the required value. This action can also ease the RMS current requirements on a single capacitor. A careful study of bias and temperature variation of any capacitor bank must be made to make sure that the minimum value of *effective* capacitance is provided.

8.2.1 Design Requirements

Table 8-1 lists the design requirements for a typical buck application using the LM5168E.

Table 8-1. Detailed Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Nominal input voltage	24V
Input voltage range	12V to 115V
Output voltage	5V
Output current	0.3A
Switching frequency	500kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Switching Frequency (R_T)

The switching frequency of the LM5168E is set by the on-time programming resistor connected to the R_T pin. Use Equation 13 to calculate R_T based on the desired switching frequency and output voltage. A 24.9kΩ resistor is used for 500kHz switching frequency and 5V output.

$$R_T\,(K\Omega) = \frac{V_{OUT} \times 2500}{F_{SW}\,(kHz)} \tag{13}$$

Note that at very low duty cycles, the 50ns minimum controllable on time of the high-side MOSFET, $t_{ON(min)}$, limits the maximum switching frequency. In CCM, $t_{ON(min)}$ limits the voltage conversion step-down ratio for a given switching frequency. Use Equation 14 to calculate the minimum controllable duty cycle.

$$D_{MIN} = t_{ON(min)} \times F_{SW} \tag{14}$$

Ultimately, the choice of switching frequency for a given output voltage affects the available input voltage range, design size, and efficiency. Use Equation 15 to calculate the maximum supply voltage for a given $t_{ON(min)}$ to maintain the full switching frequency.

$$V_{IN(max)} = \frac{V_{OUT}}{t_{ON(min)} \times F_{SW}} \tag{15}$$

8.2.2.2 Buck Inductor Selection

For most applications, choose an inductance such that the inductor ripple current, ΔI_L, is between 30% and 50% of the rated load current at nominal input voltage. Use Equation 16 to calculate the inductance. For this example, assume V_{IN} = 24V, F_{SW} = 500kHz, and a ripple current of 30% of 0.3A. This gives us an inductance of about 65µH. Choose the next standard value of 68µH for this design. Next, use Equation 17 to calculate the actual inductor ripple current across the input voltage range. Finally, use Equation 18 to determine the peak inductor current at our maximum input voltage and compare with the current limit of the LM5168E. Arrive at a peak current of about 0.37A at V_{IN} = 115V, which is less than the current limit of the LM5168E.

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \tag{16}$$

$$\Delta I_L = \frac{V_{OUT}}{F_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \tag{17}$$

$$I_{L(peak)} = I_{OUT} + \frac{\Delta I_L}{2} \tag{18}$$

Ideally, the saturation current rating of the inductor is at least as large as the peak current limit. This size makes sure that the inductor does not saturate even during a short circuit on the output. When the inductor core material saturates, the inductance falls to a very low value, causing the inductor current to rise very rapidly.

Although the valley current limit is designed to reduce the risk of current run-away, a saturated inductor can cause the current to rise to high values very rapidly. This rise can lead to component damage. Do not allow the inductor to saturate. Inductors with a ferrite core material have very *hard* saturation characteristics, but usually have lower core losses than powdered iron cores. Powered iron cores exhibit a *soft* saturation, allowing some relaxation in the current rating of the inductor. However, powered iron cores have more core losses at frequencies above about 1MHz. In any case, the inductor saturation current must not be less than the maximum peak inductor current at full load.

8.2.2.3 Setting the Output Voltage

The LM5168E regulates the output voltage by maintaining the FB voltage equal to the internal reference voltage, V_{REF} = 1.2V (typical). A resistor divider programs the output voltage based on Equation 19.

$$R_{FBT} = R_{FBB} \times \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \tag{19}$$

TI recommends selecting R_{FBB} in the range of 10kΩ to 1MΩ for most applications. A larger R_{FBB} consumes less DC current, which is mandatory if light-load efficiency is critical. TI does not recommend R_{FBB} larger than 1MΩ as the feedback path becomes more susceptible to noise. For this example select R_{FBB} = 143kΩ. This action gives R_{FBT} = 453kΩ. Route the feedback trace away from the noisy area of the PCB and keep the feedback resistors close to the FB pin.

8.2.2.4 Type 3 Ripple Network

This example uses a Type 3 ripple injection network. This network uses an RC filter consisting of R_A and C_A across SW and V_{OUT} to generate a triangular ramp that is in phase with the inductor current. This triangular ramp is then AC-coupled into the feedback node through capacitor C_B. Type 3 ripple injection is an excellent choice for applications where low output voltage ripple is crucial, and allows the use of low-ESR ceramic output capacitors.

Use Equation 20 to calculate C_A. With the values used in this example, C_A > 184pF. A value of 3300pF is selected to keep R_A within practical limits. In general, the user needs 20mV of ripple at the feedback pin for reliable operation, calculated at nominal input voltage. The minimum value of ripple must not be less than 12mV at minimum input voltage. Using Equation 21 with nominal input voltage, a value of R_A > 120kΩ was found and a value of 121kΩ is selected.

$$C_A \geq \frac{10}{F_{SW} \times (R_{FBB} \,||\, R_{FBT})} \tag{20}$$

$$R_A \leq \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{0.02 \times V_{IN} \times F_{SW} \times C_A} \tag{21}$$

While the magnitude of the generated ripple does not affect the output voltage ripple, the magnitude produces a DC error of approximately half the amplitude of the generated ripple, scaled by the feedback divider ratio. Therefore, the amount of DC offset, tolerable in the output voltage, imposes an upper bound on the feedback ripple.

Finally, use Equation 22 to calculate the coupling capacitance C_B. In the equation, t_R is the approximate settling time of the control loop to a load transient disturbance. This was taken as 50µs.

$$C_B \geq \frac{t_R}{3 \times R_{FBT}} \tag{22}$$

where

- t_R = 50µs (typical)

A value greater than 37pF was calculated for C_B and a value of 56pF is selected for this example. This value avoids excessive coupling capacitor discharge by the feedback resistors during sleep intervals when operating at light loads. Note that the minimum value of C_B is 47pF.

8.2.2.5 Output Capacitor Selection

The Type 3 ripple injection network allows the use of small, low-ESR, ceramic output capacitors, while the ripple injection network provides the proper signal to the regulation comparator.

One way to select the value of output capacitance is with Equation 23. This equation sizes the output capacitor based on a specified load current transient and output voltage transient.

$$C_{OUT} > \frac{L \times \left(I_{OUT} + \frac{\Delta I_L}{2}\right)^2}{2 \times \Delta V \times V_{OUT}} \tag{23}$$

Where:

- ΔV = Change in output voltage during load transient.
- ΔI_L = inductor ripple current from Equation 17

For this example we specify ΔV = 50mV for a full load transient of 300mA. Use Equation 18 to calculate I_{peak}. Arrive at C_{OUT} greater than about 17µF. A 22µF, 25V rated capacitor with X7R dielectric is selected with voltage coefficients of ceramic capacitors taken into consideration. More output capacitance can be used to provide smaller load transients or lower output voltage ripple. Keep in mind that the minimum output capacitance must be greater than 2.2µF. Use Equation 24 to estimate the switching frequency output ripple, assuming that the output capacitor ESR is not dominant.

$$V_r \geq \frac{\Delta I_L}{8 \times F_{SW} \times C_{OUT}} \tag{24}$$

Where:

- V_r = peak-to-peak output voltage ripple at the switching frequency
- ΔI_L = inductor ripple current from Equation 17.

8.2.2.6 Input Capacitor Considerations

The ceramic input capacitors provide a low impedance source to the regulator in addition to supplying the ripple current and isolating switching noise from other circuits. A minimum of 2.2µF of ceramic capacitance is required on the input of the LM5168E regulator, connected directly between VIN and GND. This must be rated for at least the maximum input voltage that the application requires; preferably twice the maximum input voltage. This capacitance can be increased to help reduce input voltage ripple and maintain the input voltage during load transients. More input capacitance is required for larger output currents. Keep in mind that the value of 2.2µF is the actual value after all derating is applied. For this example, four 1µF, 250V, X7R (or better) ceramic capacitors are chosen due to voltage derating. If larger case size, higher voltage capacitors, or both can be used, then the total number can be reduced. Designs with reduced input voltage range can use capacitors with lower voltage ratings.

Many times, using an electrolytic capacitor on the input in parallel with the ceramics is desirable. This statement is especially true if long leads or traces (greater than about 5cm) are used to connect the input supply to the regulator. The moderate ESR of this capacitor can help damp any ringing on the input supply caused by the long power leads. The use of this additional capacitor also helps with voltage dips caused by input supplies with unusually high impedance.

Most of the input switching current passes through the ceramic input capacitor or capacitors. Use Equation 25 to calculate the approximate RMS current. This value must be checked against the manufacturers' maximum ratings.

$$I_{RMS} \cong \frac{I_{OUT}}{2} \tag{25}$$

The input capacitor is part of the buck converter high di/dt current loop. The high di/dt current, together with excessive parasitic inductance between the IC and the input capacitor, can result in excessive voltage ringing on the SW node of the IC. The placement of the input capacitor on the board is critical for minimizing the parasitic inductance in the high di/dt loop and accordingly minimizing the SW node ringing at each switching transition.

For designs targeting the maximum operating voltage of the regulator, make sure the ringing on the SW node does not exceed the absolute maximum rating of the device. The SW node ringing is a function of how well the input capacitor is positioned with respect to the IC. Refer to the PCB layout example in Figure 8-28 for proper placement of the input capacitors.

8.2.2.7 C_{BST} Selection

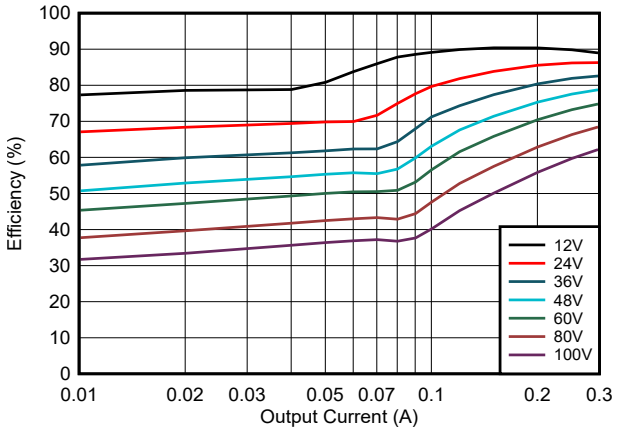
The LM5168E requires a bootstrap capacitor connected between the BST and SW. This capacitor stores energy that is used to supply the gate driver for the high-side MOSFET. A high-quality ceramic capacitor of 2.2nF is required. Be sure to take into account the DC bias derating of the capacitor. The value of C_{BST} must not exceed 2.5nF.

8.2.2.8 Example Design Summary

The preceding design procedure is typical of the steps needed to create a buck regulator with LM5168E. For another example of designing a buck regulator with the LM5168E see the *LM5168PEVM User's Guide*. See also *Related Documentation* for more information about designing COT buck converters.

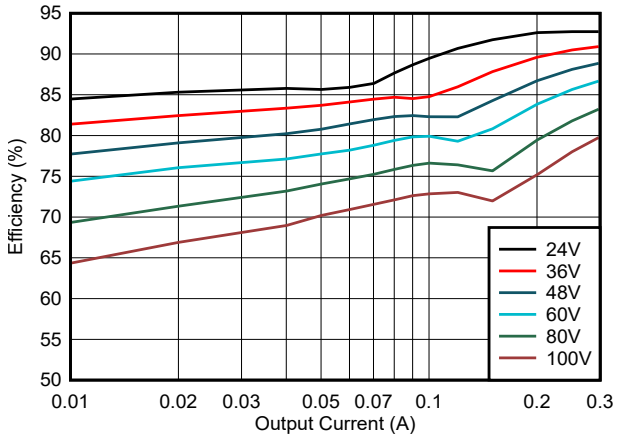
8.2.3 Application Curves

The curves in this section were taken using the LM5168E. Unless otherwise specified, the following conditions apply: T_A = 25°C.



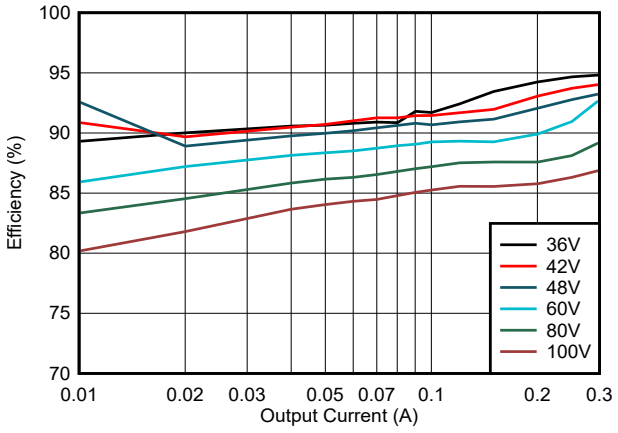
V_{OUT} = 5V F_{SW} = 500kHz

Figure 8-2. Efficiency: V_{OUT} = 5V



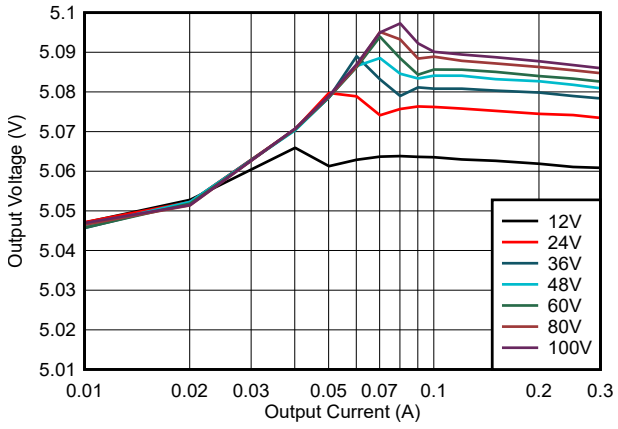
V_{OUT} = 12V F_{SW} = 500kHz

Figure 8-3. Efficiency: V_{OUT} = 12V



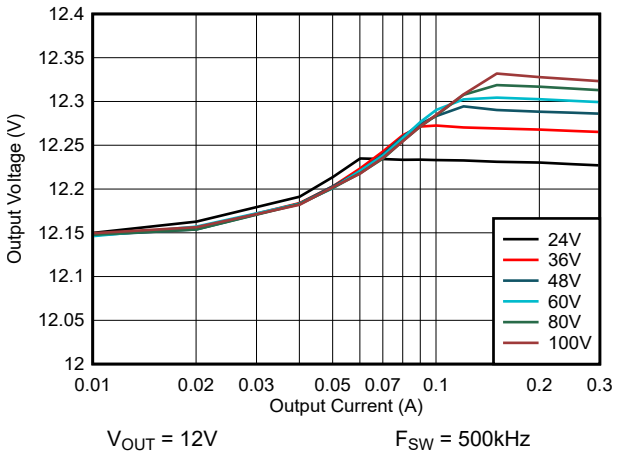
V_{OUT} = 24V F_{SW} = 500kHz

Figure 8-4. Efficiency: V_{OUT} = 24V



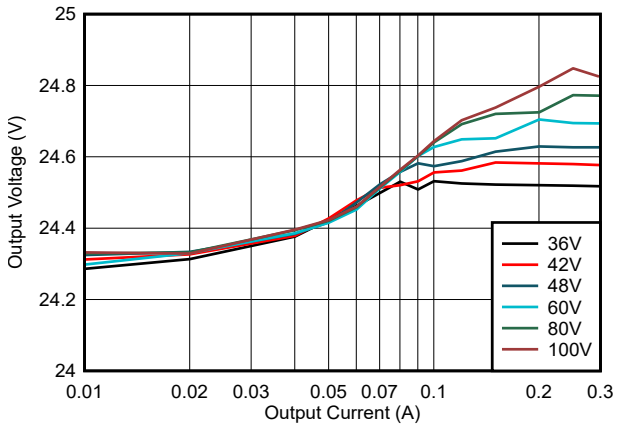
V_{OUT} = 5V F_{SW} = 500kHz

Figure 8-5. Line and Load Regulation: V_{OUT} = 5V



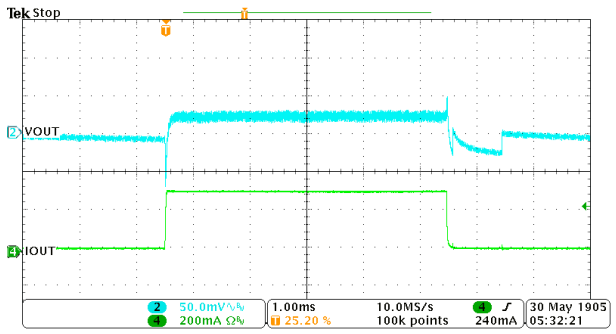
V_{OUT} = 12V F_{SW} = 500kHz

Figure 8-6. Line and Load Regulation: V_{OUT} = 12V



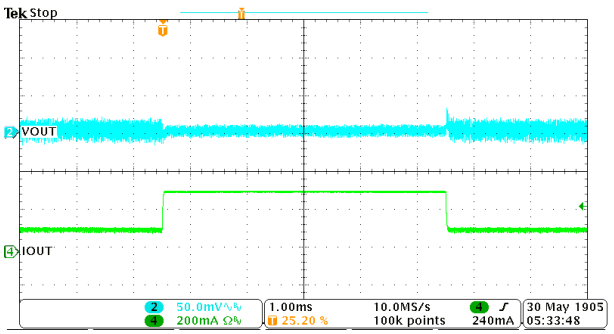
V_{OUT} = 24V F_{SW} = 500kHz

Figure 8-7. Line and Load Regulation: V_{OUT} = 24V



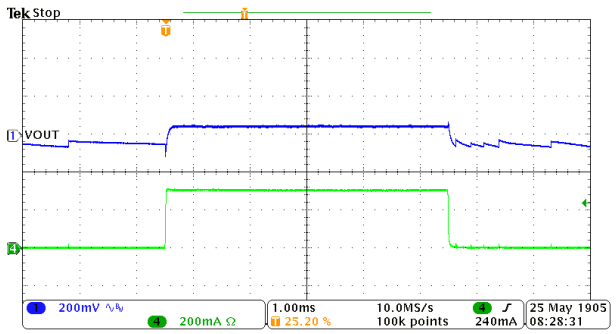
V_{IN} = 48V I_{OUT} = 0A to 0.3A
$t_R = t_F$ = 1µs

Figure 8-8. Load Transient: V_{OUT} = 5V



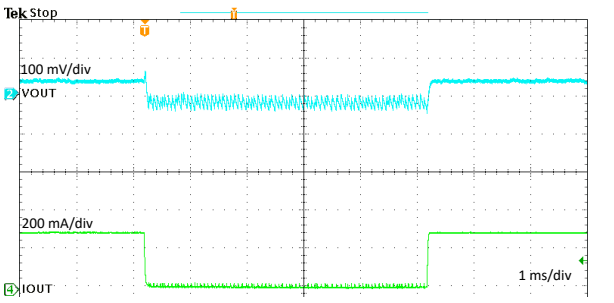
V_{IN} = 48V I_{OUT} = 0.1A to 0.3A
$t_R = t_F$ = 1µs

Figure 8-9. Load Transient: V_{OUT} = 5V



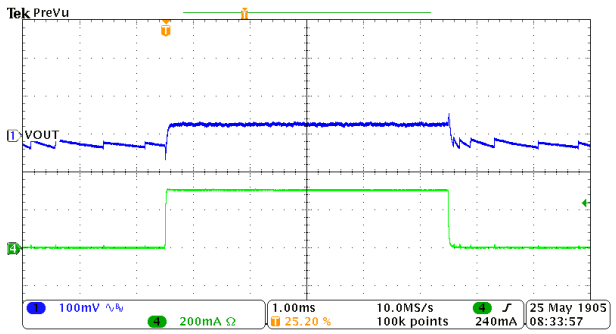
V_{IN} = 48V I_{OUT} = 0A to 0.3A
$t_R = t_F$ = 1µs

Figure 8-10. Load Transient: V_{OUT} = 12V



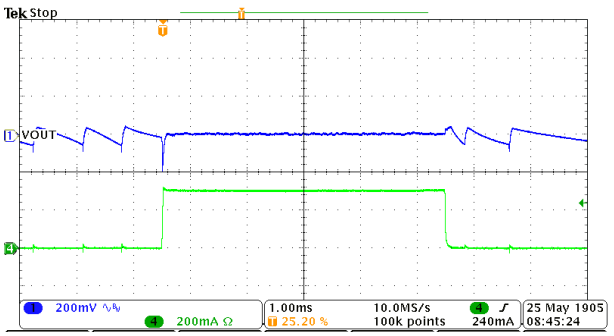
V_{IN} = 24V I_{OUT} = 0A to 0.3A
$t_R = t_F$ = 1µs – 55°C ambient

Figure 8-11. Load Transient: V_{OUT} = 12V



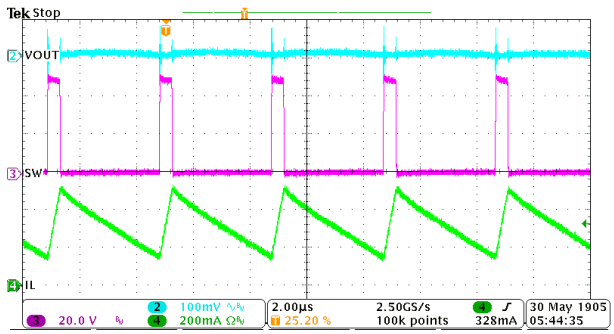
V_{IN} = 24V I_{OUT} = 0A to 0.3A
$t_R = t_F$ = 1µs

Figure 8-12. Load Transient: V_{OUT} = 12V



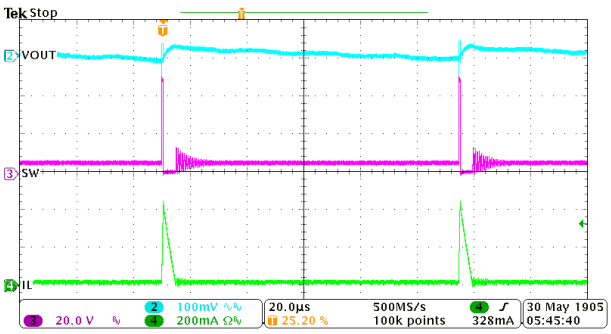
V_{IN} = 36V I_{OUT} = 0A to 0.3A
$t_R = t_F$ = 1µs

Figure 8-13. Load Transient: V_{OUT} = 24V



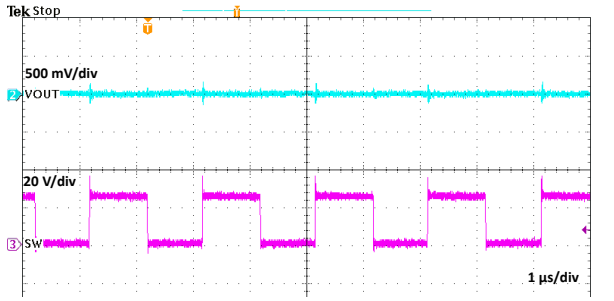
V_{IN} = 48V
I_{OUT} = 300mA
V_{OUT} = 5V
F_{SW} = 500kHz

Figure 8-14. Typical Switching Waveforms



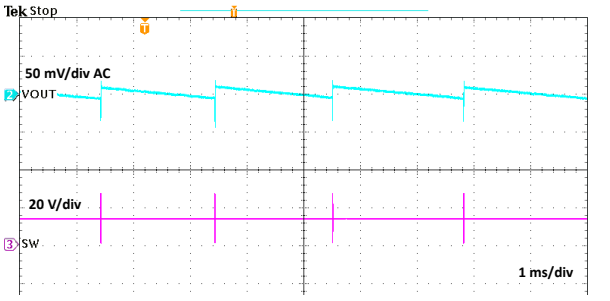
V_{IN} = 48V
I_{OUT} = 10mA
V_{OUT} = 5V
F_{SW} = 500kHz

Figure 8-15. Typical Switching Waveforms



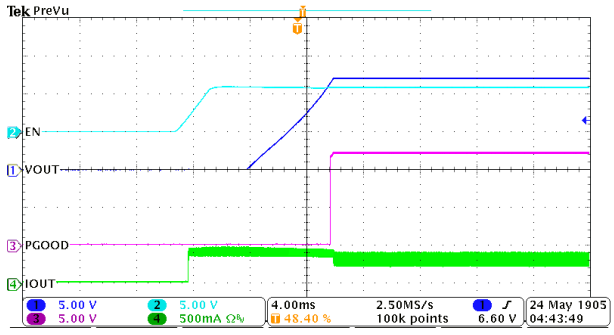
V_{IN} = 24V
I_{OUT} = 300mA
V_{OUT} = 12V
– 55°C ambient

Figure 8-16. Typical Extended Temp Switching Waveforms



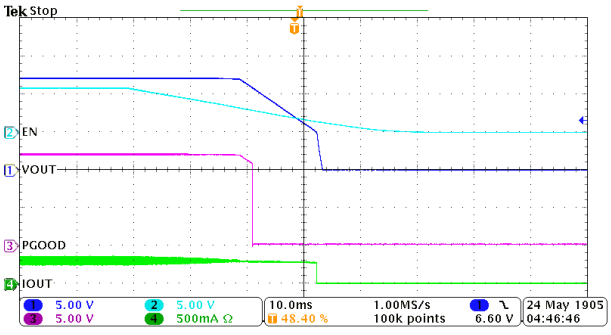
V_{IN} = 24V
I_{OUT} = 10mA
V_{OUT} = 12V
-55°C ambient

Figure 8-17. Typical Extended Temp Switching Waveforms



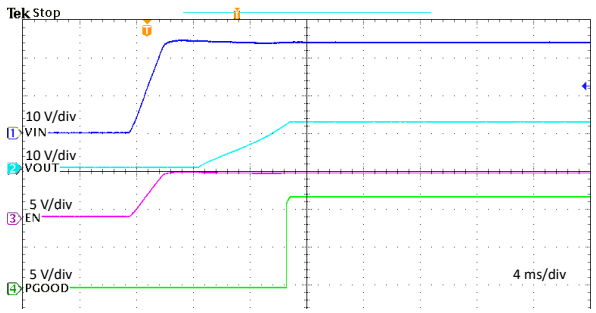
V_{IN} = 48V
I_{OUT} = 300mA
V_{OUT} = 5V

Figure 8-18. Typical Start-up Waveforms



V_{IN} = 48V
I_{OUT} = 300mA
V_{OUT} = 5V

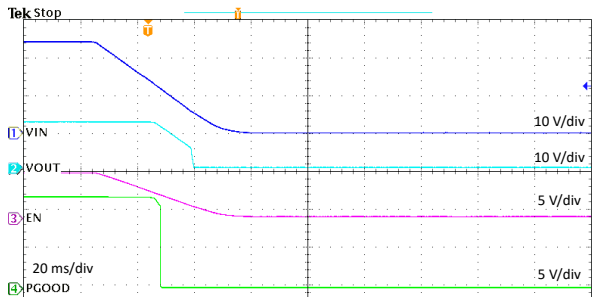
Figure 8-19. Typical Shutdown Waveforms



V_{IN} = 24V
I_{OUT} = 300mA

V_{OUT} = 12V
-55°C ambient

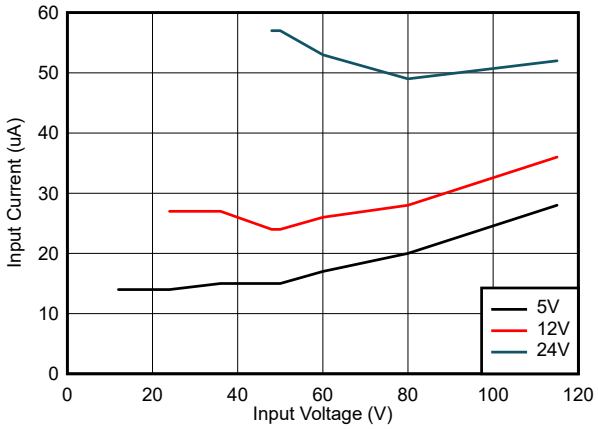
Figure 8-20. Typical Extended Temp Start-up Waveforms



V_{IN} = 24V
I_{OUT} = 300mA

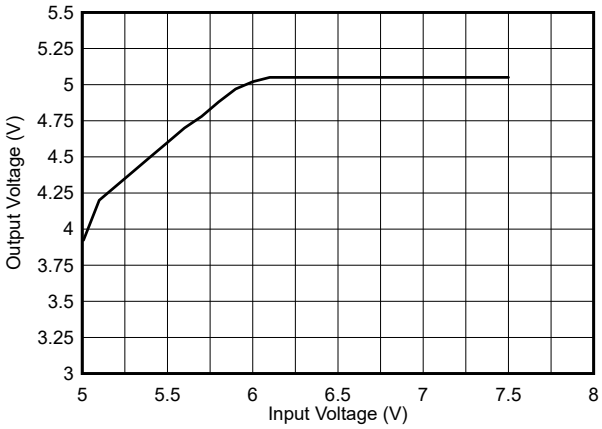
V_{OUT} = 12V
-55°C ambient

Figure 8-21. Typical Extended Temp Shutdown Waveforms



I_{OUT} = 0A

Figure 8-22. No-Load Input Supply Current



I_{OUT} = 300mA

Figure 8-23. Drop-Out Response

Table 8-2. BOM for Application Curves

V_{OUT}	R_A	R_{FBB}	R_{FBT}	C_A	C_B	C_{OUT}	L
5V	121kΩ	143kΩ	453kΩ	3300pF	56pF	2 × 22µF	68µH, 0.17Ω
12V	182kΩ	49.9kΩ	453kΩ	3300pF	56pF	2 × 22µF	68µH, 0.17Ω
24V	243kΩ	23.7kΩ	453kΩ	3300pF	56pF	2 × 22µF	68µH, 0.17Ω

8.3 Power Supply Recommendations

The LM5168E buck converter is designed to operate from a wide input voltage range between 6V and 115V. The characteristics of the input supply must be compatible with the *Absolute Maximum Ratings* and *Recommended Operating Conditions* tables. In addition, the input supply must be capable of delivering the required input current to the fully loaded regulator. Use Equation 26 to estimate the average input current.

$$I_{IN} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (26)$$

where

η = efficiency

If the converter is connected to an input supply through long wires or PCB traces with a large impedance, the parasitic inductance and resistance of the input cables can have an adverse affect on converter operation. The parasitic inductance in combination with the low-ESR ceramic input capacitors form an under-damped resonant circuit. This circuit can cause overvoltage transients at VIN each time the input supply is cycled ON and OFF. The parasitic resistance causes the input voltage to dip during a load transient. If the converter is operating close to the minimum input voltage, this dip can cause false UVLO fault triggering and a system reset. The best way to solve such issues is to reduce the distance from the input supply to the regulator and use an aluminum electrolytic input capacitor in parallel with the ceramics. The moderate ESR of the electrolytic capacitor helps to damp the input resonant circuit and reduce any voltage overshoots. A 10µF electrolytic capacitor with a typical ESR of 0.5Ω provides enough damping for most input circuit configurations.

An EMI input filter is often used in front of the regulator that, unless carefully designed, can lead to instability as well as some of the effects mentioned above. The *AN-2162 Simple Success With Conducted EMI From DCDC Converters* application note provides helpful suggestions when designing an input filter for any switching regulator.

8.4 Layout

8.4.1 Layout Guidelines

PCB layout is a critical portion of good power supply design. There are several paths that conduct high slew-rate currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise and EMI or degrade the power supply performance.

- Bypass the VIN pin to GND with a low-ESR ceramic bypass capacitor with a high-quality dielectric to help eliminate these problems. Place C_{IN} as close as possible to the LM5168E VIN and GND pins. Grounding for both the input and output capacitors must consist of localized top-side planes that connect to the GND pin and GND PAD.
- Minimize the loop area formed by the input capacitor connections to the VIN and GND pins. The input capacitor is part of the buck converter high di/dt current loop. The high di/dt current, together with excessive parasitic inductance between the IC and the input capacitor, can result in excessive voltage ringing on the SW node of the IC. The placement of the input capacitor on the board is critical for minimizing the parasitic inductance in the high di/dt loop and accordingly minimizing the SW node ringing at each switching. For designs targeting the maximum operating voltage of the regulator, make sure the ringing on the SW node does not exceed the absolute maximum rating of the device. The SW node voltage ringing is a function of how well the input capacitor is positioned with respect to the IC. Refer to the PCB layout example in Figure 8-28 for proper placement of the input capacitors.
- Locate the inductor close to the SW pin. Minimize the area of the SW trace or plane to prevent excessive capacitive coupling.
- Tie the GND pin directly to the power pad under the device and to a heat-sinking PCB ground plane.
- Use a ground plane in one of the middle layers as a noise shielding and heat dissipation path.
- Have a single-point ground connection to the plane. Route the ground connections for the feedback, and enable components to the ground plane. This action prevents any switched or load currents from flowing in analog ground traces. If not properly handled, poor grounding results in degraded load regulation or erratic output voltage ripple behavior.

- Make V_{IN}, V_{OUT}, and ground bus connections as wide as possible. This guidelines reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
- Minimize the trace length to the FB pin. Place both feedback resistors, R_{FB1} and R_{FB2}, close to the FB pin. Place C_{FF} (if used) directly in parallel with R_{FB1}. If output setpoint accuracy at the load is important, connect the V_{OUT} sense at the load. Route the V_{OUT} sense path away from noisy nodes and preferably through a layer on the other side of a grounded shielding layer.
- Note that the R_T pin is sensitive to noise. Therefore, locate the R_T resistor as close as possible to the device and route with minimal lengths of trace. The parasitic capacitance from RT to GND must not exceed 20pF.
- Provide adequate heat sinking for the LM5168E to keep the junction temperature below 150°C. For operation at full rated load, the top-side ground plane is an important heat-dissipating area. Use an array of heat-sinking vias to connect the exposed pad to the PCB ground plane. If the PCB has multiple copper layers, these thermal vias must also be connected to inner layer heat-spreading ground planes.

8.4.1.1 Compact PCB Layout for EMI Reduction

Radiated EMI generated by high di/dt components relates to pulsing currents in switching converters. The larger the area covered by the path of a pulsing current, the more electromagnetic emission is generated. The key to minimizing radiated EMI is to identify the pulsing current path and minimize the area of that path. Figure 8-24 shows the critical switching loop of the buck converter power stage in terms of EMI. The topological architecture of a buck converter means that a particularly high di/dt current path exists in the loop comprising the input capacitor and the integrated MOSFETs of the LM5168E, and reducing the parasitic inductance of this loop by minimizing the effective loop area becomes mandatory.

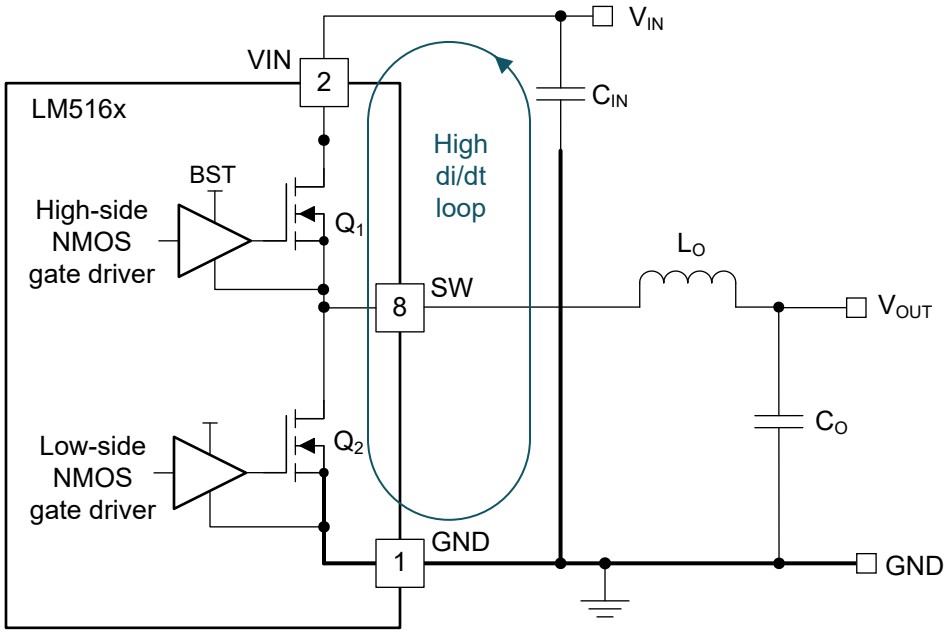


Figure 8-24. Critical Current Loops in the Buck Converter

The input capacitor provides the primary path for the high di/dt components of the current of the high-side MOSFET. Placing a ceramic capacitor as close as possible to the VIN and GND pins is the key to EMI reduction. Keep the trace connecting SW to the inductor as short as possible and just wide enough to carry the load current without excessive heating. Use short, thick traces or copper pours (shapes) for current conduction path to minimize parasitic resistance. Place the output capacitor close to the V_{OUT} side of the inductor, and connect the return terminal of the capacitor to the GND pin and exposed PAD of the LM5168E.

8.4.1.2 Feedback Resistors

Reduce noise sensitivity of the output voltage feedback path by placing the resistor divider close to the FB pin, rather than close to the load. This reduces the trace length of FB signal and noise coupling. The FB pin is the

input to the feedback comparator, and as such, is a high-impedance node sensitive to noise. The output node is a low-impedance node, so the trace from V_{OUT} to the resistor divider can be long if a short path is not available.

Route the voltage sense trace from the load to the feedback resistor divider, keeping away from the SW node, the inductor, and V_{IN} to avoid contaminating the feedback signal with switch noise, while also minimizing the trace length. This is most important when high feedback resistances greater than 100kΩ are used to set the output voltage. Also, route the voltage sense trace on a different layer from the inductor, SW node, and V_{IN} so there is a ground plane that separates the feedback trace from the inductor and SW node copper polygon. This action provides further shielding for the voltage feedback path from switching noise sources.

8.4.2 Thermal Considerations

As with any power conversion device, the LM5168E dissipates internal power while operating. The effect of this power dissipation is to raise the internal temperature of the converter above ambient. The internal die temperature (T_J) is a function of the following:

- Ambient temperature
- Power loss
- Effective thermal resistance, $R_{\theta JA}$, of the application
- PCB layout

The maximum internal die temperature for the LM5168E must be limited to 150°C. This limit establishes a limit on the maximum device power dissipation and, therefore, the load current. Equation 27 shows the relationships between the important parameters. Seeing that larger ambient temperatures (T_A) and larger values of $R_{\theta JA}$ reduce the maximum available output current. The converter efficiency can be estimated by using the curves provided in this data sheet. Note that these curves include the power loss in the inductor. If the desired operating conditions cannot be found in one of the curves, then interpolation can be used to estimate the efficiency. Alternatively, the EVM can be adjusted to match the desired application requirements and the efficiency can be measured directly. The correct value of $R_{\theta JA}$ is more difficult to estimate. As stated in the *Semiconductor and IC Package Thermal Metrics* application note, the value of $R_{\theta JA}$ given in the *Thermal Information* table is not valid for design purposes and must not be used to estimate the thermal performance of the application. The values reported in that table were measured under a specific set of conditions that are rarely obtained in an actual application. The data given for $R_{\theta JC(bott)}$ and Ψ_{JT} can be useful when determining thermal performance. The value of $R_{\theta JA(EVM)}$ is applicable to the LM5168PEVM and is given for reference only. See also the *Semiconductor and IC Package Thermal Metrics* application note for more information and the resources given at the end of this section.

$$I_{OUT}\Big|_{MAX} = \frac{(T_J - T_A)}{R_{\theta JA}} \times \frac{\eta}{(1-\eta)} \times \frac{1}{V_{OUT}} \tag{27}$$

where

η is the efficiency.

The effective $R_{\theta JA}$ is a critical parameter and depends on many factors, such as the following:

- Power dissipation
- Air temperature, flow
- PCB area
- Copper heat-sink area
- Number of thermal vias under the package
- Adjacent component placement

The LM5168E features a die attach paddle, or "exposed pad" (EP), to provide a place to solder down to the PCB heat-sinking copper. This provides a good heat conduction path from the regulator junction to the heat sink and must be properly soldered to the PCB heat sink copper. Typical examples of $R_{\Theta JA}$ can be found in Figure 8-25. The copper area given in the graph is for each layer. The top and bottom layers are 2oz copper each, while the inner layers are 1oz.

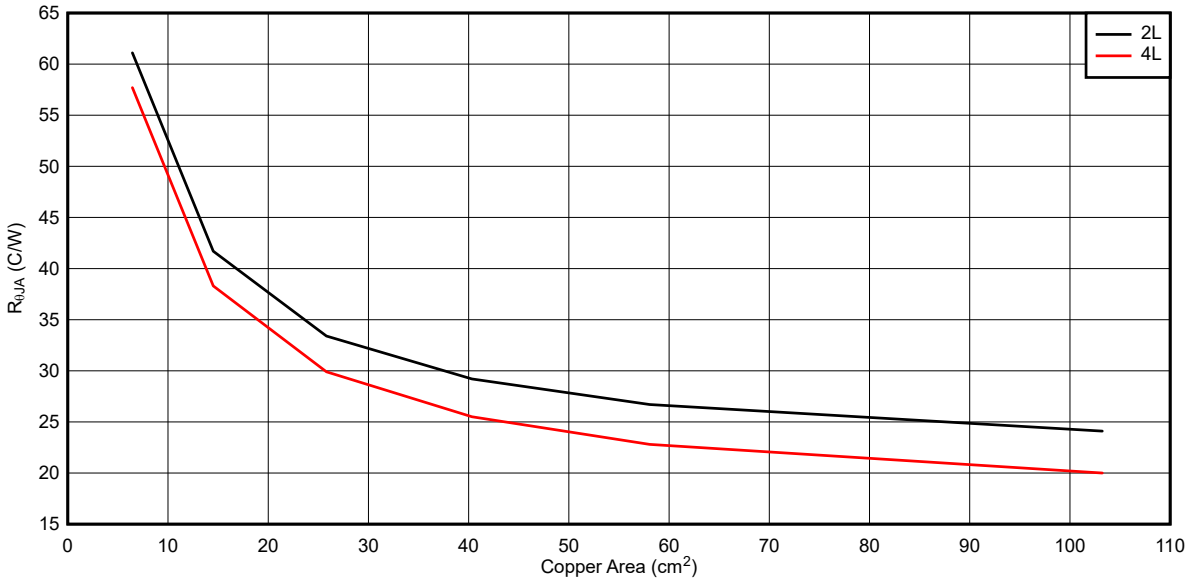


Figure 8-25. Typical $R_{\Theta JA}$ Versus Copper Area for DDA package

Use the data in Figure 8-26 and Figure 8-27 as a guide to determine the maximum output current for a given set of conditions. The particular conditions under which these graphs were taken are indicated in the notes following each graph.

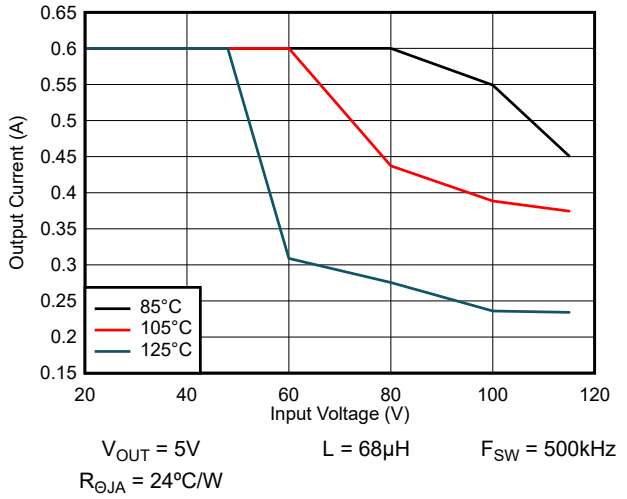


Figure 8-26. Maximum Output Current: VOUT = 5V

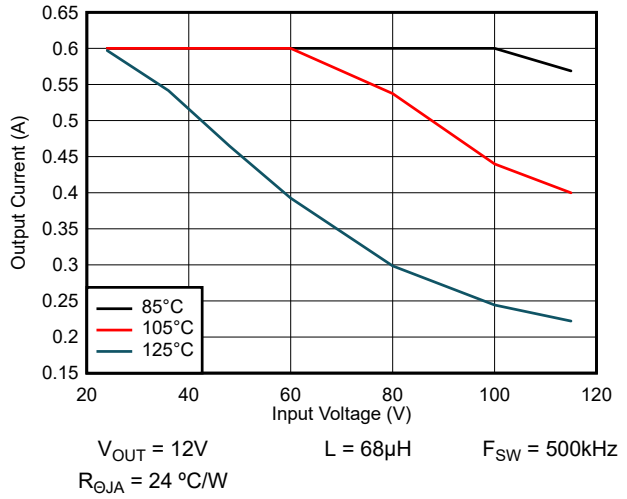


Figure 8-27. Maximum Output Current: VOUT = 12V

Remember that the data given in Figure 8-25 through Figure 8-27 is for illustration purposes only, and the actual performance in any given application depends on all of the previously mentioned factors.

The following resources can be used as a guide to excellent thermal PCB design and estimating $R_{\theta JA}$ for a given application environment:

- *LM501x Thermals and Example PCB Design* application note
- *Semiconductor and IC Package Thermal Metrics* application note
- *AN-2020 Thermal Design By Insight, Not Hindsight* application note
- *A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages* application note
- *Using New Thermal Metrics* application note
- *PCB Thermal Design Tips for Automotive DC/DC Converters* application note

8.4.3 Layout Example

Figure 8-28 shows an example layout using DDA package for the PCB top layer with essential components placed on the top side.

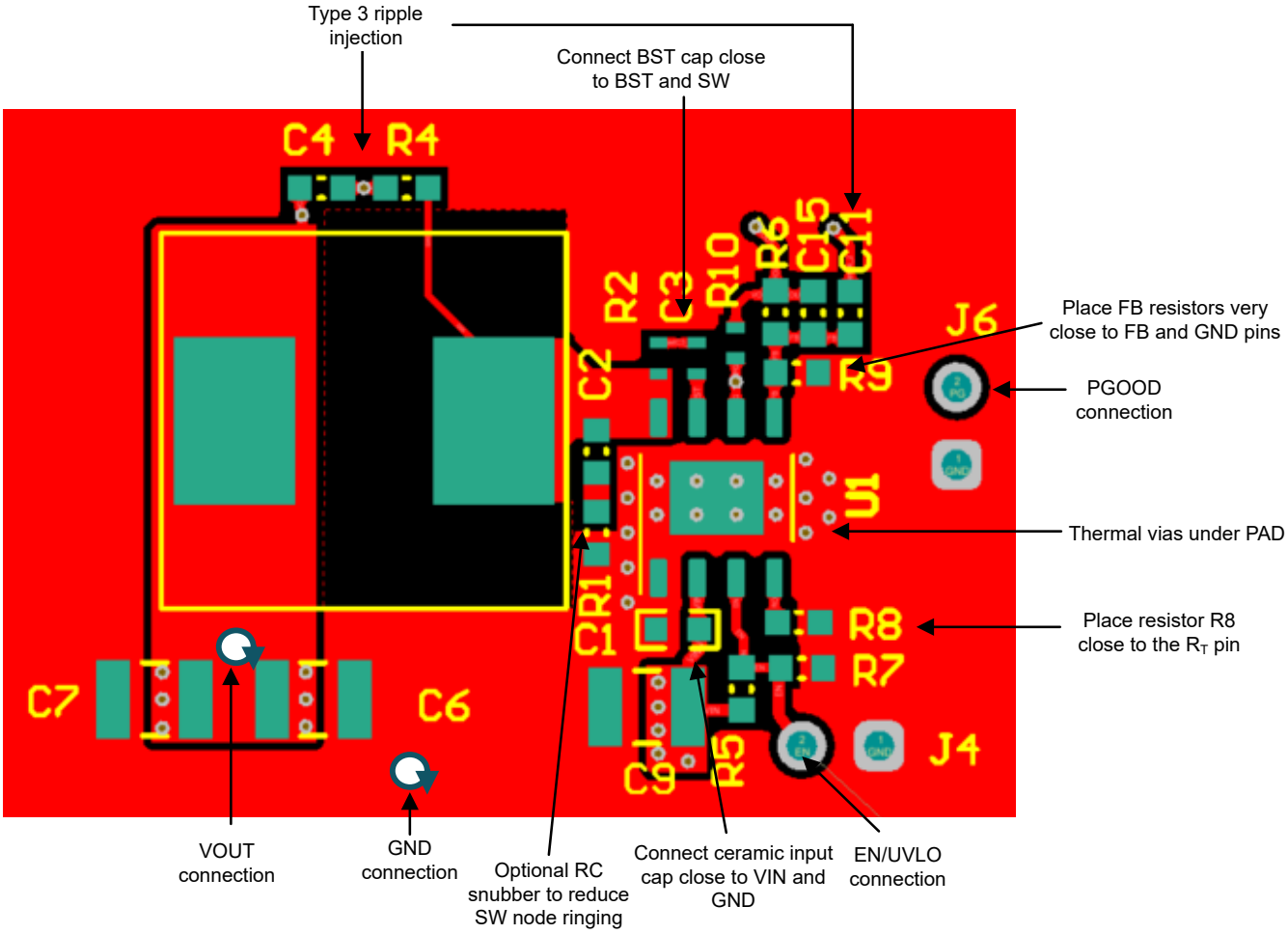


Figure 8-28. LM5168E PCB Layout Example for DDA package

9 Device and Documentation Support

9.1 Device Support

9.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Stability Analysis of COT Type-III Ripple Circuit* application note
- Texas Instruments, *Designing an Isolated Fly-buck Converter* application note
- Texas Instruments, *Design a Fly-buck Solution with Opto-coupler* application note
- Texas Instruments, *Designing an Isolated Fly-buck Converter Using the LMR36520* application note
- Texas Instruments, *Selecting an Ideal Ripple Generation Network for Your COT Buck Converter* application note
- Texas Instruments, *Valuing Wide V_{IN}, Low-EMI Synchronous Buck Circuits for Cost-Effective, Demanding Applications* white paper
- Texas Instruments, *An Overview of Conducted EMI Specifications for Power Supplies* white paper
- Texas Instruments, *An Overview of Radiated EMI Specifications for Power Supplies* white paper
- Texas Instruments, *24V AC Power Stage with Wide V_{IN} Converter and Battery Gauge for Smart Thermostat* design guide
- Texas Instruments, *Accurate Gauging and 50µA Standby Current, 13S, 48-V Li-ion Battery Pack Reference* design guide
- Texas Instruments, *AN-2162: Simple Success with Conducted EMI from DC/DC Converters application report*
- Texas Instruments, *Powering Drones with a Wide V_{IN} DC/DC Converter* application note
- Texas Instruments, *Using New Thermal Metrics* application note

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

DATE	REVISION	NOTES
August 2025	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM5168PEDDAR	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 150	5168PET

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

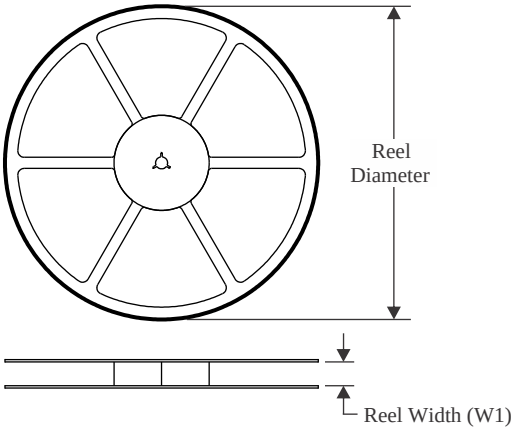
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

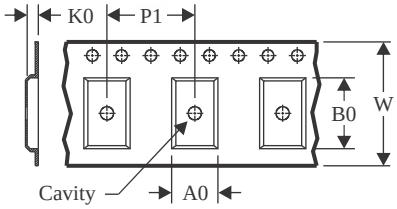
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

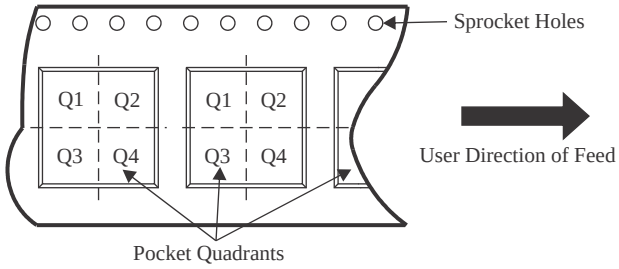


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

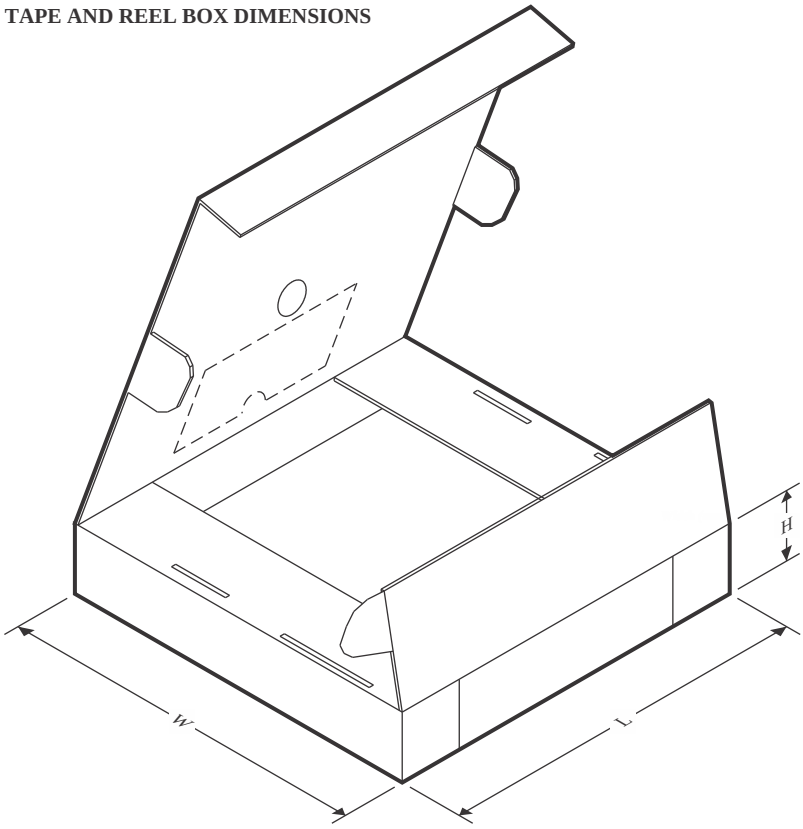
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5168PEDDAR	SO PowerPAD	DDA	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

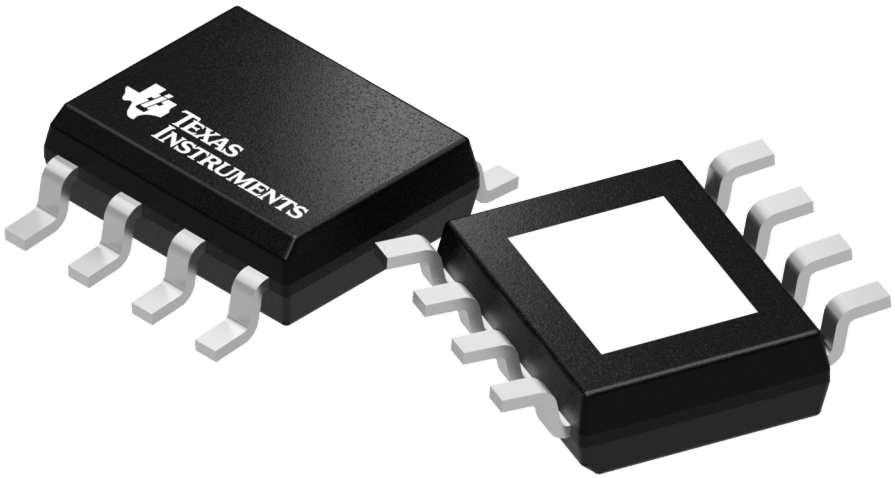


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5168PEDDAR	SO PowerPAD	DDA	8	2500	353.0	353.0	32.0

DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



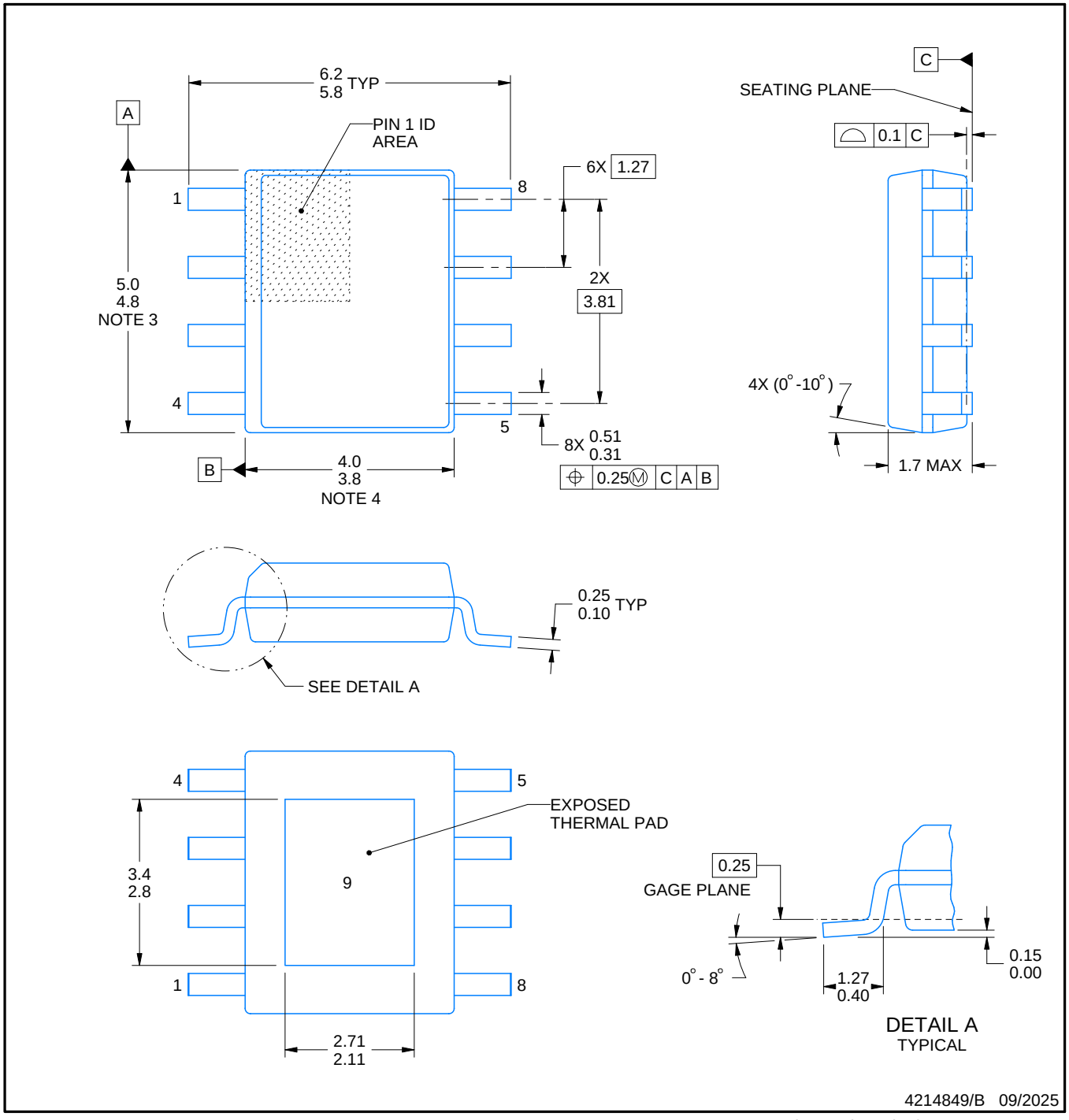
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



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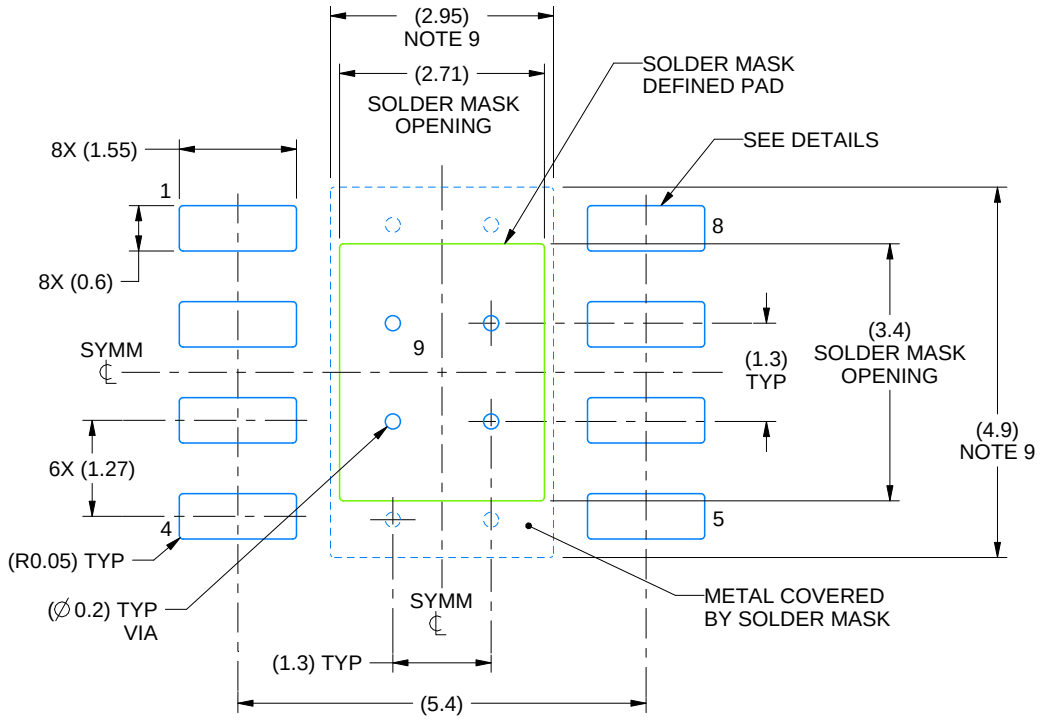
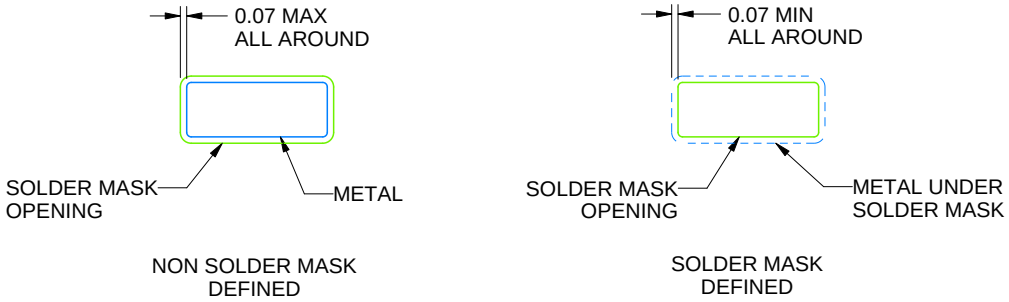
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
PADS 1-8

4214849/B 09/2025

NOTES: (continued)

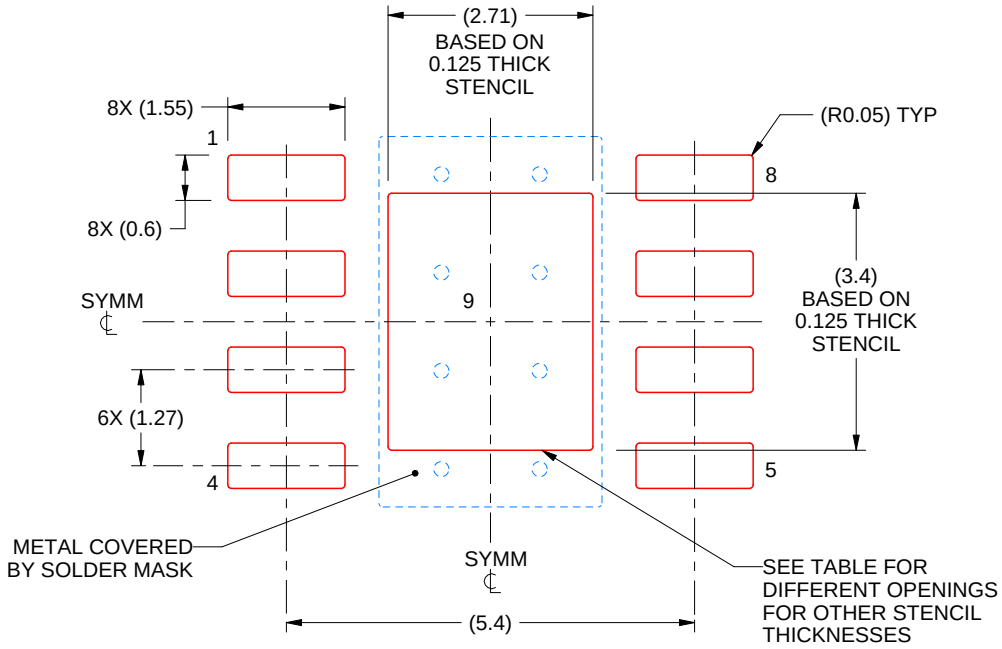
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.03 X 3.80
0.125	2.71 X 3.40 (SHOWN)
0.150	2.47 X 3.10
0.175	2.29 X 2.87

4214849/B 09/2025

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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