LM654B0-Q1 Pin-Compatible 20A (25A Peak) ZEN 1 Stackable Automotive Buck Converter

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
- Built in clocking for stacking of converters
- Internal or external compensation
- Pin selectable output voltage 3.3V and 5V fixed or adjustable from 0.8V to 0.9 × V_{IN}
- Wide input voltage range: 3V to 36V
- ZEN 1 switcher technology
  - Optimized for low EMI requirements
  - Facilitates CISPR 25 Class 5 CISPR 11 Class B compliance
  - Enhanced HotRod™ QFN package with symmetrical pinout
- Switching frequency from 300kHz to 2.2MHz
  - Pin-configurable AUTO or FPWM operation
  - Synchronizable with external clock
- Low minimum on time: 40ns (maximum)
  - Enables 36V to 3.3V conversion at 2.2MHz
- High-efficiency and high power density

2 Applications

- Advanced driver assistance systems (ADAS)
- Automotive infotainment and cluster
- Hybrid, electric, and powertrain systems
- Medical imaging systems
- Test and measurement systems
- Wireless infrastructure systems

3 Description

The LM654B0-Q1 is a buck converter designed for high efficiency, high power density, and low EMI performance with ZEN switcher technology for automotive applications. The converter operates over a wide input voltage range of 3V to 36V with pin selectable fixed output voltages of 3.3V and 5V or an adjustable output.

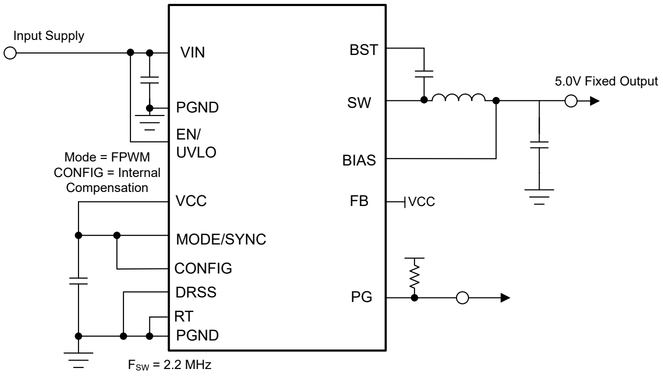
The low EMI operation is enabled with minimized loop inductance, optimized SW node slew-rate, and dual-random spread spectrum (DRSS). The DRSS significantly reduces peak emissions through a combination of triangular and pseudo-random modulation while keeping output voltage ripple very low.

The current-mode control architecture with 32ns typical minimum on-time allows high conversion ratios at high frequencies, fast transient response, and excellent load and line regulation.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LM654B0-Q1	VDA (WQFN-FCRLF, 26)	4.5mm × 4.5mm

(1) For more information, see Section 7.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

Table of Contents

4 Device Comparison Table

DEVICE	ORDERABLE PART NUMBER	ENGINEERING PART NUMBER	RATED OUTPUT CURRENT	TOP-SIDE EXPOSED THERMAL PAD	BOTTOM EXPOSED THERMAL PAD	PACKAGE	JUNCTION TEMPERATURE RANGE
LM654B0-Q1	LM654B0VDARQ1	PLM654B0VDARQ1	20	YES	YES	VDA (26)	–40°C to 150°C

5 Device and Documentation Support

5.1 Device Support

5.1.1 Third-Party Products Disclaimer

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5.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

5.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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5.4 Trademarks

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5.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

5.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

6 Revision History

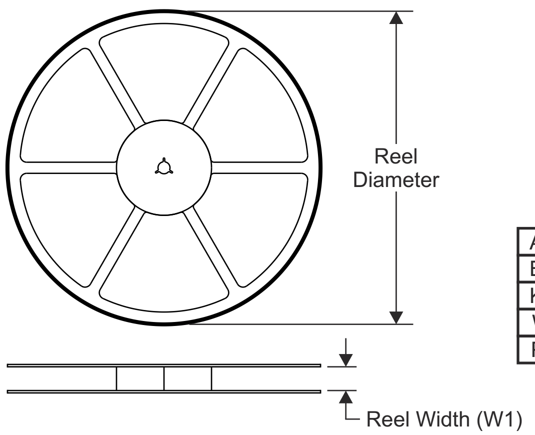
DATE	REVISION	NOTES
November 2025	*	Initial Release

7 Mechanical, Packaging, and Orderable Information

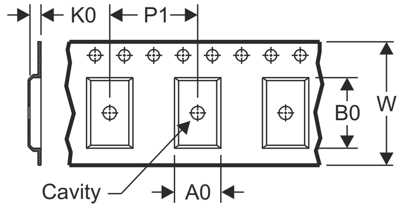
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Tape and Reel Information

REEL DIMENSIONS

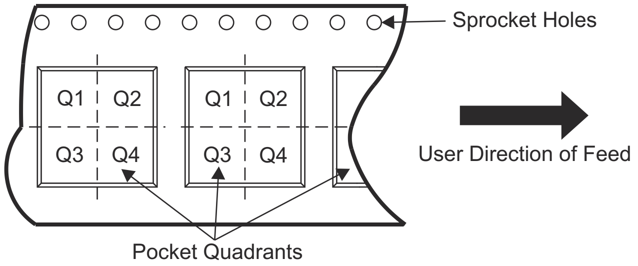


TAPE DIMENSIONS



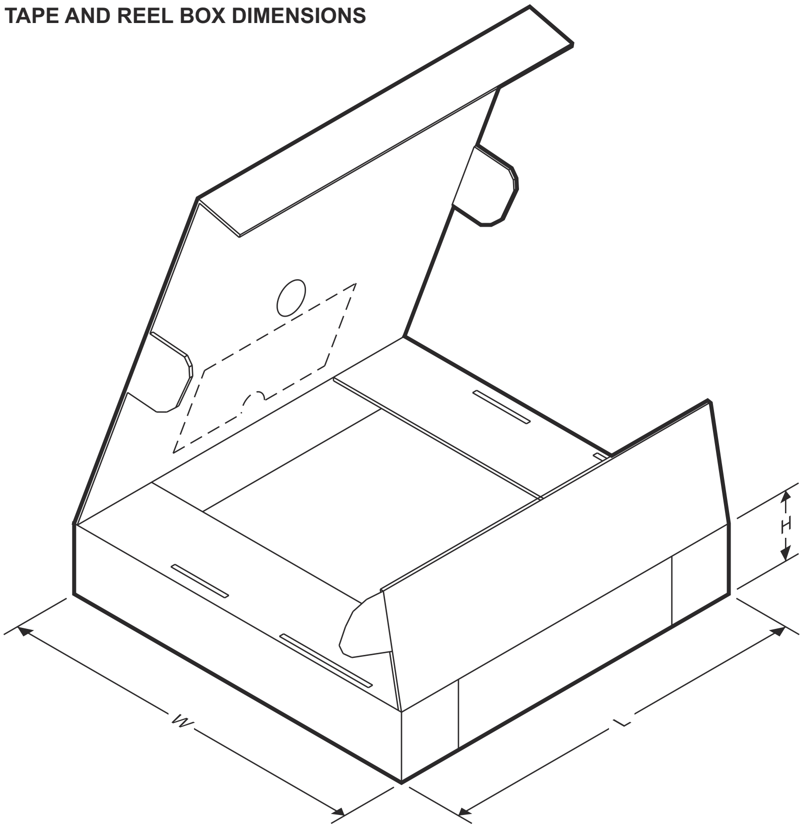
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PLM654B0VDARQ1	WQFN-FCRLF	VDA	26	3000	330	12.4	4.8	4.8	1.4	8.0	12	Q2

TAPE AND REEL BOX DIMENSIONS



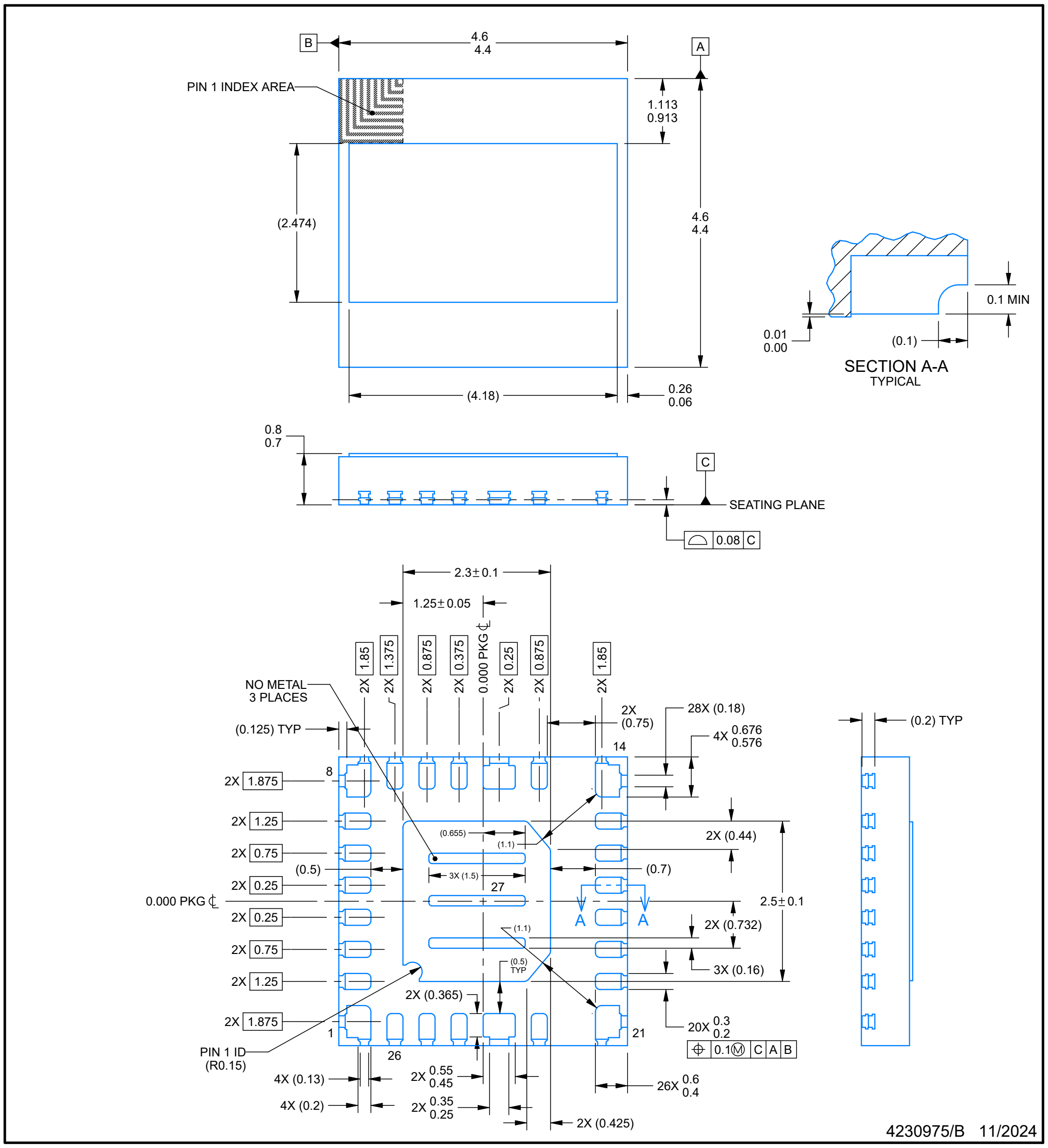
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PLM654B0VDARQ1	WQFN-FCRLF	VDA0026A	26	3000	346	346	33

PACKAGE OUTLINE

VDA0026A

WQFN-FCRLF - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

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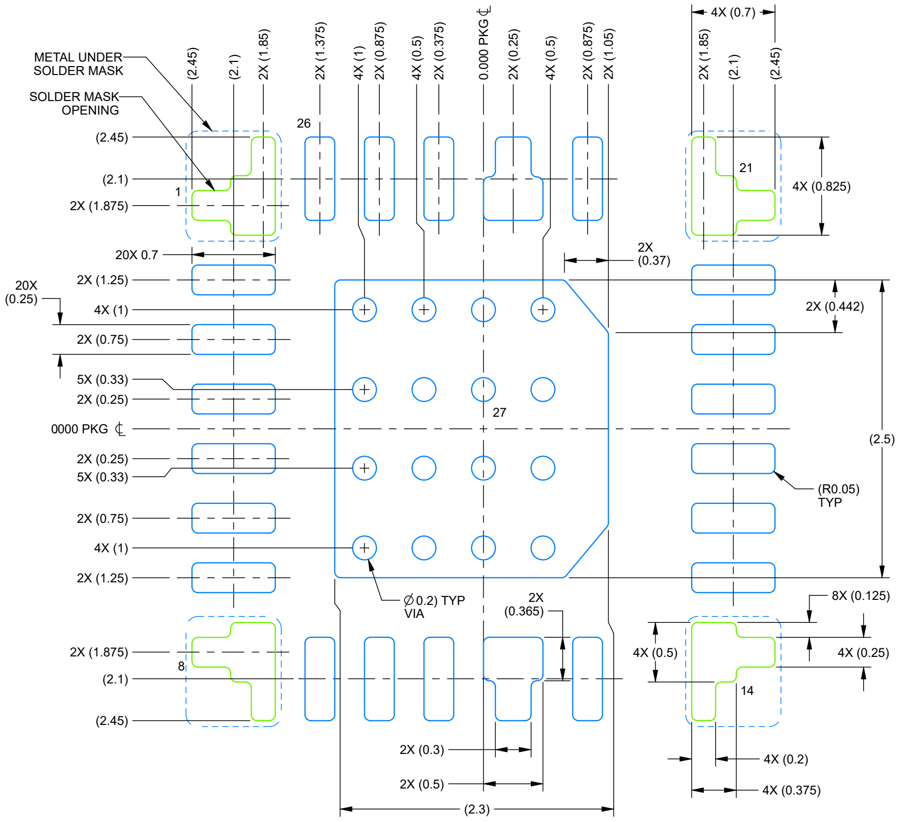
EXAMPLE BOARD LAYOUT

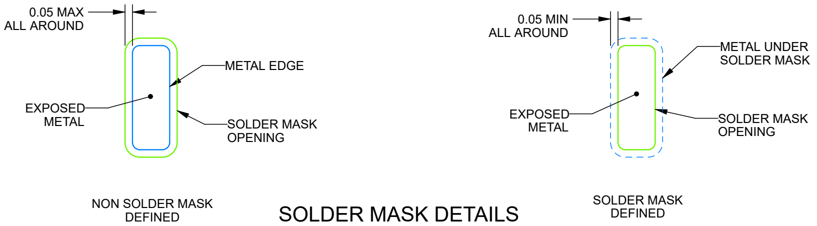
VDA0026A

WQFN-FCRLF - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

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NOTES: (continued)

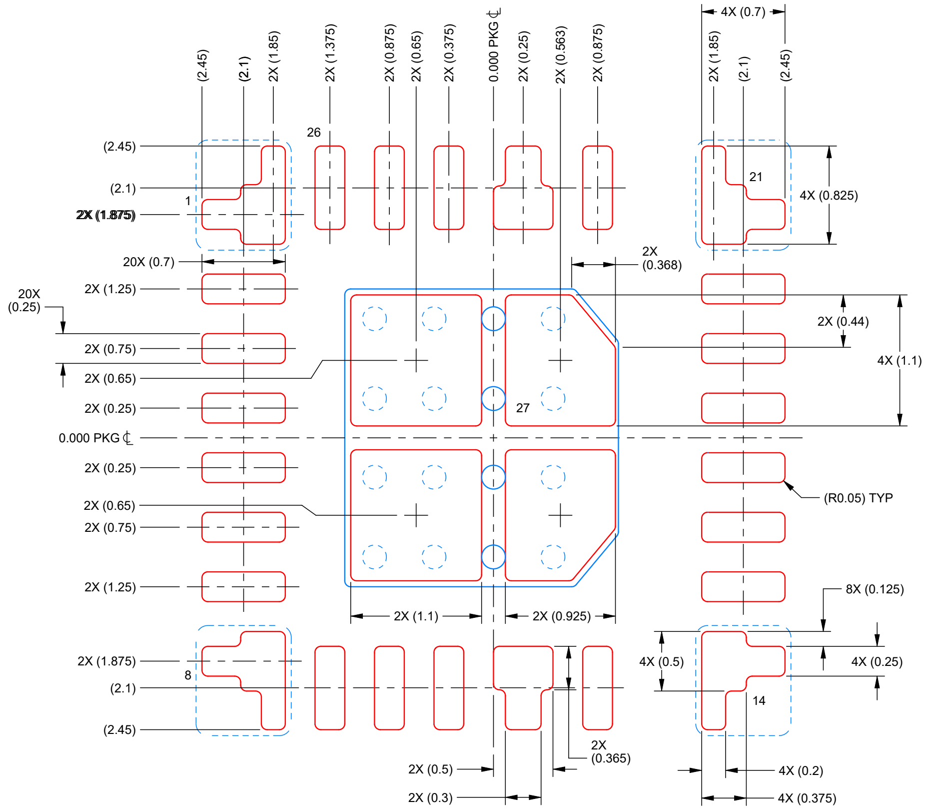
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

VDA0026A

WQFN-FCRLF - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PAD 27: 84%

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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ADVANCE INFORMATION

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PLM654B0VDARQ1	Active	Preproduction	WQFN-FCRLF (VDA) | 26	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 150	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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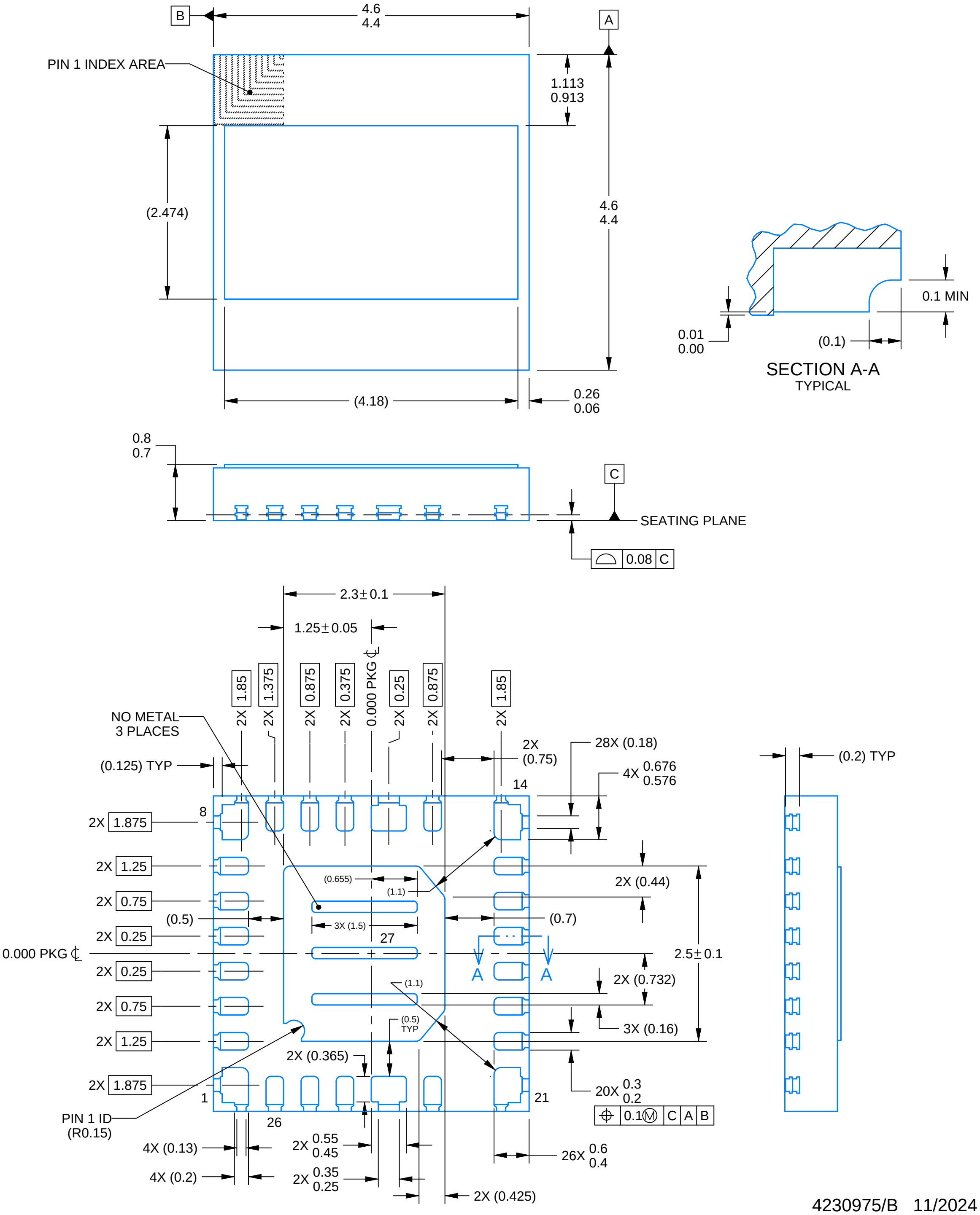

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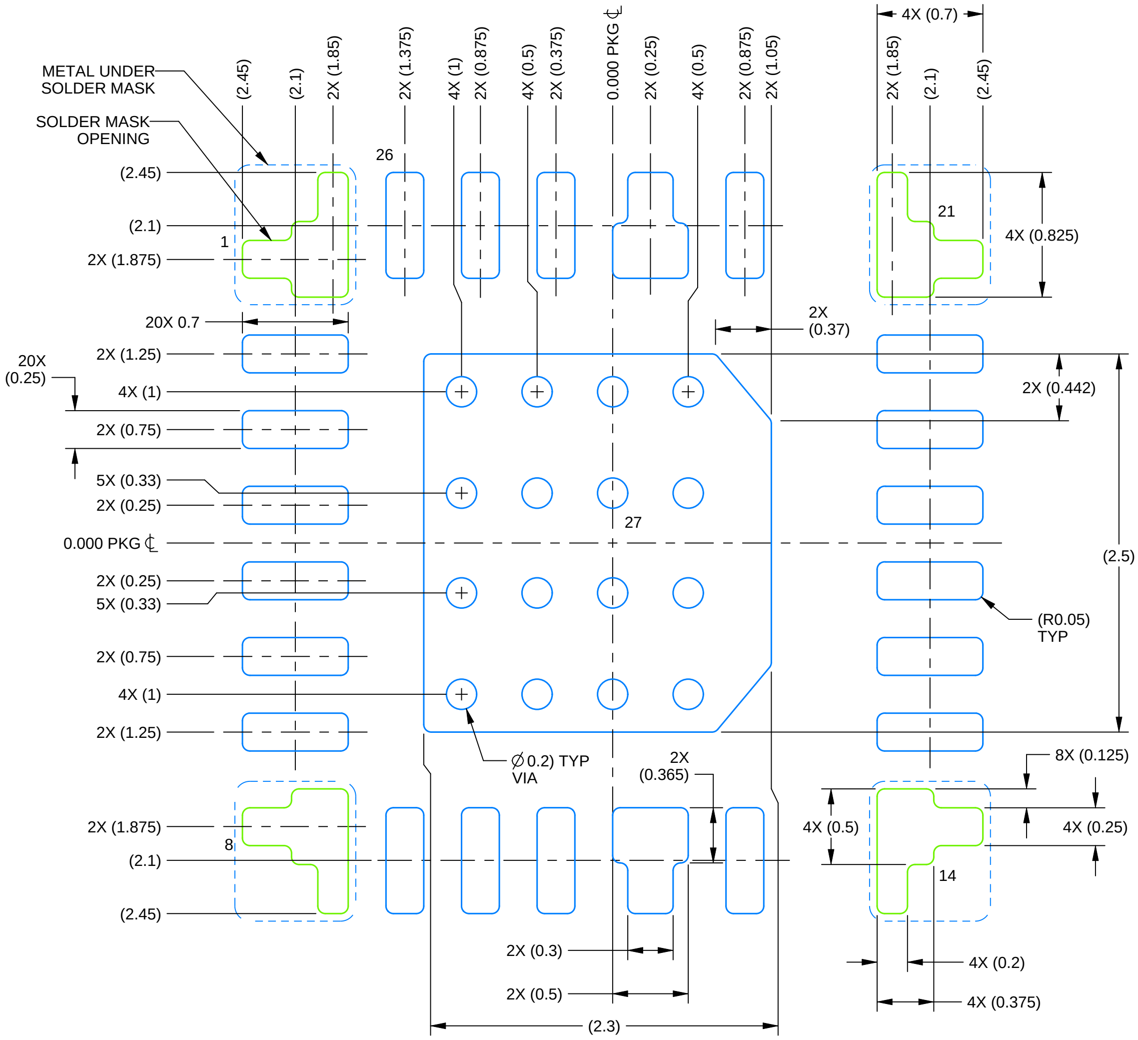

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

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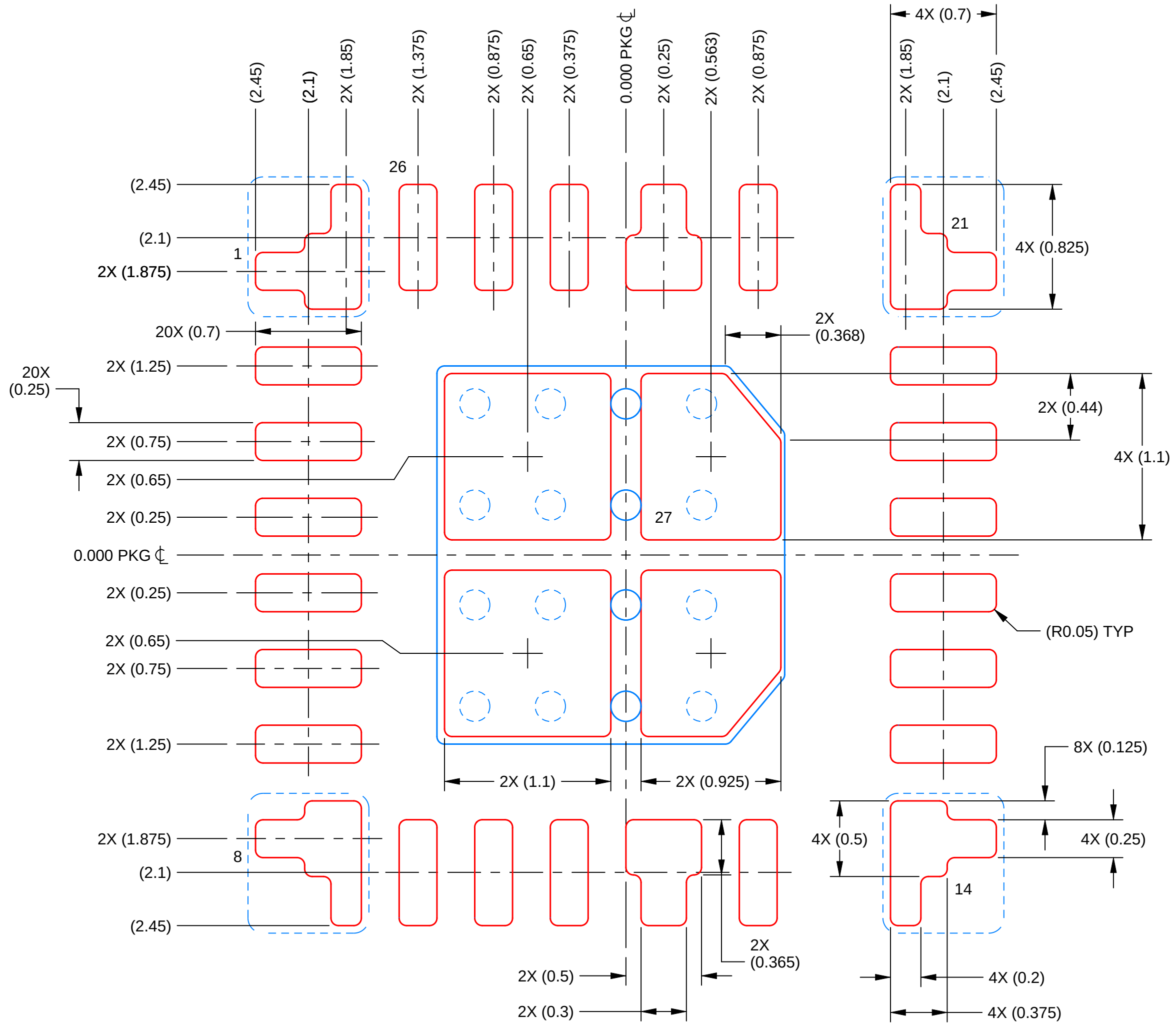

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PAD 27: 84%

NOTES: (continued)

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Last updated 10/2025