LM8261 Single RRIO High Output Current and Unlimited Cap Load Op Amp

1 Features

- GBWP: 24MHz
- Wide supply voltage range: 2.7V to 32V
- Slew rate: 35V/µs
- Supply current: 1.35mA
- Unlimited Cap Load Drive
- Output short circuit current: ±125mA
- Rail to Rail Input and Output: 3V
- Input voltage noise: 12nV/ $\sqrt{\text{Hz}}$
- Input current noise: 1pA/ $\sqrt{\text{Hz}}$
- THD+N < 0.00022%

2 Applications

- TFT-LCD flat panel V_{COM} driver
- A/D converter buffer
- High side or low side sensing
- Headphone amplifier

3 Description

The LM8261 is a Rail-to-Rail input and output Op Amp which can operate with a wide supply voltage range. This device has high output current drive, greater than Rail-to-Rail input common mode voltage range, unlimited capacitive load drive capability, and provides tested and guaranteed high speed and slew rate while requiring only 1.35mA supply current. It is designed to handle the requirements of flat panel TFT panel V_{COM} driver applications as well as being suitable for other low power, and medium speed applications which require ease of use and enhanced performance over existing devices.

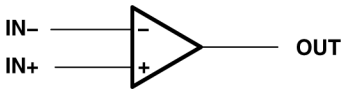
Greater than Rail-to-Rail input common mode voltage range with 90dB of Common Mode Rejection allows high side and low side sensing, among many applications, without concern over exceeding the range and with no compromise in accuracy. Exceptionally wide operating supply voltage range of 2.7V to 32V alleviates any concerns over functionality under extreme conditions and offers flexibility for use in multitude of applications. In addition, most device parameters are insensitive to power supply variations; this design enhancement is yet another step in simplifying its usage.

The LM8261 is offered in the space-saving SOT-23-5 package.

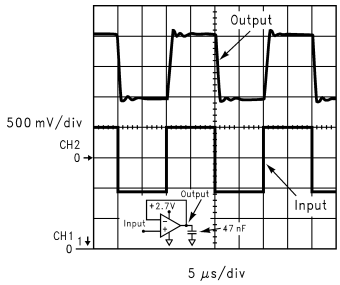
Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE (NOM)(2)
LM8261	SOT-23 (5)	2.9mm × 2.8mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Symbol (Each Amplifier)



Output Response with Heavy Capacitive Load

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4 Pin Configuration and Functions

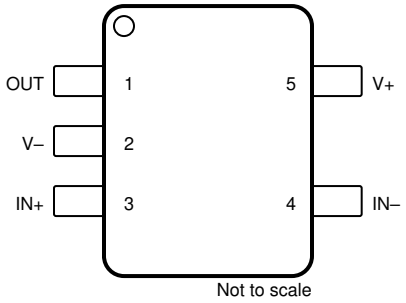


Figure 4-1. 5-Pin SOT-23
DBV Package
(Top View)

Table 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NUMBER	NAME		
1	Output	O	Output
2	V-	I	Negative Supply
3	IN+	I	Non-inverting input
4	IN-	I	Inverting Input
5	V+	I	Positive Supply

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)		0	33	V
Signal input pins	Common-mode voltage(3)	(V–) – 0.5	(V+) + 0.5	V
	Differential voltage(4)		±10	V
	Current(3)		±10	mA
Output short-circuit(2)		Continuous		
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operating the device beyond the ratings listed under *Absolute Maximum Ratings* will cause permanent damage to the device. These are stress ratings only, based on process and design limitations, and this device has not been designed to function outside the conditions indicated under *Recommended Operating Conditions*. Exposure to any condition outside *Recommended Operating Conditions* for extended periods, including absolute-maximum-rated conditions, may affect device reliability and performance.
(2) Short-circuit to ground, one amplifier per package. Extended short-circuit current, especially with higher supply voltage, can cause excessive heating and eventual destruction.
(3) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5V beyond the supply rails must be current limited to 10mA or less.
(4) Input pins are connected by back-to-back diodes for input protection. If the differential input voltage may exceed 0.5V, limit the input current to 10mA or less.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

	MIN	MAX	UNIT
Supply Voltage (V^+ - V^-)	2.7	32	V
Temperature Range(2)	−40	+85	°C

5.4 Thermal Information

THERMAL METRIC(1) (2)		DBV (5 PINS)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	185.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The maximum power dissipation is a function of $T_{J(max)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ R_{\theta JA}$. All numbers apply for packages soldered directly onto a PC board.

5.5 Electrical Characteristics

For V_S = (V+) – (V–) = 2.7V to 32V (±1.35V to ±16V) at T_A = 25°C, R_L = 10kΩ connected to V_S / 2, V_{CM}= V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.(1)

PARAMETER		TEST CONDITIONS		MIN	TYP(2)	MAX(3)	UNIT
V_{OS}	Input Offset Voltage	V_{CM} =V–			±0.7	±7	mV
			−40°C ≤ T_A ≤ +125°C			± 9	
TC V_{OS}	Input Offset Average Drift	V_{CM} =V–	−40°C ≤ T_A ≤ +125°C		±2		µV/°C
I_B	Input Bias Current				±0.4	±2	µA
			−40°C ≤ T_A ≤ +125°C			±2.8	
I_{OS}	Input Offset Current				30	275	nA
V_{CM}	Input Common-Mode Voltage Range			V–		V+	V
CMRR	Common Mode Rejection Ratio	V– < V_{CM} < (V+) – 2V	−40°C ≤ T_A ≤ +125°C	80	100		dB
PSRR	Power Supply Rejection Ratio	V_{CM}= V–, V_S = 5V to 32V	−40°C ≤ T_A ≤ +125°C		±3.5	±22	µV/V
A_{OL}	Open Loop Voltage Gain	V_S = 32V, V_{CM} = V_S / 2, (V–) + 1V < V_O < (V+) – 1V	−40°C ≤ T_A ≤ +125°C		85		dB
	Voltage Output Swing from Rail	Positive and negative rail headroom	V_S = 32V, R_L = 10 KΩ		15.94		V
			V_S = 32V, R_L = 2 KΩ		15.8		
			V_S = 32V, R_L = 10 KΩ		−15.94		V
			V_S = 32V, R_L = 2 KΩ		−15.8		
I_{SC}	Output Short Circuit Current				125	±62	mA
I_S	Supply Current	V_{CM} = V–, I_O = 0A			1.30	1.93	mA
			−40°C ≤ T_A ≤ +125°C			2.23	
SR	Slew Rate	V_S = 32V, V_{STEP} = 10V, G = +1, C_L = 20pF			35		V/µs
GBW	Gain-Bandwidth Product				24		MHz
Phi_m	Phase Margin	G = +1, R_L = 10kΩ, C_L = 20pF			50		°
e_n	Input Voltage Noise Density	f = 1kHz			12		nV/ $\sqrt{Hz}$
i_n	Input Current Noise Density	f = 1kHz			1		pA/ $\sqrt{Hz}$
t_s	Settling Time	T_O 0.1%, V_S = 32V, V_{STEP} = 10V, G = +1, C_L = 50pF			430		ns
THD+N	Total Harmonic Distortion +Noise	V_S = 32V, V_O = $3V_{RMS}$, G = 1, f = 1kHz, R_L = 10kΩ			113		dB

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated.
(2) Typical Values represent the most likely parametric norm.
(3) All limits are guaranteed by testing or statistical analysis.

5.6 Typical Characteristics

T_A = 25°C, V_S = ±16V, V_{CM} = V_S/2, Unless Otherwise Noted

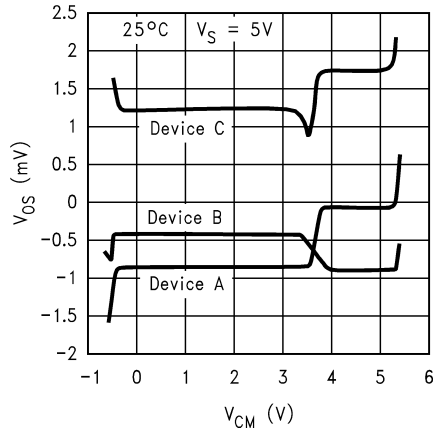


Figure 5-1. V_{OS} vs. V_{CM} for 3 Representative Units, Old Die

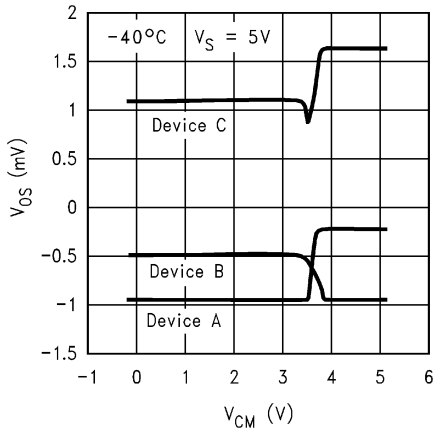


Figure 5-2. V_{OS} vs. V_{CM} for 3 Representative Units, Old Die

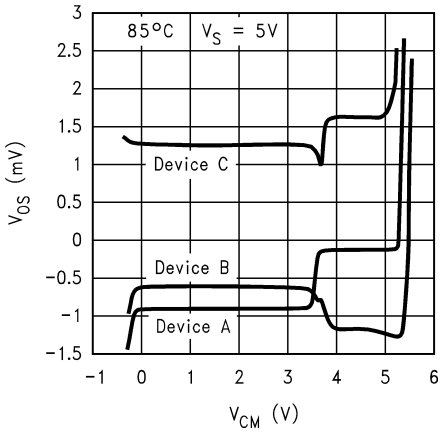


Figure 5-3. V_{OS} vs. V_{CM} for 3 Representative Units, Old Die

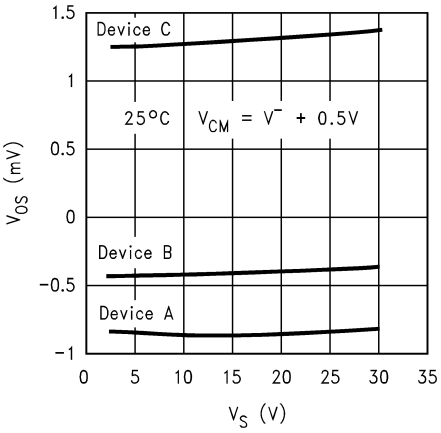


Figure 5-4. V_{OS} vs. V_S for 3 Representative Units, Old Die

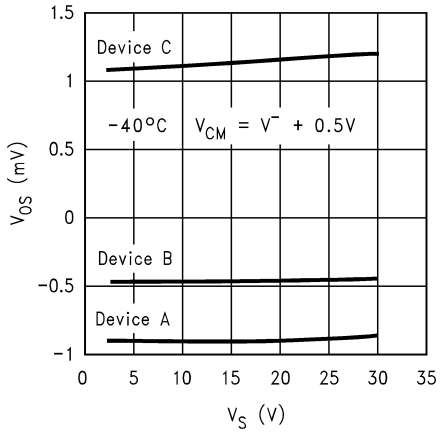


Figure 5-5. V_{OS} vs. V_S for 3 Representative Units, Old Die

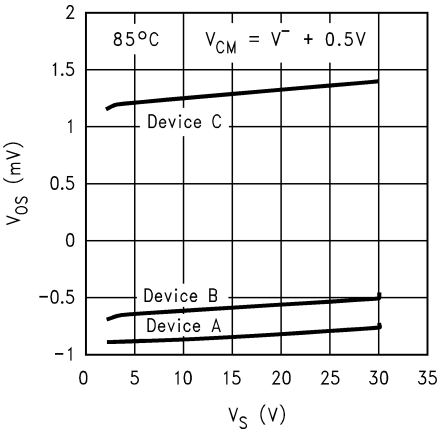


Figure 5-6. V_{OS} vs. V_S for 3 Representative Units, Old Die

5.6 Typical Characteristics (continued)

T_A = 25°C, V_S = ±16V, V_{CM} = V_S/2, Unless Otherwise Noted

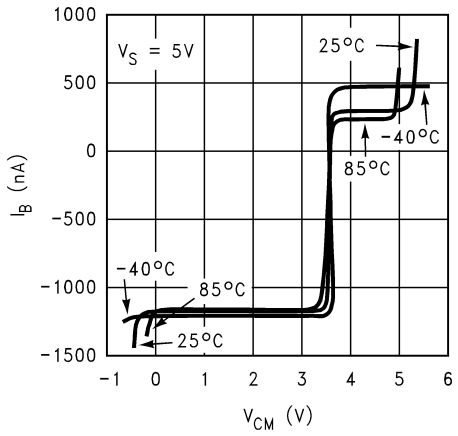


Figure 5-7. I_B vs. V_{CM}, Old Die

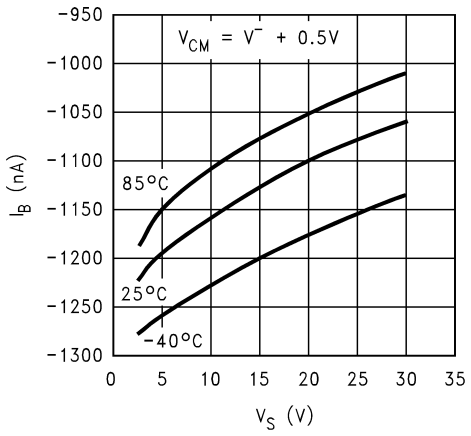


Figure 5-8. I_B vs. V_S, Old Die

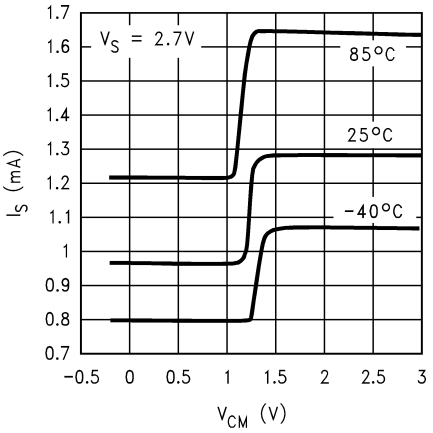


Figure 5-9. I_S vs. V_{CM}, Old Die

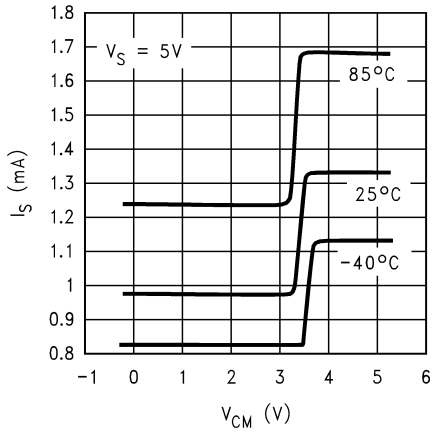


Figure 5-10. I_S vs. V_{CM}, Old Die

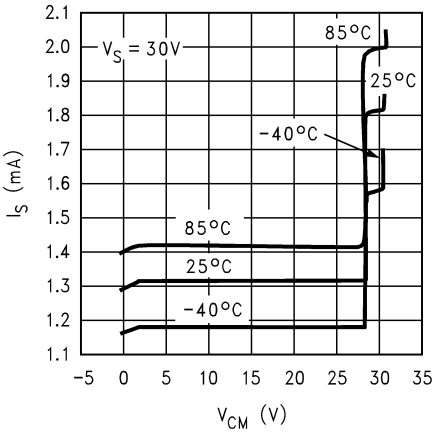


Figure 5-11. I_S vs. V_{CM}, Old Die

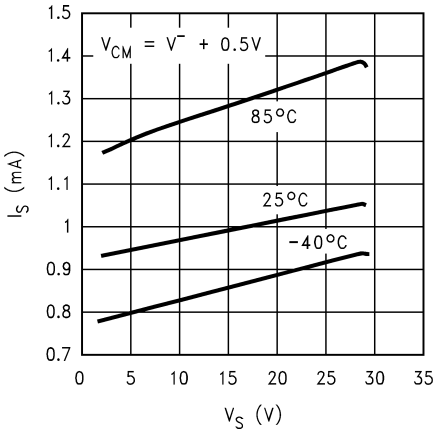


Figure 5-12. I_S vs. V_S (PNP side), Old Die

5.6 Typical Characteristics (continued)

T_A = 25°C, V_S = ±16V, V_{CM} = V_S/2, Unless Otherwise Noted

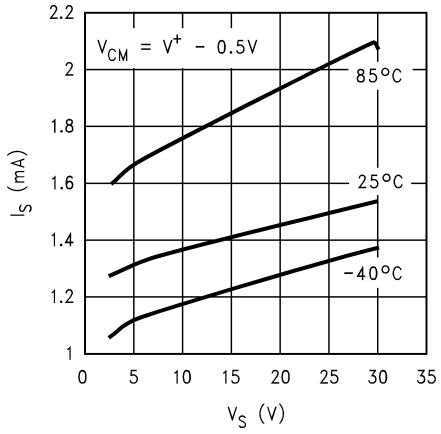


Figure 5-13. I_S vs. V_S (NPN side), Old Die

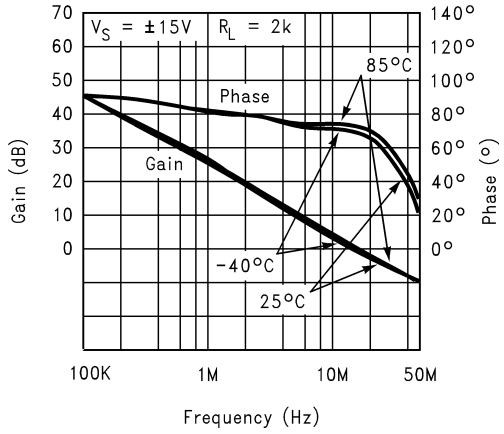


Figure 5-14. Gain/Phase vs. Frequency, Old Die

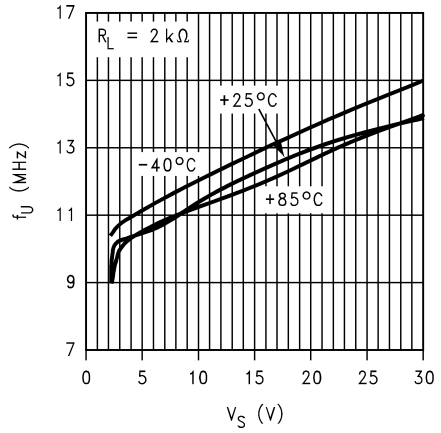


Figure 5-15. Unity Gain Frequency vs. V_S, Old Die

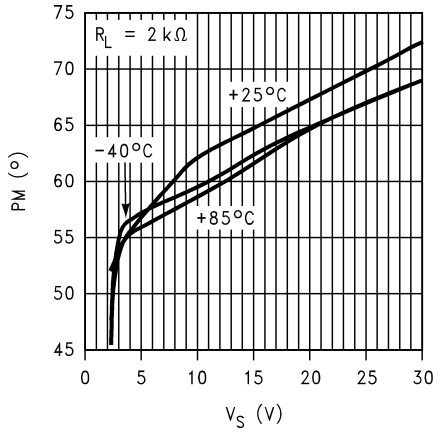


Figure 5-16. Phase Margin vs. V_S, Old Die

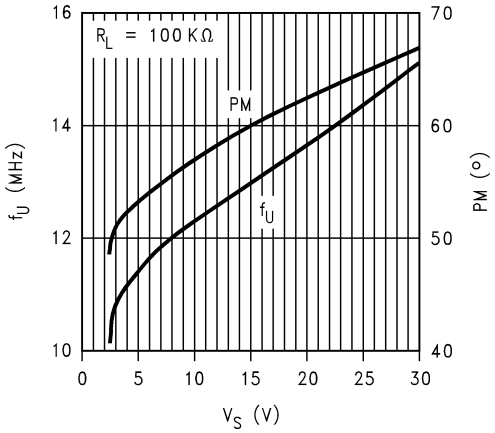


Figure 5-17. Unity Gain Freq. and Phase Margin vs. V_S, Old Die

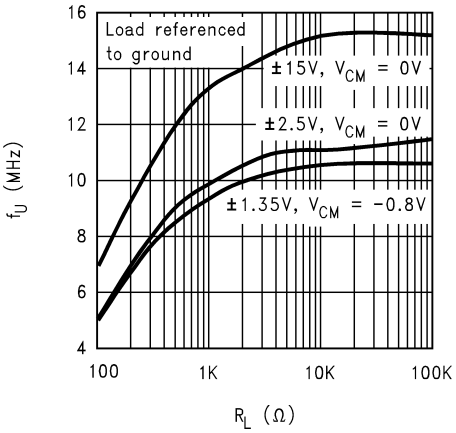


Figure 5-18. Unity Gain Frequency vs. Load, Old Die

5.6 Typical Characteristics (continued)

T_A = 25°C, V_S = ±16V, V_{CM} = V_S/2, Unless Otherwise Noted

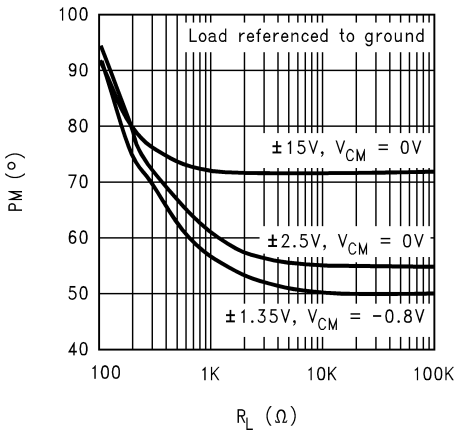


Figure 5-19. Phase Margin vs. Load, Old Die

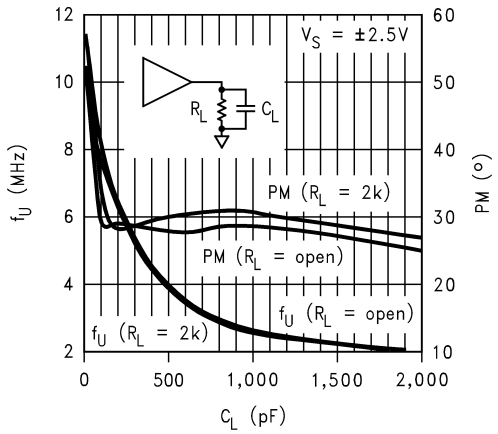


Figure 5-20. Unity Gain Freq. and Phase Margin vs. C_L, Old Die

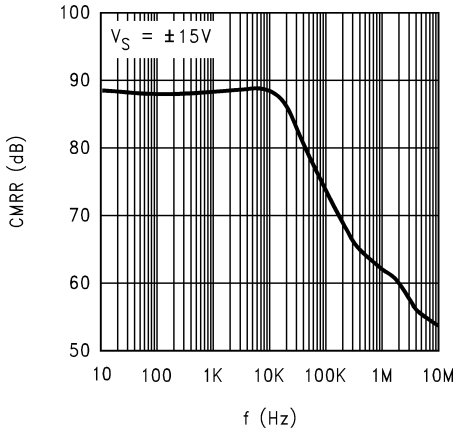


Figure 5-21. CMRR vs. Frequency, Old Die

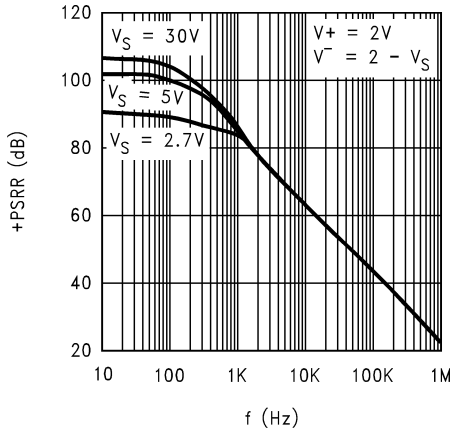


Figure 5-22. +PSRR vs. Frequency, Old Die

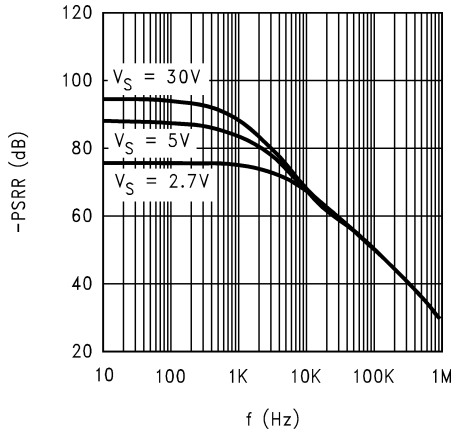


Figure 5-23. −PSRR vs. Frequency, Old Die

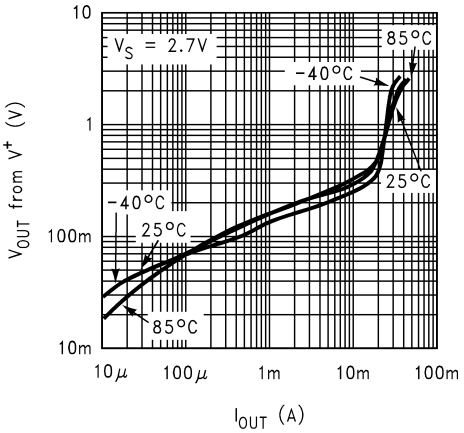


Figure 5-24. Output Voltage vs. Output Sourcing Current, Old Die

5.6 Typical Characteristics (continued)

T_A = 25°C, V_S = ±16V, V_{CM} = V_S/2, Unless Otherwise Noted

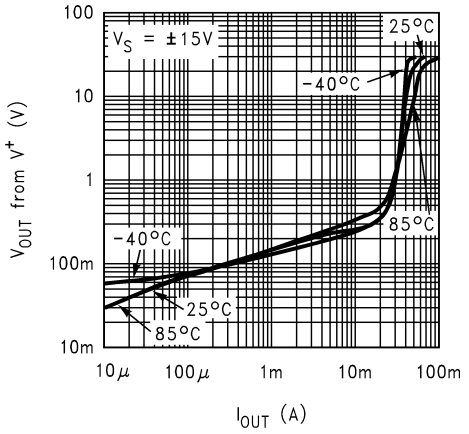


Figure 5-25. Output Voltage vs. Output Sourcing Current, Old Die

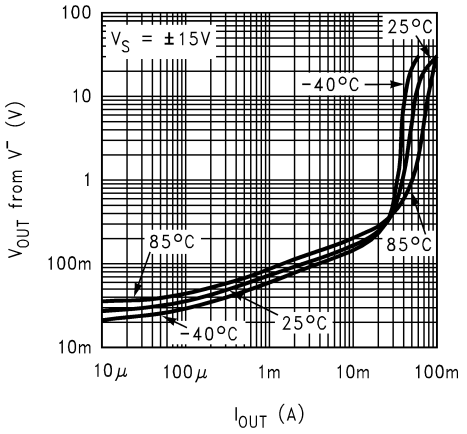


Figure 5-26. Output Voltage vs. Output Sinking Current, Old Die

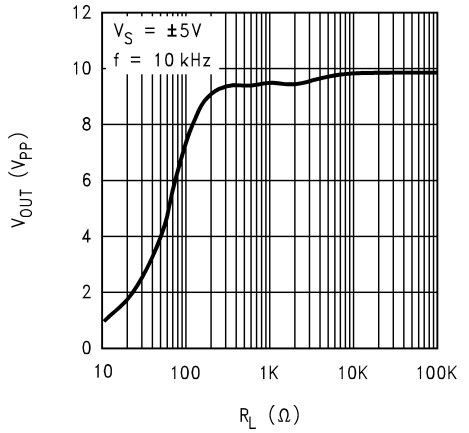


Figure 5-27. Max Output Swing vs. Load, Old Die

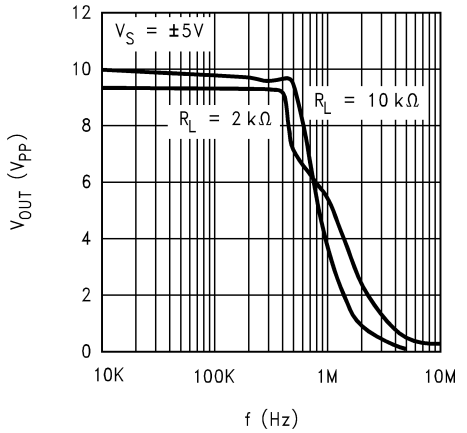


Figure 5-28. Max Output Swing vs. Frequency, Old Die

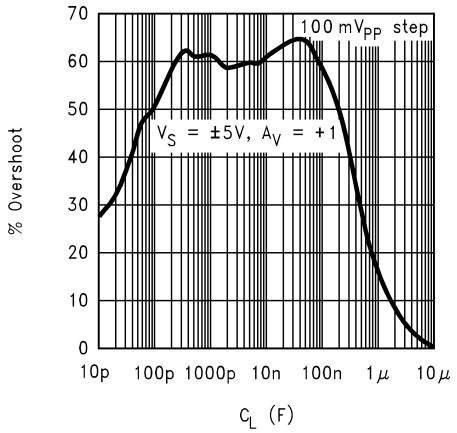


Figure 5-29. % Overshoot vs. Cap Load, Old Die

5.6 Typical Characteristics (continued)

T_A = 25°C, V_S = ±16V, V_{CM} = V_S/2, Unless Otherwise Noted

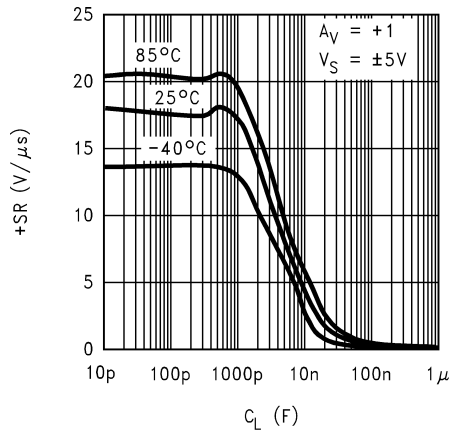


Figure 5-30. +SR vs. Cap Load, Old Die

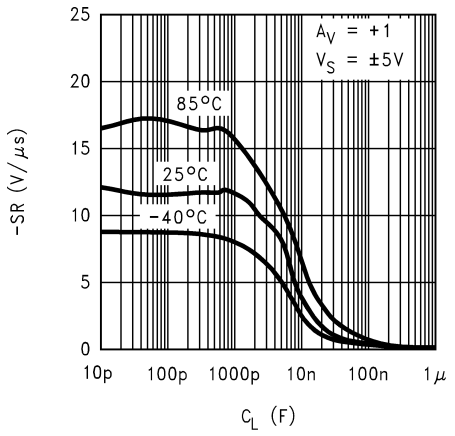


Figure 5-31. −SR vs. Cap Load, Old Die

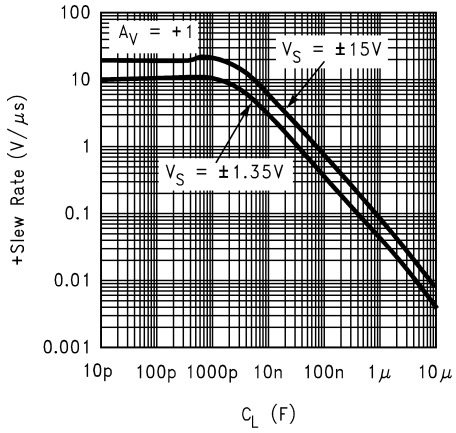


Figure 5-32. +SR vs. Cap Load, Old Die

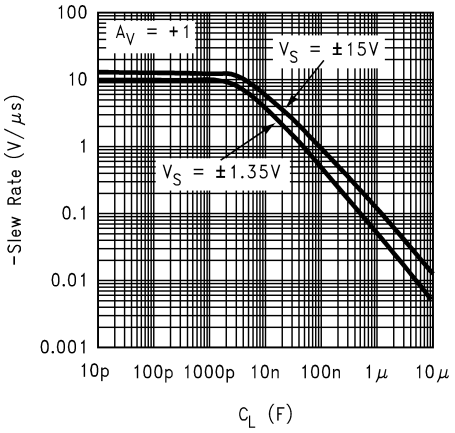


Figure 5-33. −SR vs. Cap Load, Old Die

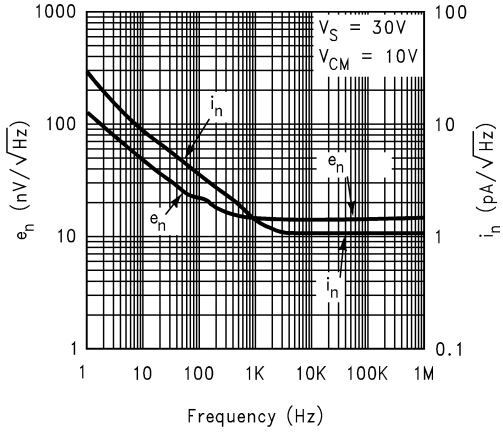


Figure 5-34. Input Noise Voltage/Current vs. Frequency, Old Die

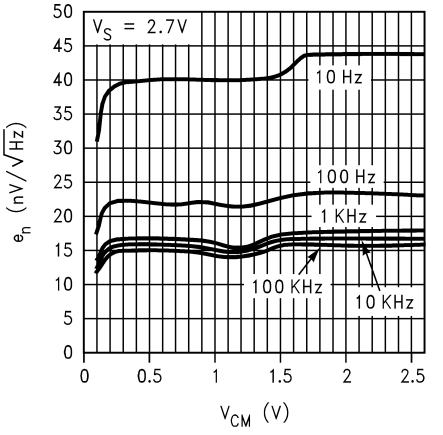


Figure 5-35. Input Noise Voltage vs. V_{CM}, Old Die

5.6 Typical Characteristics (continued)

T_A = 25°C, V_S = ±16V, V_{CM} = V_S/2, Unless Otherwise Noted

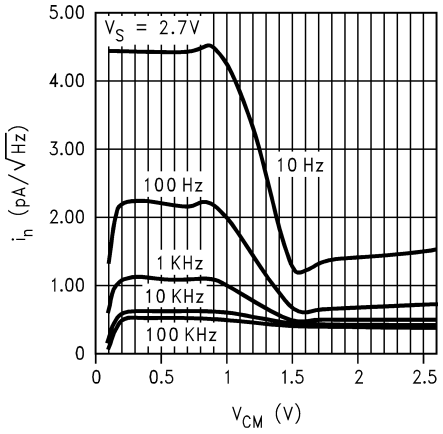


Figure 5-36. Input Noise Current vs. V_{CM}, Old Die

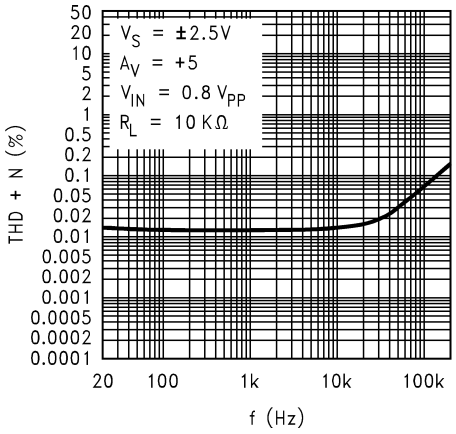


Figure 5-37. THD+N vs. Frequency, Old Die

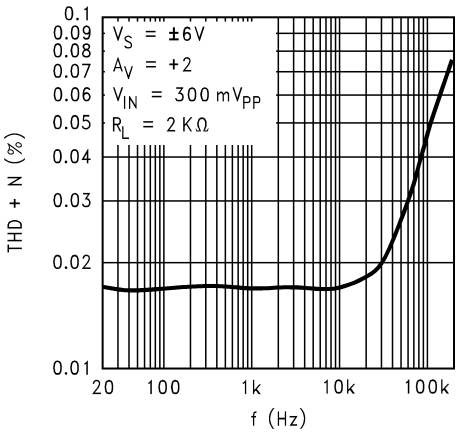


Figure 5-38. THD+N vs. Frequency, Old Die

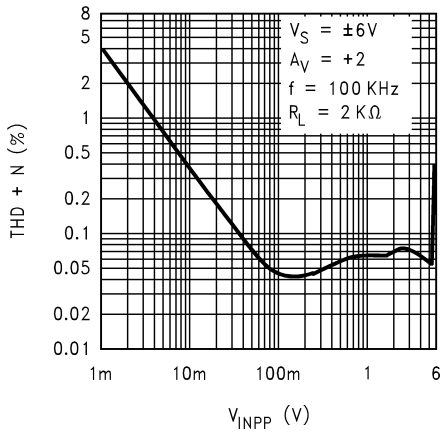


Figure 5-39. THD+N vs. Amplitude, Old Die

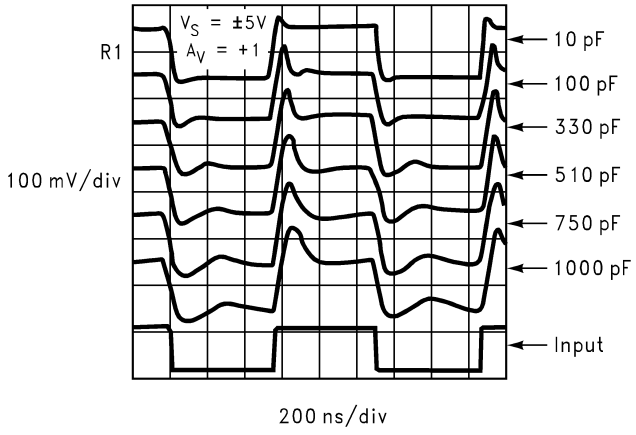


Figure 5-40. Small Signal Step Response, Old Die

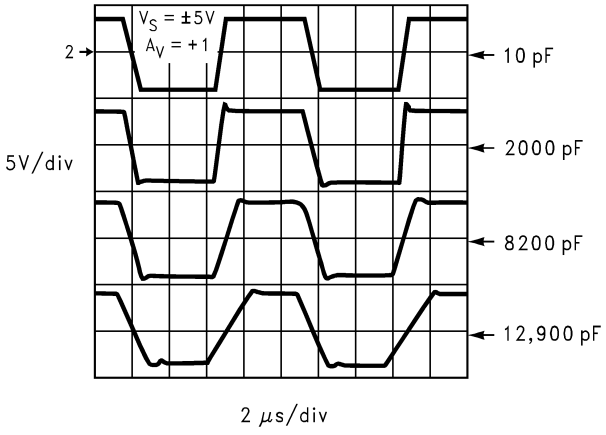
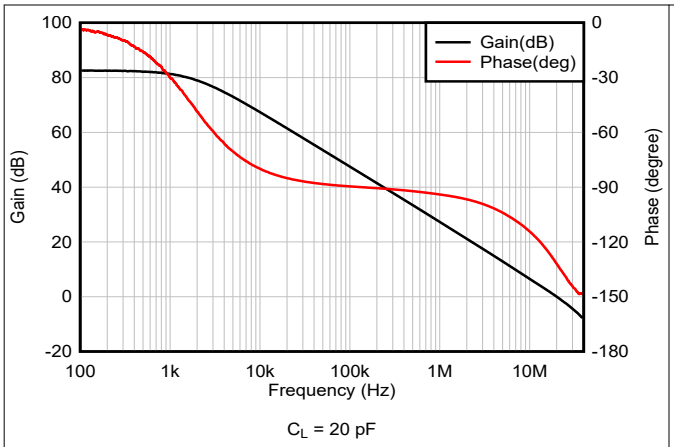


Figure 5-41. Large Signal Step Response, Old Die

5.6 Typical Characteristics (continued)

T_A = 25°C, V_S = ±16V, V_{CM} = V_S/2, Unless Otherwise Noted



C_L = 20 pF

Figure 5-42. Open-Loop Gain and Phase vs Frequency, New Die

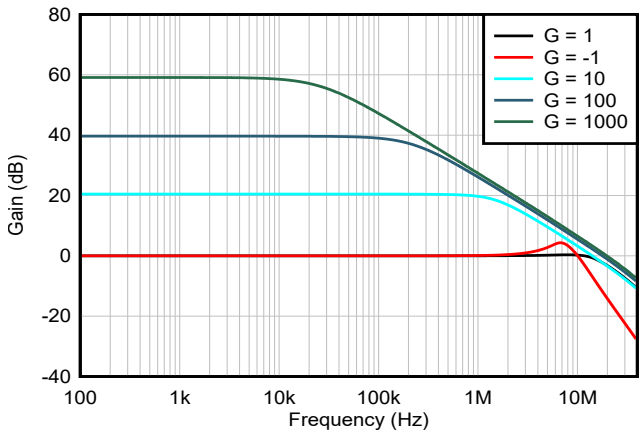


Figure 5-43. Closed-Loop Gain vs Frequency, New Die

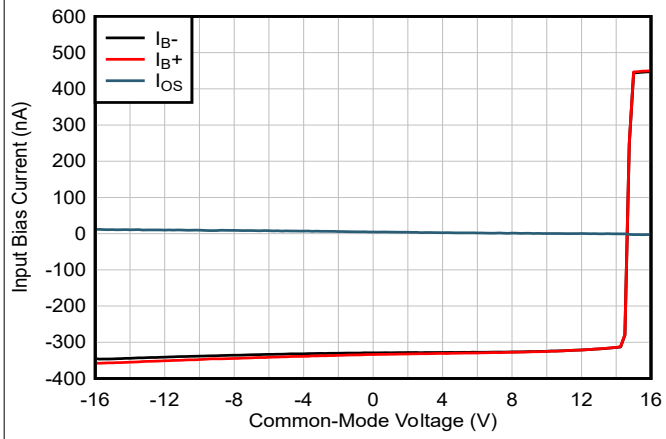
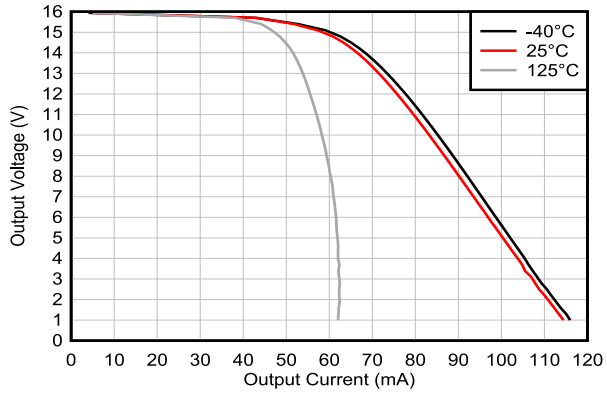
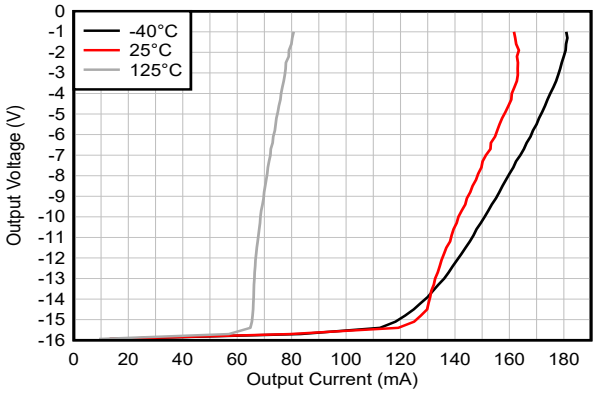


Figure 5-44. Input Bias Current and Offset Current vs Common-Mode Voltage, New Die



V_S = 32 V

Figure 5-45. Output Voltage Swing vs Output Current (Sourcing), New Die



V_S = 32 V

Figure 5-46. Output Voltage Swing vs Output Current (Sinking), New Die

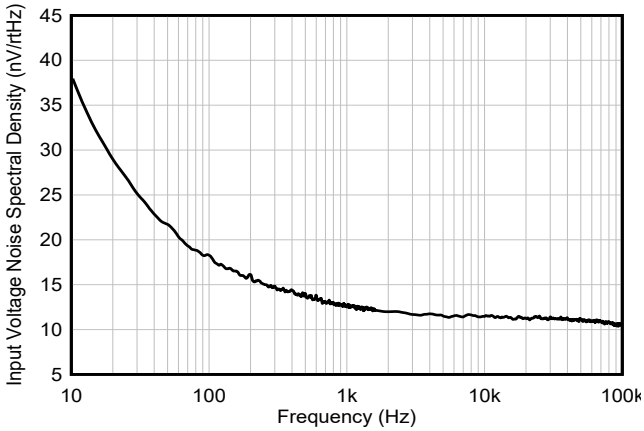


Figure 5-47. Input Voltage Noise Spectral Density vs Frequency, New Die

5.6 Typical Characteristics (continued)

T_A = 25°C, V_S = ±16V, V_{CM} = V_S/2, Unless Otherwise Noted

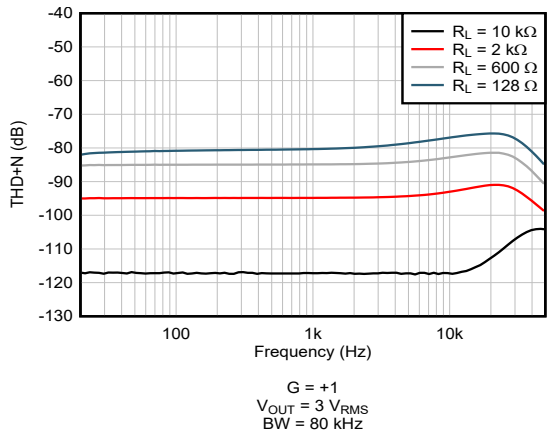


Figure 5-48. THD+N Ratio vs Frequency, New Die

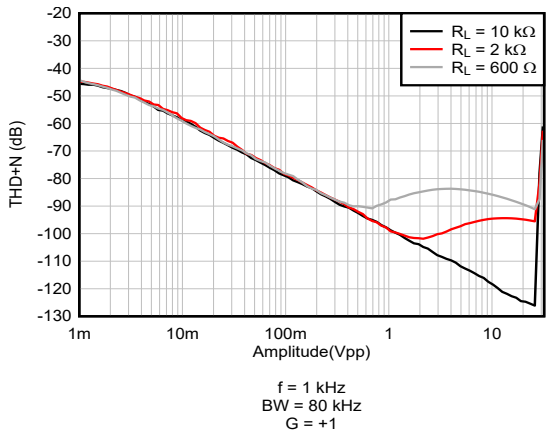


Figure 5-49. THD+N vs Output Amplitude, New Die

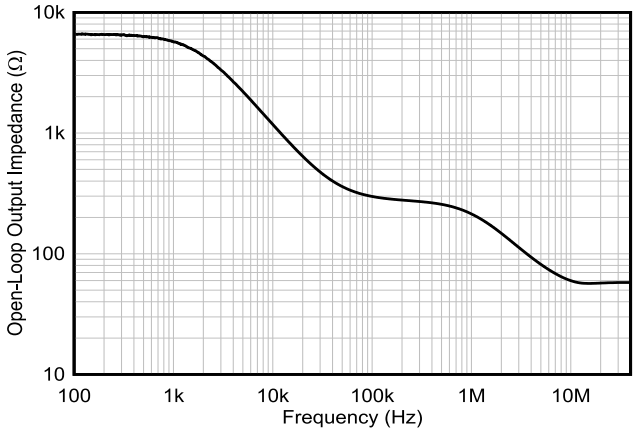


Figure 5-50. Open-Loop Output Impedance vs Frequency, New Die

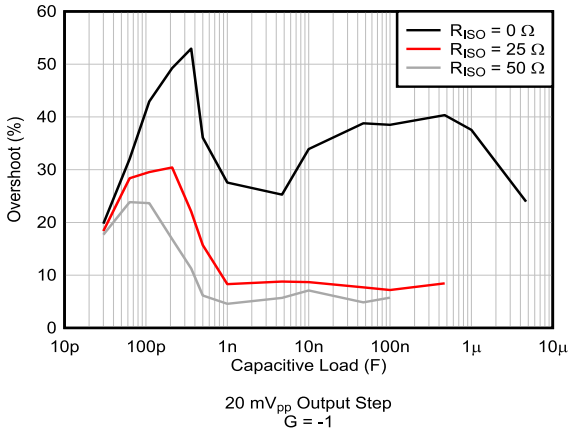


Figure 5-51. Small-Signal Overshoot vs Capacitive Load, New Die

5.7 Old Versus New Die Comparison

As of the publication of revision K of this data sheet, Texas Instruments has moved manufacturing of the die for LM8261 to a modern fabrication site. The two different die are referred to in this document as “old” (previous fabrication site) and “new” die. The die origin can be separated from the “Chip Source Origin” (CSO) parameter in the shipping information. The old die CSO is “GF6”, for the new die the CSO is “RFB”. The old die information is in the shipping information. The old die CSO is “GF6”, for the new die the CSO is “RFB”. The old die information is maintained in this data sheet for comparison purposes, but all new manufacturing has moved to the new die.

6 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

6.1 Driving Capacitive Loads

The LM8261 is specifically designed to drive unlimited capacitive loads without oscillations. In addition, the output current handling capability of the device allows for good slewing characteristics even with large capacitive loads. The combination of these features is designed for applications such as TFT flat panel buffers, A/D converter input amplifiers, and so forth.

However, as in most Op Amps, addition of a series isolation resistor between the Op Amp and the capacitive load improves the settling and overshoot performance.

6.2 Low-Side Current Measurement

Figure 6-1 shows the LM8261 configured in a low-side current sensing application. For a full analysis of the circuit including theory, calculations, simulations, and measured data, see TI Precision Design.

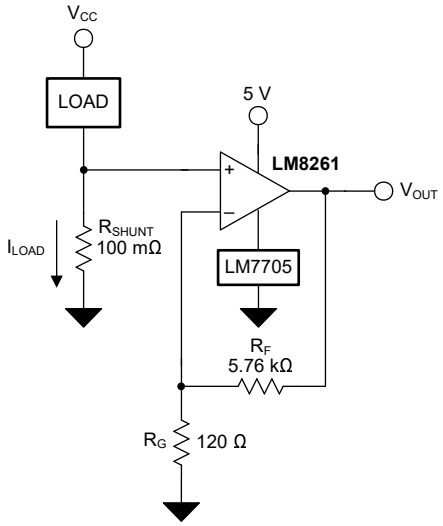


Figure 6-1. LM8261 in a Low-Side, Current-Sensing Application

6.3 Output Short Circuit Current and Dissipation Issues

The LM8261 output stage is designed for maximum output current capability. Even though momentary output shorts to ground and either supply can be tolerated at all operating voltages, longer lasting short conditions can cause the junction temperature to rise beyond the absolute maximum rating of the device, especially at higher supply voltage conditions.

With the Op Amp tied to a load, the device power dissipation consists of the quiescent power due to the supply current flow into the device, in addition to power dissipation due to the load current. The load portion of the power itself could include an average value (due to a DC load current) and an AC component. DC load current would flow if there is an output voltage offset, or the output AC average current is non-zero, or if the Op Amp operates in a single supply application where the output is maintained somewhere in the range of linear operation. Therefore:

$$P_{TOTAL} = P_Q + P_{DC} + P_{AC} \quad (1)$$

Op Amp Quiescent Power Dissipation:

$$P_Q = I_S \cdot V_S \quad (2)$$

DC Load Power:

$$P_{DC} = I_O \cdot (V_R - V_O) \quad (3)$$

AC Load Power:

$$P_{AC} = \text{(outlined in table below)} \quad (4)$$

where

- I_S is Supply Current
- V_S is Total Supply Voltage (V+ - V−)
- I_O is Average Load Current
- V_O is Average Output Voltage
- V_R is V+ for sourcing and V− for sinking current

Table 6-1 shows the maximum AC component of the load power dissipated by the Op Amp for standard Sinusoidal, Triangular, and Square Waveforms:

Table 6-1. Normalized AC Power Dissipated in the Output Stage for Standard Waveforms

P_{AC} (W.Ω/V^2)		
Sinusoidal	Triangular	Square
50.7 x 10^{-3}	46.9 x 10^{-3}	62.5 x 10^{-3}

The table entries are normalized to $V_S{}^2/ R_L$. To calculate the AC load current component of power dissipation, simply multiply the table entry corresponding to the output waveform by the factor $V_S{}^2/ R_L$. For example, with ±15 V supplies, a 600-Ω load, and triangular waveform power dissipation in the output stage is calculated as:

$$P_{AC} = (46.9 \times 10^{-3}) \cdot [30^2/600] = 70.4 \text{ mW} \quad (5)$$

6.4 Other Application Hints

The use of supply decoupling is mandatory in most applications. As with most relatively high speed/high output current Op Amps, best results are achieved when each supply line is decoupled with two capacitors; a small value ceramic capacitor (~0.01 µF) placed very close to the supply lead in addition to a large value Tantalum or Aluminum (> 4.7 µF). The large capacitor can be shared by more than one device if necessary. The small ceramic capacitor maintains low supply impedance at high frequencies while the large capacitor will act as the charge "bucket" for fast load current spikes at the Op Amp output. The combination of these capacitors will provide supply decoupling and will help keep the Op Amp oscillation free under any load.

6.5 Power Supply Recommendations

The LM8261 can operate off a single supply or with dual supplies. The input CM capability of the parts (CMVR) extends covers the entire supply voltage range for maximum flexibility. Supplies should be decoupled with low inductance, often ceramic, capacitors to ground less than 0.5 inches from the device pins. The use of ground plane is recommended, and as in most high speed devices, it is advisable to remove ground plane close to device sensitive pins such as the inputs.

6.6 Layout

6.6.1 Layout Guidelines

Generally, a good high frequency layout will keep power supply and ground traces away from the inverting input and output pins. Parasitic capacitances on these nodes to ground will cause frequency response peaking and possible circuit oscillations. General high-speed, signal-path layout suggestions include:

- Continuous ground planes are preferred for signal routing with matched impedance traces for longer runs. However, open up both ground and power planes around the capacitive sensitive input and output device pins. After the signal is sent into a resistor, parasitic capacitance becomes more of a bandlimiting issue and less of a stability issue.
- Use good, high-frequency decoupling capacitors (0.1 µF) on the ground plane at the device power pins. For best high-frequency decoupling, consider X2Y supply-decoupling capacitors that offer a much higher self-resonance frequency over standard capacitors.
- When using differential signal routing over any appreciable distance, use microstrip layout techniques with matched impedance traces.
- The input summing junction is very sensitive to parasitic capacitance. Connect any Rf, and Rg elements into the summing junction with minimal trace length to the device pin side of the resistor. The other side of these elements can have more trace length if needed to the source or to ground.

7 Device and Documentation Support

7.1 Documentation Support

7.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *IC Package Thermal Metrics* application report

7.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

7.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

7.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision J (January 2015) to Revision K (February 2026)	Page
• Removed (V_S = 5 V, T_A = 25°C, typical values unless specified)	1
• Removed ±5% settling time 400 ns (500 pF, 100 mV_{PP} step)	1
• Updated GBWP from 21MHz to 24MHz	1
• Updated Wide supply voltage range from 2.5V to 2.7V and from 30V to 32V	1
• Updated Slew rate from 12V/µs to 35V/µs	1
• Updated Supply current from 0.97mA to 1.35mA	1
• Updated Output short circuit current from 53 mA/ −75 mA to ±125mA	1
• Updated Input Voltage Noise from 15nV/ $\sqrt{Hz}$ to 12nV/ $\sqrt{Hz}$	1
• Updated THD+N from <0.05% to < 0.00022%	1
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated the description as per new die	1
• Updated Table and Footnotes as per new die specifications	5
• Updated Electrostatic discharge value for CDM from ±200V to ±1500V	5
• Updated footnotes	5
• Updated Supply Voltage minimum from 2.5V to 2.7V and maximum from 30V to 32V	5
• Updated Junction-to-ambient thermal resistance from 325°C/W to 185.4°C/W	5

- Changed *Electrical characteristics* from ±15V to ±16V. 6
- Updated Table description. 6
- Updated Input offset voltage test conditions to V_{CM} =V^- 6
- Removed Input bias current test conditions for V_{CM} =14.5 V and curresponding value for range −40°C ≤ T_A ≤ +125°C. 6
- Removed Input Offest current test conditions for V_{CM} =±14.5 V and corresponding value for range −40°C ≤ T_A ≤ +125°C. 6
- Updated Common Mode Rejection Ratio test conditions from V_{CM} stepped from −15 V to 13 V to V^- < V_{CM} < (V^+) – 2V and from −65°C ≤ T_J ≤ +150°C to −40°C ≤ T_A ≤ +125°C. 6
- Removed Common Mode Rejection Ratio test conditions and corresponding values for V_{CM} stepped from 14V to 15V and for V_{CM} stepped from −15V to 15V. 6
- Updated Power Supply Rejection Ratio test conditions from V^+ = ±12V to ±15V to V_{CM}= V^-, V_S = 5V to 32V and from −65°C ≤ T_J ≤ +150°C to −40°C ≤ T_A ≤ +125°C. 6
- Updated Power Supply Rejection Ratio typical value from 100dB to ±3.5µV/V and maximum value from 70dB to ±22µV/V 6
- Removed Negative Power Supply Rejection Ratio. 6
- Removed CMVR values. 6
- Updated V_{CM} value minimum V^- and maximum V^+ 6
- Updated Open Loop Voltage Gain typical value 85dB. 6
- Removed Large Signal Voltage Gain. 6
- Removed Output swing high. 6
- Updated Voltage Output Swing from Rail for R_L=10kΩ from 14.83V to 15.94V. 6
- Updated Voltage Output Swing from Rail for R_L=2kΩ from 14.73V to 15.8V. 6
- Updated Voltage Output Swing from Rail for R_L=10kΩ from −14.91V to −15.94V. 6
- Updated Voltage Output Swing from Rail for R_L=2kΩ from −14.83V to −15.8V. 6
- Updated Output Short Circuit Current from 60mA to 125mA typical and maximum from 40mA to ±62mA. 6
- Removed all test conditions for Output Short Circuit Current 6
- Updated Supply Current maximum from 1.50mA to 1.93mA and 1.90mA to 2.23mA 6
- Updated Slew Rate from 15V/µs to 35V/µs 6
- Removed Unity Gain Frequency. 6
- Removed Gain Bandwidth maximum value. 6
- Updated Phase margin typical value from 58° to 50°. 6
- Updated Input Voltage Noise Density typical value from 15nV/ $\sqrt{\text{hZ}}$ to 12nV/ $\sqrt{\text{hZ}}$ 6
- Removed Full Power Bandwidth. 6
- Updated Settling time typical value from 320ns to 430ns. 6
- Updated Total Harmonic Distortion +Noise from 0.01% to 113dB. 6
- Updated Open-Loop Gain and Phase vs Frequency plot. 7
- Updated Closed-Loop Gain vs Frequency plot. 7
- Updated Input Bias Current and Offset Current vs Common-Mode Voltage plot. 7
- Updated Output Voltage Swing vs Output Current (Sourcing) plot. 7
- Updated Output Voltage Swing vs Output Current (Sinking) plot. 7
- Updated Input Voltage Noise Spectral Density vs Frequency plot. 7
- Updated THD+N Ratio vs Frequency plot. 7
- Updated THD+N vs Output Amplitude plot. 7
- Updated Open-Loop Output Impedance vs Frequency plot 7
- Updated Small-Signal Overshoot vs Capacitive Load plot 7
- Added *Old Versus New Die Comparison* 15
- Removed Block diagram and operational description. 16
- Removed *Estimating the Output Voltage Swing* section. 16
- Removed *TFT Application* section. 16
- Added *Low-Side Current Measurement* section. 16
- Removed *LM8261 Advantages* section. 17
- Updated guidelines as per new die. 18

- Removed *Layout Example* section..... 18

Changes from Revision I (March 2013) to Revision J (January 2015) **Page**

- Added, updated, or revised the following sections: *Pin Configuration and Functions*, *Specifications*, *Detailed Description* , *Application and Implementation*, *Power Supply Recommendations* , *Layout* , *Device and Documentation Support* , and *Mechanical, Packaging, and Orderable Information* section 1
- Changed from -1.0 V to -0.8 V in *Section 5* 5

Changes from Revision H (March 2013) to Revision I (March 2013) **Page**

- Changed layout of National Data Sheet to TI format.....1

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM8261M5/NOPB	Obsolete	Production	SOT-23 (DBV) | 5	-	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A45A
LM8261M5X/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A45A
LM8261M5X/NOPB.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A45A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

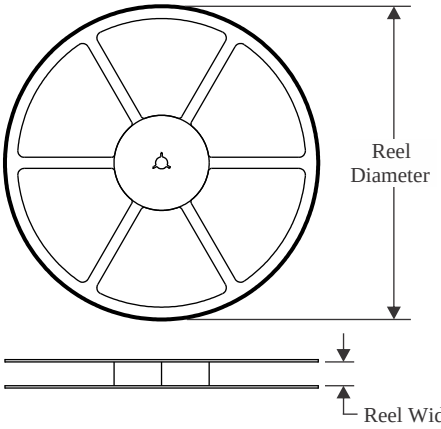
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

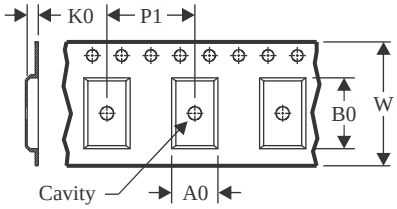
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

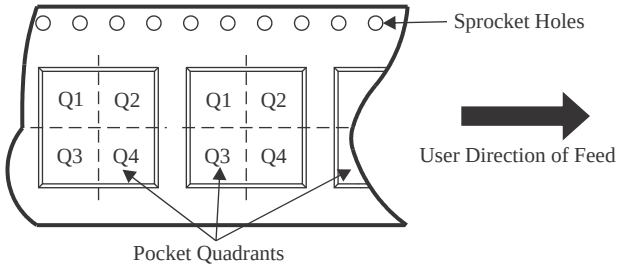


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

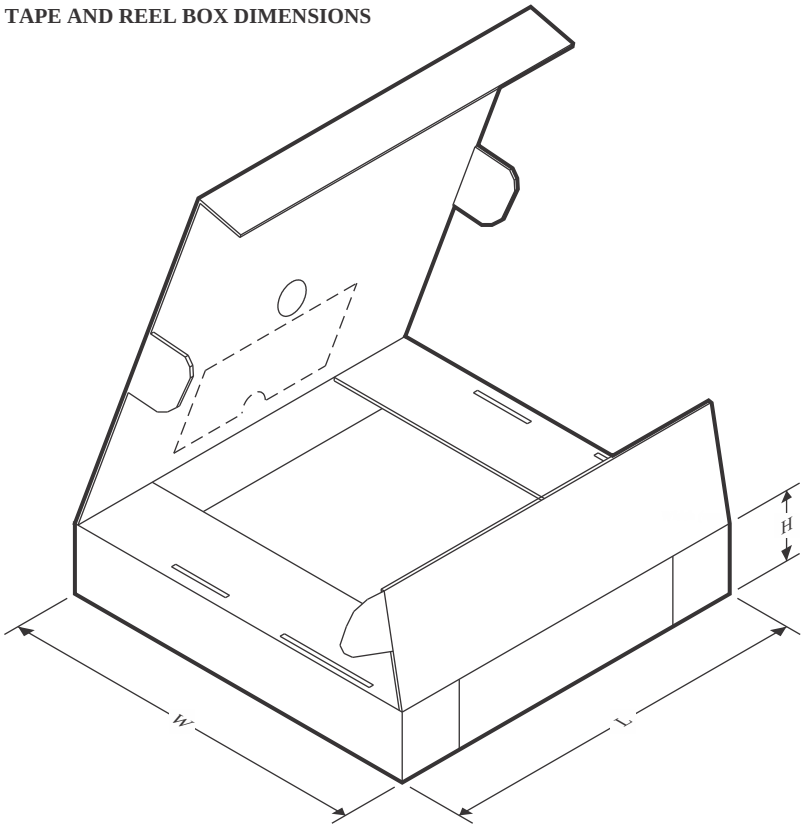
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM8261M5/NOPB	SOT-23	DBV	5	0	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM8261M5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM8261M5X/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

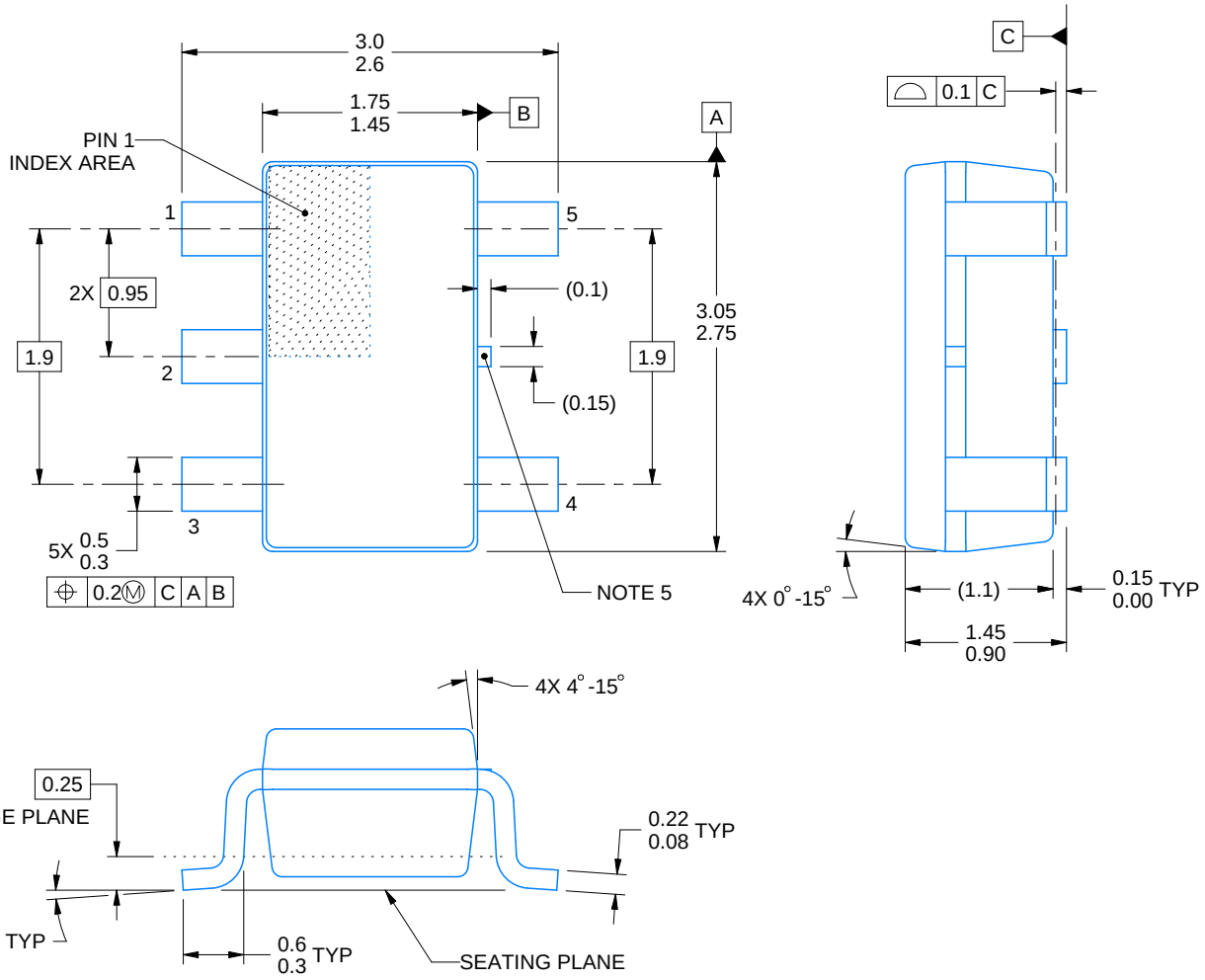
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM8261M5/NOPB	SOT-23	DBV	5	0	208.0	191.0	35.0
LM8261M5X/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LM8261M5X/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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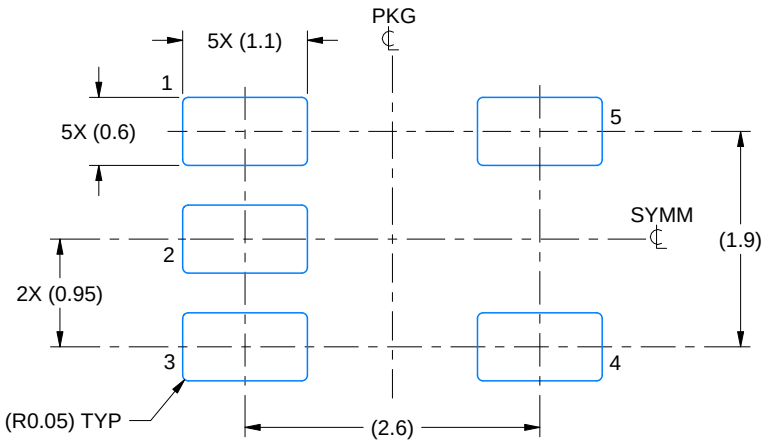
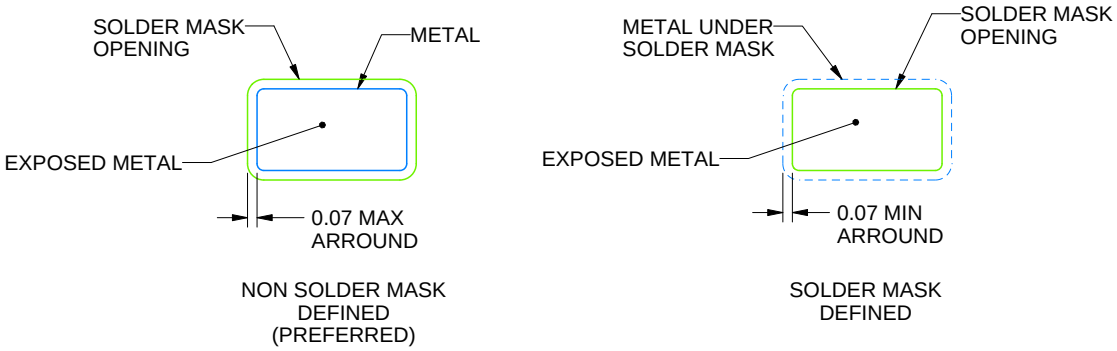
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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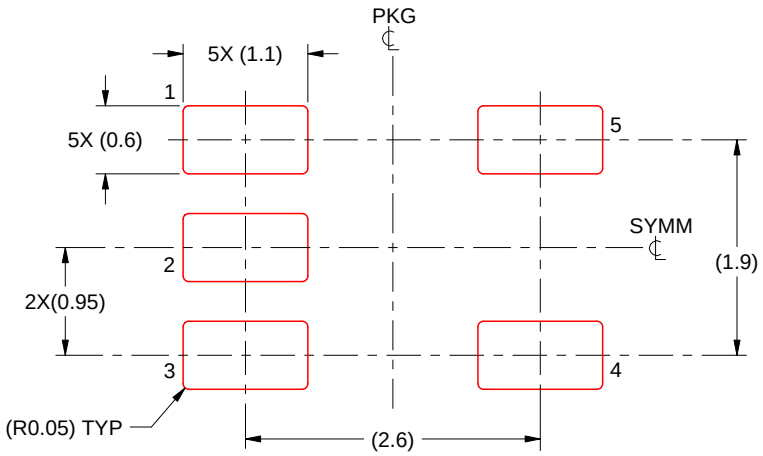
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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