

# LM94 TruTherm™ Hardware Monitor with PI Loop Fan Control for Server Management

## 1 Features

- 8-bit  $\Sigma\Delta$  ADC
- Monitors 16 Power Supplies
- Monitors 4 Remote Thermal Diodes and 2 LM60
- New TruTherm Technology Support for Precision Thermal Diode Measurements
- Internal Ambient Temperature Sensing
- Programmable Autonomous Fan Control Based on Temperature Readings with Fan Boost Support
- Fan Boost Support on Tachometer Limit Error Event
- Fan Control Based on 13-step Lookup Table or PI Control Loop or Combination of Both
- PI Fan Control Loop Supports Tcontrol
- Temperature Reading Digital Filters
- 0.5°C digital Temperature Sensor Resolution
- 0.0625°C Filtered Temperature Resolution for Fan Control
- 2 PWM Fan Speed Control Outputs
- 4 Fan Tachometer Inputs
- Dual Processor Thermal Throttling ( PROCHOT ) Monitoring
- Dual Dynamic VID Monitoring (6/7 VIDs per processor) Supports VRD10.2/11
- 8 General Purpose I/Os:
  - 4 Can be Configured as Fan tachometer Inputs
  - 2 Can be Configured to Connect to Processor THERMTRIP
  - 2 are Standard GPIOs that Could be Used to Monitor IERR Signal
- 2 General Purpose Inputs that Can be Used to Monitor the 7th VID Signal for VRD11
- Limit Register Comparisons of all Monitored Values
- 2-wire Serial Digital Interface, SMBus 2.0 Compliant
  - Supports Byte/block Read and Write
  - Selectable Slave Address (Tri-level Pin Selects 1 of 3 Possible Addresses)
  - ALERT Output Supports Interrupt or Comparator Modes
- 2.5V Reference Voltage Output
- 56-pin TSSOP Package
- XOR-tree Test Mode

## • Key Specifications:

- Voltage Measurement Accuracy ...  $\pm 2\%$  FS (max)
- Temperature Resolution ... 9-bits, 0.5°C
- Temperature Sensor Accuracy ...  $\pm 2.5$  °C (max)
- Temperature Range:
  - LM94 Operational ... 0°C to +85°C
  - Remote Temp Accuracy ... 0°C to +125°C
- Power Supply Voltage ... +3.0V to +3.6V
- Power Supply Current ... 1.6 mA

## 2 Applications

- Servers
- Workstations
- Multi-processor based equipment

## 3 Description

The LM94 hardware monitor has a two wire digital interface compatible with SMBus 2.0. Using a  $\Sigma\Delta$  ADC, the LM94 measures the temperature of four remote diode connected transistors as well as its own die and 16 power supply voltages. The LM94 has new TruTherm technology that supports precision thermal diode measurements of processors on sub-micron processes.

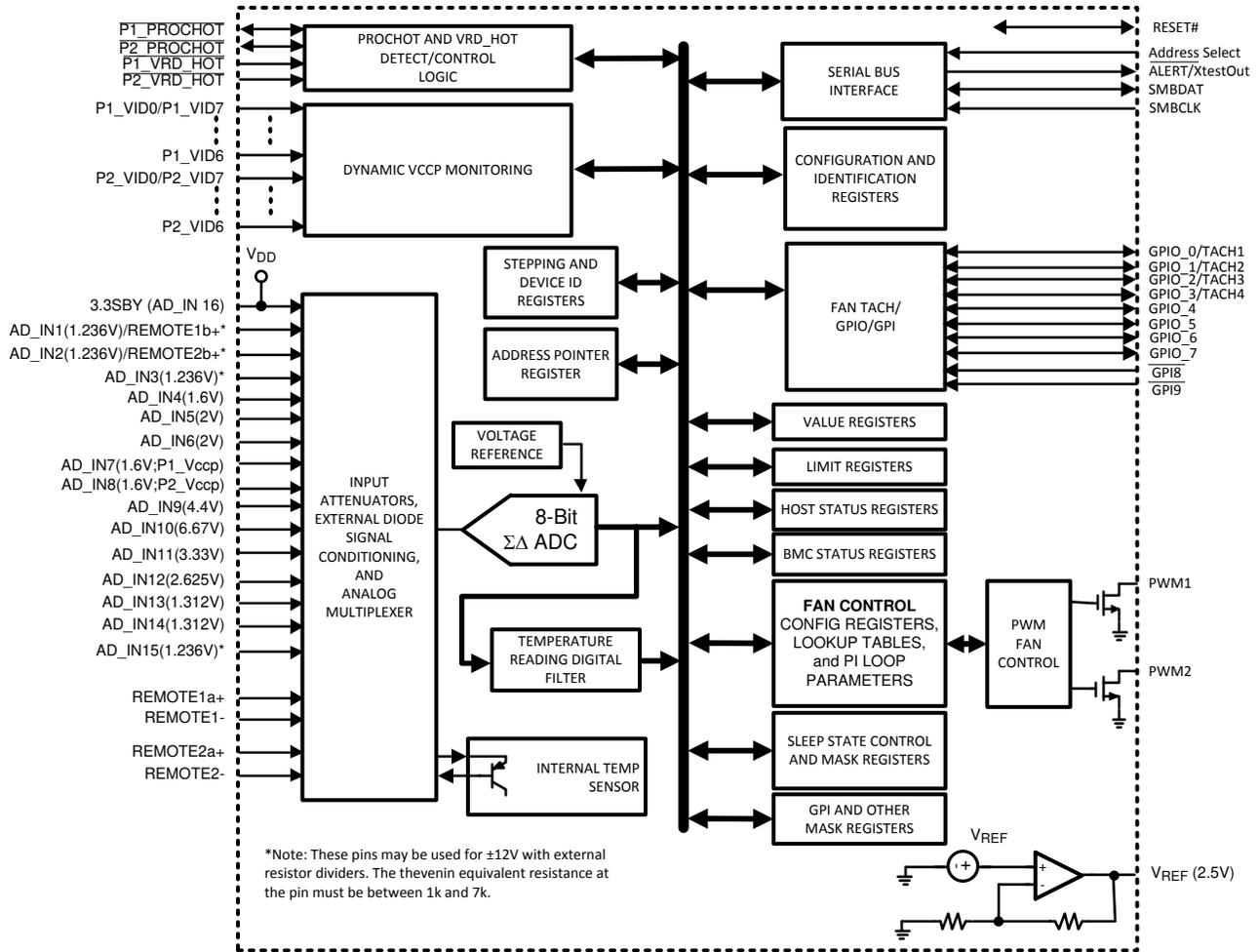
To set fan speed, the LM94 has two PWM outputs that are each controlled by up to six temperature zones. The fan-control algorithm can be based on a lookup table, PI (proportional/integral) control loop, or a combination of both. The LM94 includes digital filters that can be invoked to smooth temperature readings for better control of fan speed such that acoustical noise is minimized. The LM94 has four tachometer inputs to measure fan speed. Limit and status registers for all measured values are included.

The LM94 builds upon the functionality of previous motherboard server management ASICs, such as the LM93. It also adds measurement and control support for dynamic Vccp monitoring for VRD10/11 and PROCHOT. It is designed to monitor a dual processor Xeon class motherboard with a minimum of external components.



### 3.1 Functional Block Diagram

The block diagram of LM94 hardware is illustrated below. The hardware implementation is a single chip ASIC solution.



## Table of Contents

|  |   |
|--|---|
| <p><b>1 Features</b>..... 1</p> <p><b>2 Applications</b>..... 1</p> <p><b>3 Description</b>..... 1</p> <p>    3.1 Functional Block Diagram..... 2</p> <p><b>4 Pin Configuration and Functions</b>..... 4</p> <p>    4.1 Server Terminology..... 7</p> <p><b>5 Specifications</b>..... 9</p> <p>    5.1 Absolute Maximum Ratings ..... 9</p> <p>    5.2 Operating Ratings ..... 9</p> <p>    5.3 DC Electrical Characteristics..... 10</p> <p>    5.4 AC Electrical Characteristics..... 12</p> <p><b>6 Detailed Description</b>..... 15</p> <p>    6.1 Overview..... 15</p> <p>    6.2 Feature Description..... 15</p> <p>    6.3 Programming..... 34</p> <p>    6.4 Registers..... 43</p> | <p><b>7 Application and Implementation</b>..... 100</p> <p>    7.1 Application Information..... 100</p> <p>    7.2 Typical Application..... 103</p> <p><b>8 Layout</b>..... 107</p> <p>    8.1 Recommended Implementation..... 107</p> <p>    8.2 PCB Layout for Minimizing Noise..... 108</p> <p><b>9 Device and Documentation Support</b>..... 109</p> <p>    9.1 Documentation Support..... 109</p> <p>    9.2 Receiving Notification of Documentation Updates.. 109</p> <p>    9.3 Support Resources..... 109</p> <p>    9.4 Trademarks..... 109</p> <p>    9.5 Electrostatic Discharge Caution..... 109</p> <p>    9.6 Glossary..... 109</p> <p><b>10 Revision History</b>..... 109</p> <p><b>11 Mechanical, Packaging, and Orderable Information</b>..... 109</p> |
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## 4 Pin Configuration and Functions

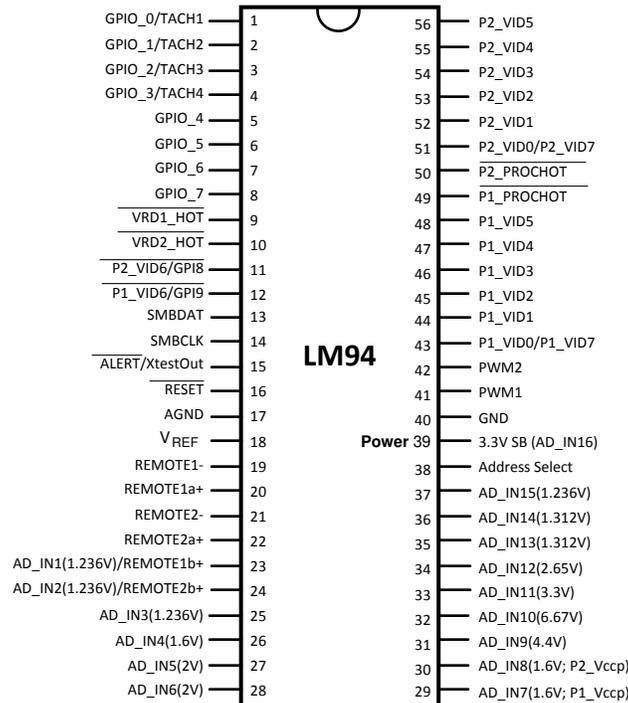


Figure 4-1. 56 Pin TSSOP Package See Package Number DGG0056A TOP VIEW

Table 4-1. Pin Descriptions<sup>(1)</sup>

| Symbol                | Pin No. | Type                     | Function  |
|-----------------------|---------|--------------------------|---|
| GPIO_0/TACH1          | 1       | Digital I/O (Open-Drain) | Can be configured as fan tach input or a general purpose open-drain digital I/O.  |
| GPIO_1/TACH2          | 2       | Digital I/O (Open-Drain) | Can be configured as fan tach input or a general purpose open-drain digital I/O.  |
| GPIO_2/TACH3          | 3       | Digital I/O (Open-Drain) | Can be configured as fan tach input or a general purpose open-drain digital I/O.  |
| GPIO_3/TACH4          | 4       | Digital I/O (Open-Drain) | Can be configured as fan tach input or a general purpose open-drain digital I/O..   |
| GPIO_4 / P1_THERMTRIP | 5       | Digital I/O (Open-Drain) | A general purpose open-drain digital I/O. Can be configured to monitor a CPU's THERMTRIP signal to mask other errors. Supports TTL input logic levels and AGTL compatible input logic levels. |
| GPIO_5 / P2_THERMTRIP | 6       | Digital I/O (Open-Drain) | A general purpose open-drain digital I/O. Can be configured to monitor a CPU's THERMTRIP signal to mask other errors. Supports TTL input logic levels and AGTL compatible input logic levels. |
| GPIO_6                | 7       | Digital I/O (Open-Drain) | Can be used to detect the state of CPU1 IERR or a general purpose open-drain digital I/O. Supports TTL input logic levels and AGTL compatible input logic levels.                             |
| GPIO_7                | 8       | Digital I/O (Open-Drain) | Can be used to detect the state of CPU2 IERR or a general purpose open-drain digital I/O. Supports TTL input logic levels and AGTL compatible input logic levels.                             |
| VRD1_HOT              | 9       | Digital Input            | CPU1 voltage regulator HOT. Supports TTL input logic levels and AGTL compatible input logic levels.   |
| VRD2_HOT              | 10      | Digital Input            | CPU2 voltage regulator HOT. Supports TTL input logic levels and AGTL compatible input logic levels.   |
| P2_VID6/ GPI8         | 11      | Digital Input            | CPU2 VID6 input. Could also be used as a general purpose input to trigger an error event. Supports TTL input logic levels and AGTL compatible input logic levels.                             |

**Table 4-1. Pin Descriptions<sup>(1)</sup> (continued)**

| Symbol           | Pin No. | Type  | Function  |
|------------------|---------|---|---|
| P1_VID6/ GPI9    | 12      | Digital Input                                 | CPU1 VID6 input. Could also be used as a general purpose input to trigger an error event. Supports TTL input logic levels and AGTL compatible input logic levels.   |
| SMBDAT           | 13      | Digital I/O (Open-Drain)                      | Bidirectional System Management Bus Data. Output configured as 5V tolerant open-drain. SMBus 2.0 compliant.   |
| SMBCLK           | 14      | Digital Input                                 | System Management Bus Clock. Driven by an open-drain output, and is 5V tolerant. SMBus 2.0 Compliant.   |
| ALERT/XtestOut   | 15      | Digital Output (Open-Drain)                   | Open-drain ALERT output used in an interrupt driven system to signal that an error event has occurred. Masked error events do not activate the ALERT output. When in XOR tree test mode, functions as XOR Tree output.  |
| RESET            | 16      | Digital I/O (Open-Drain)                      | Open-drain reset output when power is first applied to the LM94. Used as a reset for devices powered by 3.3V stand-by. After reset, this pin becomes a reset input. See Section 7.1.2 for more information. If this pin is not used, connection to an external resistive pull-up is required to prevent LM94 malfunction.   |
| AGND             | 17      | GROUND Input                                  | Analog Ground. Digital ground and analog ground need to be tied together at the chip then both taken to a low noise system ground. A voltage difference between analog and digital ground may cause erroneous results.  |
| V <sub>REF</sub> | 18      | Analog Output                                 | 2.5V used for external ADC reference, or as a V <sub>REF</sub> reference voltage  |
| REMOTE1-         | 19      | Remote Thermal Diode_1- Input (CPU 1 THERMDC) | This is the negative input (current sink) from both of the CPU1 thermal diodes. Connected to THERMDC pin of Pentium processor or the emitter of a diode connected MMBT3904 NPN transistor. Serves as the negative input into the A/D for thermal diode voltage measurements. A 100 pF capacitor is optional and can be connected between REMOTE1- and REMOTE1+.   |
| REMOTE1a+        | 20      | Remote Thermal Diode_1+ I/O (CPU1 THERMDA1)   | This is a positive connection to the first CPU1 thermal diode. Serves as the positive input into the A/D for thermal diode voltage measurements. It also serves as a current source output that forward biases the thermal diode. Connected to THERMDA pin of Pentium processor or the base of a diode connected MMBT3904 NPN transistor. A 100 pF capacitor is optional and can be connected between REMOTE1- and each REMOTE1+. |
| REMOTE2-         | 21      | Remote Thermal Diode_2 - Input (CPU2 THERMDC) | This is the negative input (current sink) from both of the CPU2 thermal diodes. Connected to THERMDC pins of Pentium processor or the emitter of a diode connected MMBT3904 NPN transistor. Serves as the negative input into the A/D for thermal diode voltage measurements. A 100 pF capacitor is optional and can be connected between REMOTE2- and each REMOTE2+.   |
| REMOTE2a+        | 22      | Remote Thermal Diode_2 + I/O (CPU2 THERMDA1)  | This is a positive connection to the first CPU2 thermal diode. Serves as the positive input into the A/D for thermal diode voltage measurements. It also serves as a current source output that forward biases the thermal diode. Connected to THERMDA pin of Pentium processor or the base of a diode connected MMBT3904 NPN transistor. A 100 pF capacitor is optional and can be connected between REMOTE2- and REMOTE2+.      |
| AD_IN1/REMOTE1b+ | 23      | Analog Input (+12V1 or CPU1 THERMDA2)         | Analog Input for +12V Rail 1 monitoring, for CPU1 voltage regulator. External attenuation resistors required such that 12V is attenuated to 0.927V for nominal ¾ scale reading. This pin may also serve as the second positive thermal diode input for CPU1.  |
| AD_IN2/REMOTE2b+ | 24      | Analog Input (+12V2 or CPU2 THERMDA2)         | Analog Input for +12V Rail 2 monitoring, for CPU2 voltage regulator. External attenuation resistors required such that 12V is attenuated to 0.927V for nominal ¾ scale reading. This pin may also serve as the second positive thermal diode input for CPU2.  |
| AD_IN3           | 25      | Analog Input (+12V3)                          | Analog Input for +12V Rail 3, for Memory/3GIO slots. External attenuation resistors required such that 12V is attenuated to 0.927V for nominal ¾ scale reading.   |
| AD_IN4           | 26      | Analog Input (FSB_Vtt)                        | Analog input for 1.2V monitoring, nominal ¾ scale reading   |
| AD_IN5           | 27      | Analog Input (3GIO / PXH / MCH_Core)          | Analog input for 1.5V monitoring, nominal ¾ scale reading   |
| AD_IN6           | 28      | Analog Input (ICH_Core)                       | Analog input for 1.5V monitoring, nominal ¾ scale reading   |

**Table 4-1. Pin Descriptions<sup>(1)</sup> (continued)**

| Symbol            | Pin No. | Type   | Function  |
|-------------------|---------|--|---|
| AD_IN7 (P1_Vccp)  | 29      | Analog Input (CPU1_Vccp)                     | Analog input for +Vccp (processor voltage) monitoring.  |
| AD_IN8 (P2_Vccp)  | 30      | Analog Input (CPU2_Vccp)                     | Analog input for +Vccp (processor voltage) monitoring.  |
| AD_IN9            | 31      | Analog Input (+3.3V)                         | Analog input for +3.3V monitoring, nominal ¾ scale reading  |
| AD_IN10           | 32      | Analog Input (+5V)                           | Analog input for +5V monitoring silver box supply monitoring, nominal ¾ scale reading   |
| AD_IN11           | 33      | Analog Input (SCSI_Core)                     | Analog input for +2.5V monitoring, nominal ¾ scale reading. This pin may also be used to monitor an analog temperature sensor such as the LM60, since readings from this input can be routed to the fan control logic.  |
| AD_IN12           | 34      | Analog Input (Mem_Core)                      | Analog input for +1.969V monitoring, nominal ¾ scale reading.   |
| AD_IN13           | 35      | Analog Input (Mem_Vtt)                       | Analog input for +0.984V monitoring, nominal ¾ scale reading.   |
| AD_IN14           | 36      | Analog Input (Gbit_Core)                     | Analog input for +0.984V S/B monitoring, nominal ¾ scale reading.   |
| AD_IN15           | 37      | Analog Input (-12V)                          | Analog input for -12V monitoring. External resistors required to scale to positive level. Full scale reading at 1.236V, nominal ¾ scale reading. This pin may also be used to monitor an analog temperature sensor such as the LM60, since readings from this input can be routed to the fan control logic.   |
| Address Select    | 38      | 3 level analog input                         | This input selects the lower two bits of the LM94 SMBus slave address.  |
| 3.3V SB (AD_IN16) | 39      | POWER (V <sub>DD</sub> ) +3.3V standby power | V <sub>DD</sub> power input for LM94. Generally this is connected to +3.3V standby power. The LM94 can be powered by +3.3V if monitoring in low power states is not required, but power should be applied to this input before any other pins. This pin also serves as the analog input to monitor the 3.3V stand-by (SB) voltage. It is necessary to bypass this pin with a 0.1 µF in parallel with 100 pF. A bulk capacitance of 10 µF should be in the near vicinity. The 100 pF should be closest to the power pin. |
| GND               | 40      | GROUND                                       | Digital Ground. Digital ground and analog ground need to be tied together at the chip then both taken to a low noise system ground. A voltage difference between analog and digital ground may cause erroneous results.   |
| PWM1              | 41      | Digital Output (Open-Drain)                  | Fan control output 1.   |
| PWM2              | 42      | Digital Output (Open-Drain)                  | Fan control output 2  |
| P1_VID0/P1_VID7   | 43      | Digital Input                                | Voltage Identification signal from the processor. Supports TTL input logic levels and AGTL compatible input logic levels.   |
| P1_VID1           | 44      | Digital Input                                | Voltage Identification signal from the processor. Supports TTL input logic levels and AGTL compatible input logic levels.   |
| P1_VID2           | 45      | Digital Input                                | Voltage Identification signal from the processor. Supports TTL input logic levels and AGTL compatible input logic levels.   |
| P1_VID3           | 46      | Digital Input                                | Voltage Identification signal from the processor. Supports TTL input logic levels and AGTL compatible input logic levels.   |
| P1_VID4           | 47      | Digital Input                                | Voltage Identification signal from the processor. Supports TTL input logic levels and AGTL compatible input logic levels.   |
| P1_VID5           | 48      | Digital Input                                | Voltage Identification signal from the processor. Supports TTL input logic levels and AGTL compatible input logic levels.   |
| P1_PROCHOT        | 49      | Digital I/O (Open-Drain)                     | Connected to CPU1 PROCHOT (processor hot) signal through a bidirectional level shifter. Supports TTL input logic level.   |
| P2_PROCHOT        | 50      | Digital I/O (Open-Drain)                     | Connected to CPU2 PROCHOT (processor hot) signal through a bidirectional level shifter. Supports TTL input logic level.   |
| P2_VID0/P2_VID7   | 51      | Digital Input                                | Voltage Identification signal from the processor. Supports TTL input logic levels and AGTL compatible input logic levels.   |
| P2_VID1           | 52      | Digital Input                                | Voltage Identification signal from the processor. Supports TTL input logic levels and AGTL compatible input logic levels.   |

**Table 4-1. Pin Descriptions<sup>(1)</sup> (continued)**

| Symbol  | Pin No. | Type          | Function  |
|---------|---------|---------------|---|
| P2_VID2 | 53      | Digital Input | Voltage Identification signal from the processor. Supports TTL input logic levels and AGTL compatible input logic levels. |
| P2_VID3 | 54      | Digital Input | Voltage Identification signal from the processor. Supports TTL input logic levels and AGTL compatible input logic levels. |
| P2_VID4 | 55      | Digital Input | Voltage Identification signal from the processor. Supports TTL input logic levels and AGTL compatible input logic levels. |
| P2_VID5 | 56      | Digital Input | Voltage Identification signal from the processor. Supports TTL input logic levels and AGTL compatible input logic levels. |

(1) The over-score indicates the signal is active low (“Not”).

## 4.1 Server Terminology

|                  |  |
|------------------|--|
| A/D              | Analog to Digital Converter  |
| ACPI             | Advanced Configuration and Power Interface   |
| ALERT            | SMBus signal to bus master that an event occurred that has been flagged for attention. |
| ASF              | Alert Standard Format  |
| BMC              | Baseboard Management Controller  |
| BW               | Bandwidth  |
| DIMM             | Dual in line memory module   |
| DP               | Dual-processor   |
| ECC              | Error checking and correcting  |
| FRU              | Field replaceable unit   |
| FSB              | Front side bus   |
| FW               | Firmware   |
| Gb               | Gigabit  |
| GB               | Gigabyte   |
| Gbe              | Gigabit Ethernet   |
| GPI              | General purpose input  |
| GPIO             | General purpose I/O  |
| HW               | Hardware   |
| I <sup>2</sup> C | Inter integrated circuit (bus)   |
| LAN              | Local area network   |
| LSb              | Least Significant Bit  |
| LSB              | Least Significant Byte   |
| LVDS             | Low-Voltage Differential Signaling   |
| LUT              | Look-Up Table  |
| Mb               | Megabit  |
| MB               | Megabyte   |
| MP               | Multi-processor  |
| MSb              | Most Significant Bit   |
| MSB              | Most Significant Byte  |
| MTBF             | Mean time between failures   |
| MTTR             | Mean time to repair  |
| NIC              | Network Interface Card (Ethernet Card)   |
| OS               | Operating system   |
| P/S              | Power Supply   |
| PCI              | PCI Local Bus  |

**LM94**

SNAS264D – APRIL 2006 – REVISED FEBRUARY 2024

|                   |  |
|-------------------|--|
| PDB               | Power Distribution Board   |
| POR               | Power On Reset   |
| PS                | Power Supply   |
| SMBCLK and SMBDAT | These signals comprise the SMBus interface (data and clock). See the <a href="#">Section 6.3.1</a> section for more information. |
| VRD               | Voltage Regulator Down - regulates Vccp voltage for a CPU  |

## 5 Specifications

### 5.1 Absolute Maximum Ratings

See (1) (2) (3)

|  |                      |                               |
|--|----------------------|-------------------------------|
| Positive Supply Voltage ( $V_{DD}$ )   |                      | 6.0V                          |
| Voltage on Any Digital Input or Output Pin   |                      | -0.3V to 6.0V                 |
| Voltage on +5V Input   |                      | -0.3V to +6.667V              |
| Voltage at Positive Remote Diode Inputs, AD_IN1, AD_IN2, AD_IN3, and AD_IN15 Inputs  |                      | -0.3V to ( $V_{DD} + 0.05V$ ) |
| Voltage at Other Analog Voltage Inputs   |                      | -0.3V to +6.0V                |
| Input Current at Thermal Diode Negative Inputs   |                      | $\pm 1$ mA                    |
| Input Current at any pin (4)   |                      | $\pm 10$ mA                   |
| Package Input Current (4)  |                      | $\pm 100$ mA                  |
| Maximum Junction Temperature (5) ( $T_{JMAX}$ )  |                      | 150 °C                        |
| ESD Susceptibility (6)   | Human Body Model     | 3 kV                          |
|  | Machine Model        | 300V                          |
|  | Charged Device Model | 750V                          |
| Storage Temperature(7)   |                      | -65°C to +150°C               |
| For soldering specifications, see product folder at <a href="http://www.ti.com/packaging">www.ti.com/packaging</a> and <a href="#">SNOA549</a> (8) |                      |                               |

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
- (2) All voltages are measured with respect to GND, unless otherwise noted.
- (3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
- (4) When the input voltage ( $V_{IN}$ ) at any pin exceeds the power supplies ( $V_{IN} < (GND \text{ or } AGND)$  or  $V_{IN} > V_{DD}$ , except for analog voltage inputs), the current at that pin should be limited to 10 mA. The 100 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 10 mA to ten. Parasitic components and/or ESD protection circuitry are shown below for the LM94's pins. Care should be taken not to forward bias the parasitic diode, D1, present on pins D+ and D- as shown in circuits C and D. Doing so by more than 50 mV may corrupt temperature measurements. D1 and the ESD Clamp are connected between V+ ( $V_{DD}$ , AD\_IN16) and GND as shown in circuit B. SNP stands for snap-back device.
- (5) Typical parameters are at  $T_J = T_A = 25$  °C and represent most likely parametric norm.
- (6) Human body model, 100 pF discharged through a 1.5 k $\Omega$  resistor. Machine model, 200 pF discharged directly into each pin. Charged device model (CDM) simulates a pin slowly acquiring charge (such as from a device sliding down the feeder in an automated assembler) then rapidly being discharged.
- (7) Reflow temperature profiles are different for lead-free and non lead-free packages.
- (8) See the URL "[www.ti.com/packaging](http://www.ti.com/packaging)" for other recommendations and methods of soldering surface mount devices.

### 5.2 Operating Ratings

See (1) (2)

|                                   |  |                                 |
|-----------------------------------|--|---------------------------------|
|                                   |  | $T_{MIN} \leq T_A \leq T_{MAX}$ |
| Operating Temperature Range       |  | 0°C $\leq T_A \leq$ +85°C       |
| Nominal Supply Voltage            |  | 3.3V                            |
| Supply Voltage Range ( $V_{DD}$ ) |  | +3.0V to +3.6V                  |
| VID0-VID5                         |  | -0.05V to +5.5V                 |
| Digital Input Voltage Range       |  | -0.05V to ( $V_{DD} + 0.05V$ )  |
| Package Thermal Resistance (3)    |  | 79°C/W                          |

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the

Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

- (2) All voltages are measured with respect to GND, unless otherwise noted.
- (3) The maximum power dissipation must be de-rated at elevated temperatures and is dictated by  $T_{JMAX}$ ,  $\theta_{JA}$  and the ambient temperature,  $T_A$ . The maximum allowable power dissipation at any temperature is  $P_{D MAX} = (T_{JMAX} - T_A) / \theta_{JA}$ . The  $\theta_{JA}$  for the LM94 when mounted to 1 oz. copper foil PCB the  $\theta_{JA}$  with different air flow is listed in the following table.

| Air Flow            | Junction to Ambient Thermal Resistance, $\theta_{JA}$ |
|---------------------|---|
| 0 m/s               | 79 °C/W   |
| 1.14 m/s (225 LFPM) | 62 °C/W   |
| 2.54 m/s (500 LFPM) | 52 °C/W   |

### 5.3 DC Electrical Characteristics

The following limits apply for +3.0 V<sub>DC</sub> to +3.6 V<sub>DC</sub>, unless otherwise noted. **Bold face limits apply for  $T_A = T_J$  over  $T_{MIN}$  to  $T_{MAX}$  of the operating range;** all other limits  $T_A = T_J = 25^\circ\text{C}$  unless otherwise noted.  $T_A$  is the ambient temperature of the LM94;  $T_J$  is the junction temperature of the LM94;  $T_D$  is the junction temperature of the thermal diode.

| Parameter  | Test Conditions  | Typical<br>(1) | Limits<br>(2)               | Units<br>(Limits)      |
|--|--|----------------|-----------------------------|------------------------|
| <b>POWER SUPPLY CHARACTERISTICS</b>  |  |                |                             |                        |
| Power Supply Current   | Converting, Interface and Fans Inactive, Peak Current  | 2              | <b>2.75</b>                 | mA (max)               |
|  | Converting, Interface and Fans Inactive, Average Current   | 1.6            |                             | mA                     |
| Power-On Reset Threshold Voltage   |  | 2              | <b>1.6</b>                  | V (min)                |
|  |  |                | <b>2.7</b>                  | V (max)                |
| <b>TEMPERATURE-TO-DIGITAL CONVERTER CHARACTERISTICS</b>  |  |                |                             |                        |
| Local Temperature Accuracy Over Full Range   | $0^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$   | $\pm 2$        | <b><math>\pm 3</math></b>   | $^\circ\text{C}$ (max) |
|  | $T_A = +55^\circ\text{C}$  | $\pm 1$        | <b><math>\pm 2.5</math></b> | $^\circ\text{C}$ (max) |
| Local Temperature Resolution   |  | 1              |                             | $^\circ\text{C}$       |
| Remote Thermal Diode Temperature Accuracy Over Full Range; targeted for a typical Pentium processor on 90 nm or 65 nm process <sup>(3)</sup> | $0^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ and $0^\circ\text{C} \leq T_D \leq 100^\circ\text{C}$ |                | <b><math>\pm 3</math></b>   | $^\circ\text{C}$ (max) |
|  | $0^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ and $T_D = 70^\circ\text{C}$                          |                | <b><math>\pm 2.5</math></b> | $^\circ\text{C}$ (max) |
| Remote Thermal Diode Temperature Accuracy; targeted for a typical Pentium processor on 90nm or 65nm process <sup>(3)</sup>                   | $0^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ and $25^\circ\text{C} \leq T_D \leq 70^\circ\text{C}$ | $\pm 1$        |                             | $^\circ\text{C}$       |
| Remote Temperature Resolution  |  | 1              |                             | $^\circ\text{C}$       |
| Thermal Diode Source Current   | High Level   | 172            | <b>230</b>                  | $\mu\text{A}$ (max)    |
|  | Low Level  | 10.75          |                             | $\mu\text{A}$          |
| Thermal Diode Current Ratio  |  | 16             |                             |                        |
| $T_C$  | Total Monitoring Cycle Time  |                | <b>100</b>                  | ms (max)               |
| <b>ANALOG-TO-DIGITAL VOLTAGE MEASUREMENT CONVERTER CHARACTERISTICS</b>   |  |                |                             |                        |
| TUE  | Total Unadjusted Error <sup>(4) (5)</sup>  |                | <b><math>\pm 2</math></b>   | % of FS (max)          |
| DNL  | Differential Non-Linearity   | $\pm 1$        |                             | LSB                    |
| PSS  | Power Supply ( $V_{DD}$ ) Sensitivity  | $\pm 1$        |                             | %/V (of FS)            |
| $T_C$  | Total Monitoring Cycle Time  |                | <b>100</b>                  | ms (max)               |
|  | Input Resistance for Inputs with Dividers  | 200            | <b>140</b>                  | k $\Omega$ (min)       |
|  | AD_IN1- AD_IN3 and AD_IN15 Analog Input Leakage Current <sup>(6)</sup>                                 |                | 60                          | nA (max)               |
| <b>REFERENCE OUTPUT (<math>V_{REF}</math>) CHARACTERISTICS</b>   |  |                |                             |                        |

### 5.3 DC Electrical Characteristics (continued)

The following limits apply for +3.0 V<sub>DC</sub> to +3.6 V<sub>DC</sub>, unless otherwise noted. **Bold face limits apply for T<sub>A</sub> = T<sub>J</sub> over T<sub>MIN</sub> to T<sub>MAX</sub> of the operating range;** all other limits T<sub>A</sub> = T<sub>J</sub> = 25°C unless otherwise noted. T<sub>A</sub> is the ambient temperature of the LM94; T<sub>J</sub> is the junction temperature of the LM94; T<sub>D</sub> is the junction temperature of the thermal diode.

| Parameter   |  | Test Conditions   | Typical<br>(1) | Limits<br>(2)                | Units<br>(Limits)  |
|---|--|---|----------------|------------------------------|--------------------|
|   | Tolerance  |   |                | <b>±1</b>                    | % (max)            |
| V <sub>REF</sub>  | Output Voltage (7)   |   | 2.500          | <b>2.525</b><br><b>2.475</b> | V (max)<br>V (min) |
|   | Load Regulation  | I <sub>SOURCE</sub> = -2 mA<br>I <sub>SINK</sub> = 2 mA | 0.1            |                              | %                  |
| <b>DIGITAL OUTPUTS: PWM1, PWM2</b>  |  |   |                |                              |                    |
| I <sub>OL</sub>   | Maximum Current Sink   |   |                | <b>8</b>                     | mA (min)           |
| V <sub>OL</sub>   | Output Low Voltage   | I <sub>OUT</sub> = 8.0 mA                               |                | <b>0.4</b>                   | V (max)            |
| <b>DIGITAL OUTPUTS: ALL</b>   |  |   |                |                              |                    |
| V <sub>OL</sub>   | Output Low Voltage (Note excessive current flow causes self-heating and degrades the internal temperature accuracy.) | I <sub>OUT</sub> = 4.0 mA                               |                | <b>0.4</b>                   | V (min)            |
|   |  | I <sub>OUT</sub> = 6 mA                                 |                | <b>0.55</b>                  | V (min)            |
| I <sub>OH</sub>   | High Level Output Leakage Current  | V <sub>OUT</sub> = V <sub>DD</sub>                      | 0.1            | <b>10</b>                    | µA (max)           |
| I <sub>OTMAX</sub>  | Maximum Total Sink Current for all Digital Outputs Combined  |   |                | <b>32</b>                    | mA (max)           |
| C <sub>O</sub>  | Digital Output Capacitance   |   | 20             |                              | pF                 |
| <b>DIGITAL INPUTS: ALL</b>  |  |   |                |                              |                    |
| V <sub>IH</sub>   | Input High Voltage Except Address Select(8)  |   |                | <b>2.1</b>                   | V (min)            |
| V <sub>IL</sub>   | Input Low Voltage Except Address Select(8)   |   |                | <b>0.8</b>                   | V (max)            |
| V <sub>IH</sub>   | Input High Voltage for Address Select(8)   |   |                | <b>90% V<sub>DD</sub></b>    | V (min)            |
| V <sub>IM</sub>   | Input Mid Voltage for Address Select   |   |                | <b>43% V<sub>DD</sub></b>    | V (min)            |
|   |  |   |                | <b>57% V<sub>DD</sub></b>    | V (max)            |
| V <sub>IL</sub>   | Input Low Voltage for Address Select(8)  |   |                | <b>10% V<sub>DD</sub></b>    | V (max)            |
| V <sub>HYST</sub>   | DC Hysteresis  |   | 0.3            |                              | V                  |
| I <sub>IH</sub>   | Input High Current   | V <sub>IN</sub> = V <sub>DD</sub>                       |                | <b>-10</b>                   | µA (min)           |
| I <sub>IL</sub>   | Input Low Current  | V <sub>IN</sub> = 0V                                    |                | <b>10</b>                    | µA (max)           |
| C <sub>IN</sub>   | Digital Input Capacitance  |   | 20             |                              | pF                 |
| <b>DIGITAL INPUTS: P1_VIDx, P2_VIDx, GPI_9, GPI_8, GPIO_7, GPIO_6, GPIO_5, GPIO_4 (When respective bit set in Register BEh GPI/VID Level Control)</b> |  |   |                |                              |                    |
| V <sub>IH</sub>   | Alternate Input High Voltage (AGTL+ Compatible)  |   |                | <b>0.8</b>                   | V (min)            |
| V <sub>IL</sub>   | Alternate Input Low Voltage (AGTL+ Compatible)   |   |                | <b>0.4</b>                   | V (max)            |

- (1) Typical parameters are at T<sub>J</sub> = T<sub>A</sub> = 25 °C and represent most likely parametric norm.
- (2) Limits are specified to Texas Instrument's AOQL (Average Outgoing Quality Level).
- (3) At the time of first publication of this specification (Jan 2006), this specification applies to either Pentium or Xeon Processors on 90nm or 65nm process when TruTherm is selected. When TruTherm is deselected this specification applies to an MMBT3904. This specification does include the error caused by the variability of the diode ideality and series resistance parameters.
- (4) Total Monitoring Cycle Time includes all temperature and voltage conversions.
- (5) TUE (Total Unadjusted Error) includes Offset, Gain and Linearity errors of the ADC.
- (6) Leakage current approximately doubles every 20 °C.
- (7) A total digital I/O current of 40 mA can cause 6 mV of offset in Vref.
- (8) Timing specifications are tested at the TTL logic levels, V<sub>IL</sub> = 0.4V for a falling edge and V<sub>IH</sub> = 2.4V for a rising edge. TRI-STATE output voltage is forced to 1.4V.

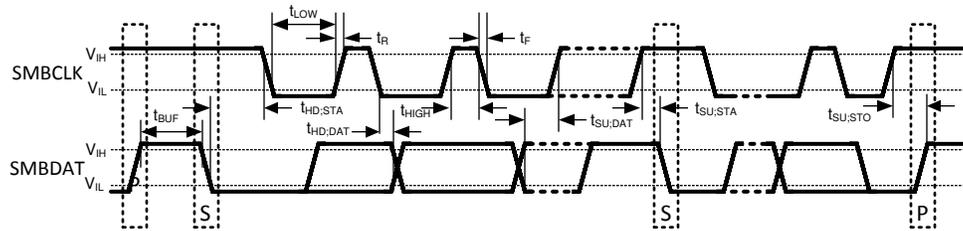
## 5.4 AC Electrical Characteristics

The following limits apply for +3.0 V<sub>DC</sub> to +3.6 V<sub>DC</sub>, unless otherwise noted. **Bold face limits apply for T<sub>A</sub> = T<sub>J</sub> = T<sub>MIN</sub> to T<sub>MAX</sub> of the operating range;** all other limits T<sub>A</sub> = T<sub>J</sub> = 25°C unless otherwise noted.

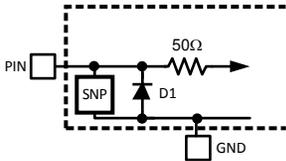
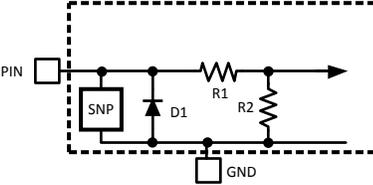
| Parameter                                 |  | Test Conditions           | Typical<br>(1) | Limits<br>(2)             | Units<br>(Limits)          |
|---|--|---------------------------|----------------|---------------------------|----------------------------|
| <b>FAN RPM-TO-DIGITAL CHARACTERISTICS</b> |  |                           |                |                           |                            |
|   | Counter Resolution   |                           | 14             |                           | bits                       |
|   | Number of fan tach pulses count is based on  |                           | 2              |                           | pulses                     |
|   | Counter Frequency  |                           | 22.5           |                           | kHz                        |
|   | Accuracy   |                           |                | <b>±6</b>                 | % (max)                    |
| <b>PWM OUTPUT CHARACTERISTICS</b>         |  |                           |                |                           |                            |
|   | Frequency Tolerances   |                           |                | <b>±6</b>                 | % (max)                    |
|   | Duty-Cycle Tolerance   |                           | ±2             | <b>±6</b>                 | % (max)                    |
| <b>RESET INPUT/OUTPUT CHARACTERISTICS</b> |  |                           |                |                           |                            |
|   | Output Pulse Width Upon Power Up   |                           |                | <b>250</b><br><b>330</b>  | ms (min)<br>ms (max)       |
|   | Minimum Input Pulse Width  |                           |                | <b>10</b>                 | µs (min)                   |
|   | Reset Output Fall Time   | 1.6V to 0.4V Logic Levels |                | <b>1</b>                  | µs (max)                   |
| <b>SMBus TIMING CHARACTERISTICS</b>       |  |                           |                |                           |                            |
| f <sub>SMBCLK</sub>                       | SMBCLK (Clock) Clock Frequency   |                           |                | <b>10</b><br><b>100</b>   | kHz (min)<br>kHz (max)     |
| t <sub>BUF</sub>                          | SMBus Free Time between Stop and Start Conditions  |                           |                | <b>4.7</b>                | µs (min)                   |
| t <sub>HD,STA</sub>                       | Hold time after (Repeated) Start Condition. After this period, the first clock is generated.   |                           |                | <b>4.0</b>                | µs (min)                   |
| t <sub>SU,STA</sub>                       | Repeated Start Condition Setup Time  |                           |                | <b>4.7</b>                | µs (min)                   |
| t <sub>SU,STO</sub>                       | Stop Condition Setup Time  |                           |                | <b>4.0</b>                | µs (min)                   |
| t <sub>SU,DAT</sub>                       | Data Input Setup Time to SMBCLK High   |                           |                | <b>250</b>                | ns (min)                   |
| t <sub>HD,DAT</sub>                       | Data Output Hold Time after SMBCLK Low   |                           |                | <b>300</b><br><b>1075</b> | ns (min)<br>ns (max)       |
| t <sub>LOW</sub>                          | SMBCLK Low Period  |                           |                | <b>4.7</b><br><b>50</b>   | µs (min)<br>µs (max)       |
| t <sub>HIGH</sub>                         | SMBCLK High Period   |                           |                | <b>4.0</b><br><b>50</b>   | µs (min)<br>µs (max)       |
| t <sub>R</sub>                            | Rise Time  |                           |                | <b>1</b>                  | µs (max)                   |
| t <sub>F</sub>                            | Fall Time  |                           |                | <b>300</b>                | ns (max)                   |
| t <sub>TIMEOUT</sub>                      | Timeout SMBDAT or SMBCLK low time required to reset the Serial Bus Interface to the Idle State |                           | 31             | <b>25</b><br><b>35</b>    | ms<br>ms (min)<br>ms (max) |
| t <sub>POR</sub>                          | Time in which a device must be operational after power-on reset                                | V <sub>DD</sub> > +2.8V   |                | <b>500</b>                | ms (max)                   |
| C <sub>L</sub>                            | Capacitance Load on SMBCLK and SMBDAT  |                           |                | <b>400</b>                | pF (max)                   |

(1) Typical parameters are at T<sub>J</sub> = T<sub>A</sub> = 25 °C and represent most likely parametric norm.

(2) Limits are specified to Texas Instrument's AOQL (Average Outgoing Quality Level).



| Symbol                | Pin No. | Circuit                            | All Input Circuits                  |
|-----------------------|---------|------------------------------------|-------------------------------------|
| GPIO_0/TACH1          | 1       | A                                  | <p><b>Figure 5-1. Circuit A</b></p> |
| GPIO_1/TACH2          | 2       | A                                  |                                     |
| GPIO_2/TACH3          | 3       | A                                  |                                     |
| GPIO_3/TACH4          | 4       | A                                  |                                     |
| GPIO_4 / P1_THERMTRIP | 5       | A                                  |                                     |
| GPIO_5 / P2_THERMTRIP | 6       | A                                  |                                     |
| GPIO_6                | 7       | A                                  |                                     |
| GPIO_7                | 8       | A                                  |                                     |
| VRD1_HOT              | 9       | A                                  |                                     |
| VRD2_HOT              | 10      | A                                  |                                     |
| SCSI_TERM1            | 11      | A                                  |                                     |
| SCSI_TERM2            | 12      | A                                  |                                     |
| SMBDAT                | 13      | A                                  |                                     |
| SMBCLK                | 14      | A                                  |                                     |
| ALERT/XtestOut        | 15      | A                                  |                                     |
| RESET                 | 16      | A                                  |                                     |
| AGND                  | 17      | B (Internally shorted to GND pin.) |                                     |
| V <sub>REF</sub>      | 18      | A                                  | <p><b>Figure 5-3. Circuit C</b></p> |
| REMOTE1-              | 19      | C                                  |                                     |
| REMOTE1+              | 20      | D                                  |                                     |
| REMOTE2-              | 21      | C                                  |                                     |
| REMOTE+               | 22      | D                                  |                                     |
| AD_IN1                | 23      | D                                  |                                     |
| AD_IN2                | 24      | D                                  |                                     |
| AD_IN3                | 25      | D                                  |                                     |
| AD_IN4                | 26      | E                                  |                                     |
| AD_IN5                | 27      | E                                  |                                     |
| AD_IN6                | 28      | E                                  |                                     |
| AD_IN7                | 29      | E                                  |                                     |
| AD_IN8                | 30      | E                                  |                                     |
| AD_IN9                | 31      | E                                  |                                     |
| AD_IN10               | 32      | E                                  |                                     |
| AD_IN11               | 33      | E                                  |                                     |

| Symbol                       | Pin No. | Circuit                        | All Input Circuits  |  |
|------------------------------|---------|--------------------------------|---|--|
| AD_IN12                      | 34      | E                              |  <p><b>Figure 5-4. Circuit D</b></p> |  |
| AD_IN13                      | 35      | E                              |   |  |
| AD_IN14                      | 36      | E                              |   |  |
| AD_IN15                      | 37      | D                              |   |  |
| ADDR_SEL                     | 38      | A                              |   |  |
| AD_IN16/V <sub>DD</sub> (V+) | 39      | B                              |   |  |
| GND                          | 40      | B (Internally shorted to AGND) |   |  |
| PWM1                         | 41      | A                              |   |  <p><b>Figure 5-5. Circuit E</b></p> |
| PWM2                         | 42      | A                              |   |  |
| P1_VID0                      | 43      | A                              |   |  |
| P1_VID1                      | 44      | A                              |   |  |
| P1_VID2                      | 45      | A                              |   |  |
| P1_VID3                      | 46      | A                              |   |  |
| P1_VID4                      | 47      | A                              |   |  |
| P1_VID5                      | 48      | A                              |   |  |
| P1_PROCHOT                   | 49      | A                              |   |  |
| P2_PROCHOT                   | 50      | A                              |   |  |
| P2_VID0                      | 51      | A                              |   |  |
| P2_VID1                      | 52      | A                              |   |  |
| P2_VID2                      | 53      | A                              |   |  |
| P2_VID3                      | 54      | A                              |   |  |
| P2_VID4                      | 55      | A                              |   |  |
| P2_VID5                      | 56      | A                              |   |  |

## 6 Detailed Description

### 6.1 Overview

The LM94 provides 16 channels of voltage monitoring, 4 remote thermal diode monitors, an internal/local ambient temperature sensor, 2  $\overline{\text{PROCHOT}}$  monitors, 4 fan tachometers, 8 GPIOs, THERMTRIP monitor for masking error events, 2 sets of 7 VID inputs, an  $\overline{\text{ALERT}}$  output and all the associated limit registers on a single chip, and communicates to the rest of the baseboard over the System Management Bus (SMBus). The LM94 also provides 2 PWM outputs and associated fan control logic for controlling the speed of system fans. There are two sets of fan control logic, a lookup table and a PI (proportional/integral) loop controller. The lookup table and PI controller are interactive, such that the fans run at the fastest required speed. Upon a temperature or fan tach error event, the PWM outputs may be programmed such that they automatically boost to 100% duty cycle. A timer is included that sets the minimum time that the fans are in the boost condition when activated by a fan tach error.

The LM94 incorporates Texas Instruments' TruTherm technology for precision "Remote Diode" readings of processors on 90nm process geometry or smaller. Readings from the external thermal diodes and the internal temperature sensor are made available as an 9-bit two's-complement digital value with the LSB representing 0.5°C. Filtered temperature readings are available as a 12-bit two's-complement digital value with the LSB representing 0.0625°C.

All but 4 of the analog inputs include internal scaling resistors. External scaling resistors are required for measuring  $\pm 12\text{V}$ . The inputs are converted to 8-bit digital values such that a nominal voltage appears at  $\frac{3}{4}$  scale for positive voltages and  $\frac{1}{4}$  scale for negative voltages. The analog inputs are intended to be connected to both baseboard resident VRDs and to standard voltage rails supplied by a SSI compliant power supply.

The LM94 has logic that ties a set of dynamically moving VID inputs to their associated V<sub>ccp</sub> analog input for real time window comparison fault determination. Voltage mapping for VRD10, VRD10 extended and VRD11 are supported by the LM94. When VRD10 mode is selected GPI8 and GPI9 can be used to detect external error flags whose state is reflected in the status registers.

Error events are captured in two sets of mirrored status registers (BMC Error Status Registers and Host Status Registers) allowing two controllers access to the status information without any interference.

The LM94's  $\overline{\text{ALERT}}$  output supports interrupt mode or comparator mode of operation. The comparator mode is only functional for thermal monitoring.

The LM94 provides a number of internal registers, which are detailed in the [Section 6.4](#) section of this document.

### 6.2 Feature Description

#### 6.2.1 Monitoring Cycle Time

When the LM94 is powered up, it cycles through each temperature measurement followed by the analog voltages in sequence, and it continuously loops through the sequence. The total monitoring cycle time is not more than 100 ms, as this is the time period that most external micro-controllers require to read the register values.

Each measured value is compared to values stored in the limit registers. When the measured value violates the programmed limit, a corresponding status bit in the B\_Error and H\_Error Status Registers is set.

The  $\overline{\text{PROCHOT}}$ , tachometer and dynamic VID/V<sub>ccp</sub> monitoring is performed independently of the analog and temperature monitoring cycle.

#### 6.2.2 $\Sigma\Delta$ A/D Inherent Averaging

The  $\Sigma\Delta$  A/D architecture filters the input signal. During one conversion many samples are taken of the input voltage and these samples are effectively averaged to give the final result. The output of the  $\Sigma\Delta$  A/D is the average value of the signal during the sampling interval. For a voltage measurement, the samples are accumulated for 1.5 ms. For a temperature measurement, the samples are accumulated for 8.4 ms.

### 6.2.3 Temperature Monitoring

The LM94 remote diode target is the embedded thermal diode found in a Xeon class processor in 90nm processes but can also work with any Intel based processor in 90nm or 65nm. The LM94 has an advanced thermal diode input stage using TI's TruTherm technology that reduces the spread in ideality found in sub-micron geometry thermal diodes. Internal analog filtering has been included in the thermal diode input stage thus minimizing the need for external thermal diode filter capacitors. In addition a digital filter has been included for the thermal diode temperature readings.

In some cases instead of using the embedded thermal diode, found on the Xeon processor, a diode connected 2N3904 transistor type can also be used. An example of this would be a MMBT3904 with its collector and base tied to the thermal diode REMOTE+ pin and the emitter tied to the thermal diode REMOTE- pin. Since the MMBT3904 is a surface mount device and has very small thermal mass, it measures the board temperature where it is mounted. The ideality and series resistance varies for different diodes. Therefore the LM94 has register support to allow calibration selection between a 2N3904 or a Xeon processor. The LM94 is optimized for typical Intel processors on 90nm or 65nm process or 2N3904 transistor. Other transistor types may be used but may have additional error that can be corrected for by programming the appropriate Zone Adjustment Offset register.

The LM94 acquires temperature data from four different sources:

- 4 external diodes (embedded in a processor or discrete)
- 1 internal diode (internal to the LM94)
- 2 analog temperature sensors, such as the LM60, that are connected to the AD\_IN11 or AD\_15 pins
- a temperature value can be externally written into an LM94 register from the SMBus.

All of these values, although not necessarily simultaneously, can be used to control fans, compared against limits, etc.

The temperature value registers are located at addresses 06h-09h, 50h-55h and 10h-23h. The temperature sources are referred to as "zones" for convenience:

| Zone    | Description   |
|---------|---|
| Zone 1a | Processor 1 remote diode 1 (REMOTE1a+, REMOTE1-)  |
| Zone 1b | Processor 1 remote diode 2 (REMOTE1b+, REMOTE1-)  |
| Zone 2a | Processor 2 remote diode 1 (REMOTE2a+, REMOTE2-)  |
| Zone 2b | Processor 2 remote diode 2 (REMOTE2b+, REMOTE2-)  |
| Zone 3  | Internal LM94 on-chip sensor or external LM60 analog sensor connected to AD_IN11; also accepts writes via SMBus         |
| Zone 4  | External digital temperature value from SMBus write to register 53h or external LM60 analog sensor connected to AD_IN15 |

#### 6.2.3.1 "Remote Diode" TruTherm Mode

The processor "remote thermal diode" is more correctly described as a transistor. The LM93 treated the "remote diode" as a diode thus introducing inaccuracies. These inaccuracies have become more apparent as the geometry of processors is shrinking. The LM94 can sense the "remote diode" using a new TruTherm technology that treats the remote device as a transistor. The TruTherm Mode is more accurate for processors on 90nm and smaller geometry. The LM94 still supports the old diode method and is calibrated for 2N3904 transistor type.

### 6.2.3.2 Temperature Data Format

Most of the temperature data for the LM94 is represented in three formats:

- 8-bit, two's complement byte with the LSb equal to 1.0°C; this applies to temperature measurements as well as any temperature limit registers and some configuration registers.

| Temperature <sup>(1)</sup> | Binary    | Hex |
|----------------------------|-----------|-----|
| +125°C                     | 0111 1101 | 7Dh |
| +25°C                      | 0001 1001 | 19h |
| +1.0°C                     | 0000 0001 | 01h |
| 0°C                        | 0000 0000 | 00h |
| -1.0°C                     | 1111 1111 | FFh |
| -25°C                      | 1110 0111 | E7h |
| -55°C                      | 1100 1001 | C9h |
| -127°C                     | 1000 0001 | 81h |

(1) A value of 80h has a special meaning in the limit registers. It means that the temperature channel is masked. In addition, temperature readings of 80h indicate thermal diode faults.

- 9-bit two's complement word with the LSb equal to 0.5°C; this applies to unfiltered temperature measurement extended resolution value registers

| Temperature | Binary    |           | Hex    |
|-------------|-----------|-----------|--------|
|             | MSB       | LSB       |        |
| +125.5°C    | 0111 1101 | 1000 0000 | 7D 80h |
| +25.5°C     | 0001 1001 | 1000 0000 | 19 80h |
| +0.5°C      | 0000 0000 | 1000 0000 | 00 80h |
| 0°C         | 0000 0000 | 0000 0000 | 00 00h |
| -0.5°C      | 1111 1111 | 1000 0000 | FF 80h |
| -25.5°C     | 1110 0111 | 1000 0000 | E7 80h |
| -55.5°C     | 1100 1001 | 1000 0000 | C9 80h |
| -127.5°C    | 1000 0001 | 1000 0000 | 81 80h |

- 12-bit two's complement word with the LSb equal to 0.0625°C; this applies to extended filtered temperature measurement extended resolution value registers

| Temperature | Binary    |           | Hex    |
|-------------|-----------|-----------|--------|
|             | MSB       | LSB       |        |
| +125.0625°C | 0111 1101 | 0001 0000 | 7D 10h |
| +25.0625°C  | 0001 1001 | 0001 0000 | 19 10h |
| +1.0625°C   | 0000 0001 | 0001 0000 | 01 10h |
| 0°C         | 0000 0000 | 0000 0000 | 00 00h |
| -0.0625°C   | 1111 1111 | 1111 0000 | FF F0h |
| -25.0625°C  | 1110 0111 | 1111 0000 | E7 F0h |
| -55.0625°C  | 1100 1001 | 1111 0000 | C9 F0h |
| -127.0625°C | 1000 0000 | 1111 0000 | 80 F0h |

Some fan control configuration registers use four bits and have an unsigned binary format, please see the [Section 6.2.18](#) configuration register descriptions for further details on this 4-bit format.

### 6.2.3.3 Thermal Diode Fault Status

The LM94 provides for indications of a fault (open or short circuit) with the remote thermal diodes. Before a remote diode conversion is updated, the status of the remote diode is checked for an open or short circuit condition. If such a fault condition occurs, a status bit is set in the status register. A short circuit is defined as the diode pins connected to each other. When an open or short circuit is detected, the corresponding temperature register is set to 80h.

### 6.2.4 Event Errors for Fan Boost

Temperature boost error and tachometer error events can cause the fan control PWM output(s) to go to full on. A boost temperature error event will cause both PWM outputs to go to full on, while a tachometer event can be either bound to PWM1 or PWM2.

A fan boost temperature event occurs if any of the four temperature zones exceeds the temperature Fan Boost Limit for that zone. Once a temperature has exceeded the boost limit, it must drop to a value equal to the boost limit minus the boost hysteresis before the boost condition is deactivated. The default setting for Zones 1 and 2 is 60°C and for Zones 3 and 4 it is 35°C.

The tachometer error boost function is enabled via the Tachometer Fan Boost Control register. Depending on the setting of the tachometer to PWM binding bits one or both of the PWM outputs will go to 100% duty cycle upon the detection of an unmasked Fan Tachometer Error Event. A Fan Tachometer Error event occurs when a tachometer reading exceeds the value set in it's FAN Tach Limit register. Once the error event ends the PWM output(s) will remain at 100% duty cycled for a time interval, Tach Boost Timeout, as programmed in the Tachometer Fan Boost Control register. If the tachometer error event returns during the middle of the timeout interval the Tach Boost Timeout interval will be reset and restart once the error event ends.

### 6.2.5 Voltage Monitoring

The LM94 contains inputs for monitoring voltages. Scaling is such that the correct value refers to approximately 3/4 scale or 192 decimal on all inputs, except the  $\pm 12V$ . Scaling is accomplished by using internal resistor dividers, except for the  $\pm 12V$ . The typical input resistance of these inputs is 200 k ohms. Input voltages are converted by an 8-bit Delta-Sigma ( $\Delta\Sigma$ ) A/D. The Delta-Sigma A/D architecture provides inherent filtering and spike smoothing of the analog input signal.

The  $\pm 12V$  inputs must be scaled externally. A full scale reading is achieved when 1.236V is applied to these inputs. For optimum performance the +12V should be scaled to provide a nominal  $\frac{3}{4}$  full scale reading, while the -12V should be scaled to provide a nominal  $\frac{1}{4}$  scale reading. The thevenin resistance at the pin should be kept between 1 k $\Omega$  and 7 k $\Omega$ .

The -12V monitoring is particularly challenging. It is required that an external offset voltage and external resistors be used to bring the -12V rail into the positive input voltage region of the A/D input. It is suggested that the supply rail for the LM94 device be used as the offset voltage. This voltage is usually derived from the P/S 5V stand-by voltage rail via a  $\pm 1\%$  accurate linear regulator. In this fashion we can always assume that the offset voltage is present when the -12V rail is present as the system cannot be turned on without the 3.3V stand-by voltage being present.

**Table 6-1. Voltage vs Register Reading**

| Pin    | Normal Use | Nominal Voltage | Register Reading at Nominal Voltage | Maximum Voltage | Register Reading at Maximum Voltage | Minimum Voltage | Register Reading at Minimum Voltage | Absolute Maximum Range        |
|--------|------------|-----------------|-------------------------------------|-----------------|-------------------------------------|-----------------|-------------------------------------|-------------------------------|
| AD_IN1 | +12V1      | 0.927V          | C0h                                 | 1.236V          | FFh                                 | 0V              | 00h                                 | -0.3V to ( $V_{DD} + 0.05V$ ) |
| AD_IN2 | +12V2      | 0.927V          | C0h                                 | 1.236V          | FFh                                 | 0V              | 00h                                 | -0.3V to ( $V_{DD} + 0.05V$ ) |
| AD_IN3 | +12V3      | 0.927V          | C0h                                 | 1.236V          | FFh                                 | 0V              | 00h                                 | -0.3V to ( $V_{DD} + 0.05V$ ) |
| AD_IN4 | FSB_Vtt    | 1.20V           | C0h                                 | 1.60V           | FFh                                 | 0V              | 00h                                 | -0.3V to +6.0V                |

**Table 6-1. Voltage vs Register Reading (continued)**

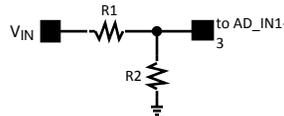
| Pin     | Normal Use | Nominal Voltage | Register Reading at Nominal Voltage | Maximum Voltage | Register Reading at Maximum Voltage | Minimum Voltage | Register Reading at Minimum Voltage | Absolute Maximum Range             |
|---------|------------|-----------------|-------------------------------------|-----------------|-------------------------------------|-----------------|-------------------------------------|------------------------------------|
| AD_IN5  | 3GIO       | 1.5V            | C0h                                 | 2V              | FFh                                 | 0V              | 00h                                 | -0.3V to +6.0V                     |
| AD_IN6  | ICH_Core   | 1.5V            | C0h                                 | 2V              | FFh                                 | 0V              | 00h                                 | -0.3V to +6.0V                     |
| AD_IN7  | Vccp1      | 1.20V           | C0h                                 | 1.60V           | FFh                                 | 0V              | 00h                                 | -0.3V to +6.0V                     |
| AD_IN8  | Vccp2      | 1.20V           | C0h                                 | 1.60V           | FFh                                 | 0V              | 00h                                 | -0.3V to +6.0V                     |
| AD_IN9  | +3.3V      | 3.30V           | C0h                                 | 4.40V           | FFh                                 | 0V              | 00h                                 | -0.3V to +6.0V                     |
| AD_IN10 | +5V        | 5.0V            | C0h                                 | 6.667V          | FAh                                 | 0V              | 00h                                 | -0.3V to +6.5V                     |
| AD_IN11 | SCSI_Core  | 2.5V            | C0h                                 | 3.333V          | FFh                                 | 0V              | 00h                                 | -0.3V to +6.0V                     |
| AD_IN12 | Mem_Core   | 1.969V          | C0h                                 | 2.625V          | FFh                                 | 0V              | 00h                                 | -0.3V to +6.0V                     |
| AD_IN13 | Mem_Vtt    | 0.984V          | C0h                                 | 1.312V          | FFh                                 | 0V              | 00h                                 | -0.3V to +6.0V                     |
| AD_IN14 | Gbit_Core  | 0.984V          | C0h                                 | 1.312V          | FFh                                 | 0V              | 00h                                 | -0.3V to +6.0V                     |
| AD_IN15 | -12V       | 0.309V          | 40h                                 | 1.236V          | FFh                                 | 0V              | 00h                                 | -0.3V to (V <sub>DD</sub> + 0.05V) |
| AD_IN16 | +3.3V S/B  | 3.3V            | C0h                                 | 3.6V            | D1h                                 | 3.0V            | A Eh                                | -0.3V to +6.0V                     |

The nominal voltages listed in this table are only typical values. Voltage rails with different nominal voltages can be monitored, but the register reading at the nominal value is no longer C0h. For example, a Mem\_Core rail at 2.5V nominal could be monitored with AD\_IN12, or a Mem\_Vtt rail at 1.2V could be monitored with AD\_IN13.

AD\_IN16 is also the power pin of the LM94, therefore special limitations apply to this AD input. The specified operational voltage range for the LM94 is 3.0V to 3.6V, therefore the voltage input to this pin is limited by this restriction. Care should also be taken not to apply more than 6V to this pin to prevent catastrophic damage.

### 6.2.6 Recommended External Scaling Resistors for +12V Power Rails

The +12V inputs require external scaling resistors. The resistors need to scale 12V down to 0.927V.



**Figure 6-1. Required External Scaling Resistors for +12V Power Input**

To calculate the required ratio of R1 to R2 use this equation:

$$\frac{R1}{R2} = \frac{12}{0.927} - 1 = 11.04498 \tag{1}$$

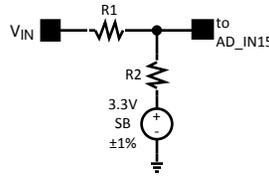
It is recommended that the equivalent thevenin resistance of the divider be between 1k and 7k to minimize errors caused by leakage currents at extreme temperatures. The best values for the resistors are: R1=13.7 kΩ and R2=1.15 kΩ. This yields a ratio of 11.94498, which has a +0.27% deviation from the theoretical. It is also recommended that the resistors have ±1% tolerance or better.

Each LSB in the voltage value registers has a weight of 12V / 192 = 62.5 mV. To calculate the actual voltage of the +12V power input, use the following equation:

$$V_{IN} = (8\text{-bit value register code}) \times (62.5 \text{ mV}) \tag{2}$$

### 6.2.7 Recommended External Scaling Circuit for -12V Power Input

The -12V input requires external resistors to level shift the nominal input voltage of -12V to +0.309V.



**Figure 6-2. Required External Level Shifting Resistors for –12V Power Input**

The +3.3V standby voltage is used as a reference for the level shifting. Therefore, the tolerance of this voltage directly effects the accuracy of the –12V reading. To minimize ratio errors, a tolerance of better than  $\pm 1\%$  should be used. It is recommended that the equivalent thevenin resistance of the divider is between 1k and 7k to minimize errors caused by leakage currents at extreme temperatures. To calculate the ratio of R1 to R2 use this equation:

$$\frac{R1}{R2} = \frac{(V_{IN} - V_{REF})}{(AD\_IN - V_{REF})} - 1 \quad (3)$$

where  $V_{IN}$  is the nominal input voltage of –12V,  $V_{REF}$  is the reference voltage of +3.3V and AD\_IN is the voltage required at the AD input for a  $\frac{1}{4}$  scale reading or 0.309V.

Therefore, for this case:

$$\frac{R1}{R2} = \frac{(-12 - 3.3)}{(0.309 - 3.3)} - 1 = 4.11535 \quad (4)$$

Using standard 1% resistor values for R1 of 5.76 k $\Omega$  and R2 of 1.4 k $\Omega$  yields an R1 to R2 ratio of 4.1143.

The input voltage  $V_{IN}$  can be calculated using the value register reading (VR) using this equation:

$$\begin{aligned} V_{IN} \frac{R1}{R2} &= ( + 1) \times \left[ \left( 1.236V \times \frac{VR}{256} \right) - 3.3V \right] + 3.3V \\ &= (24.69 \text{ mV} \times VR) - 13.5771V \end{aligned} \quad (5)$$

The table below summarizes the theoretical voltage values for value register readings near –12V.

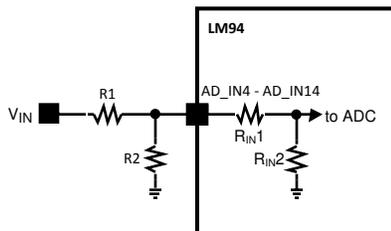
| Value Register | $V_{IN}$ | % $\Delta$ from –12V |
|----------------|----------|----------------------|
| 15             | -13.2068 | -10.0563             |
| 16             | -13.1821 | -9.8505              |
| 17             | -13.1574 | -9.6448              |
| 18             | -13.1327 | -9.4390              |
| 19             | -13.1080 | -9.2332              |
| 20             | -13.0833 | -9.0275              |
| 21             | -13.0586 | -8.8217              |
| 22             | -13.0339 | -8.6159              |
| 23             | -13.0092 | -8.4101              |
| 24             | -12.9845 | -8.2044              |
| 25             | -12.9598 | -7.9986              |
| 26             | -12.9351 | -7.7928              |
| 27             | -12.9104 | -7.5871              |
| 28             | -12.8858 | -7.3813              |
| 29             | -12.8611 | -7.1755              |
| 30             | -12.8364 | -6.9698              |

| Value Register | V <sub>IN</sub> | % Δ from -12V |
|----------------|-----------------|---------------|
| 31             | -12.8117        | -6.7640       |
| 32             | -12.7870        | -6.5582       |
| 33             | -12.7623        | -6.3524       |
| 34             | -12.7376        | -6.1467       |
| 35             | -12.7129        | -5.9409       |
| 36             | -12.6882        | -5.7351       |
| 37             | -12.6635        | -5.5294       |
| 38             | -12.6388        | -5.3236       |
| 39             | -12.6141        | -5.1178       |
| 40             | -12.5894        | -4.9121       |
| 41             | -12.5648        | -4.7063       |
| 42             | -12.5401        | -4.5005       |
| 43             | -12.5154        | -4.2947       |
| 44             | -12.4907        | -4.0890       |
| 45             | -12.4660        | -3.8832       |
| 46             | -12.4413        | -3.6774       |
| 47             | -12.4166        | -3.4717       |
| 48             | -12.3919        | -3.2659       |
| 49             | -12.3672        | -3.0601       |
| 50             | -12.3425        | -2.8544       |
| 51             | -12.3178        | -2.6486       |
| 52             | -12.2931        | -2.4428       |
| 53             | -12.2684        | -2.2370       |
| 54             | -12.2438        | -2.0313       |
| 55             | -12.2191        | -1.8255       |
| 56             | -12.1944        | -1.6197       |
| 57             | -12.1697        | -1.4140       |
| 58             | -12.1450        | -1.2082       |
| 59             | -12.1203        | -1.0024       |
| 60             | -12.0956        | -0.7967       |
| 61             | -12.0709        | -0.5909       |
| 62             | -12.0462        | -0.3851       |
| 63             | -12.0215        | -0.1793       |
| 64             | -11.9968        | 0.0264        |
| 65             | -11.9721        | 0.2322        |
| 66             | -11.9474        | 0.4380        |
| 67             | -11.9228        | 0.6437        |
| 68             | -11.8981        | 0.8495        |
| 69             | -11.8734        | 1.0553        |
| 70             | -11.8487        | 1.2610        |
| 71             | -11.8240        | 1.4668        |
| 72             | -11.7993        | 1.6726        |
| 73             | -11.7746        | 1.8784        |
| 74             | -11.7499        | 2.0841        |
| 75             | -11.7252        | 2.2899        |
| 76             | -11.7005        | 2.4957        |

| Value Register | V <sub>IN</sub> | % Δ from -12V |
|----------------|-----------------|---------------|
| 77             | -11.6758        | 2.7014        |
| 78             | -11.6511        | 2.9072        |
| 79             | -11.6264        | 3.1130        |
| 80             | -11.6018        | 3.3188        |
| 81             | -11.5771        | 3.5245        |
| 82             | -11.5524        | 3.7303        |
| 83             | -11.5277        | 3.9361        |
| 84             | -11.5030        | 4.1418        |
| 85             | -11.4783        | 4.3476        |
| 86             | -11.4536        | 4.5534        |
| 87             | -11.4289        | 4.7591        |
| 88             | -11.4042        | 4.9649        |
| 89             | -11.3795        | 5.1707        |
| 90             | -11.3548        | 5.3765        |
| 91             | -11.3301        | 5.5822        |
| 92             | -11.3054        | 5.7880        |
| 93             | -11.2807        | 5.9938        |
| 94             | -11.2561        | 6.1995        |
| 95             | -11.2314        | 6.4053        |
| 96             | -11.2067        | 6.6111        |
| 97             | -11.1820        | 6.8168        |
| 98             | -11.1573        | 7.0226        |
| 99             | -11.1326        | 7.2284        |
| 100            | -11.1079        | 7.4342        |
| 101            | -11.0832        | 7.6399        |
| 102            | -11.0585        | 7.8457        |
| 103            | -11.0338        | 8.0515        |
| 104            | -11.0091        | 8.2572        |
| 105            | -10.9844        | 8.4630        |
| 106            | -10.9597        | 8.6688        |
| 107            | -10.9351        | 8.8745        |
| 108            | -10.9104        | 9.0803        |
| 109            | -10.8857        | 9.2861        |
| 110            | -10.8610        | 9.4919        |
| 111            | -10.8363        | 9.6976        |
| 112            | -10.8116        | 9.9034        |
| 113            | -10.7869        | 10.1092       |

### 6.2.8 Adding External Scaling Resistors to Other Analog Inputs

All analog inputs, except AD\_IN1 through AD\_IN3 and AD\_IN15, include internal resistor dividers. Further scaling of AD\_IN4 through AD\_IN14 inputs with external scaling resistors is possible if the errors due to the internal dividers are accounted. The internal resistors,  $R_{IN1} + R_{IN2}$  shown in [Figure 6-3](#), will present to the external divider a minimum resistive load of 140 kΩ.



**Figure 6-3. Internal Resistors, RIN1 + RIN2**

### 6.2.9 Dynamic Vccp Monitoring Using VID

The AD\_IN7 (CPU1 Vccp) and AD\_IN8 (CPU2 Vccp) inputs are dynamically monitored using the P1\_VIDx and P2\_VIDx inputs to determine the limits. The dynamic comparisons operate independently of the static comparisons which use the statically programmed limits. The LM94 supports 3 different specifications for the Voltage Regulator (VRM or VRD) used on motherboards with Intel CPUs with four different VID Modes of operation. The Voltage Regulator Specifications supported are the VRD10/VRM10, VRD10.2 Extended and VRD11/VRM11, and in this document they will be referred to as the VRD10, VRD10.2 and VRD11 specifications, respectively.

According to the VRD 10 specification when a VID signal is ramping to a new value, it steps by one LSB at a time, and one step occurs every 5  $\mu$ s. In worse case, up to 20 steps may occur at once over 100  $\mu$ s. The Vccp voltage from the VRD has to settle to the new value within 50  $\mu$ s of the last VID change. The LM94 expects that the VID changes will not occur more frequently than every 5  $\mu$ s in the VRD10 mode. Similarly the LM94 can support the timing requirements of the VRD10.2 and VRD11 specifications.

The VID signals can be changed by the processor under program control, by internal thermal events or by external control, like force  $\overline{\text{PROCHOT}}$ .

The reference voltages selected by each value of the VID code can be found in the different VRM/VRD specifications. Transient VID values caused by line-to-line skew are ignored by the LM94. See the VRM/VRD specifications for the worst case line-to-line skew.

The LM94 averages the VID values over a sampling window to determine the average voltage that the VID input was indicating during the sampling window. At the completion of a voltage conversion cycle the LM94 performs limit comparisons based on average VID values and not instantaneous values. The upper limit is determined by adding the upper limit offset to the average voltage indicated by VID. The lower limit is determined by subtracting the lower limit offset from average voltage indicated by VID. If the AD\_IN7 (or AD\_IN8) voltage falls outside the upper and lower limits, an error event is generated. Dynamic and static comparisons are performed once every 100 ms. The averaging time interval is 1.5 ms.

If at any time during the Vccp sampling window, the VID code indicates that the VRD/VRM should turn off its output, the dynamic Vccp checking is disabled for that sample.

The comparison accuracy is  $\pm 25$  mV, therefore the comparison limits must be set to include this error. Since the Vccp voltage may be in the process of settling to a new value (due to a VID change), this settling should be taken into account when setting the upper and lower limit offsets.

The LM94 has a limitation on the upper limit voltage for dynamic Vccp checking. The upper limit cannot exceed 1.5875V. If the sum of the voltage indicated by VID and the upper offset voltage exceed 1.5875, the upper limit checking is disabled.

Pins 11 and 12 have dual purpose. When VRD10 mode is selected they can be used as general purpose inputs whose state is reflected the BMC and Host Error Status registers. In the other VRD modes they are used as a VID6 input.

### 6.2.10 Monitoring Analog Temperature Sensors

AD\_IN11 and AD\_IN15 readings can be routed to the fan control logic to facilitate the use of external temperature sensors such as the LM60. When these inputs are used for temperature sensing the digital output returned is in signed format, that is the MSb is inverted.

The following table lists critical parameters necessary for converting the binary data to temperature.

| Input   | V NOM              | Full Scale<br>(code 256) V | 254.5<br>code V | mV<br>/LSb | LM60<br>deg<br>/LSb | LM50<br>deg<br>/LSb |
|---------|--------------------|----------------------------|-----------------|------------|---------------------|---------------------|
| AD_IN11 | 2.500<br>(¼ scale) | 3.3333                     | 3.3138          | 13.0       | 2.0833              | 1.3021              |
| AD_IN15 | 0.309<br>(¼ scale) | 1.2360                     | 1.2288          | 4.8        | 0.7725              | 0.4828              |

The following table lists the equations to use for converting the AD\_IN11 or AD\_IN15 Digital Value (DV) to a temperature value.

| Input   | LM60 Equation                    | LM50 Equation                    |
|---------|----------------------------------|----------------------------------|
| AD_IN11 | $(DV + 95.44) \times 2.0833$ (6) | $(DV + 89.60) \times 1.3021$ (7) |
| AD_IN15 | $(DV + 40.18) \times 0.7725$ (8) | $(DV + 24.44) \times 0.4828$ (9) |

The following table lists the ideal values generated when using the LM60 at different temperatures.

| Temp | LM60<br>Ideal<br>Vout | AD_IN11 Reading   |               | AD_IN15 Reading   |               |
|------|-----------------------|-------------------|---------------|-------------------|---------------|
|      |                       | Signed<br>Decimal | Signed<br>Hex | Signed<br>Decimal | Signed<br>Hex |
| 0    | 0.424                 | -95.44            | A1            | -40.18            | D8            |
| 25   | 0.5803                | -83               | AD            | -8                | F8            |
| 30   | 0.6115                | -81               | AF            | -1                | FF            |
| 35   | 0.6428                | -79               | B1            | 5                 | 5             |
| 40   | 0.6740                | -76               | B4            | 12                | C             |
| 45   | 0.7053                | -74               | B6            | 18                | 12            |
| 50   | 0.7365                | -71               | B9            | 25                | 19            |
| 55   | 0.7678                | -69               | BB            | 31                | 1F            |
| 60   | 0.7990                | -67               | BD            | 37                | 25            |
| 65   | 0.8303                | -64               | C0            | 44                | 2C            |
| 70   | 0.8615                | -62               | C2            | 50                | 32            |
| 75   | 0.8928                | -59               | C5            | 57                | 39            |
| 80   | 0.9240                | -57               | C7            | 63                | 3F            |
| 85   | 0.9553                | -55               | C9            | 70                | 46            |
| 90   | 0.9865                | -52               | CC            | 76                | 4C            |
| 95   | 1.0178                | -50               | CE            | 83                | 53            |
| 100  | 1.0490                | -47               | D1            | 89                | 59            |
| 105  | 1.0803                | -45               | D3            | 96                | 60            |
| 110  | 1.1115                | -43               | D5            | 102               | 66            |

| Temp | LM60<br>Ideal<br>Vout | AD_IN11 Reading   |               | AD_IN15 Reading   |               |
|------|-----------------------|-------------------|---------------|-------------------|---------------|
|      |                       | Signed<br>Decimal | Signed<br>Hex | Signed<br>Decimal | Signed<br>Hex |
| 115  | 1.1428                | -40               | D8            | 109               | 6D            |
| 120  | 1.1740                | -38               | DA            | 115               | 73            |
| 125  | 1.2053                | -35               | DD            | 122               | 7A            |
| 130  | 1.2365                | -33               | DF            | 127               | 7F            |

The following table lists the expected ideal digital values when using the LM50.

| Temp | LM50<br>Ideal<br>Vout | AD_IN11 Reading   |               | AD_IN15 Reading   |               |
|------|-----------------------|-------------------|---------------|-------------------|---------------|
|      |                       | Signed<br>Decimal | Signed<br>Hex | Signed<br>Decimal | Signed<br>Hex |
| 0    | 0.5                   | -89.60            | A7            | -24.44            | E8            |
| 25   | 0.7500                | -70               | BA            | 27                | 1B            |
| 30   | 0.8000                | -67               | BD            | 38                | 26            |
| 35   | 0.8500                | -63               | C1            | 48                | 30            |
| 40   | 0.9000                | -59               | C5            | 58                | 3A            |
| 45   | 0.9500                | -55               | C9            | 69                | 45            |
| 50   | 1.0000                | -51               | CD            | 79                | 4F            |
| 55   | 1.0500                | -47               | D1            | 89                | 59            |
| 60   | 1.1000                | -44               | D4            | 100               | 64            |
| 65   | 1.1500                | -40               | D8            | 110               | 6E            |
| 70   | 1.2000                | -36               | DC            | 121               | 79            |
| 75   | 1.2500                | -32               | E0            | 127               | 7F            |
| 80   | 1.3000                | -28               | E4            | 127               | 7F            |
| 85   | 1.3500                | -24               | E8            | 127               | 7F            |
| 90   | 1.4000                | -20               | EC            | 127               | 7F            |
| 95   | 1.4500                | -17               | EF            | 127               | 7F            |
| 100  | 1.5000                | -13               | F3            | 127               | 7F            |
| 105  | 1.5500                | -9                | F7            | 127               | 7F            |
| 110  | 1.6000                | -5                | FB            | 127               | 7F            |
| 115  | 1.6500                | -1                | FF            | 127               | 7F            |
| 120  | 1.7000                | 3                 | 3             | 127               | 7F            |
| 125  | 1.7500                | 6                 | 6             | 127               | 7F            |
| 130  | 1.8000                | 10                | A             | 127               | 7F            |

### 6.2.11 $V_{REF}$ Output

$V_{REF}$  is a fixed voltage to be used by an external VRD or as a voltage reference input for the BMC A/D inputs.  $V_{REF}$  is 2.5V  $\pm$ 1%. There is internal current limit protection for the  $V_{REF}$  output in case it gets shorted to supply or ground accidentally.

### 6.2.12 $\overline{PROCHOT}$ Background Information

$\overline{PROCHOT}$  is an output from a processor that indicates that the processor has reached a predetermined temperature trip point. At this trip point the processor can be programmed to lower its internal operating frequency and/or lower its supply voltage by changing the value of the 6 bit VID that it supplies to the VRD. The final VID setting and the rate at which it transitions to the new VID is programmable within the processor.

If  $\overline{PROCHOT}$  is 100% throttled, it does not mean that the CPU is not executing, but it may mean that the CPU is about to encounter a thermal trip if the processor temperature continues to rise.

$\overline{\text{PROCHOT}}$  is also an input to some processors so that an external controller can force a thermal throttle based on external events.

$\overline{\text{PROCHOT}}$  is no longer asserted by the processor when the temperature drops below the predefined thermal trip point.

Oscillation around the trip point is avoided by the processor by requiring that the temperature be above/below the trip point for a predetermined period of time. A counter inside the processor is used to track this time and it has to be incremented to a max count for an above temperature trip and decremented to zero when below the trip temperature setting, to remove the trip.

The minimum time for  $\overline{\text{PROCHOT}}$  assertion is time dependant on the FSB frequency. The minimum time that the processor asserts  $\overline{\text{PROCHOT}}$  is estimated to be 187  $\mu\text{s}$ .

### 6.2.13 $\overline{\text{PROCHOT}}$ Monitoring

$\overline{\text{PROCHOT}}$  monitoring applies to both the  $\overline{\text{P1\_PROCHOT}}$  and  $\overline{\text{P2\_PROCHOT}}$  inputs. Both inputs are monitored in the same fashion, but the following description discusses a single monitor. ( $\overline{\text{Px\_PROCHOT}}$  represents both  $\overline{\text{P1\_PROCHOT}}$  and  $\overline{\text{P2\_PROCHOT}}$ ).

$\overline{\text{PROCHOT}}$  monitoring is meant to achieve two goals. One goal is to measure the percentage of time that  $\overline{\text{PROCHOT}}$  is asserted over a programmable time period. The result of this measurement can be read from an 8-bit register where one LSB equals 1/256th of the  $\overline{\text{PROCHOT}}$  Time Interval (0.39%). The second goal is to have a status register that indicates, as a coarse percentage, the amount of time a processor has been throttled. This second goal is required in order to communicate information over the NIC using ASF, i.e. status can be sent, not values.

To achieve the first goal, the  $\overline{\text{PROCHOT}}$  input is monitored over a period of time as defined by the  $\overline{\text{PROCHOT}}$  Time Interval Register. At the end of each time period, the 8-bit measurement is transferred to the Current  $\overline{\text{Px\_PROCHOT}}$  register. Also at the end of each measurement period, the Current  $\overline{\text{Px\_PROCHOT}}$  register value is moved to the Average  $\overline{\text{Px\_PROCHOT}}$  register by adding the new value to the old value and dividing the result by 2. Note that the value that is averaged into the Average  $\overline{\text{Px\_PROCHOT}}$  register is not the new measurement but rather the previous measurement. If the SMBus writes to the Current  $\overline{\text{P1\_PROCHOT}}$  (or Current  $\overline{\text{P2\_PROCHOT}}$ ) register, the capture cycle restarts for both monitoring channels ( $\overline{\text{P1\_PROCHOT}}$  and  $\overline{\text{P2\_PROCHOT}}$ ). Also note, that a strict average of two 8-bit values may result in Average  $\overline{\text{Px\_PROCHOT}}$  reflecting a value that is one LSB lower than the Current  $\overline{\text{Px\_PROCHOT}}$  in steady state.

It should be noted that the 8-bit result has a positive bias of one half of an LSB. This is necessary because a value of 00h represents that  $\overline{\text{Px\_PROCHOT}}$  was not asserted at all during the sampling window. Any amount of throttling results in a reading of 01h.

The following table demonstrates the mapping for the 8-bit result:

| 8-Bit Result | Percentage Thottled         |
|--------------|-----------------------------|
| 0            | Exactly 0%                  |
| 1            | Between 0% and 0.39%        |
| 2            | Between 0.39% and 0.78%     |
| -            | -                           |
| n            | Between (n-1)/256 and n/256 |
| -            | -                           |
| 253          | Between 98.4% and 98.8%     |
| 254          | Between 98.8% and 99.2%     |
| 255          | Greater than 99.2%          |

To achieve the second goal, the LM94 has several comparators that compare the measured percentage reading against several fixed and 1 variable value. The variable value is user programmable.

The result of these comparisons generates several error status bits described in the following table:

| Status Description                               | Comparison Formula  |
|--|---|
| 100% Throttle                                    | PROCHOT was never de-asserted during monitoring interval. |
| Greater than or equal to 75% and less than 100%  | $193 \leq \text{measured value}$ and not 100%             |
| Greater than or equal to 50% and less than 75%   | $129 \leq \text{measured value} < 193$                    |
| Greater than or equal to 25% and less than 50%   | $65 \leq \text{measured value} < 129$                     |
| Greater than or equal to 12.5% and less than 25% | $33 \leq \text{measured value} < 65$                      |
| Greater than 0% and less than 12.5%              | $0 < \text{measured value} < 33$                          |
| Greater than 0%                                  | $0 < \text{measured value}$                               |
| Greater than user limit                          | $\text{user limit} < \text{measured value}$               |

These status bits are reflected in the  $\overline{\text{PROCHOT}}$  Error Status Registers. Each of the  $\overline{\text{P1\_PROCHOT}}$  and  $\overline{\text{P2\_PROCHOT}}$  inputs is monitored independently, and each has its own set of status registers.

In S3 and S4/5 sleep states, the  $\overline{\text{PROCHOT}}$  Monitoring function does not run.  $\overline{\text{VRDx\_HOT}}$  is disabled from activating  $\overline{\text{PROCHOT}}$  pins in S3 and S4/5. The Current  $\overline{\text{Px\_PROCHOT}}$  registers are reset to 00h and the Average  $\overline{\text{Px\_PROCHOT}}$  registers hold their current state. Once the sleep state changes back to S0, the monitoring function is restarted. After the first  $\overline{\text{PROCHOT}}$  measurement has been made, the measurement is written directly into the Current and Average  $\overline{\text{Px\_PROCHOT}}$  registers without performing any averaging. Averaging returns to normal on the second measurement.

#### 6.2.14 $\overline{\text{PROCHOT}}$ Output Control

In some cases, it is necessary for the LM94 to drive the  $\overline{\text{Px\_PROCHOT}}$  outputs low. There are several conditions that cause this to happen.

The LM94 can be told to logically short the two  $\overline{\text{PROCHOT}}$  inputs together. When this is done, the LM94 monitors each of the  $\overline{\text{Px\_PROCHOT}}$  inputs. If any external device asserts one of the  $\overline{\text{PROCHOT}}$  signals, the LM94 responds by asserting the other  $\overline{\text{PROCHOT}}$  signal until the first  $\overline{\text{PROCHOT}}$  signal is de-asserted. This feature should never be enabled if the  $\overline{\text{PROCHOT}}$  signals are already being shorted by another means.

Whenever one of the  $\overline{\text{VRDx\_HOT}}$  inputs is asserted, the corresponding  $\overline{\text{Px\_PROCHOT}}$  pins are asserted by the LM94. The response time is less than 10  $\mu\text{s}$ . When the  $\overline{\text{VRDx\_HOT}}$  input is de-asserted, the  $\overline{\text{Px\_PROCHOT}}$  pin is no longer asserted by the LM94. If the LM94 is configured to short the  $\overline{\text{PROCHOT}}$  signals together, it always asserts them together whenever either of the  $\overline{\text{VRDx\_HOT}}$  inputs is asserted. This response is disabled in sleep states 3 and 4/5 and can be disabled through the  $\overline{\text{PROCHOT}}$  Control register.

Software can manually program the LM94 to drive a PWM type signal onto  $\overline{\text{P1\_PROCHOT}}$  or  $\overline{\text{P2\_PROCHOT}}$ . This is done via the  $\overline{\text{PROCHOT}}$  Override register. See the [description of this register](#) for more details. Once again, if the LM94 is configured to short the  $\overline{\text{PROCHOT}}$  signals together, it always asserts them together whenever this function is enabled.

#### 6.2.15 Fan Speed Measurement

The fan tach circuitry measures the period of the fan pulses by enabling a counter for two periods of the fan tach signal. The accumulated count is proportional to the fan tach period and inversely proportional to the fan speed. All four fan tach signals are measured within 1 second.

Fans in general do not over-speed if run from the correct voltage, so the failure condition of interest is under speed due to electrical or mechanical failure. For this reason only low-speed limits are programmed into the limit registers for the fans. It should be noted that, since fan period rather than speed is being measured, a fan tach error event occurs when the measurement *exceeds* the limit value.

### 6.2.16 Smart Fan Speed Measurement

If a fan's speed is varied using PWM drive of either of the fans power pins, the tachometer output of the fan is corrupted. The LM94 includes smart tachometer circuitry that allows an accurate tachometer reading to be achieved despite the signal corruption. In smart tach mode all four signals are measured within 4 seconds.

A smart tach capture cycle works according to the following steps:

1. Both PWM outputs are synchronized such that they activate simultaneously.
2. Both PWM output active times are extended for up to 50 ms.
3. The number of tach signal periods during the 50 ms interval are tracked:
  - a) If less than 1 period is sensed during the 50 ms extension the result returned is 3FFh.
  - b) After one period occurs the count for that period is memorized.
  - c) If during the 50 ms interval 2 periods do not occur, the tach value reported is the 1 period count multiplied by 2.
  - d) If 2 periods do occur, the 2 period count is loaded into the value register and the 50 ms PWM extension is terminated.

The lowest two bits in each of the Fan Tach value registers are reserved. The smart tach feature takes advantage of these bits. In normal tach mode, these bits return 00. In smart tach mode the two bits determine the accuracy level of the reading. 11 is most accurate (2 periods used) and 10 is the least accurate (1 period used). If less than 1 period occurred during the measurement cycle, the lower two bits are set to 10.

In smart fan tach mode, the TACH\_EDGE field is honored in the LM94 Status/Control register. If only one edge type is active, the measurement always uses that edge type (rising or falling). If both are active, the measurement uses whichever edge type occurs first.

Typically the minimum RPM captured by smart fan tach mode is 900 RPM for a fan that produces two pulses per revolution at about 50% duty cycle.

### 6.2.17 Inputs/Outputs

Besides all the pins associated with sensor inputs the LM94 has several pins that are assigned for other specific functions.

#### 6.2.17.1 ALERT Output

The  $\overline{\text{ALERT}}$  output is an active-low open drain output signal. The  $\overline{\text{ALERT}}$  output is used to signal a micro-controller that one or more sensors have crossed their corresponding limit thresholds. This is generally not a fatal event unless the micro-controller decides it to be.

If enabled, the  $\overline{\text{ALERT}}$  output is asserted whenever any bit in any BMC Error Status register is set (with the exception of the fixed  $\overline{\text{PROCHOT}}$  threshold bits). By definition, when  $\overline{\text{ALERT}}$  is enabled, it always matches the inverse of the BMC\_ERR bit in the LM94 Status/Control register. When the  $\overline{\text{ALERT}}$  output is disabled, an alert event can still be determined by reading the state of the BMC\_ERR bit.

The  $\overline{\text{ALERT}}$  functions like an interrupt. The LM94 does not support the SMBus ARA (Alert Response Address) protocol.

$\overline{\text{ALERT}}$  is only de-asserted when there are no error status bits set in any BMC Error Status registers. Alternatively, software can disable the  $\overline{\text{ALERT}}$  output to cause it to de-assert. The  $\overline{\text{ALERT}}$  output re-asserts once enabled if any BMC Error Status register bits are still set.

The  $\overline{\text{ALERT}}$  output also functions in comparator mode for thermal events, that is the  $\overline{\text{ALERT}}$  output will be asserted for unmasked thermal error events and will de-assert immediately when the error event ceases. The operation of the  $\overline{\text{ALERT}}$  output is controlled by the LM94 Configuration register.

Further information on how the  $\overline{\text{ALERT}}$  output behaves can be found in [Section 7.1.7](#).

### 6.2.17.2 $\overline{\text{RESET}}$ Input/Output

This pin acts as an active low reset output when power is applied to the LM94. It is asserted when the LM94 first sees a voltage that exceeds the internal POR level on its +3.3V S/B  $V_{DD}$  input. The internal registers of the LM94 are reset to their defaults when power is applied.

After this reset has completed, the  $\overline{\text{RESET}}$  pin becomes an input. When an external device asserts  $\overline{\text{RESET}}$ , the LM94 clears the LOCK bit in the LM94 Configuration register. This feature allows critical registers to be locked and provides a controlled mechanism to unlock them.

If the LM94  $\overline{\text{RESET}}$  is not used it must be tied high through an external resistive pull-up to prevent LM94 malfunction.

Within 10  $\mu\text{sec}$  of asserting  $\overline{\text{RESET}}$  externally, the Sleep State Control register shall be automatically set to S4/5. This causes several error events to be masked according to the S4/5 masking definitions. Refer to the [register descriptions](#) for more information.  $\overline{\text{RESET}}$  may not be detected if it is asserted for less than 4  $\mu\text{sec}$ .

### 6.2.17.3 PWM1 and PWM2 Outputs

The PWM outputs are used to control the speed of fans. The duty cycle of each output is automatically controlled by the temperature of one or more temperature zones. They are also influenced by various other inputs and registers. See [Section 6.2.18](#) for further information on the behavior of the PWM outputs.

### 6.2.17.4 $\overline{\text{VRD1\_HOT}}$ and $\overline{\text{VRD2\_HOT}}$ Inputs

These inputs monitor the thermal sensor associated with each processor VRD on a baseboard. When one of the inputs is activated, it indicates that the VRD has exceeded a predetermined temperature threshold. The LM94 responds by gradually increasing the duty cycle of any PWM outputs that are bound to the corresponding processor and setting the appropriate error status bits. The corresponding  $\overline{\text{PROCHOT}}$  signal is also asserted. See the [Section 6.2.18](#) and the [Section 6.2.14](#) for more information.

### 6.2.17.5 GPIO and GPI PINS

The LM94 has 8 GPIO pins that can act as either as general purpose inputs or outputs and 2 GPI pins that can act as general purpose inputs. Each can be configured and controlled independently. When acting as an input the pin can be masked to prevent it from setting a corresponding bit in the GPI Error status registers. Some of these pins can also function as tachometer or VID inputs.

### 6.2.17.6 Fan Tach Inputs

The fan inputs are Schmitt-Trigger digital inputs. Schmitt-Trigger input circuitry is included to accommodate slow rise and fall times typical of fan tachometer outputs.

The maximum input signal range is 0V to +6.0V, even when  $V_{DD}$  is less than 5V. In the event that these inputs are supplied from fan outputs, which exceed 0V to +6.0V, either resistive attenuation of the fan signal or diode clamping must be included to keep inputs within an acceptable range, thereby preventing damage to the LM94.

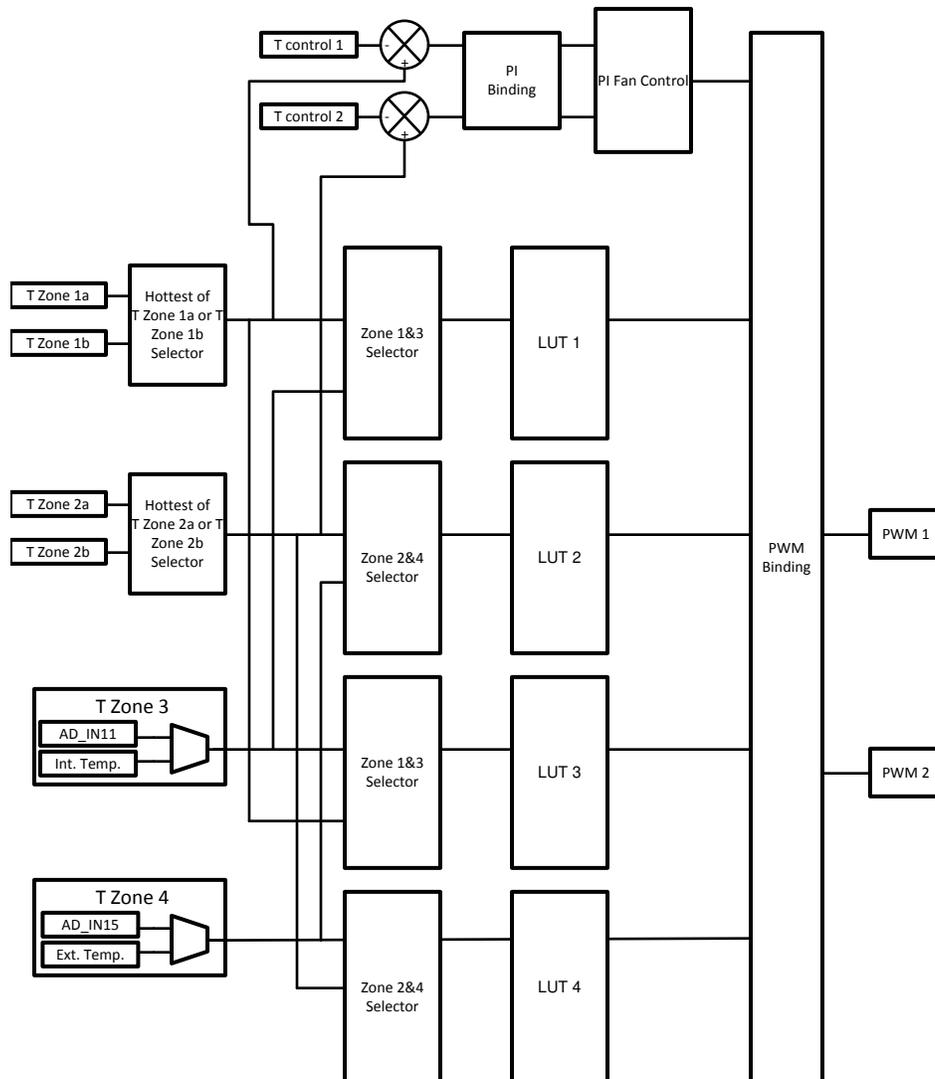
Hot plugging fans can involve spikes on the Tach signals of up to 12V so diode protection or other circuitry is required. For “Hot Plug” fans, external clamp diodes may be required for signal conditioning.

## 6.2.18 Fan Control

### 6.2.18.1 Automatic Fan Control Methods

The LM94 fan speed control method is optimized for fan noise reduction, fan power efficiency, fan reliability and minimum cost. The PWMx outputs can be filtered using an external switching regulator type output stage that provides 5V to 12V DC for fan power. A high PWM frequency is required to minimize the size and cost of the inductor and other components used in the output stage. The PWM outputs of the LM94 can operate up to 22.5 kHz with a variable step size depending on the fan control mode of operation. The LM94 supports LUT (Lookup Table) and PI (Proportional Integral) fan control methods. These methods can function interactively or independently as controlled by the PWM binding registers. [Figure 6-4](#) shows the high level block diagram for these fan control methods. The mapping/binding of the temperature zones to the LUTs is completely independent of the PI loops. The temperature zones can be first independently bound to the LUTs and/or PI

loops then each LUT or PI loop can be bound to either PWM Output. The LUT parameters are independent of the temperature zone binding. The PI loop controller is a proportional-integral feedback controller. It generates a 9-bit PWM duty cycle and uses temperature feedback from the processor thermal zones (Zones 1 and 2). The PWM output controls the airflow over the processors and thus the temperature of the processors is adjusted by the PI loop to maintain the hottest temperature reading between the values  $T_{control}$  and  $T_{control} - \text{hysteresis}$ . The LM94 supports 2 processors and each processor can have two thermal sub-zones. The hottest of each processor temperature is reported to the Zone selectors and PI loop inputs. Each processor has an independent  $T_{control}$  setting.



**Figure 6-4. LUT and PI controller high level block diagram**

### 6.2.18.2 LUT Fan Control Duty Cycles

Several registers in the LM94 use 4-bit values to represent a duty cycle. All of them use a common mapping that associates the 4-bit value with a duty cycle. The 4-bit values correspond also with the 14 steps of the auto fan control algorithm. The mapping is shown below. This applies for PWM outputs running at the default 22.5 kHz (high) frequency.

| 4-Bit Value | Step | 22.5 kHz (High Frequency) Duty Cycle |
|-------------|------|--------------------------------------|
| 0h          |      | 0.00%                                |
| 1h          | 1    | 25.00%                               |
| 2h          | 2    | 31.25%                               |
| 3h          | 3    | 37.50%                               |
| 4h          | 4    | 43.75%                               |
| 5h          | 5    | 50.00%                               |
| 6h          | 6    | 56.25%                               |
| 7h          | 7    | 62.50%                               |
| 8h          | 8    | 68.75%                               |
| 9h          | 9    | 75.00%                               |
| Ah          | 10   | 81.25%                               |
| Bh          | 11   | 87.50%                               |
| Ch          | 12   | 93.75%                               |
| Dh          | 13   | 100.00%                              |
| Eh          | —    | Reserved                             |
| Fh          | —    | Reserved                             |

### 6.2.18.3 Alternate LUT PWM Mapping

The PWM output can operate at lower frequencies, instead of the default 22.5 kHz. The lower frequencies can be enabled through the PWMx Control 4 registers. Operating in the lower frequency mode, enables an alternate mapping of step numbers to duty cycle. This effects the auto fan control and all LM94 registers that describe a duty cycle using a 4-bit value. This alternate mapping can also be enable when using the default 22.5 kHz PWM frequency.

The alternate LUT PWM duty cycle mapping is listed in the following table:

| 4-Bit Value | LUT Step | Alternate LUT Duty Cycle |
|-------------|----------|--------------------------|
| 0h          |          | 0%                       |
| 1h          | 1        | 25.00%                   |
| 2h          | 2        | 28.57%                   |
| 3h          | 3        | 32.14%                   |
| 4h          | 4        | 35.71%                   |
| 5h          | 5        | 39.29%                   |
| 6h          | 6        | 42.86%                   |
| 7h          | 7        | 46.43%                   |
| 8h          | 8        | 50.00%                   |
| 9h          | 9        | 53.57%                   |
| Ah          | 10       | 57.14%                   |
| Bh          | 11       | 71.43%                   |
| Ch          | 12       | 85.71%                   |
| Dh          | 13       | 100.00%                  |

| 4-Bit Value | LUT Step | Alternate LUT Duty Cycle |
|-------------|----------|--------------------------|
| Eh          | —        | Reserved                 |
| Fh          | —        | Reserved                 |

#### 6.2.18.4 Fan Control Priorities

The automatic fan control is not the only function that influences PWM duty cycle. There are several other functions that influence the PWM duty cycle. All the functions can be classified into several categories:

| Category # | Category Name                                   |
|------------|---|
| 1          | PWM to 100% conditions                          |
| 2          | $\overline{\text{VRDx\_HOT}}$ ramp-up/ramp-down |
| 3          | PROCHOT ramp-up/ramp-down function              |
| 4          | Manual PWM Override                             |
| 5          | Fan Spin-Up Control                             |
| 6          | Automatic Fan Control Algorithm                 |

The ultimate PWM duty cycle that is chosen can be described by the following formula:

If (Manual PWM Override is active)

$$\text{PWM} = \max(1,2,3,4)$$

Else

$$\text{PWM} = \max(1,2,3,5,6)$$

So in general, categories 1, 2 and 3 are always active. In addition to that, either category 4 or categories 5 and 6 are active depending on whether manual override is enabled. In this sense the manual override, when enabled, replaces category 5 and 6.

#### 6.2.18.5 PWM to 100% Conditions

There are several conditions that cause the duty cycles of all PWM outputs to immediately get set to 100%. They are:

1. any of the four temperature zones exceed the programmed Fan Boost Limit setting but has not yet cooled down enough to drop below the hysteresis point
2. a tachometer reading exceeds its limit
3. the OVRID bit is set in the LM94 Status/Control

#### 6.2.18.6 $\overline{\text{VRDx\_HOT}}$ Ramp-Up/Ramp-Down

This function causes the duty cycle of the PWM outputs to gradually increase over time if  $\overline{\text{VRD1\_HOT}}$  or  $\overline{\text{VRD2\_HOT}}$  are asserted.

When  $\overline{\text{VRDx\_HOT}}$  is asserted, the ramp function is enabled. The enabling process involves two steps:

1. The current duty cycle being requested by other PWM functions is memorized.
2. The ramp function immediately adds one PWM duty cycle step to the memorized value and requests this duty cycle.

Once the function is enabled, it gradually adds additional duty cycle steps every X milliseconds whenever  $\overline{\text{VRDx\_HOT}}$  is asserted (X is programmable via the PWM Ramp Control register). If  $\overline{\text{VRDx\_HOT}}$  remains asserted for a long enough time, the duty cycle eventually reaches 100%.

Whenever  $\overline{\text{VRDx\_HOT}}$  is de-asserted, the ramp function begins to ramp down by subtracting one PWM duty cycle step every X milliseconds. If  $\overline{\text{VRDx\_HOT}}$  is currently de-asserted, and the ramp function is less than to the PWM duty cycle being requested by other functions, the ramp function is disabled.

As long as the function is enabled, it continues to ramp up or ramp down depending on the state of  $\overline{\text{VRDx\_HOT}}$ . The ramp enabling process described above can only re-occur after the ramp function has been disabled. Rapid assertion/de-assertion of  $\overline{\text{VRDx\_HOT}}$  does not trigger the enabling process unless  $\overline{\text{VRDx\_HOT}}$  was de-asserted long enough for the ramp function to disable itself.

This ramp function operates independently for  $\overline{\text{VRD1\_HOT}}$  and  $\overline{\text{VRD2\_HOT}}$ . In addition, the ramp function only applies to the PWM(s) that are bound to one or two  $\overline{\text{VRDx\_HOT}}$  inputs. Depending on the bindings, it is possible that up to four independent ramp functions are active at any given moment:

- PWM1/VRD1
- PWM1/VRD2
- PWM2/VRD1
- PWM2/VRD2

If a PWM is bound to both  $\overline{\text{VRD1\_HOT}}$  and  $\overline{\text{VRD2\_HOT}}$ , then two ramp functions are active for that PWM output. In this case the duty cycle that is used is the maximum of the two ramp functions.

#### 6.2.18.7 *PROCHOT Ramp-Up/Ramp-Down*

This function is very similar to the  $\overline{\text{VRDx\_HOT}}$  ramp-up/ramp-down function. The PWM duty cycle ramps up in the same fashion whenever the  $\overline{\text{PROCHOT}}$  measurement exceeds the user programmed threshold. Once a new  $\overline{\text{PROCHOT}}$  measurement is made that no longer exceeds the user limit, the PWM will begin to ramp down.

Just as with the  $\overline{\text{VRDx\_HOT}}$  ramp function, the  $\overline{\text{PROCHOT}}$  ramp function uses independent bindings to determine which PWM outputs should be effected by each  $\overline{\text{PROCHOT}}$  input (  $\overline{\text{P1\_PROCHOT}}$  or  $\overline{\text{P2\_PROCHOT}}$ ).

If a PWM is bound to both  $\overline{\text{P1\_PROCHOT}}$  and  $\overline{\text{P2\_PROCHOT}}$ , two  $\overline{\text{PROCHOT}}$  ramp functions could be active at the same time. In this case the duty cycle that is used is the maximum of the two ramp functions.

#### 6.2.18.8 *Manual PWM Override*

When a PWM channel is configured for manual PWM override, software can manually control the PWM duty cycle. There are some PWM control functions that could still cause the duty cycle to be higher than the manual setting. See the [Section 6.2.18.4](#) for details.

#### 6.2.18.9 *Fan Spin-Up Control*

All of the other PWM control functions are combined to produce a final duty cycle that is actually used for the PWM output. If this final value changes from zero to a non-zero value, the Fan Spin-Up Control function is triggered. Once triggered, the Fan Spin-Up Control requests the programmed duty cycle for a programmed period of time.

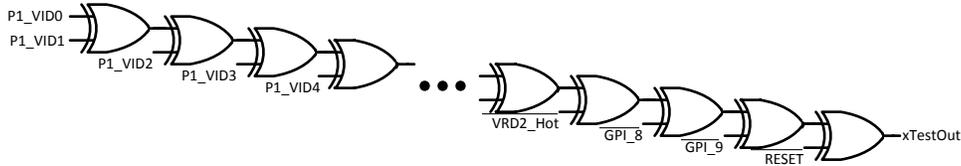
#### 6.2.19 XOR TREE TEST

An XOR tree is provided in the LM94 for Automated Test Equipment (ATE) board level connectivity testing. This allows the functionality of all digital inputs to be tested in a simple manner and any pins that are non-functional or shorted together to be identified. When the test mode is enabled by setting the 'XEN' bit in the XOR Test register, the part enters XOR test mode.

**Table 6-2. The following signals are included in the XOR test tree:**

|         |        |      |            |          |      |       |
|---------|--------|------|------------|----------|------|-------|
| Px_VIDy | GPIO_x | PWMx | Px_PROCHOT | VRDx_HOT | GPIx | RESET |
|---------|--------|------|------------|----------|------|-------|

Since the test mode is XOR tree, the order of the signals in the tree is not important. SMBDAT and SMBCLK should not be included in the test tree.



**Figure 6-5. Example of XOR Test Tree (not showing all signals)**

To properly implement the XOR TREE test on the PCB, no pins listed in the tree should be connected directly to power or ground. If a pin needs to be configured as a permanent low, such as a GPI, it should be connected to ground through a low value resistor such as 10 k $\Omega$ , to allow the ATE (Automatic Test Equipment) to drive it high.

When generating test waveforms, a typical propagation delay of 500 ns through the XOR tree should be allowed for.

## 6.3 Programming

### 6.3.1 SMBus Interface

The SMBus is used to communicate with the LM94. LM94 SMBus interface lines are designed to be tolerant to 5V signalling. Necessary pull-ups are located on the baseboard. Care should be taken to ensure that only one pull-up is used for each SMBus signal. The SMBus interface obeys the SMBus 2.0 protocols and signaling levels.

The SMBus interface of the LM94 does not load down the SMBus if no power is applied to the LM94. This allows a module containing the LM94 to be powered down and replaced, if necessary.

#### 6.3.1.1 SMBus ADDRESSING

Each time the LM94 is powered up, it latches the assigned SMBus slave address (determined by ADDR\_SEL) during the first valid SMBus transaction in which the first five bits of the targeted slave address match those of the LM94 slave address. Once the address has been latched, the LM94 continues to use that address for all future transactions until power is lost.

The address select input detects three different voltage levels and allows for up to 3 devices to exist in a system. The address assignment is as follows:

| Address Select Pin (ADDR_SEL) | Slave Address Assignment |
|-------------------------------|--------------------------|
| High                          | 01011 01                 |
| $V_{DD}/2$                    | 01011 10                 |
| Low                           | 01011 00                 |

#### 6.3.1.2 DIGITAL NOISE EFFECT ON SMBus COMMUNICATION

Noise coupling into the digital lines (greater than 150mV), overshoot greater than  $V_{DD}$  and undershoot less than GND, may prevent successful SMBus communication with the LM94. SMBus No Acknowledge (NACK) is the most common symptom, causing unnecessary traffic on the bus. Although, the SMBus maximum frequency of communication is rather low (100 kHz max), care still needs to be taken to ensure proper termination within a system with multiple parts on the bus and long printed circuit board traces. The LM94 includes on chip low-pass filtering of the SMBCLK and SMBDAT signals to make it more noise immune. Minimize noise coupling by keeping digital traces out of switching baseboard areas as well as ensuring that digital lines containing high speed data communications cross at right angles to the SMBDAT and SMBCLK lines.

#### 6.3.1.3 GENERAL SMBus TIMING

The SMBus 2.0 specification defines specific conditions for different types of read and write operations but in general the SMBus protocol operates as follows:

The master initiates data transfer by establishing a START condition, defined as a high to low transition on the serial data line SMBDAT while the serial clock line SMBCLK remains high. This indicates that a data stream follows. All slave peripherals connected to the serial bus respond to the START condition, and shift in the next 8 bits. This consists of a 7-bit slave address (MSB first) plus a R/W bit, which determines the direction of the data transfer, i.e. whether data is written to or read from the slave device (0 = write, 1 = read).

The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the low period before the ninth clock pulse, known as the Acknowledge Bit, and holding it low during the high period of this clock pulse. All other devices on the bus now remain idle while the selected device waits for data to be read from or written to it. If the R/W bit is a 0 then the master writes to the slave device. If the R/W bit is a 1 the master reads from the slave device.

Data is sent over the serial bus in sequences of 9 clock pulses, 8 bits of data followed by an Acknowledge bit. Data transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, as a low to high transition when the clock is high may be interpreted as a STOP signal.

If the operation is a write operation, the first data byte after the slave address is a command byte. This tells the slave device what to expect next. It may be an instruction, such as telling the slave device to expect a block write, or it may simply be a register address that tells the slave where subsequent data is to be written.

Since data can flow in only one direction as defined by the R/W bit, it is not possible to send a command to a slave device during a read operation. Before doing a read operation, it is necessary to do a write operation to tell the slave what sort of read operation to expect and/or the address from which data is to be read.

When all data bytes have been read or written, stop conditions are established. In WRITE mode, the master will allow the data line to go high during the 10th clock pulse to assert a STOP condition. In READ mode, the slave drives the data not the master. For the bit in question, the slave is looking for an acknowledge and the master doesn't drive low. This is known as 'No Acknowledge'. The master then takes the data line low during the low period before the 10th clock pulse, then high during the 10th clock pulse to assert a STOP condition.

Note, a repeated START may be given only between a write and read operation that are in succession.

#### **6.3.1.4 SMBus ERROR SAFETY FEATURES**

To provide a more robust SMBus interface, the LM94 incorporates a timeout feature for both SMBCLK and SMBDAT. If either signal is low for a long period of time (see [SMBus AC specs](#)), the LM94 SMBus state machine reverts to the idle state and waits for a START signal. Large block transfers of all zeros should be avoided if the SMBCLK is operating at a very low frequency to avoid accidental timeouts. Pulling the Reset pin low does not reset the SMBus state machine. If the LM94 SMBDAT pin is low during a system reset, the LM94's state machine timeouts and resets automatically. If the LM94's SMBDAT pin is high during a system reset, the first assertion of a start by the master resets the LM94's interface state machine.

Although it is a violation of the SMBus specification, in some cases a START or STOP signal occurs in the middle of a byte transfer instead of coming after an acknowledge bit. If this occurs, only a partial byte was transferred. If a byte was being written, it is aborted and the partial byte is not committed. If a byte was being read from a read-to-clear register, the register is not cleared.

#### **6.3.1.5 Serial Interface Protocols**

The LM94 contains volatile registers, the registers occupy address locations from 00h to EFh.

Data can be read and written as a single byte, a word, or as a block of several bytes. The LM94 supports the following SMBus/I<sup>2</sup>C transactions/protocols:

- Send Byte
- Write Byte
- Write Word
- SMBus Write Block
- I<sup>2</sup>C Block Write

- Read Byte
- Read Word
- SMBus Read Block
- SMBus Block-Write Block-Read Process Call
- I<sup>2</sup>C Block Read

In addition to these transactions the LM94 supports a few extra items and also has some behavior that must be defined beyond the SMBus 2.0 specification. No other SMBus 2.0 transactions are supported (PEC, ARA etc.).

The SMBus specification defines several protocols for different types of read and write operations. The ones used in the LM94 are discussed below. The following abbreviations are used in the diagrams:

- S** — START
- P** — STOP
- R** — READ
- W** — WRITE
- A** — ACKNOWLEDGE
- /A** — NO ACKNOWLEDGE

#### 6.3.1.5.1 Address Incrementing

The established base address does not increment. Repeatedly reading without re-establishing a new base address returns data from the same address each time. I<sup>2</sup>C read transactions can use this information and skip reestablishing the base address, when only one master is used. One exception to this rule exists when a block write and block read is used to emulate a block write/read process call. This is detailed later, see the [Section 6.3.1.5.4.3](#) description.

#### 6.3.1.5.2 Block Command Code Summary

Block command codes control the block read and write operations of the LM94 as summarized in the following table:

| Command Code Name   | Value | Description   |
|---------------------|-------|---|
| Block Write Command | F0h   | SMBus Block Write Command Code                            |
| Block Read Command  | F1h   | SMBus Block Write/Read Process Call                       |
| Fixed Block 0       | F2h   | Fixed Block Read Command Code: address 40h, size 8 bytes  |
| Fixed Block 1       | F3h   | Fixed Block Read Command Code: address 48h, size 8 bytes  |
| Fixed Block 2       | F4h   | Fixed Block Read Command Code: address 50h, size 6 bytes  |
| Fixed Block 3       | F5h   | Fixed Block Read Command Code: address 56h, size 16 bytes |
| Fixed Block 4       | F6h   | Fixed Block Read Command Code: address 67h, size 4 bytes  |
| Fixed Block 5       | F7h   | Fixed Block Read Command Code: address 6Eh, size 8 bytes  |
| Fixed Block 6       | F8h   | Fixed Block Read Command Code: address 78h, size 12 bytes |
| Fixed Block 7       | F9h   | Fixed Block Read Command Code: address 90h, size 32 bytes |
| Fixed Block 8       | FAh   | Fixed Block Read Command Code: address B4h, size 8 bytes  |
| Fixed Block 9       | FBh   | Fixed Block Read Command Code: address C8h, size 8 bytes  |

| Command Code Name | Value | Description  |
|-------------------|-------|--|
| Fixed Block 10    | FCh   | Fixed Block Read Command Code: address D00h, size 16 bytes |
| Fixed Block 11    | FDh   | Fixed Block Read Command Code: address E5h, size 9 bytes   |

### 6.3.1.5.3 Write Operations

The LM94 supports the following SMBus write protocols.

#### 6.3.1.5.3.1 Write Byte

In this operation the master device sends an address byte and one data byte to the slave device, as follows:

1. The master device asserts a START condition.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK.
4. The master sends a command code (register address).
5. The slave asserts ACK.
6. The master sends the data byte.
7. The slave asserts ACK.
8. The master asserts a STOP condition to end the transaction.

|   |               |   |   |                  |   |           |   |   |
|---|---------------|---|---|------------------|---|-----------|---|---|
| 1 | 2             |   | 3 | 4                | 5 | 6         | 7 | 8 |
| S | Slave Address | W | A | Register Address | A | Data Byte | A | P |

#### 6.3.1.5.3.2 Write Word

In this operation the master device sends an address byte and two data bytes to the slave device, as follows:

1. The master device asserts a START condition.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK.
4. The master sends a command code (register address).
5. The slave asserts ACK.
6. The master sends the low data byte.
7. The slave asserts ACK.
8. The master sends the high data byte.
9. The slave asserts ACK.
10. The master asserts a STOP condition to end the transaction.

|   |               |   |   |                  |   |               |   |                |   |    |
|---|---------------|---|---|------------------|---|---------------|---|----------------|---|----|
| 1 | 2             |   | 3 | 4                | 5 | 6             | 7 | 8              | 9 | 10 |
| S | Slave Address | W | A | Register Address | A | Data Byte Low | A | Data Byte High | A | P  |

#### 6.3.1.5.3.3 SMBus Write Block to Any Address

The start address for a block write is embedded in this transaction. In this operation the master sends a block of data to the slave as follows:

1. The master device asserts a START condition.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK.
4. The master sends a command code that tells the slave device to expect a block write. The LM94 command code for a block write is F0h.
5. The slave asserts ACK.
6. The master sends a byte that tells the slave device how many data bytes it will send (N). The SMBus specification allows a maximum of 32 data bytes to be sent in a block write.
7. The slave asserts ACK.

8. The master sends data byte 1, the starting address of the block write.
9. The slave asserts ACK after each data byte.
10. The master sends data byte 2.
11. The slave asserts ACK.
12. The master continues to send data bytes and the slave asserts ACK for each byte.
13. The master asserts a STOP condition to end the transaction.

|   |               |   |   |                           |   |                |   |                             |   |             |    |   |             |   |    |
|---|---------------|---|---|---------------------------|---|----------------|---|-----------------------------|---|-------------|----|---|-------------|---|----|
| 1 | 2             |   | 3 | 4                         | 5 | 6              | 7 | 8                           | 9 | 10          | 11 | ~ | 12          |   | 13 |
| S | Slave Address | W | A | Command F0h (Block Write) | A | Byte Count (N) | A | Data Byte 1 (Start Address) | A | Data Byte 2 | A  | ~ | Data Byte N | A | P  |

### Special Notes

1. Any attempts to write to bytes beyond normal address space are acknowledged by the LM94 but are ignored.
2. Block writes do not wrap from address FFh back to 00h the address remains at FFh.
3. The Byte Count field is ignored by the LM94. The master device may send more or less bytes and the LM94 accepts them.
4. The SMBus specification requires that block writes never exceed 32 data bytes. Meeting this requirement means that only 31 actual data bytes can be sent (the register address counts as one byte). The LM94 does not care if this requirement is met.

#### 6.3.1.5.3.4 I2C<sup>®</sup> Block Write

In this transaction the master sends a block of data to the LM94 as follows:

1. The master device asserts a START condition.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK.
4. The master sends the starting address of the block write.
5. The slave asserts ACK after each data byte.
6. The master sends data byte 1.
7. The slave asserts ACK.
8. The master continues to send data bytes and the slave asserts ACK for each byte.
9. The master asserts a STOP condition to end the transaction.

|   |               |   |   |                  |   |             |   |   |             |   |   |
|---|---------------|---|---|------------------|---|-------------|---|---|-------------|---|---|
| 1 | 2             |   | 3 | 4                | 5 | 6           | 7 | 8 |             | 9 |   |
| S | Slave Address | W | A | Register Address | A | Data Byte 1 | A | ~ | Data Byte N | A | P |

### Special Notes:

1. Any attempts to write to bytes beyond normal address space are acknowledged by the LM94 but are ignored.
2. Block writes do not wrap from address FFh back to 00h the address remains at FFh.

#### 6.3.1.5.4 Read Operations

The LM94 uses the following SMBus read protocols.

##### 6.3.1.5.4.1 Read Byte

In the LM94, the read byte protocol is used to read a single byte of data from a register. In this operation the master device receives a single byte from a slave device, as follows:

1. The master device asserts a START condition.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK.
4. The master sends a register address.

5. The slave asserts an ACK.
6. The master sends a Repeated START.
7. The master sends the slave address followed by the read bit (high).
8. The slave asserts an ACK.
9. The master receives a data byte and asserts a NACK.
10. The master asserts a STOP condition and the transaction ends.

|   |               |   |   |                  |   |   |               |   |   |           |    |    |
|---|---------------|---|---|------------------|---|---|---------------|---|---|-----------|----|----|
| 1 | 2             |   | 3 | 4                | 5 | 6 | 7             |   | 8 | 9         |    | 10 |
| S | Slave Address | W | A | Register Address | A | S | Slave Address | R | A | Data Byte | /A | P  |

#### 6.3.1.5.4.2 Read Word

In the LM94, the read word protocol is used to read two bytes of data from a register or two consecutive registers. In this operation the master device reads two bytes from a slave device, as follows:

1. The master device asserts a START condition.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK.
4. The master sends a register address.
5. The slave asserts an ACK.
6. The master sends a Repeated START.
7. The master sends the slave address followed by the read bit (high).
8. The slave asserts an ACK.
9. The master receives the Low data byte and asserts an ACK.
10. The master receives the High data byte and asserts a NACK.
11. The master asserts a STOP condition and the transaction ends.

|   |               |   |   |                  |   |   |               |   |   |               |   |                |    |    |
|---|---------------|---|---|------------------|---|---|---------------|---|---|---------------|---|----------------|----|----|
| 1 | 2             |   | 3 | 4                | 5 | 6 | 7             |   | 8 | 9             |   | 10             |    | 11 |
| S | Slave Address | W | A | Register Address | A | S | Slave Address | R | A | Data Byte Low | A | Data Byte High | /A | P  |

#### 6.3.1.5.4.3 SMBus Block-Write Block-Read Process Call

This transaction is used to read a block of data from the LM94. Below is the sequence of events that occur in this transaction:

1. The master device asserts a START condition.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK.
4. The master sends a command code that tells the slave device to expect a block read (F1h) and the slave asserts ACK.
5. The master sends the Byte Count for this write which is 2 and the slave asserts ACK.
6. The master sends the Start Register Address for the block read and the slave asserts the ACK.
7. The master sends the Byte Count (1-32) for the block read processes call and the slave asserts ACK.
8. The master asserts a repeat START condition.
9. The master sends the 7-bit slave address followed by the read bit (high).
10. The slave asserts ACK.
11. The master receives a byte count data byte that tells it how many data bytes will received. This field reflects the number of bytes requested by the Byte Count transmitted to the LM94. The SMBus specification allows a maximum of 32 data bytes to be received in a block read. Then master asserts ACK.
12. The master receives byte 1 and then asserts ACK.
13. The master receives byte 2 and then asserts ACK.
14. The master receives N-3 data bytes, and asserts ACK for each one.
15. The master receives data byte N and asserts a NACK.
16. The master asserts a STOP condition to end the transaction.

|   |                        |   |   |                               |   |                 |   |                        |             |                        |    |   |               |   |    |   |
|---|------------------------|---|---|-------------------------------|---|-----------------|---|------------------------|-------------|------------------------|----|---|---------------|---|----|---|
| 1 | 2                      |   | 3 | 4                             |   | 5               |   | 6                      |             | 7                      |    | 8 | 9             |   | 10 | ~ |
| S | Slave Address          | W | A | Block Read Command Code (F1h) | A | Byte Count (2h) | A | Start Register Address | A           | Byte Count (1–20h) (N) | A  | S | Slave Address | R | A  |   |
| ~ | 11                     |   |   | 12                            |   |                 |   | 13                     |             | 14                     | 15 |   | 15            |   | 16 |   |
|   | Byte Count (1–20h) (N) |   | A | Data Byte 1                   | A | Data Byte 2     | A | ~                      | Data Byte N | /A                     | P  |   |               |   |    |   |

**Special Notes:**

1. The LM94 returns 00h when address locations outside of normal address space are read.
2. Block reads do not wrap around from address FFh to 00h
3. If the master acknowledges more bytes than it requested, the LM94 continues to supply data until the master does not acknowledge a byte.
4. If the master does not acknowledge a byte to prematurely abort a block read, the LM94 gets off the bus to allow the master to issue a STOP signal.

**6.3.1.5.4.4 Simulated SMBus Block-Write Block-Read Process Call**

Alternatively, if the master cannot support an SMBus Block-Write Block-Read process call, it can be emulated by two transactions (a block write followed by a block read). This should only be done in a single master system, since in a dual master system collisions can occur that corrupt the data and transaction. Below is the sequence of events for these transactions:

1. The master issues a START to start this transaction.
2. The master sends the 7-bit slave address followed by a write bit (low).
3. The slave asserts the ACK.
4. The master sends the Block Read command code (F1h) and the slave asserts the ACK.
5. The master sends the Byte Count (2h) for this transaction and the slave asserts the ACK.
6. The master sends the Start Register Address and the slave asserts the ACK.
7. The master sends the Byte Count (1-20h) for the Block-Read Process Call and the slave asserts the ACK.
8. The master sends a STOP to end this transaction.
9. The master sends a START to start this transaction.
10. The master sends the 7-bit slave address followed by a write bit (low) and the slave asserts the ACK.
11. The master sends the Block Read Command code (F1h) and the slave asserts the ACK.
12. The master sends a repeat START.
13. The master sends the 7-bit slave address followed by a read bit (high) and the slave asserts the ACK.
14. The master receives Byte Count (this matches the size sent by the master in step 7) and asserts the ACK.
15. The master receives Data Byte 1 and asserts the ACK.
16. The master receives Data Byte 2 and asserts the ACK.
17. The master receives N-3 data bytes, and asserts ACK for each one.
18. The master receives the last data byte and asserts a NACK.
19. The master issues a STOP to end this transaction.

|   |               |   |   |                               |   |                 |   |                        |   |                        |   |   |   |               |   |   |
|---|---------------|---|---|-------------------------------|---|-----------------|---|------------------------|---|------------------------|---|---|---|---------------|---|---|
| 1 | 2             |   | 3 | 4                             |   | 5               |   | 6                      |   | 7                      |   | 8 | 9 | 10            |   | ~ |
| S | Slave Address | W | A | Block Read Command Code (F1h) | A | Byte Count (2h) | A | Start Register Address | A | Byte Count (1–20h) (N) | A | P | S | Slave Address | W | A |

|   |                               |   |    |               |   |   |  |                        |   |             |   |             |   |               |    |    |
|---|-------------------------------|---|----|---------------|---|---|--|------------------------|---|-------------|---|-------------|---|---------------|----|----|
| ~ | 11                            |   | 12 | 13            |   |   |  | 14                     |   | 15          |   | 16          |   | 17            |    | 16 |
|   | Block Read Command Code (F1h) | A | S  | Slave Address | R | A |  | Byte Count (1–20h) (N) | A | Data Byte 1 | A | Data Byte 2 | A | ~ Data Byte N | /A | P  |

**Special Notes:**

- Steps 9 through 19 can be repeated to read another block of data. The address auto-increments such that the next block starts where the last block left off. The size returned by the LM94 is the same each time.
- The LM94 returns 00h when address locations outside of normal address space are read.
- Block reads do not wrap around from address FFh to 00h
- If the master acknowledges more bytes than it requested, the LM94 continues to supply data until the master does not acknowledge a byte.
- If the master does not acknowledge a byte to prematurely abort a block read, the LM94 gets off the bus to allow the master to issue a STOP signal.
- After a block read is finished, the base address of the LM94 is updated to point to the byte just beyond the last byte read.

**6.3.1.5.4.5 SMBus Fixed Address Block Reads**

Block reads can be performed from pre-defined addresses. A special command code has been reserved for each pre-defined address. See the [Section 6.3.1.5.2](#) for more details on the command codes. Below is the sequence of events that occur for this type of block read:

- The master sends a START to start this transaction.
- The master sends the 7-bit slave address followed by a write bit (low).
- The slave asserts an ACK.
- The master sends a Fixed Block Command Code (F2h–FDh) and the slave asserts an ACK.
- The master sends a repeated START.
- The master sends the 7-bit slave address followed by a read bit (high).
- The slave asserts an ACK.
- The master receives the Byte Count (depends on the Fixed Block Command Code used) and asserts an ACK.
- The master receives the first data byte and asserts an ACK.
- The master continues to receive data bytes and asserting an ACK.
- The master receives the last data byte.
- The master asserts a NACK.
- The master issues a STOP to end this transaction.

|   |               |   |   |                                    |   |   |               |   |   |                |   |             |   |               |    |    |    |
|---|---------------|---|---|------------------------------------|---|---|---------------|---|---|----------------|---|-------------|---|---------------|----|----|----|
| 1 | 2             |   | 3 | 4                                  |   | 5 | 6             |   | 7 | 8              |   | 9           |   | 10            | 11 | 12 | 13 |
| S | Slave Address | W | A | Fixed Block Command Code (F2h–FDh) | A | S | Slave Address | R | A | Byte Count (N) | A | Data Byte 1 | A | ~ Data Byte N | /A | P  |    |

**Special Notes:**

- The LM94 returns 00h when address locations outside of normal address space are read.
- Block reads do not wrap around from address FFh to 00h.
- If the master acknowledges more bytes than it requested, the LM94 continues to supply data until the master does not acknowledge a byte.
- If the master does not acknowledge a byte to prematurely abort a block read, the LM94 gets off the bus to allow the master to issue a STOP signal.

### 6.3.1.5.4.6 I<sup>2</sup>C Block Reads

The LM94 supports I<sup>2</sup>C block reads. The following sequence of events occur in this transaction:

1. The master sends a START to start this transaction .
2. The master send 7-bit slave address followed by a write bit (low).
3. The slave asserts an ACK.
4. The master sends the register address and the slave asserts an ACK.
5. The master sends a repeated START.
6. The master sends the 7-bit slave address followed by a read bit (high).
7. The slave asserts an ACK.
8. The master receives Data Byte 1 and asserts an ACK.
9. The master continues to receive bytes and asserting an ACK for each byte received.
10. The master receives the last byte.
11. The master asserts a NACK.
12. The master issues a STOP.

|   |               |   |   |                  |   |   |               |   |   |             |   |             |   |   |             |    |    |
|---|---------------|---|---|------------------|---|---|---------------|---|---|-------------|---|-------------|---|---|-------------|----|----|
| 1 | 2             |   | 3 | 4                |   | 5 | 6             |   | 7 | 8           |   | 9           |   | ~ | 10          | 11 | 12 |
| S | Slave Address | W | A | Register Address | A | S | Slave Address | R | A | Data Byte 1 | A | Data Byte 2 | A | ~ | Data Byte N | /A | P  |

#### Special Notes:

1. The LM94 returns 00h when address locations outside of normal address space are read.
2. Block reads do not wrap around from address FFh to 00h.
3. If the master acknowledges more bytes that it requested, the LM94 continues to supply data until the master does not acknowledge a byte.
4. If the master does not acknowledges a byte to prematurely abort a block read, the LM94 gets off the bus to allow the master to issue a STOP signal.

### 6.3.1.6 READING AND WRITING 16-BIT REGISTERS

Whenever the low byte of a 16-bit register is read, the high byte is frozen. After the high byte is read, it is unfrozen. This ensures that the entire 16-bit value is read properly and the high byte matches with the low byte. If the low byte of a different 16-bit register is read, the currently frozen high byte is unfrozen and the high byte of the new 16-bit register is frozen. In a system with two SMBus masters, it is very important that only one master reads any 16-bit registers at a time. One possible method to achieve this would involve using 16-bit SMBus reads (instead of two separate 8-bit reads) to read 16-bit registers.

Whenever the low byte of a 16-bit register is written, the write is buffered and does not take effect until the corresponding high byte is written. If the low byte of a different 16-bit register is written, the previously buffered low byte of the first register is discarded. If a device attempts to write the high byte of a 16-bit register, and the corresponding low byte was not written (or was discarded), then the LM94 will NACK the byte.

## 6.4 Registers

### 6.4.1 Register Warnings

In most cases, reserved registers and register bits return zero when read. This should not be relied upon, since reserved registers can be used for future expansion of the LM94 functions.

Some registers have “N/D” for their default value. This means that the power-up default of the register is not defined. In the case of value registers, care should be taken to ensure that software does not read a value register until the associated measurement function has acquired a measurement. This applies to temperatures, voltages, fan RPM, and PROCHOT monitoring.

### 6.4.2 Register Summary Table

**Table 6-3. Register Key**

| Term | Description            |
|------|------------------------|
| N/D  | Not Defined            |
| N/A  | Not Applicable         |
| R    | Read Only              |
| R/W  | Read or Write          |
| RWC  | Read or Write to Clear |

| Lock   | Register Name                        | Address | Default | Description  |
|--|--------------------------------------|---------|---------|--|
| <b>FACTORY REGISTERS</b>                               |                                      |         |         |  |
| x  | XOR Test                             | 00h     | 00h     | Used to set the XOR test tree mode   |
|  | SMBus Test                           | 01h     | 00      | SMBus read/write test register   |
|  | Reserved                             | 02h-04h | N/D     |  |
| <b>“REMOTE DIODE” MODE SELECT</b>                      |                                      |         |         |  |
| x  | Transistor Mode Select               | 05h     | 00h     | Selects Diode Mode (default) or Transistor Mode for “Remote Diode” measurements                  |
| <b>VALUE REGISTER SECTION 1</b>                        |                                      |         |         |  |
|  | Zone 1b (CPU1 Diode b) Temp          | 06h     | 00h     | Measured value of remote thermal diode temperature channel 1b                                    |
|  | Zone 2b (CPU2 Diode b) Temp          | 07h     | 00h     | Measured value of remote thermal diode temperature channel 2b                                    |
|  | Zone 1b (CPU1 Diode b) Filtered Temp | 08h     | 00h     | Filtered value of remote thermal diode temperature channel 1b                                    |
|  | Zone 2b (CPU2 Diode b) Filtered Temp | 09h     | 00h     | Filtered value of remote thermal diode temperature channel 2b                                    |
|  | PWM1 8-bit Duty Cycle Value          | 0Ah     | 00h     | 8- bit value of the PWM1 duty cycle.   |
|  | PWM2 8-bit Duty Cycle Value          | 0Bh     | 00h     | 8-bit value of the PWM2 duty cycle   |
| <b>HIGH RESOLUTION PWM OVERRIDE REGISTERS</b>          |                                      |         |         |  |
| x  | PWM1 Duty Cycle Override (low byte)  | 0Ch     | 00h     | Lower byte of the high resolution PWM1 duty cycle register                                       |
| x  | PWM1 Duty Cycle Override (high byte) | 0Dh     | 00h     | Upper byte of the high resolution PWM1 duty cycle register                                       |
| x  | PWM2 Duty Cycle Override (low byte)  | 0Eh     | 00h     | Lower byte of the high resolution PWM2 duty cycle register                                       |
| x  | PWM2 Duty Cycle Override (high byte) | 0Fh     | 00h     | Upper byte of the high resolution PWM2 duty cycle register                                       |
| <b>EXTENDED RESOLUTION TEMPERATURE VALUE REGISTERS</b> |                                      |         |         |  |
|  | Z1a_LSB                              | 10h     | 00h     | Zone 1a (CPU1) extended resolution unfiltered temperature value register, least-significant byte |
|  | Z1a_MSB                              | 11h     | 00h     | Zone 1a (CPU1) extended resolution unfiltered temperature value register, most-significant byte  |
|  | Z1b_LSB                              | 12h     | 00h     | Zone 1b (CPU1) extended resolution unfiltered temperature value register, least-significant-byte |
|  | Z1b_MSB                              | 13h     | 00h     | Zone 1b (CPU1) extended resolution unfiltered temperature value register, most-significant byte  |

| Lock | Register Name | Address | Default | Description  |
|------|---------------|---------|---------|--|
|      | Z2a_LSB       | 14h     | 00h     | Zone 2a (CPU2) extended resolution unfiltered temperature value register, least-significant-byte |
|      | Z2a_MSB       | 15h     | 00h     | Zone 2a (CPU2) extended resolution unfiltered temperature value register, most-significant byte  |
|      | Z2b_LSB       | 16h     | 00h     | Zone 2b (CPU2) extended resolution unfiltered temperature value register, least-significant-byte |
|      | Z2b_MSB       | 17h     | 00h     | Zone 2b (CPU2) extended resolution unfiltered temperature value register, most-significant byte  |
|      | Z1a_F_LSB     | 18h     | 00h     | Zone 1a (CPU1) extended resolution filtered temperature value register, least-significant byte   |
|      | Z1a_F_MSB     | 19h     | 00h     | Zone 1a (CPU1) extended resolution filtered temperature value register, most-significant byte    |
|      | Z1b_F_LSB     | 1Ah     | 00h     | Zone 1b (CPU1) extended resolution filtered temperature value register, least-significant-byte   |
|      | Z1b_F_MSB     | 1Bh     | 00h     | Zone 1b (CPU1) extended resolution filtered temperature value register, most-significant byte    |
|      | Z2a_F_LSB     | 1Ch     | 00h     | Zone 2a (CPU2) extended resolution filtered temperature value register, least-significant-byte   |
|      | Z2a_F_MSB     | 1Dh     | 00h     | Zone 2a (CPU2) extended resolution filtered temperature value register, most-significant byte    |
|      | Z2b_F_LSB     | 1Eh     | 00h     | Zone 2b (CPU2) extended resolution filtered temperature value register, least-significant-byte   |
|      | Z2b_F_MSB     | 1Fh     | 00h     | Zone 2b (CPU2) extended resolution filtered temperature value register, most-significant byte    |
|      | Z3_LSB        | 20h     | 00h     | Zone 3 (Internal) extended resolution temperature value register, least-significant byte         |
|      | Z3_MSB        | 21h     | 00h     | Zone 3 (Internal) extended resolution temperature value register, least-significant byte         |
|      | Z4_LSB        | 22h     | 00h     | Zone 4 (External Digital) extended resolution temperature value register, most-significant byte  |
|      | Z4_MSB        | 23h     | 00h     | Zone 4 (External Digital) extended resolution temperature value register, least-significant byte |
|      | Reserved      | 24h-30h | N/D     |  |

#### PI LOOP AND FAN CONTROL SETUP REGISTERS

|   |  |     |     |   |
|---|--|-----|-----|---|
| x | Temperature Source Select                | 31h | 00h | Selects the temperature source for some temperature zones.                      |
| x | PWM Filter Settings                      | 32h | 00h | Sets the IIR filter coefficients for the PWM outputs for low resolution sources |
| x | PWM1 Filter Shutoff Threshold            | 33h | 00h | PWM1 Filter Shutoff Threshold   |
| x | PWM2 Filter Shutoff Threshold            | 34h | 00h | PWM2 Filter Shutoff Threshold   |
| x | PI/LUT Fan Control Bindings              | 35h | 30h | PI/LUT fan control binding configuration  |
| x | PI Controller Minimum PWM and Hysteresis | 36h | 00h | PI Controller Minimum PWM and Hysteresis settings                               |
| x | Zone 1 Tcontrol                          | 37h | 00h | Zone 1 (CPU1) PI Controller Target Temperature (Tcontrol)                       |
| x | Zone 2 Tcontrol                          | 38h | 00h | Zone 2 (CPU2) PI Controller Target Temperature (Tcontrol)                       |
| x | Zone 1 Toff                              | 39h | 80h | Zone 1 (CPU1) PI Controller Off Temperature (Toff)                              |
| x | Zone 2 Toff                              | 3Ah | 80h | Zone 2 (CPU2) PI Controller Off Temperature (Toff)                              |
| x | P Coefficient                            | 3Bh | 00h | PI controller proportional coefficient  |
| x | I Coefficient                            | 3Ch | 00h | PI controller integral coefficient  |
| x | PI Exponents                             | 3Dh | 00h | PI controller coefficient exponents   |

| Lock                                   | Register Name                  | Address | Default | Description   |
|--|--------------------------------|---------|---------|---|
| <b>DEVICE IDENTIFICATION REGISTERS</b> |                                |         |         |   |
|  | Manufacturer ID                | 3Eh     | 01h     | Contains manufacturer ID code                                 |
|  | Version/Stepping               | 3Fh     | 79h     | Contains code for major and minor revisions                   |
| <b>BMC ERROR STATUS REGISTERS</b>      |                                |         |         |   |
|  | B_Error Status 1               | 40h     | 00h     | BMC error status register 1                                   |
|  | B_Error Status 2               | 41h     | 00h     | BMC error register 2  |
|  | B_Error Status 3               | 42h     | 00h     | BMC error register 3  |
|  | B_Error Status 4               | 43h     | 00h     | BMC error register 4  |
|  | B_P1_PROCHOT Error Status      | 44h     | 00h     | BMC error register for P1_PROCHOT                             |
|  | B_P2_PROCHOT Error Status      | 45h     | 00h     | BMC error register for P2_PROCHOT                             |
|  | B_GPI Error Status             | 46h     | 00h     | BMC error register for GPIs                                   |
|  | B_Fan Error Status             | 47h     | 00h     | BMC error register for Fans                                   |
| <b>HOST ERROR STATUS REGISTERS</b>     |                                |         |         |   |
|  | H_Error Status 1               | 48h     | 00h     | HOST error status register 1                                  |
|  | H_Error Status 2               | 49h     | 00h     | HOST error register 2   |
|  | H_Error Status 3               | 4Ah     | 00h     | HOST error register 3   |
|  | H_Error Status 4               | 4Bh     | 00h     | HOST error register 4   |
|  | H_P1_PROCHOT Error Status      | 4Ch     | 00h     | HOST error register for P1_PROCHOT                            |
|  | H_P2_PROCHOT Error Status      | 4Dh     | 00h     | HOST error register for P2_PROCHOT                            |
|  | H_GPI Error Status             | 4Eh     | 00h     | HOST error register for GPIs                                  |
|  | H_Fan Error Status             | 4Fh     | 00h     | HOST error register for Fans                                  |
| <b>VALUE REGISTERS SECTION 2</b>       |                                |         |         |   |
|  | Zone 1a (CPU1) Temp            | 50h     | 00h     | Measured value of remote thermal diode temperature channel 1a |
|  | Zone 2a (CPU2) Temp            | 51h     | 00h     | Measured value of remote thermal diode temperature channel 2a |
|  | Zone 3 (Internal) Temp         | 52h     | 00h     | Measured temperature from on-chip sensor                      |
|  | Zone 4 (External Digital) Temp | 53h     | 00h     | Measured temperature from external temperature sensor         |
|  | Zone 1a (CPU1) Filtered Temp   | 54h     | 00h     | Filtered value of remote thermal diode temperature channel 1a |
|  | Zone 2a (CPU2) Filtered Temp   | 55h     | 00h     | Filtered value of remote thermal diode temperature channel 2a |
|  | AD_IN1 Voltage                 | 56h     | N/D     | Measured value of AD_IN1                                      |
|  | AD_IN2 Voltage                 | 57h     | N/D     | Measured value of AD_IN2                                      |
|  | AD_IN3 Voltage                 | 58h     | N/D     | Measured value of AD_IN3                                      |
|  | AD_IN4 Voltage                 | 59h     | N/D     | Measured value of AD_IN4                                      |
|  | AD_IN5 Voltage                 | 5Ah     | N/D     | Measured value of AD_IN5                                      |
|  | AD_IN6 Voltage                 | 5Bh     | N/D     | Measured value of AD_IN6                                      |
|  | AD_IN7 Voltage                 | 5Ch     | N/D     | Measured value of AD_IN7                                      |
|  | AD_IN8 Voltage                 | 5Dh     | N/D     | Measured value of AD_IN8                                      |
|  | AD_IN9 Voltage                 | 5Eh     | N/D     | Measured value of AD_IN9                                      |
|  | AD_IN10 Voltage                | 5Fh     | N/D     | Measured value of AD_IN10                                     |
|  | AD_IN11 Voltage                | 60h     | N/D     | Measured value of AD_IN11                                     |
|  | AD_IN12 Voltage                | 61h     | N/D     | Measured value of AD_IN12                                     |
|  | AD_IN13 Voltage                | 62h     | N/D     | Measured value of AD_IN13                                     |
|  | AD_IN14 Voltage                | 63h     | N/D     | Measured value of AD_IN14                                     |
|  | AD_IN15 Voltage                | 64h     | N/D     | Measured value of AD_IN15                                     |
|  | AD_IN16 Voltage                | 65h     | N/D     | Measured value of AD_IN16 ( $V_{DD}$ 3.3V S/B)                |
|  | Reserved                       | 66h     | N/D     |   |

| Lock   | Register Name                       | Address | Default | Description  |
|--|-------------------------------------|---------|---------|--|
|  | Current P1_PROCHOT                  | 67h     | 00h     | Measured P1_PROCHOT throttle percentage  |
|  | Average P1_PROCHOT                  | 68h     | 00h     | Average P1_PROCHOT throttle percentage   |
|  | Current P2_PROCHOT                  | 69h     | 00h     | Measured P2_PROCHOT throttle percentage  |
|  | Average P2_PROCHOT                  | 6Ah     | 00h     | Average P2_PROCHOT throttle percentage   |
|  |                                     |         |         |  |
|  | GPI State                           | 6Bh     | 00h     | Current GPIO state   |
|  |                                     |         |         |  |
|  | P1_VID                              | 6Ch     | 00h     | Current VID value of Processor 1   |
|  | P2_VID                              | 6Dh     | 00h     | Current VID value of Processor 2   |
|  |                                     |         |         |  |
|  | FAN Tach 1 LSB                      | 6Eh     | 00h     | Measured FAN Tach 1 LSB  |
|  | FAN Tach 1 MSB                      | 6Fh     | 00h     | Measured FAN Tach 1 MSB  |
|  | FAN Tach 2 LSB                      | 70h     | 00h     | Measured FAN Tach 2 LSB  |
|  | FAN Tach 2 MSB                      | 71h     | 00h     | Measured FAN Tach 2 MSB  |
|  | FAN Tach 3 LSB                      | 72h     | 00h     | Measured FAN Tach 3 LSB  |
|  | FAN Tach 3 MSB                      | 73h     | 00h     | Measured FAN Tach 3 MSB  |
|  | FAN Tach 4 LSB                      | 74h     | 00h     | Measured FAN Tach 4 LSB  |
|  | FAN Tach 4 MSB                      | 75h     | 00h     | Measured FAN Tach 4 MSB  |
|  |                                     |         |         |  |
|  | Reserved                            | 76h-77h | N/D     |  |
|  |                                     |         |         |  |
| <b>TEMPERATURE LIMIT REGISTERS</b>                             |                                     |         |         |  |
|  | Zone 1 (CPU1) Low Temp              | 78h     | 80h     | Low limit for external thermal diode temperature channel 1 (D1) measurement          |
|  | Zone 1 (CPU1) High Temp             | 79h     | 80h     | High limit for external thermal diode temperature channel 1 (D1) measurement         |
|  | Zone 2 (CPU2) Low Temp              | 7Ah     | 80h     | Low limit for external thermal diode temperature channel 2 (D2) measurement          |
|  | Zone 2 (CPU2) High Temp             | 7Bh     | 80h     | High limit for external thermal diode temperature channel 2 (D2) measurement         |
|  | Zone 3 (Internal) Low Temp          | 7Ch     | 80h     | Low limit for local temperature measurement  |
|  | Zone 3 (Internal) High Temp         | 7Dh     | 80h     | High limit for local temperature measurement   |
|  | Zone 4 (External Digital) Low Temp  | 7Eh     | 80h     | Low limit for external digital temperature sensor                                    |
|  | Zone 4 (External Digital) High Temp | 7Fh     | 80h     | High limit for external digital temperature sensor                                   |
|  |                                     |         |         |  |
| x  | Fan Boost Temp Zone 1               | 80h     | 3Ch     | Zone 1 (CPU1) fan boost temperature  |
| x  | Fan Boost Temp Zone 2               | 81h     | 3Ch     | Zone 2 (CPU2) fan boost temperature  |
| x  | Fan Boost Temp Zone 3               | 82h     | 23h     | Zone 3 (Internal) fan boost temperature  |
| x  | Fan Boost Temp Zone 4               | 83h     | 23h     | Zone 4 (External Digital) fan boost temperature                                      |
|  | Zone1 and Zone 2 Hysteresis         | 84h     | 00h     | Zone 1 and Zone 2 hysteresis for limit comparisons                                   |
|  | Zone 3 and Zone 4 Hysteresis        | 85h     | 00h     | Zone 3 and Zone 4 hysteresis for limit comparisons                                   |
|  |                                     |         |         |  |
|  | Reserved                            | 86h-8Dh | N/D     |  |
|  |                                     |         |         |  |
| <b>ZONE 1b and 2b TEMPERATURE READING ADJUSTMENT REGISTERS</b> |                                     |         |         |  |
|  | Zone 1b Temp Adjust                 | 8Eh     | 00h     | Allows all Zone 1b temperature measurements to be adjusted by a programmable offset. |

| Lock                         | Register Name         | Address | Default | Description  |
|------------------------------|-----------------------|---------|---------|--|
|                              | Zone 2b Temp Adjust   | 8Fh     | 00h     | Allows all Zone 2b temperature measurements to be adjusted by a programmable offset. |
| <b>OTHER LIMIT REGISTERS</b> |                       |         |         |  |
|                              | AD_IN1 Low Limit      | 90h     | 00h     | Low limit for analog input 1 measurement   |
|                              | AD_IN1 High Limit     | 91h     | FFh     | High limit for analog input 1 measurement  |
|                              | AD_IN2 Low Limit      | 92h     | 00h     | Low limit for analog input 2 measurement   |
|                              | AD_IN2 High Limit     | 93h     | FFh     | High limit for analog input 2 measurement  |
|                              | AD_IN3 Low Limit      | 94h     | 00h     | Low limit for analog input 3 measurement   |
|                              | AD_IN3 High Limit     | 95h     | FFh     | High limit for analog input 3 measurement  |
|                              | AD_IN4 Low Limit      | 96h     | 00h     | Low limit for analog input 4 measurement   |
|                              | AD_IN4 High Limit     | 97h     | FFh     | High limit for analog input 4 measurement  |
|                              | AD_IN5 Low Limit      | 98h     | 00h     | Low limit for analog input 5 measurement   |
|                              | AD_IN5 High Limit     | 99h     | FFh     | High limit for analog input 5 measurement  |
|                              | AD_IN6 Low Limit      | 9Ah     | 00h     | Low limit for analog input 6 measurement   |
|                              | AD_IN6 High Limit     | 9Bh     | FFh     | High limit for analog input 6 measurement  |
|                              | AD_IN7 Low Limit      | 9Ch     | 00h     | Low limit for analog input 7 measurement   |
|                              | AD_IN7 High Limit     | 9Dh     | FFh     | High limit for analog input 7 measurement  |
|                              | AD_IN8 Low Limit      | 9Eh     | 00h     | Low limit for analog input 8 measurement   |
|                              | AD_IN8 High Limit     | 9Fh     | FFh     | High limit for analog input 8 measurement  |
|                              | AD_IN9 Low Limit      | A0h     | 00h     | Low limit for analog input 9 measurement   |
|                              | AD_IN9 High Limit     | A1h     | FFh     | High limit for analog input 9 measurement  |
|                              | AD_IN10 Low Limit     | A2h     | 00h     | Low limit for analog input 10 measurement  |
|                              | AD_IN10 High Limit    | A3h     | FFh     | High limit for analog input 10 measurement   |
|                              | AD_IN11 Low Limit     | A4h     | 00h     | Low limit for analog input 11 measurement  |
|                              | AD_IN11 High Limit    | A5h     | FFh     | High limit for analog input 11 measurement   |
|                              | AD_IN12 Low Limit     | A6h     | 00h     | Low limit for analog input 12 measurement  |
|                              | AD_IN12 High Limit    | A7h     | FFh     | High limit for analog input 12 measurement   |
|                              | AD_IN13 Low Limit     | A8h     | 00h     | Low limit for analog input 13 measurement  |
|                              | AD_IN13 High Limit    | A9h     | FFh     | High limit for analog input 13 measurement   |
|                              | AD_IN14 Low Limit     | AAh     | 00h     | Low limit for analog input 14 measurement  |
|                              | AD_IN14 High Limit    | ABh     | FFh     | High limit for analog input 14 measurement   |
|                              | AD_IN15 Low Limit     | ACh     | 00h     | Low limit for analog input 15 measurement  |
|                              | AD_IN15 High Limit    | ADh     | FFh     | High limit for analog input 15 measurement   |
|                              | AD_IN16 Low Limit     | A Eh    | 00h     | Low limit for analog input 16 measurement  |
|                              | AD_IN16 High Limit    | AFh     | FFh     | High limit for analog input 16 measurement   |
|                              |                       |         |         |  |
|                              | P1_PROCHOT User Limit | B0h     | FFh     | User settable limit for P1_PROCHOT   |
|                              | P2_PROCHOT User Limit | B1h     | FFh     | User settable limit for P2_PROCHOT   |
|                              |                       |         |         |  |
|                              | Vccp1 Limit Offsets   | B2h     | 17h     | VID offset values for window comparator for CPU1 Vccp (AD_IN7)                       |
|                              | Vccp2 Limit Offsets   | B3h     | 17h     | VID offset values for window comparator for CPU2 Vccp (AD_IN8)                       |
|                              |                       |         |         |  |
|                              | FAN Tach 1 Limit LSB  | B4h     | FCh     | FAN Tach 1 Limit LSB   |
|                              | FAN Tach 1 Limit MSB  | B5h     | FFh     | FAN Tach 1 Limit MSB   |
|                              | FAN Tach 2 Limit LSB  | B6h     | FCh     | FAN Tach 2 Limit LSB   |
|                              | FAN Tach 2 Limit MSB  | B7h     | FFh     | FAN Tach 2 Limit MSB   |

| Lock                   | Register Name                     | Address | Default | Description  |
|------------------------|-----------------------------------|---------|---------|--|
|                        | FAN Tach 3 Limit LSB              | B8h     | FCh     | FAN Tach 3 Limit LSB   |
|                        | FAN Tach 3 Limit MSB              | B9h     | FFh     | FAN Tach 3 Limit MSB   |
|                        | FAN Tach 4 Limit LSB              | BAh     | FCh     | FAN Tach 4 Limit LSB   |
|                        | FAN Tach 4 Limit MSB              | BBh     | FFh     | FAN Tach 4 Limit MSB   |
| <b>SETUP REGISTERS</b> |                                   |         |         |  |
|                        | Special Function Control 1        | BCh     | 00h     | Controls the hysteresis for voltage limit comparisons. Also selects filtered or unfiltered temperature usage for temperature limit comparisons and fan control.                    |
|                        | Special Function Control 2        | BDh     | 00h     | Enables smart tach detection. Also selects 0.5°C or 1.0°C resolution for fan control.  |
| x                      | GPI / VID Level Control           | BEh     | 00h     | Control the input threshold levels for the P1_VIDx, P2_VIDx and GPIO_x inputs.   |
| x                      | PWM Ramp Control                  | BFh     | 00h     | Controls the ramp rate of the PWM duty cycle when $\overline{\text{VRDx\_HOT}}$ is asserted, as well as the ramp rate when $\overline{\text{PROCHOT}}$ exceeds the user threshold. |
| x                      | Fan Boost Hysteresis (Zones 1/2)  | C0h     | 44h     | Fan Boost Hysteresis for zones 1 and 2   |
| x                      | Fan Boost Hysteresis (Zones 3/4)  | C1h     | 44h     | Fan Boost Hysteresis for zones 3 and 4   |
| x                      | Zones 1/2 Spike Smoothing Control | C2h     | 00h     | Configures Spike Smoothing for zones 1 and 2   |
| x                      | LUT 1/2 MinPWM and Hysteresis     | C3h     | 00h     | Controls MinPWM and hysteresis setting for LUT 1 and 2 auto-fan control  |
| x                      | LUT 3/4 MinPWM and Hysteresis     | C4h     | 00h     | Controls MinPWM and hysteresis setting for LUT 3 and 4 auto-fan control  |
|                        |                                   |         |         |  |
|                        | GPO                               | C5h     | 00h     | Controls the output state of the GPIO pins   |
|                        |                                   |         |         |  |
|                        | PROCHOT Control                   | C6h     | 00h     | Controls assertion of P1_PROCHOT or P2_PROCHOT   |
|                        | PROCHOT Time Interval             | C7h     | 11h     | Configures the time window over which the $\overline{\text{PROCHOT}}$ inputs are measured  |
|                        |                                   |         |         |  |
| x                      | PWM1 Control 1                    | C8h     | 00h     | Controls PWM control source bindings.  |
| x                      | PWM1 Control 2                    | C9h     | 00h     | Controls PWM override and output polarity  |
| x                      | PWM1 Control 3                    | CAh     | 00h     | Controls PWM spin-up duration and duty cycle   |
| x                      | PWM1 Control 4                    | CBh     | 00h     | Frequency control for PWM1.  |
|                        |                                   |         |         |  |
| x                      | PWM2 Control 1                    | CCh     | 00h     | Controls PWM control source bindings.  |
| x                      | PWM2 Control 2                    | CDh     | 00h     | Controls PWM override and output polarity  |
| x                      | PWM2 Control 3                    | CEh     | 00h     | Controls PWM spin-up duration and duty cycle   |
| x                      | PWM2 Control 4                    | CFh     | 00h     | Frequency control for PWM2   |
|                        |                                   |         |         |  |
| x                      | LUT 1 Base Temperature            | D0h     | 00h     | Base temperature to which look-up table offset is applied for LUT 1  |
| x                      | LUT 2 Base Temperature            | D1h     | 00h     | Base temperature to which look-up table offset is applied for LUT 2  |
| x                      | LUT 3 Base Temperature            | D2h     | 00h     | Base temperature to which look-up table offset is applied for LUT 3  |
| x                      | LUT 4 Base Temperature            | D3h     | 00h     | Base temperature to which look-up table offset is applied for LUT 4  |
|                        |                                   |         |         |  |
| x                      | Step 2 Temp Offset                | D4h     | 00h     | Step 2 LUT 1/2 and LUT 3/4 Offset Temperatures   |
| x                      | Step 3 Temp Offset                | D5h     | 00h     | Step 3 LUT 1/2 and LUT 3/4 Offset Temperatures   |
| x                      | Step 4 Temp Offset                | D6h     | 00h     | Step 4 LUT 1/2 and LUT 3/4 Offset Temperatures   |
| x                      | Step 5 Temp Offset                | D7h     | 00h     | Step 5 LUT 1/2 and LUT 3/4 Offset Temperatures   |
| x                      | Step 6 Temp Offset                | D8h     | 00h     | Step 6 LUT 1/2 and LUT 3/4 Offset Temperatures   |

| Lock   | Register Name                 | Address | Default | Description   |
|--|-------------------------------|---------|---------|---|
| x  | Step 7 Temp Offset            | D9h     | 00h     | Step 7 LUT 1/2 and LUT 3/4 Offset Temperatures  |
| x  | Step 8 Temp Offset            | DAh     | 00h     | Step 8 LUT 1/2 and LUT 3/4 Offset Temperatures  |
| x  | Step 9 Temp Offset            | DBh     | 00h     | Step 9 LUT 1/2 and LUT 3/4 Offset Temperatures  |
| x  | Step 10 Temp Offset           | DCh     | 00h     | Step 10 LUT 1/2 and LUT 3/4 Offset Temperatures   |
| x  | Step 11 Temp Offset           | DDh     | 00h     | Step 11 LUT 1/2 and LUT 3/4 Offset Temperatures   |
| x  | Step 12 Temp Offset           | DEh     | 00h     | Step 12 LUT 1/2 and LUT 3/4 Offset Temperatures   |
| x  | Step 13 Temp Offset           | DFh     | 00h     | Step 13 LUT 1/2 and LUT 3/4 Offset Temperatures   |
|  |                               |         |         |   |
|  | TACH to PWM Binding           | E0h     | 00h     | Controls the tachometer input to PWM output binding   |
| x  | Tach Boost Control            | E1h     | 3Fh     | Controls the fan boost function upon a tach error   |
|  |                               |         |         |   |
| x  | LM94 Status/Control           | E2h     | 00h     | Gives Master error status, ASF reset control and Max PWM control                              |
| x  | LM94 Configuration            | E3h     | 00h     | Configures various outputs and provides START bit   |
| <b>SLEEP STATE CONTROL AND MASK REGISTERS</b>                  |                               |         |         |   |
|  | Sleep State Control           | E4h     | 03h     | Used to communicate the system sleep state to the LM94  |
|  | S1 GPI Mask                   | E5h     | FFh     | Sleep state S1 GPI error mask register  |
|  | S1 Fan Mask                   | E6h     | 0Fh     | Sleep state S1 fan tach error mask register   |
|  | S3 GPI Mask                   | E7h     | FFh     | Sleep state S3 GPI error mask register  |
|  | S3 Fan Mask                   | E8h     | 0Fh     | Sleep state S3 fan tach error mask register   |
|  | S3 Temperature/Voltage Mask   | E9h     | 07h     | Sleep state S3 temperature or voltage error mask register                                     |
|  | S4/5 GPI Mask                 | EAh     | FFh     | Sleep state S4/5 GPI error mask register  |
|  | S4/5 Temperature/Voltage Mask | EBh     | 07h     | Sleep state S4/5 temperature or voltage error mask register                                   |
| <b>OTHER MASK REGISTERS</b>                                    |                               |         |         |   |
|  | GPI Error Mask                | ECh     | FFh     | Error mask register for GPI faults  |
|  | Miscellaneous Error Mask      | EDh     | 3Fh     | Error mask register for $\overline{\text{VRDx\_HOT}}$ , GPI, and dynamic Vccp limit checking. |
|  |                               |         |         |   |
| <b>ZONE 1a AND 2a TEMPERATURE READING ADJUSTMENT REGISTERS</b> |                               |         |         |   |
|  | Zone 1a Temp Adjust           | EEh     | 00h     | Allows all Zone 1a temperature measurements to be adjusted by a programmable offset           |
|  | Zone 2a Temp Adjust           | EFh     | 00h     | Allows all Zone 2a temperature measurements to be adjusted by a programmable offset           |
| <b>BLOCK COMMANDS</b>  |                               |         |         |   |
|  | Block Write Command           | F0h     | N/A     | SMBus Block Write Command Code  |
|  | Block Read Command            | F1h     | N/A     | SMBus Block Write/Read Process call   |
|  | Fixed Block 0                 | F2h     | N/A     | Fixed block code address 40h, size 8 bytes  |
|  | Fixed Block 1                 | F3h     | N/A     | Fixed block code address 48h, size 8 bytes  |
|  | Fixed Block 2                 | F4h     | N/A     | Fixed block code address 50h, size 6 bytes  |
|  | Fixed Block 3                 | F5h     | N/A     | Fixed block code address 56h, size 16 bytes   |
|  | Fixed Block 4                 | F6h     | N/A     | Fixed block code address 67h, size 4 bytes  |
|  | Fixed Block 5                 | F7h     | N/A     | Fixed block code address 6Eh, size 8 bytes  |
|  | Fixed Block 6                 | F8h     | N/A     | Fixed block code address 78h, size 12 bytes   |
|  | Fixed Block 7                 | F9h     | N/A     | Fixed block code address 90h, size 32 bytes   |
|  | Fixed Block 8                 | FAh     | N/A     | Fixed block code address B4h, size 8 bytes  |
|  | Fixed Block 9                 | FBh     | N/A     | Fixed block code address C8h, size 8 bytes  |
|  | Fixed Block 10                | FCh     | N/A     | Fixed block code address D0h, size 16 bytes   |
|  | Fixed Block 11                | FDh     | N/A     | Fixed block code address E5h, size 9 bytes  |

| Lock | Register Name | Address | Default | Description                  |
|------|---------------|---------|---------|------------------------------|
|      | Reserved      | FEh-FFh | N/A     | Reserved for future commands |

### 6.4.3 Factory Registers 00h–04h

#### 6.4.3.1 Register 00h XOR Test

| Register Address | Read/Write | Register Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|---------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 00h              | R/W        | XOR Test      | RES   |       |       |       |       |       |       | XEN   | 00h           |

| Bit | Name | R/W | Default | Description  | Sleep Masking |
|-----|------|-----|---------|--|---------------|
| 0   | XEN  | R/W | 0       | The LM94 incorporates an XOR tree test mode. When the test mode is enabled by setting this bit, the part enters XOR test mode. Clearing this bit brings the part out of XOR test mode. | N/A           |
| 7:1 | RES  | R   | 0       | Reserved   | N/A           |

#### 6.4.3.2 Register 01h SMBus Test

| Register Address | Read/Write | Register Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|---------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 01h              | R/W        | SMBus Test    | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |

This register can be used to verify that the SMBus can read and write to the device without effecting any programmed settings.

### 6.4.3.3 “REMOTE DIODE” MODE SELECT

#### 6.4.3.3.1 Register 05h Remote-Diode Transistor Mode Select

| Register Address | Read/Write | Register Name          | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3    | Bit 2    | Bit 1    | Bit 0    | Default Value |
|------------------|------------|------------------------|-------|-------|-------|-------|----------|----------|----------|----------|---------------|
| 05h              | R/W        | Transistor Mode Select | RES   | RES   | RES   | RES   | P2b_T_EN | P2a_T_EN | P1b_T_EN | P1a_T_EN | 00h           |

| Bit | Name     | R/W | Description   |
|-----|----------|-----|---|
| 0   | P1a_T_EN | R/W | If set, Processor 1 Remote-Diode “a” Transistor Mode enabled. |
| 1   | P1b_T_EN | R/W | If set, Processor 1 Remote-Diode “b” Transistor Mode enabled. |
| 2   | P2a_T_EN | R/W | If set, Processor 2 Remote-Diode “a” Transistor Mode enabled. |
| 3   | P2b_T_EN | R/W | If set, Processor 2 Remote-Diode “b” Transistor Mode enabled. |
| 7:4 | RES      | R   | Reserved  |

### 6.4.4 Value Registers Section 1

#### 6.4.4.1 Registers 06-07h and 50–53h Unfiltered Temperature Value Registers

| Register Address | Read/Write | Register Name       | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|---------------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 06h              | R          | Zone 1b (CPU1) Temp | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| 07h              | R          | Zone 2b (CPU2) Temp | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |

| Register Address | Read/Write | Register Name                  | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|--------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 50h              | R          | Zone 1a (CPU1) Temp            | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| 51h              | R          | Zone 2a (CPU2) Temp            | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| 52h              | R          | Zone 3 (Internal) Temp         | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| 53h              | R/W        | Zone 4 (External Digital) Temp | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |

Zones 1 and 2 are all automatically updated by the LM94. The Zone 3 (Internal) Temp and Zone 4 (External Digital) Temp registers may be written by an external SMBus device or can be assigned to AD\_IN11 and AD\_IN15, respectively.

The temperature registers for zones 1 and 2 will return a value of 80h if the remote diode pins are not implemented by the board designer or are not functioning properly.

#### 6.4.4.2 Registers 08–09h and 54–55h Filtered Temperature Value Registers

| Register Address | Read/Write | Register Name                | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 08h              | R          | Zone 1b (CPU1) Filtered Temp | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| 09h              | R          | Zone 2b (CPU2) Filtered Temp | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| 54h              | R          | Zone 1a (CPU1) Filtered Temp | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| 55h              | R          | Zone 2a (CPU2) Filtered Temp | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |

These registers reflect the temperature of zones 1 and 2 after the spike smoothing filter has been applied.

The characteristics of the filtering can be adjusted by using the Zones 1/2 Spike Smoothing Control register.

#### 6.4.4.3 Register 0Ah and 0Bh PWM1 and PWM2 8-bit Duty Cycle Value

| Register Address | Read/Write | Register Name         | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|-----------------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 0Ah              | R          | PWM1 Duty Cycle Value | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| 0Bh              | R          | PWM2 Duty Cycle Value | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |

These registers report the current duty cycle being driven on the PWM1 or PWM2 outputs. It is the upper 8 bits of the 9-bit PWM value. It reflects the maximum duty cycle of any low-resolution or high-resolution PWM sources bound to the PWM1 or PWM2 outputs.

### 6.4.5 PWM Duty Cycle Override Registers

#### 6.4.5.1 Register 0Ch PWM1 Duty Cycle Override (low byte)

| Register Address | Read/Write | Register Name                       | Bit 7      | Bit 6             | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|-------------------------------------|------------|-------------------|-------|-------|-------|-------|-------|-------|---------------|
| 0Ch              | R/W        | PWM1 Duty Cycle Override (low byte) | PWM1_DC[0] | PWM1_EN_Hres_Over | RES   | RES   | RES   | RES   | RES   | RES   | 00h           |

| Bit | Name              | R/W | Description   |
|-----|-------------------|-----|---|
| 5:0 | RES               | R   | Reserved  |
| 6   | PWM1_EN_Hres_Over | R/W | When this bit is set, high-resolution override for PWM1 is enabled. When this bit is set, PWM1 will run at the programmed duty cycle: PWM1_DC[8:0]/256 * 100%; values over 100h are reserved. |
| 7   | PWM1_DC[0]        | R/W | When this bit is set, bit [0] of the override duty cycle for PWM1 is set.   |

If manual PWM1 override is enabled in this register, all other PWM1 bindings are disabled except for the 100% override in the LM94 Status Control register (E2h).

#### 6.4.5.2 Register 0Dh PWM1 Duty Cycle Override (high byte)

| Register Address | Read/Write | Register Name                        | Bit 7        | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|--------------------------------------|--------------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 0Dh              | R/W        | PWM1 Duty Cycle Override (high byte) | PWM1_DC[8:1] | 00h   |       |       |       |       |       |       |               |

These bits set the upper 8-bits of the 9-bit override duty cycle value for PWM1.

#### 6.4.5.3 Register 0Eh PWM2 Duty Cycle Override (low byte)

| Register Address | Read/Write | Register Name                        | Bit 7      | Bit 6             | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|--------------------------------------|------------|-------------------|-------|-------|-------|-------|-------|-------|---------------|
| 0Eh              | R/W        | PWM 2 Duty Cycle Override (low byte) | PWM2_DC[0] | PWM2_EN_Hres_Over | RES   | RES   | RES   | RES   | RES   | RES   | 00h           |

| Bit | Name              | R/W | Description   |
|-----|-------------------|-----|---|
| 5:0 | RES               | R   | Reserved  |
| 6   | PWM2_EN_Hres_Over | R/W | When this bit is set, high-resolution override for PWM2 is enabled. When this bit is set, PWM2 will run at the programmed duty cycle: PWM2_DC[8:0]/256 * 100%; values over 100h are reserved. |
| 7   | PWM2_DC[0]        | R/W | When this bit is set, bit [0] of the override duty cycle for PWM2 is set.   |

If manual PWM 2 override is enabled in this register, all other PWM 2 bindings are disabled except for the 100% override in the LM94 Status Control register (E2h).

#### 6.4.5.4 Register 0Fh PWM2 Duty Cycle Override (high byte)

| Register Address | Read/Write | Register Name                        | Bit 7        | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|--------------------------------------|--------------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 0Fh              | R/W        | PWM2 Duty Cycle Override (high byte) | PWM2_DC[8:1] | 00h   |       |       |       |       |       |       |               |

These bits set the upper 8-bits of the 9-bit override duty cycle value for PWM2.

#### 6.4.6 Extended Resolution Value Registers

##### 6.4.6.1 Registers 10h - 17h Zone 1 (CPU1) and Zone 2 (CPU2) Extended Resolution Unfiltered Temperature Value Registers, Most and Least Significant Bytes

| Register Address | Read/Write | Register Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|---------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 10h              | R          | Z1a_LSB       | 0.5   | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 00h           |
| 11h              | R          | Z1a_MSB       | Sign  | 64    | 32    | 16    | 8     | 4     | 2     | 1     | 00h           |

Register 11h is a mirror of register Zone 1a (CPU1) Temp at address 50h.

| Register Address | Read/Write | Register Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|---------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 12h              | R          | Z1b_LSB       | 0.5   | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 00h           |
| 13h              | R          | Z1b_MSB       | Sign  | 64    | 32    | 16    | 8     | 4     | 2     | 1     | 00h           |

Register 13h is a mirror of register Zone 1b (CPU1) Temp at address 06h.

| Register Address | Read/Write | Register Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|---------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 14h              | R          | Z2a_LSB       | 0.5   | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 00h           |
| 15h              | R          | Z2a_MSB       | Sign  | 64    | 32    | 16    | 8     | 4     | 2     | 1     | 00h           |

Register 15h is a mirror of register Zone 2a (CPU2) Temp at address 51h.

| Register Address | Read/Write | Register Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|---------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 16h              | R          | Z2b_LSB       | 0.5   | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 00h           |
| 17h              | R          | Z2b_MSB       | Sign  | 64    | 32    | 16    | 8     | 4     | 2     | 1     | 00h           |

Register 17h is a mirror of register Zone 2b (CPU2) Temp at address 07h.

##### 6.4.6.2 Registers 18h – 1Fh Zone 1 (CPU1) and Zone 2 (CPU2) Extended Resolution Filtered Value Registers, Most and Least Significant Bytes

| Register Address | Read/Write | Register Name | Bit 7 | Bit 6 | Bit 5 | Bit 4  | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|---------------|-------|-------|-------|--------|-------|-------|-------|-------|---------------|
| 18h              | R          | Z1a_F_LSB     | 0.5   | 0.25  | 0.125 | 0.0625 | 0     | 0     | 0     | 0     | 00h           |
| 19h              | R          | Z1a_F_MSB     | Sign  | 64    | 32    | 16     | 8     | 4     | 2     | 1     | 00h           |

Register 19h is a mirror of register Zone 1a (CPU1) Filtered Temp at address 54h.

| Register Address | Read/Write | Register Name | Bit 7 | Bit 6 | Bit 5 | Bit 4  | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|---------------|-------|-------|-------|--------|-------|-------|-------|-------|---------------|
| 1Ah              | R          | Z1b_F_LSB     | 0.5   | 0.25  | 0.125 | 0.0625 | 0     | 0     | 0     | 0     | 00h           |
| 1Bh              | R          | Z1b_F_MSB     | Sign  | 64    | 32    | 16     | 8     | 4     | 2     | 1     | 00h           |

Register 1Bh is a mirror of register Zone 1b (CPU1) Filtered Temp at address 08h.

| Register Address | Read/Write | Register Name | Bit 7 | Bit 6 | Bit 5 | Bit 4  | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|---------------|-------|-------|-------|--------|-------|-------|-------|-------|---------------|
| 1Ch              | R          | Z2a_F_LSB     | 0.5   | 0.25  | 0.125 | 0.0625 | 0     | 0     | 0     | 0     | 00h           |

| Register Address | Read/Write | Register Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|---------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 1Dh              | R          | Z2a_F_MSB     | Sign  | 64    | 32    | 16    | 8     | 4     | 2     | 1     | 00h           |

Register 1Dh is a mirror of register Zone 2a (CPU2) Filtered Temp at address 55h.

| Register Address | Read/Write | Register Name | Bit 7 | Bit 6 | Bit 5 | Bit 4  | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|---------------|-------|-------|-------|--------|-------|-------|-------|-------|---------------|
| 1Eh              | R          | Z2b_F_LSB     | 0.5   | 0.25  | 0.125 | 0.0625 | 0     | 0     | 0     | 0     | 00h           |
| 1Fh              | R          | Z2b_F_MSB     | Sign  | 64    | 32    | 16     | 8     | 4     | 2     | 1     | 00h           |

Register 1Fh is a mirror of register Zone 2b (CPU2) Filtered Temp at address 09h.

#### 6.4.6.3 Registers 20h – 23h Zone 3 and Zone 4 Extended Resolution Value Registers, Most and Least Significant Bytes

| Register Address | Read/Write | Register Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|---------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 20h              | R/W        | Z3_LSB        | 0.5   | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 00h           |
| 21h              | R/W        | Z3_MSB        | Sign  | 64    | 32    | 16    | 8     | 4     | 2     | 1     | 00h           |

Register 21h is a mirror of register Zone 3 (Internal) Temp at address 52h.

| Register Address | Read/Write | Register Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|---------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 22h              | R/W        | Z4_LSB        | 0.5   | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 00h           |
| 23h              | R/W        | Z4_MSB        | Sign  | 64    | 32    | 16    | 8     | 4     | 2     | 1     | 00h           |

Register 23h is a mirror of register Zone 4 (External Digital) Temp at address 53h.

### 6.4.7 PI Loop Fan Control Setup Registers

#### 6.4.7.1 Register 31h Internal/External Temperature Source Select

| Register Address | Read/Write | Register Name                                | Bit 7 | Bit 6 | Bit 5 | Bit 4    | Bit 3 | Bit 2 | Bit 1    | Bit 0    | Default Value |
|------------------|------------|--|-------|-------|-------|----------|-------|-------|----------|----------|---------------|
| 31h              | R/W        | Internal/ External Temperature Source Select | RES   | RES   | RES   | INT_WR_E | Z2bE  | Z1bE  | EXT_AD15 | INT_AD11 | 00h           |

| Bit | Name      | R/W | Description  |
|-----|-----------|-----|--|
| 0   | INT_ADC11 | R/W | When this bit is set, the Internal Temperature Register (Zone 3) will be automatically updated with the value from the ADC_IN11 Voltage Value register minus 128 by inverting the MSb. Subtraction of 128 or inverting the MSb is required since the data in the temperature register is a signed value. When this bit is cleared the Internal Temperature Register (Zone 3) will be automatically updated with the internal temperature reading from the LM94's internal thermal diode. All functions related to the Internal Temperature Register value are affected by this bit (LUTs, Temperature Boost, etc.) |
| 1   | EXT_ADC15 | R/W | When this bit is set, the External Digital Temperature register (Zone 4) will become read-only and will be automatically updated from the ADC_IN15 Voltage Value register minus 128 by inverting the MSb. Subtraction of 128 or inverting the MSb is required since the data in the temperature registers are signed. When this bit is cleared the External Digital Temperature register is writable and must be updated over the SMBus by software. All functions related to the External Digital Temperature register are affected by this bit (LUTs, Temperature Boost, etc.)                                   |
| 2   | Z1bE      | R/W | When this bit is set, pin 23 is enabled as a Remote 1b input. When this bit is cleared pin 23 is set as a AD_IN1 input.  |

| Bit | Name     | R/W | Description   |
|-----|----------|-----|---|
| 3   | Z2bE     | R/W | When this bit is set, pin 24 is enabled as a Remote 2b input. When this bit is cleared pin 24 is set as a AD_IN2 input.   |
| 4   | INT_WR_E | R/W | When this bit is set, the Internal Temperature Value register may be updated by an external SMBus write. All automatic updates of the Internal Temperature Value register will cease. |
| 7:3 | RES      | R   | Reserved  |

#### 6.4.7.2 Register 32h PWM Filter Settings

| Register Address | Read/Write | Register Name | Bit 7 | Bit 6        | Bit 5 | Bit 4        | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|---------------|-------|--------------|-------|--------------|-------|-------|-------|-------|---------------|
| 32h              | R/W        | PWM_Filter    | RES   | FC_PWM2[2:0] | RES   | FC_PWM1[2:0] |       |       | 00h   |       |               |

| Bit | Name         | R/W | Description  |
|-----|--------------|-----|--|
| 2:0 | FC_PWM1[2:0] | R/W | Sets the filter coefficient for the IIR filter on PWM1 low resolution sources. |
| 3   | RES          | R   | Reserved   |
| 6:4 | FC_PWM2[2:0] | R/W | Sets the filter coefficient for the IIR filter on PWM2 low resolution sources. |
| 7   | RES          | R   | Reserved   |

| FC_PWM1[2:0] or FC_PWM2[2:] | 95% Settling Time Interval |
|-----------------------------|----------------------------|
| 000                         | Filter bypassed            |
| 001                         | 0.098s                     |
| 010                         | 0.237s                     |
| 011                         | 0.510s                     |
| 100                         | 1.056s                     |
| 101                         | 2.147s                     |
| 110                         | 4.328s                     |
| 111                         | 8.689s                     |

#### 6.4.7.3 Register 33h PWM1 Filter Shutoff Threshold

| Register Address | Read/Write | Register Name           | Bit 7             | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|-------------------------|-------------------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 33h              | R/W        | PWM1_Filter Shut_Thresh | PWM1_SHUT_DC[4:0] | RES   | RES   | RES   | 00h   |       |       |       |               |

| Bit | Name              | R/W | Description   |
|-----|-------------------|-----|---|
| 2:0 | RES               | R   | Reserved  |
| 7:3 | PWM1_SHUT_DC[4:0] | R/W | Sets the filter shutoff threshold. The actual duty cycle threshold is 3.15% times this value. If the PWM filter is disabled the shutdown threshold is also disabled. The shutdown threshold allows the PWM1 output to be turned off for duty cycles less than the programmed value. |

| Bit [7:3] | 9-bit Threshold | Corresponding Duty Cycle |
|-----------|-----------------|--------------------------|
| 0         | 0               | 0.000%                   |
| 1         | 8               | 3.125%                   |
| 2         | 16              | 6.25%                    |
| ·         | ·               | ·                        |
| ·         | ·               | ·                        |
| 29        | 232             | 90.625%                  |

| Bit [7:3] | 9-bit Threshold | Corresponding Duty Cycle |
|-----------|-----------------|--------------------------|
| 30        | 240             | 93.750%                  |
| 31        | 248             | 96.875%                  |

#### 6.4.7.4 Register 34h PWM2 Filter Shutoff Threshold

| Register Address | Read/Write | Register Name           | Bit 7             | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|-------------------------|-------------------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 34h              | R/W        | PWM2_Filter Shut_Thresh | PWM2_SHUT_DC[4:0] | RES   | RES   | RES   | 00h   |       |       |       |               |

| Bit | Name              | R/W | Description   |
|-----|-------------------|-----|---|
| 2:0 | RES               | R   | Reserved  |
| 7:3 | PWM2_SHUT_DC[4:0] | R/W | Sets the filter shutoff threshold. The actual duty cycle threshold is 3.15% times this value. If the PWM filter is disabled the shutdown threshold is also disabled. The shutdown threshold allows the PWM1 output to be turned off for duty cycles less than the programmed value. |

| Bit [7:3] | 9-bit Threshold | Corresponding Duty Cycle |
|-----------|-----------------|--------------------------|
| 0         | 0               | 0.000%                   |
| 1         | 8               | 3.125%                   |
| 2         | 16              | 6.25%                    |
| ·         | ·               | ·                        |
| ·         | ·               | ·                        |
| 29        | 232             | 90.625%                  |
| 30        | 240             | 93.750%                  |
| 31        | 248             | 96.875%                  |

#### 6.4.7.5 Register 35h PI/LUT Fan Control Bindings

| Register Address | Read/Write | Register Name        | Bit 7   | Bit 6   | Bit 5   | Bit 4   | Bit 3   | Bit 2   | Bit 1 | Bit 0 | Default Value |
|------------------|------------|----------------------|---------|---------|---------|---------|---------|---------|-------|-------|---------------|
| 35h              | R/W        | Fan Control Bindings | LUT4_Z2 | LUT3_Z1 | LUT2_Z2 | LUT1_Z1 | PWM2_PI | PWM1_PI | PI_Z2 | PI_Z1 | 30h           |

| Bit | Name    | R/W | Description   |
|-----|---------|-----|---|
| 0   | PI_Z1   | R/W | When this bit is set, the PI controller is bound to the P1 temperature (zone 1). This also changes the available filtering options for the P1 temperature.      |
| 1   | PI_Z2   | R/W | When this bit is set, the PI controller is bound to the P2 temperature (zone 2). This also changes the available filtering options for the P2 temperature zone. |
| 2   | PWM1_PI | R/W | When this bit is set, the PWM1 output is bound to the PI controller.  |
| 3   | PWM2_PI | R/W | When this bit is set, the PWM2 output is bound to the PI controller.  |
| 4   | LUT1_Z1 | R/W | When this bit is set, LUT1 will use the P1 temperature (zone 1) instead of the Internal temperature (zone 3).   |
| 5   | LUT2_Z2 | R/W | When this bit is set, LUT2 will use the P2 temperature (zone2) instead of the External Digital temperature (zone 4).  |
| 6   | LUT3_Z1 | R/W | When this bit is set, LUT3 will use the P1 temperature (zone1) instead of the Internal temperature (zone 3).  |
| 7   | LUT4_Z2 | R/W | When this bit is set, LUT4 will use the P2 temperature (zone 2) instead of the External Digital temperature (zone 4).   |

### 6.4.7.6 Register 36h PI Controller Minimum PWM and Hysteresis

| Register Address | Read/Write | Register Name      | Bit 7          | Bit 6        | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|--------------------|----------------|--------------|-------|-------|-------|-------|-------|-------|---------------|
| 36h              | R/W        | PI MinPWM and Hyst | PI_MinPWM[3:0] | PI_Hyst[3:0] |       |       | 00h   |       |       |       |               |

| Bit | Name           | R/W | Description  |
|-----|----------------|-----|--|
| 3:0 | PI_Hyst[3:0]   | R/W | Sets the hysteresis for the PI Loop fan controller in 0.5°C steps up to 7.5°C.             |
| 7:4 | PI_MinPWM[3:0] | R/W | Defines the minimum PWM output for the PI Loop fan controller in 6.25% steps up to 93.75%. |

| PI_Hyst[3:0] | Hysteresis (°C) |
|--------------|-----------------|
| 0h           | 0               |
| 1h           | 0.5             |
| 2h           | 1.0             |
| 3h           | 1.5             |
| 4h           | 2.0             |
| 5h           | 2.5             |
| 6h           | 3.0             |
| 7h           | 3.5             |
| 8h           | 4.0             |
| 9h           | 4.5             |
| Ah           | 5.0             |
| Bh           | 5.5             |
| Ch           | 6.0             |
| Dh           | 6.5             |
| Eh           | 7.0             |
| Fh           | 7.5             |

| PI_MinPWM[3:0] | Minimum Duty Cycle |
|----------------|--------------------|
| 0h             | 0.00%              |
| 1h             | 6.25%              |
| 2h             | 12.5%              |
| 3h             | 18.75%             |
| 4h             | 25.00%             |
| 5h             | 31.25%             |
| 6h             | 37.50%             |
| 7h             | 43.75%             |
| 8h             | 50.00%             |
| 9h             | 56.25%             |
| Ah             | 62.50%             |
| Bh             | 68.75%             |
| Ch             | 75.00%             |
| Dh             | 81.25%             |
| Eh             | 87.5%              |
| Fh             | 93.75%             |

#### 6.4.7.7 Registers 37h and 38h Zone 1 and 2 PI Controller Target Temperature (Tcontrol)

| Register Address | Read/Write | Register Name   | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|-----------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 37h              | R/W        | Zone 1 Tcontrol | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| 38h              | R/W        | Zone 2 Tcontrol | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |

Same format as temperature value register for Zone 1 and Zone 2. The PWM output controls the airflow over the processors and thus the temperature of the processors is adjusted by the PI loop to maintain the hottest Zone 1 or Zone 2 temperature reading between their respective values for Tcontrol and Tcontrol - hysteresis. Intel specifies an optimum Tcontrol temperature for some of it's processors that can be found in the MSR register space.

#### 6.4.7.8 Register 39h and 3Ah Zone 1 and 2 PI Fan Control Off Temperature (Toff)

| Register Address | Read/Write | Register Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|---------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 39h              | R/W        | Z1 Toff       | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 80h           |
| 3Ah              | R/W        | Z2 Toff       | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 80h           |

Same format as temperature value register for Zone 1 and Zone 2. When these registers are set to 80h, the Toff function is disabled. Toff is the temperature at which the PI control loop output is forced to zero duty cycle.

#### 6.4.7.9 Register 3Bh Proportional Coefficient

| Register Address | Read/Write | Register Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|---------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 3Bh              | R/W        | P Coefficient | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |

#### 6.4.7.10 Register 3Ch Integral Coefficient

| Register Address | Read/Write | Register Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|---------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 3Ch              | R/W        | I Coefficient | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |

#### 6.4.7.11 Register 3Dh PI Coefficient Exponents

| Register Address | Read/Write | Register Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3    | Bit 2    | Bit 1 | Bit 0 | Default Value |
|------------------|------------|---------------|-------|-------|-------|-------|----------|----------|-------|-------|---------------|
| 3Dh              | R/W        | PI Exponents  | RES   | RES   | RES   | RES   | PCE[1:0] | ICE[1:0] |       | 00h   |               |

| Bit | Name     | R/W | Description  |
|-----|----------|-----|--|
| 1:0 | ICE[1:0] | R/W | PI controller integral coefficient exponent (2-bit signed value)     |
| 2:3 | PCE[1:0] | R/W | PI controller proportional coefficient exponent (2-bit signed value) |
| 7:4 | RES      | R   | Reserved   |

| ICE[1:0] | Integral Exponent |
|----------|-------------------|
| 10b      | -2                |
| 11b      | -1                |
| 00b      | 0                 |
| 01b      | 1                 |

| PCE[1:0] | Proportional Exponent |
|----------|-----------------------|
| 10b      | -2                    |
| 11b      | -1                    |

| PCE[1:0] | Proportional Exponent |
|----------|-----------------------|
| 00b      | 0                     |
| 01b      | 1                     |

## 6.4.8 Device Identification Registers (3Eh-3Fh)

### 6.4.8.1 Register 3Eh Manufacturer ID

| Register Address | Read/Write | Register Name   | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|-----------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 3Eh              | R          | Manufacturer ID | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 01h           |

The Manufacturer ID register contains the manufacturer identification number. This number is assigned by Texas Instruments and is a method for uniquely identifying the part manufacturer.

### 6.4.8.2 Register 3Fh Version/Stepping

| Register Address | Read/Write | Register Name    | Bit 7    | Bit 6 | Bit 5 | Bit 4 | Bit 3    | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|------------------|----------|-------|-------|-------|----------|-------|-------|-------|---------------|
| 3Fh              | R          | Version/Stepping | VER[3:0] |       |       |       | STP[3:0] |       |       |       | 79h           |
|                  |            |                  | 0        | 1     | 1     | 1     | 1        | 0     | 0     | 1     |               |

The four least significant bits of the Version/Stepping register [3:0] contain the current stepping of the LM94 silicon. The four most significant bits [7:4] reflect the LM94 version number. The LM94 has a fixed version number of 0111b which matches the LM93, since the LM94 is closely related to the LM93. To differentiate the LM94 from the LM93 for the first stepping of LM94 this register reads 01111000b. For the second stepping of the LM94, this register reads 01111001b and so on. It is incrementally increased for future versions for the silicon. The final released silicon has a stepping of 9h therefore this register reads 79h.

The register is used by application software to identify which device in the family of hardware monitoring ASICs has been implemented in the given system. Based on this information, software can determine which registers to read from and write to. Application software may use the current stepping to implement work-a-rounds for bugs found in a specific silicon stepping.

## 6.4.9 BMC Error Status Registers 40h–47h

The B\_Error Status Registers contain several bits that each represent a particular error event that the LM94 can monitor. The LM94 sets a given bit whenever the corresponding error event occurs. The BMC\_ERR bit in the LM94 Status/Control register is also set if any bit in the BMC Error Status registers is set. If enabled, ALERT is also asserted anytime BMC\_ERR is set. The exception to this is the fixed threshold error status bits in the PROCHOT Error Status registers. They have no influence on BMC\_ERR or ALERT.

Once a bit is set in the BMC Error Status registers, it is not automatically cleared by the LM94 if the error event goes away. Each bit must be cleared by software. If software attempts to clear a bit while the error condition still exists, and the error is unmasked, the bit does not clear. If the error is masked, the bit can be cleared even if the error condition still exists.

If the LM94 is in ASF mode, the BMC Error Status registers are both read-to-clear and write-one-to-clear. When not in ASF mode, the registers are only write-one-to-clear.

Each register described in this section has a column labeled **Sleep Masking**. This column describes which error events are masked in various sleep states. The sleep state of the system is communicated to the LM94 by writing to the Sleep State Control register. If a sleep state in this column has a "\*" next to it, it denotes that the error event is optionally masked in that sleep mode, depending on the Sleep State Mask registers.

### 6.4.9.1 Register 40h B\_Error Status 1

| Register Address | Read/Write | Register Name    | Bit 7 | Bit 6 | Bit 5    | Bit 4    | Bit 3   | Bit 2   | Bit 1   | Bit 0   | Default Value |
|------------------|------------|------------------|-------|-------|----------|----------|---------|---------|---------|---------|---------------|
| 40h              | RWC        | B_Error Status 1 | RES   |       | VRD2_ERR | VRD1_ERR | ZN4_ERR | ZN3_ERR | ZN2_ERR | ZN1_ERR | 00h           |

| Bit | Name     | R/W | Description   | Sleep Masking |
|-----|----------|-----|---|---------------|
| 0   | ZN1_ERR  | RWC | This bit is set when any zone 1 temperature has fallen outside its associated temperature limits. | S3*, S4/5*    |
| 1   | ZN2_ERR  | RWC | This bit is set when any zone 2 temperature has fallen outside its associated temperature limits. | S3*, S4/5*    |
| 2   | ZN3_ERR  | RWC | This bit is set when the zone 3 temperature has fallen outside the zone 3 temperature limits.     | none          |
| 3   | ZN4_ERR  | RWC | This bit is set when the zone 4 temperature has fallen outside the zone 4 temperature limits.     | none          |
| 4   | VRD1_ERR | RWC | This bit is set when the $\overline{\text{VRD1\_HOT}}$ input has been asserted.                   | S3, S4/5      |
| 5   | VRD2_ERR | RWC | This bit is set when the $\overline{\text{VRD2\_HOT\#}}$ input has been asserted.                 | S3, S4/5      |
| 7:6 | RES      | R   | Reserved  | N/A           |

### 6.4.9.2 Register 41h B\_Error Status 2

| Register Address | Read/Write | Register Name    | Bit 7     | Bit 6     | Bit 5     | Bit 4     | Bit 3     | Bit 2     | Bit 1     | Bit 0     | Default Value |
|------------------|------------|------------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|---------------|
| 41h              | RWC        | B_Error Status 2 | ADIN8_ERR | ADIN7_ERR | ADIN6_ERR | ADIN5_ERR | ADIN4_ERR | ADIN3_ERR | ADIN2_ERR | ADIN1_ERR | 00h           |

| Bit | Name    | R/W | Description   | Sleep Masking |
|-----|---------|-----|---|---------------|
| 0   | AD1_ERR | RWC | This bit is set when the AD_IN1 voltage has fallen outside the range defined by the AD_IN1 Low Limit and the AD_IN1 High Limit registers. | S3, S4/5      |
| 1   | AD2_ERR | RWC | This bit is set when the AD_IN2 voltage has fallen outside the range defined by the AD_IN2 Low Limit and the AD_IN2 High Limit registers. | S3, S4/5      |
| 2   | AD3_ERR | RWC | This bit is set when the AD_IN3 voltage has fallen outside the range defined by the AD_IN3 Low Limit and the AD_IN3 High Limit registers. | S3, S4/5      |
| 3   | AD4_ERR | RWC | This bit is set when the AD_IN4 voltage has fallen outside the range defined by the AD_IN4 Low Limit and the AD_IN4 High Limit registers. | S3, S4/5      |
| 4   | AD5_ERR | RWC | This bit is set when the AD_IN5 voltage has fallen outside the range defined by the AD_IN5 Low Limit and the AD_IN5 High Limit registers. | S3, S4/5      |
| 5   | AD6_ERR | RWC | This bit is set when the AD_IN6 voltage has fallen outside the range defined by the AD_IN6 Low Limit and the AD_IN6 High Limit registers. | S3, S4/5      |
| 6   | AD7_ERR | RWC | This bit is set when the AD_IN7 voltage has fallen outside the range defined by the AD_IN7 Low Limit and the AD_IN7 High Limit registers. | S3, S4/5      |
| 7   | AD8_ERR | RWC | This bit is set when the AD_IN8 voltage has fallen outside the range defined by the AD_IN8 Low Limit and the AD_IN8 High Limit registers. | S3, S4/5      |

### 6.4.9.3 Register 42h B\_Error Status 3

| Register Address | Read/Write | Register Name    | Bit 7      | Bit 6      | Bit 5      | Bit 4      | Bit 3      | Bit 2      | Bit 1      | Bit 0     | Default Value |
|------------------|------------|------------------|------------|------------|------------|------------|------------|------------|------------|-----------|---------------|
| 42h              | RWC        | B_Error Status 3 | ADIN16_ERR | ADIN15_ERR | ADIN14_ERR | ADIN13_ERR | ADIN12_ERR | ADIN11_ERR | ADIN10_ERR | ADIN9_ERR | 00h           |

| Bit | Name     | R/W | Description  | Sleep Masking |
|-----|----------|-----|--|---------------|
| 0   | AD9_ERR  | RWC | This bit is set when the AD_IN9 voltage has fallen outside the range defined by the AD_IN9 Low Limit and the AD_IN9 High Limit registers.    | S3, S4/5      |
| 1   | AD10_ERR | RWC | This bit is set when the AD_IN10 voltage has fallen outside the range defined by the AD_IN10 Low Limit and the AD_IN10 High Limit registers. | S3, S4/5      |
| 2   | AD11_ERR | RWC | This bit is set when the AD_IN11 voltage has fallen outside the range defined by the AD_IN11 Low Limit and the AD_IN11 High Limit registers. | S3, S4/5      |
| 3   | AD12_ERR | RWC | This bit is set when the AD_IN12 voltage has fallen outside the range defined by the AD_IN12 Low Limit and the AD_IN12 High Limit registers. | S3*, S4/5*    |
| 4   | AD13_ERR | RWC | This bit is set when the AD_IN13 voltage has fallen outside the range defined by the AD_IN13 Low Limit and the AD_IN13 High Limit registers. | S3*, S4/5*    |
| 5   | AD14_ERR | RWC | This bit is set when the AD_IN14 voltage has fallen outside the range defined by the AD_IN14 Low Limit and the AD_IN14 High Limit registers. | S3*, S4/5*    |
| 6   | AD15_ERR | RWC | This bit is set when the AD_IN15 voltage has fallen outside the range defined by the AD_IN15 Low Limit and the AD_IN15 High Limit registers. | S3, S4/5      |
| 7   | AD16_ERR | RWC | This bit is set when the AD_IN16 voltage has fallen outside the range defined by the AD_IN16 Low Limit and the AD_IN16 High Limit registers. | none          |

#### 6.4.9.4 Register 43h B\_Error Status 4

| Register Address | Read/Write | Register Name    | Bit 7   | Bit 6   | Bit 5                   | Bit 4                   | Bit 3    | Bit 2    | Bit 1   | Bit 0   | Default Value |
|------------------|------------|------------------|---------|---------|-------------------------|-------------------------|----------|----------|---------|---------|---------------|
| 43h              | RWC        | B_Error Status 4 | D2a_ERR | D1a_ERR | DV <sub>DD</sub> P2_ERR | DV <sub>DD</sub> P1_ERR | GPI9_ERR | GPI8_ERR | D2b_ERR | D1b_ERR | 00h           |

| Bit | Name                    | R/W | Description  | Sleep Masking |
|-----|-------------------------|-----|--|---------------|
| 0   | D1b_ERR                 | RWC | Diode Fault Error<br>This bit is set if there is an open or short circuit on the REMOTE1b+ and REMOTE1- pins.                    | S3*, S4/5*    |
| 1   | D2b_ERR                 | RWC | Diode Fault Error<br>This bit is set if there is an open or short circuit on the REMOTE2b+ and REMOTE2- pins.                    | S3*, S4/5*    |
| 2   | GPI8                    | RWC | SCSI Fuse Error<br>This bit is set if GPI8 has been asserted. Enabled only when VID mode is set to VRD 10.                       | S3, S4/5      |
| 3   | GPI9                    | RWC | SCSI Fuse Error<br>This bit is set if GPI9 has been asserted. Enabled only when VID mode is set to VRD 10.                       | S3, S4/5      |
| 4   | DV <sub>DD</sub> P1_ERR | RWC | Dynamic Vccp Limit Error.<br>This bit is set if AD_IN7 (P1_Vccp) did not match the requested voltage as reported by P1_VID[7:0]. | S3, S4/5      |
| 5   | DV <sub>DD</sub> P2_ERR | RWC | Dynamic Vccp Limit Error.<br>This bit is set if AD_IN8 (P2_Vccp) did not match the requested voltage as reported by P1_VID[7:0]. | S3, S4/5      |
| 6   | D1a_ERR                 | RWC | Diode Fault Error<br>This bit is set if there is an open or short circuit on the REMOTE1a+ and REMOTE1- pins.                    | S3*, S4/5*    |
| 7   | D2a_ERR                 | RWC | Diode Fault Error<br>This bit is set if there is an open or short circuit on the REMOTE2a+ and REMOTE2- pins.                    | S3*, S4/5*    |

### 6.4.9.5 Register 44h B\_P1\_PROCHOT Error Status

| Register Address | Read/Write | Register Name             | Bit 7   | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|---------------------------|---------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 44h              | RWC        | B_P1_PROCHOT Error Status | PH1_ERR | TMAX  | T100  | T75   | T50   | T25   | T12   | T0    | 00h           |

| Bit | Name    | R/W | Description   | Sleep Masking |
|-----|---------|-----|---|---------------|
| 0   | T0      | RWC | Set when $\overline{P1\_PROCHOT}$ has had a throttled event. This bit is set for any amount of $\overline{PROCHOT}$ throttling >0%. | S3, S4/5      |
| 1   | T12     | RWC | Set when $\overline{P1\_PROCHOT}$ has throttled greater than or equal to 0.39% but less than 12.5%.                                 | S3, S4/5      |
| 2   | T25     | RWC | Set when $\overline{P1\_PROCHOT}$ has throttled greater than or equal to 12.5% but less than 25%.                                   | S3, S4/5      |
| 3   | T50     | RWC | Set when $\overline{P1\_PROCHOT}$ has throttled greater than or equal to 25% but less than 50%.                                     | S3, S4/5      |
| 4   | T75     | RWC | Set when $\overline{P1\_PROCHOT}$ has throttled greater than or equal to 50% but less than 75%.                                     | S3, S4/5      |
| 5   | T100    | RWC | Set when $\overline{P1\_PROCHOT}$ has throttled greater than or equal to 75% but less than 100%.                                    | S3, S4/5      |
| 6   | TMAX    | RWC | Set when $\overline{P1\_PROCHOT}$ has throttled 100%.   | S3, S4/5      |
| 7   | PH1_ERR | RWC | Set when $\overline{P1\_PROCHOT}$ has throttled more than the user limit.   | S3, S4/5      |

The PH1\_ERR bit is the only bit in this register that will set BMC\_ERR in the LM94 Status/Control register.

### 6.4.9.6 Register 45h B\_P2\_PROCHOT Error Status

| Register Address | Read/Write | Register Name             | Bit 7   | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|---------------------------|---------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 45h              | RWC        | B_P2_PROCHOT Error Status | PH2_ERR | TMAX  | T100  | T75   | T50   | T25   | T12   | T0    | 00h           |

| Bit | Name    | R/W | Description   | Sleep Masking |
|-----|---------|-----|---|---------------|
| 0   | T0      | RWC | Set when $\overline{P2\_PROCHOT}$ has had a throttled event. This bit is set for any amount of $\overline{PROCHOT}$ throttling >0%. | S3, S4/5      |
| 1   | T12     | RWC | Set when $\overline{P2\_PROCHOT}$ has throttled greater than or equal to 0.0% but less than 12.5%.                                  | S3, S4/5      |
| 2   | T25     | RWC | Set when $\overline{P2\_PROCHOT}$ has throttled greater than or equal to 12.5% but less than 25%.                                   | S3, S4/5      |
| 3   | T50     | RWC | Set when $\overline{P2\_PROCHOT}$ has throttled greater than or equal to 25% but less than 50%.                                     | S3, S4/5      |
| 4   | T75     | RWC | Set when $\overline{P2\_PROCHOT}$ has throttled greater than or equal to 50% but less than 75%.                                     | S3, S4/5      |
| 5   | T100    | RWC | Set when $\overline{P2\_PROCHOT}$ has throttled greater than or equal to 75% but less than 100%.                                    | S3, S4/5      |
| 6   | TMAX    | RWC | Set when $\overline{P2\_PROCHOT}$ has throttled 100%.   | S3, S4/5      |
| 7   | PH2_ERR | RWC | Set when $\overline{P2\_PROCHOT}$ has throttled more than the user limit.   | S3, S4/5      |

The PH2\_ERR bit is the only bit in this register that will set BMC\_ERR in the LM94 Status/Control register.

### 6.4.9.7 Register 46h B\_GPI Error Status

| Register Address | Read/Write | Register Name      | Bit 7    | Bit 6    | Bit 5    | Bit 4    | Bit 3    | Bit 2    | Bit 1    | Bit 0    | Default Value |
|------------------|------------|--------------------|----------|----------|----------|----------|----------|----------|----------|----------|---------------|
| 46h              | RWC        | B_GPI Error Status | GPI7_ERR | GPI6_ERR | GPI5_ERR | GPI4_ERR | GPI3_ERR | GPI2_ERR | GPI1_ERR | GPI0_ERR | 00h           |

| Bit | Name     | R/W | Description   | Sleep Masking   |
|-----|----------|-----|---|-----------------|
| 0   | GPI0_ERR | RWC | This bit is set whenever GPIO0 is driven low (unless masked via the GPI Error Mask register). | S1*, S3*, S4/5* |
| 1   | GPI1_ERR | RWC | This bit is set whenever GPIO1 is driven low (unless masked via the GPI Error Mask register). | S1*, S3*, S4/5* |
| 2   | GPI2_ERR | RWC | This bit is set whenever GPIO2 is driven low (unless masked via the GPI Error Mask register). | S1*, S3*, S4/5* |
| 3   | GPI3_ERR | RWC | This bit is set whenever GPIO3 is driven low (unless masked via the GPI Error Mask register). | S1*, S3*, S4/5* |
| 4   | GPI4_ERR | RWC | This bit is set whenever GPIO4 is driven low (unless masked via the GPI Error Mask register). | S1*, S3*, S4/5* |
| 5   | GPI5_ERR | RWC | This bit is set whenever GPIO5 is driven low (unless masked via the GPI Error Mask register). | S1*, S3*, S4/5* |
| 6   | GPI6_ERR | RWC | This bit is set whenever GPIO6 is driven low (unless masked via the GPI Error Mask register). | S1*, S3*, S4/5* |
| 7   | GPI7_ERR | RWC | This bit is set whenever GPIO7 is driven low (unless masked via the GPI Error Mask register). | S1*, S3*, S4/5* |

### 6.4.9.8 Register 47h B\_Fan Error Status

| Register Address | Read/Write | Register Name      | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3    | Bit 2    | Bit 1    | Bit 0    | Default Value |
|------------------|------------|--------------------|-------|-------|-------|-------|----------|----------|----------|----------|---------------|
| 47h              | RWC        | B_Fan Error Status | RES   |       |       |       | FAN4_ERR | FAN3_ERR | FAN2_ERR | FAN1_ERR | 00h           |

| Bit | Name     | R/W | Description   | Sleep Masking  |
|-----|----------|-----|---|----------------|
| 0   | FAN1_ERR | RWC | This bit is set when the Fan Tach 1 value register is above the value set in the Fan Tach 1 Limit register. | S1*, S3*, S4/5 |
| 1   | FAN2_ERR | RWC | This bit is set when the Fan Tach 2 value register is above the value set in the Fan Tach 2 Limit register. | S1*, S3*, S4/5 |
| 2   | FAN3_ERR | RWC | This bit is set when the Fan Tach 3 value register is above the value set in the Fan Tach 3 Limit register. | S1*, S3*, S4/5 |
| 3   | FAN4_ERR | RWC | This bit is set when the Fan Tach 4 value register is above the value set in the Fan Tach 4 Limit register. | S1*, S3*, S4/5 |
| 7:4 | RES      | R   | Reserved  | N/A            |

### 6.4.10 Host Error Status Registers

The Host Error Status Registers contain several bits that each represent a particular error event that the LM94 can monitor. The LM94 sets a given bit whenever the corresponding error event occurs. The HOST\_ERR bit in the LM94 Status/Control register also sets if any bit in the Host Error Status registers is set. The exception to this is the fixed threshold error status bits in the PROCHOT Error Status registers. They have no influence on HOST\_ERR.

Once a bit is set in the Host Error Status registers, it is not automatically cleared by the LM94 if the error event goes away. Each bit must be cleared by software. If software attempts to clear a bit while the error condition still exists, the bit does not clear.

Software must specifically write a 1 to any bits it wishes to clear in the Host Error Status registers (write-one-to-clear).

Each register described in this section has a column labeled **Sleep Masking**. This column describes which error events are masked in various sleep states. The sleep state of the system is communicated to the LM94 by writing to the Sleep State Control register. If a sleep state in this column has a "\*" next to it, it denotes that the error event is optionally masked in that sleep mode, depending on the Sleep State Mask registers.

#### 6.4.10.1 Register 48h H\_Error Status 1

| Register Address | Read/Write | Register Name    | Bit 7 | Bit 6 | Bit 5    | Bit 4    | Bit 3   | Bit 2   | Bit 1   | Bit 0   | Default Value |
|------------------|------------|------------------|-------|-------|----------|----------|---------|---------|---------|---------|---------------|
| 48h              | RWC        | H_Error Status 1 | RES   |       | VRD2_ERR | VRD1_ERR | ZN4_ERR | ZN3_ERR | ZN2_ERR | ZN1_ERR | 00h           |

| Bit | Name     | R/W | Description   | Sleep Masking |
|-----|----------|-----|---|---------------|
| 0   | ZN1_ERR  | RWC | This bit is set when any zone 1 temperature has fallen outside its associated temperature limits. | S3*, S4/5*    |
| 1   | ZN2_ERR  | RWC | This bit is set when any zone 2 temperature has fallen outside its associated temperature limits. | S3*, S4/5*    |
| 2   | ZN3_ERR  | RWC | This bit is set when the zone 3 temperature has fallen outside the zone 3 temperature limits.     | none          |
| 3   | ZN4_ERR  | RWC | This bit is set when the zone 4 temperature has fallen outside the zone 4 temperature limits.     | none          |
| 4   | VRD1_ERR | RWC | This bit is set when the $\overline{\text{VRD1\_HOT}}$ input has been asserted.                   | S3, S4/5      |
| 5   | VRD2_ERR | RWC | This bit is set when the $\overline{\text{VRD2\_HOT\#}}$ input has been asserted.                 | S3, S4/5      |
| 7:6 | RES      | R   | Reserved  | N/A           |

#### 6.4.10.2 Register 49h H\_Error Status 2

| Register Address | Read/Write | Register Name    | Bit 7     | Bit 6     | Bit 5     | Bit 4     | Bit 3     | Bit 2     | Bit 1     | Bit 0     | Default Value |
|------------------|------------|------------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|---------------|
| 49h              | RWC        | H_Error Status 2 | ADIN8_ERR | ADIN7_ERR | ADIN6_ERR | ADIN5_ERR | ADIN4_ERR | ADIN3_ERR | ADIN2_ERR | ADIN1_ERR | 00h           |

| Bit | Name    | R/W | Description   | Sleep Masking |
|-----|---------|-----|---|---------------|
| 0   | AD1_ERR | RWC | This bit is set when the AD_IN1 voltage has fallen outside the range defined by the AD_IN1 Low Limit and the AD_IN1 High Limit registers. | S3, S4/5      |
| 1   | AD2_ERR | RWC | This bit is set when the AD_IN2 voltage has fallen outside the range defined by the AD_IN2 Low Limit and the AD_IN2 High Limit registers. | S3, S4/5      |
| 2   | AD3_ERR | RWC | This bit is set when the AD_IN3 voltage has fallen outside the range defined by the AD_IN3 Low Limit and the AD_IN3 High Limit registers. | S3, S4/5      |
| 3   | AD4_ERR | RWC | This bit is set when the AD_IN4 voltage has fallen outside the range defined by the AD_IN4 Low Limit and the AD_IN4 High Limit registers. | S3, S4/5      |
| 4   | AD5_ERR | RWC | This bit is set when the AD_IN5 voltage has fallen outside the range defined by the AD_IN5 Low Limit and the AD_IN5 High Limit registers. | S3, S4/5      |
| 5   | AD6_ERR | RWC | This bit is set when the AD_IN6 voltage has fallen outside the range defined by the AD_IN6 Low Limit and the AD_IN6 High Limit registers. | S3, S4/5      |
| 6   | AD7_ERR | RWC | This bit is set when the AD_IN7 voltage has fallen outside the range defined by the AD_IN7 Low Limit and the AD_IN7 High Limit registers. | S3, S4/5      |

| Bit | Name    | R/W | Description   | Sleep Masking |
|-----|---------|-----|---|---------------|
| 7   | AD8_ERR | RWC | This bit is set when the AD_IN8 voltage has fallen outside the range defined by the AD_IN8 Low Limit and the AD_IN8 High Limit registers. | S3, S4/5      |

#### 6.4.10.3 Register 4Ah H\_Error Status 3

| Register Address | Read/Write | Register Name    | Bit 7      | Bit 6      | Bit 5      | Bit 4      | Bit 3      | Bit 2      | Bit 1      | Bit 0     | Default Value |
|------------------|------------|------------------|------------|------------|------------|------------|------------|------------|------------|-----------|---------------|
| 4Ah              | RWC        | H_Error Status 3 | ADIN16_ERR | ADIN15_ERR | ADIN14_ERR | ADIN13_ERR | ADIN12_ERR | ADIN11_ERR | ADIN10_ERR | ADIN9_ERR | 00h           |

| Bit | Name     | R/W | Description  | Sleep Masking |
|-----|----------|-----|--|---------------|
| 0   | AD9_ERR  | RWC | This bit is set when the AD_IN9 voltage has fallen outside the range defined by the AD_IN9 Low Limit and the AD_IN9 High Limit registers.    | S3, S4/5      |
| 1   | AD10_ERR | RWC | This bit is set when the AD_IN10 voltage has fallen outside the range defined by the AD_IN10 Low Limit and the AD_IN10 High Limit registers. | S3, S4/5      |
| 2   | AD11_ERR | RWC | This bit is set when the AD_IN11 voltage has fallen outside the range defined by the AD_IN11 Low Limit and the AD_IN11 High Limit registers. | S3, S4/5      |
| 3   | AD12_ERR | RWC | This bit is set when the AD_IN12 voltage has fallen outside the range defined by the AD_IN12 Low Limit and the AD_IN12 High Limit registers. | S3*, S4/5*    |
| 4   | AD13_ERR | RWC | This bit is set when the AD_IN13 voltage has fallen outside the range defined by the AD_IN13 Low Limit and the AD_IN13 High Limit registers. | S3*, S4/5*    |
| 5   | AD14_ERR | RWC | This bit is set when the AD_IN14 voltage has fallen outside the range defined by the AD_IN14 Low Limit and the AD_IN14 High Limit registers. | S3*, S4/5*    |
| 6   | AD15_ERR | RWC | This bit is set when the AD_IN15 voltage has fallen outside the range defined by the AD_IN15 Low Limit and the AD_IN15 High Limit registers. | S3, S4/5      |
| 7   | AD16_ERR | RWC | This bit is set when the AD_IN16 voltage has fallen outside the range defined by the AD_IN16 Low Limit and the AD_IN16 High Limit registers. | none          |

#### 6.4.10.4 Register 4Bh H\_Error Status 4

| Register Address | Read/Write | Register Name    | Bit 7   | Bit 6   | Bit 5                   | Bit 4                   | Bit 3    | Bit 2    | Bit 1   | Bit 0   | Default Value |
|------------------|------------|------------------|---------|---------|-------------------------|-------------------------|----------|----------|---------|---------|---------------|
| 4Bh              | RWC        | H_Error Status 4 | D2a_ERR | D1a_ERR | DV <sub>DD</sub> P2_ERR | DV <sub>DD</sub> P1_ERR | GPI9_ERR | GPI8_ERR | D2b_ERR | D1b_ERR | 00h           |

| Bit | Name                    | R/W | Description  | Sleep Masking |
|-----|-------------------------|-----|--|---------------|
| 0   | D1b_ERR                 | RWC | Diode Fault Error<br>This bit is set if there is an open or short circuit on the REMOTE1b+ and REMOTE1- pins.                    | S3*, S4/5*    |
| 1   | D2b_ERR                 | RWC | Diode Fault Error<br>This bit is set if there is an open or short circuit on the REMOTE2b+ and REMOTE2- pins.                    | S3*, S4/5*    |
| 2   | GPI8                    | RWC | SCSI Fuse Error<br>This bit is set if GPI8 has been asserted. Enabled only when VID mode is set to VRD 10.                       | S3, S4/5      |
| 3   | GPI9                    | RWC | SCSI Fuse Error<br>This bit is set if GPI9 has been asserted. Enabled only when VID mode is set to VRD 10.                       | S3, S4/5      |
| 4   | DV <sub>DD</sub> P1_ERR | RWC | Dynamic Vccp Limit Error.<br>This bit is set if AD_IN7 (P1_Vccp) did not match the requested voltage as reported by P1_VID[7:0]. | S3, S4/5      |
| 5   | DV <sub>DD</sub> P2_ERR | RWC | Dynamic Vccp Limit Error.<br>This bit is set if AD_IN8 (P2_Vccp) did not match the requested voltage as reported by P1_VID[7:0]. | S3, S4/5      |

| Bit | Name    | R/W | Description   | Sleep Masking |
|-----|---------|-----|---|---------------|
| 6   | D1a_ERR | RWC | Diode Fault Error<br>This bit is set if there is an open or short circuit on the REMOTE1a+ and REMOTE1- pins. | S3*, S4/5*    |
| 7   | D2a_ERR | RWC | Diode Fault Error<br>This bit is set if there is an open or short circuit on the REMOTE2a+ and REMOTE2- pins. | S3*, S4/5*    |

#### 6.4.10.5 Register 4Ch $\overline{H\_P1\_PROCHOT}$ Error Status

| Register Address | Read/Write | Register Name                            | Bit 7   | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|--|---------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 4Ch              | RWC        | $\overline{H\_P1\_PROCHOT}$ Error Status | PH1_ERR | TMAX  | T100  | T75   | T50   | T25   | T12   | T0    | 00h           |

| Bit | Name    | R/W | Description   | Sleep Masking |
|-----|---------|-----|---|---------------|
| 0   | T0      | RWC | Set when $\overline{P1\_PROCHOT}$ has had a throttled event. This bit is set for any amount of $\overline{PROCHOT}$ throttling >0%. | S3, S4/5      |
| 1   | T12     | RWC | Set when $\overline{P1\_PROCHOT}$ has throttled greater than or equal to 0.00% but less than 12.5%.                                 | S3, S4/5      |
| 2   | T25     | RWC | Set when $\overline{P1\_PROCHOT}$ has throttled greater than or equal to 12.5% but less than 25%.                                   | S3, S4/5      |
| 3   | T50     | RWC | Set when $\overline{P1\_PROCHOT}$ has throttled greater than or equal to 25% but less than 50%.                                     | S3, S4/5      |
| 4   | T75     | RWC | Set when $\overline{P1\_PROCHOT}$ has throttled greater than or equal to 50% but less than 75%.                                     | S3, S4/5      |
| 5   | T100    | RWC | Set when $\overline{P1\_PROCHOT}$ has throttled greater than or equal to 75% but less than 100%.                                    | S3, S4/5      |
| 6   | TMAX    | RWC | Set when $\overline{P1\_PROCHOT}$ has throttled 100%.   | S3, S4/5      |
| 7   | PH1_ERR | RWC | Set when $\overline{P1\_PROCHOT}$ has throttled more than the user limit.   | S3, S4/5      |

The PH1\_ERR bit is the only bit in this register that will set HOST\_ERR in the LM94 Status/Control register.

#### 6.4.10.6 Register 4Dh $\overline{B\_P2\_PROCHOT}$ Error Status

| Register Address | Read/Write | Register Name                            | Bit 7   | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|--|---------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 4Dh              | RWC        | $\overline{B\_P2\_PROCHOT}$ Error Status | PH2_ERR | TMAX  | T100  | T75   | T50   | T25   | T12   | T0    | 00h           |

| Bit | Name | R/W | Description   | Sleep Masking |
|-----|------|-----|---|---------------|
| 0   | T0   | RWC | Set when $\overline{P2\_PROCHOT}$ has had a throttled event. This bit is set for any amount of $\overline{PROCHOT}$ throttling >0%. | S3, S4/5      |
| 1   | T12  | RWC | Set when $\overline{P2\_PROCHOT}$ has throttled greater than or equal to 0.00% but less than 12.5%.                                 | S3, S4/5      |
| 2   | T25  | RWC | Set when $\overline{P2\_PROCHOT}$ has throttled greater than or equal to 12.5% but less than 25%.                                   | S3, S4/5      |
| 3   | T50  | RWC | Set when $\overline{P2\_PROCHOT}$ has throttled greater than or equal to 25% but less than 50%.                                     | S3, S4/5      |
| 4   | T75  | RWC | Set when $\overline{P2\_PROCHOT}$ has throttled greater than or equal to 50% but less than 75%.                                     | S3, S4/5      |

| Bit | Name    | R/W | Description  | Sleep Masking |
|-----|---------|-----|--|---------------|
| 5   | T100    | RWC | Set when $\overline{P2\_PROCHOT}$ has throttled greater than or equal to 75% but less than 100%. | S3, S4/5      |
| 6   | TMAX    | RWC | Set when $\overline{P2\_PROCHOT}$ has throttled 100%.  | S3, S4/5      |
| 7   | PH2_ERR | RWC | Set when $\overline{P2\_PROCHOT}$ has throttled more than the user limit.                        | S3, S4/5      |

The PH2\_ERR bit is the only bit in this register that will set HOST\_ERR in the LM94 Status/Control register.

#### 6.4.10.7 Register 4Eh H\_GPI Error Status

| Register Address | Read/Write | Register Name      | Bit 7    | Bit 6    | Bit 5    | Bit 4    | Bit 3    | Bit 2    | Bit 1    | Bit 0    | Default Value |
|------------------|------------|--------------------|----------|----------|----------|----------|----------|----------|----------|----------|---------------|
| 4Eh              | RWC        | H_GPI Error Status | GPI7_ERR | GPI6_ERR | GPI5_ERR | GPI4_ERR | GPI3_ERR | GPI2_ERR | GPI1_ERR | GPI0_ERR | 00h           |

| Bit | Name     | R/W | Description   | Sleep Masking   |
|-----|----------|-----|---|-----------------|
| 0   | GPI0_ERR | RWC | This bit is set whenever GPIO0 is driven low (unless masked via the GPI Error Mask register). | S1*, S3*, S4/5* |
| 1   | GPI1_ERR | RWC | This bit is set whenever GPIO1 is driven low (unless masked via the GPI Error Mask register). | S1*, S3*, S4/5* |
| 2   | GPI2_ERR | RWC | This bit is set whenever GPIO2 is driven low (unless masked via the GPI Error Mask register). | S1*, S3*, S4/5* |
| 3   | GPI3_ERR | RWC | This bit is set whenever GPIO3 is driven low (unless masked via the GPI Error Mask register). | S1*, S3*, S4/5* |
| 4   | GPI4_ERR | RWC | This bit is set whenever GPIO4 is driven low (unless masked via the GPI Error Mask register). | S1*, S3*, S4/5* |
| 5   | GPI5_ERR | RWC | This bit is set whenever GPIO5 is driven low (unless masked via the GPI Error Mask register). | S1*, S3*, S4/5* |
| 6   | GPI6_ERR | RWC | This bit is set whenever GPIO6 is driven low (unless masked via the GPI Error Mask register). | S1*, S3*, S4/5* |
| 7   | GPI7_ERR | RWC | This bit is set whenever GPIO7 is driven low (unless masked via the GPI Error Mask register). | S1*, S3*, S4/5* |

#### 6.4.10.8 Register 4Fh H\_Fan Error Status

| Register Address | Read/Write | Register Name      | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3    | Bit 2    | Bit 1    | Bit 0    | Default Value |
|------------------|------------|--------------------|-------|-------|-------|-------|----------|----------|----------|----------|---------------|
| 4Fh              | RWC        | H_Fan Error Status | RES   |       |       |       | FAN4_ERR | FAN3_ERR | FAN2_ERR | FAN1_ERR | 00h           |

| Bit | Name     | R/W | Description   | Sleep Masking  |
|-----|----------|-----|---|----------------|
| 0   | FAN1_ERR | RWC | This bit is set when the Fan Tach 1 value register is above the value set in the Fan Tach 1 Limit register. | S1*, S3*, S4/5 |
| 1   | FAN2_ERR | RWC | This bit is set when the Fan Tach 2 value register is above the value set in the Fan Tach 2 Limit register. | S1*, S3*, S4/5 |
| 2   | FAN3_ERR | RWC | This bit is set when the Fan Tach 3 value register is above the value set in the Fan Tach 3 Limit register. | S1*, S3*, S4/5 |
| 3   | FAN4_ERR | R   | This bit is set when the Fan Tach 4 value register is above the value set in the Fan Tach 4 Limit register. | S1*, S3*, S4/5 |
| 7:4 | RES      | R   | Reserved  | N/A            |

## 6.4.11 Value Registers

### 6.4.11.1 Registers 50–53h Unfiltered Temperature Value Registers

| Register Address | Read/Write | Register Name                  | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|--------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 06h              | R          | Zone 1b (CPU1) Temp            | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| 07h              | R          | Zone 2b (CPU2) Temp            | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| 50h              | R          | Zone 1a (CPU1) Temp            | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| 51h              | R          | Zone 2a (CPU2) Temp            | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| 52h              | R          | Zone 3 (Internal) Temp         | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| 53h              | R/W        | Zone 4 (External Digital) Temp | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |

Zones 1 and 2 are all automatically updated by the LM94. The Zone 3 (Internal) Temp and Zone 4 (External Digital) Temp registers may be written by an external SMBus device or can be assigned to AD\_IN11 and AD\_IN15, respectively.

The temperature registers for zones 1 and 2 will return a value of 80h if the remote diode pins are not implemented by the board designer or are not functioning properly.

### 6.4.11.2 Registers 54–55h Filtered Temperature Value Registers

| Register Address | Read/Write | Register Name                | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 08h              | R          | Zone 1b (CPU1) Filtered Temp | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| 09h              | R          | Zone 2b (CPU2) Filtered Temp | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| 54h              | R          | Zone 1a (CPU1) Filtered Temp | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| 55h              | R          | Zone 2a (CPU2) Filtered Temp | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |

These registers reflect the temperature of zones 1 and 2 after the spike smoothing filter has been applied.

The characteristics of the filtering can be adjusted by using the Zones 1/2 Spike Smoothing Control register.

### 6.4.11.3 Register 56–65h A/D Channel Voltage Registers

| Register Address | Read/Write | Register Name   | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|-----------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 56h              | R          | AD_IN1 Voltage  | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | N/D           |
| 57h              | R          | AD_IN2 Voltage  | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | N/D           |
| 58h              | R          | AD_IN3 Voltage  | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | N/D           |
| 59h              | R          | AD_IN4 Voltage  | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | N/D           |
| 5Ah              | R          | AD_IN5 Voltage  | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | N/D           |
| 5Bh              | R          | AD_IN6 Voltage  | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | N/D           |
| 5Ch              | R          | AD_IN7 Voltage  | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | N/D           |
| 5Dh              | R          | AD_IN8 Voltage  | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | N/D           |
| 5Eh              | R          | AD_IN9 Voltage  | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | N/D           |
| 5Fh              | R          | AD_IN10 Voltage | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | N/D           |
| 60h              | R          | AD_IN11 Voltage | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | N/D           |
| 61h              | R          | AD_IN12 Voltage | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | N/D           |
| 62h              | R          | AD_IN13 Voltage | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | N/D           |
| 63h              | R          | AD_IN14 Voltage | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | N/D           |
| 64h              | R          | AD_IN15 Voltage | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | N/D           |
| 65h              | R          | AD_IN16 Voltage | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | N/D           |

The voltage reading registers reflect the current voltage of the LM94 voltage monitoring inputs. Voltages are presented in the registers at  $\frac{3}{4}$  full scale for the nominal voltage. Therefore, at nominal voltage, each register reads C0h.

### 6.4.11.4 Register 67h Current $\overline{P1\_PROCHOT}$

| Register Address | Read/Write | Register Name                    | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|----------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 67h              | R          | Current $\overline{P1\_PROCHOT}$ | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |

This is the value of the  $\overline{PROCHOT}$  percentage active time for Processor 1 at the end of each  $\overline{PROCHOT}$  monitoring interval as set by the  $\overline{PROCHOT}$  Time Interval register. Writing to this register does not effect the register contents, but does restart the capture cycle for both  $\overline{P1\_PROCHOT}$  and  $\overline{P2\_PROCHOT}$ . A register value of one represents anything greater than 0% but less than 0.39% of active time.

| Register Value (Decimal) | Percentage Active Time |
|--------------------------|------------------------|
| 0                        | 0%                     |

| Register Value (Decimal) | Percentage Active Time |
|--------------------------|------------------------|
| 1                        | 0.39%                  |
| 2                        | 0.78%                  |
| •                        | •                      |
| •                        | •                      |
| •                        | •                      |
| n                        | $n/256*100$            |
| 255                      | 99.60%                 |

#### 6.4.11.5 Register 68h Average $\overline{P1\_PROCHOT}$

| Register Address | Read/Write | Register Name                    | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|----------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 68h              | R          | Average $\overline{P1\_PROCHOT}$ | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |

This is the average percentage active time of  $\overline{P1\_PROCHOT}$ . It is the result of adding the contents of this register to the contents of the Current  $\overline{P1\_PROCHOT}$  register and dividing the result by 2. The update occurs at the same time that the Current  $\overline{P1\_PROCHOT}$  register gets updated. A register value of one represents anything greater than 0% but less than 0.39% of active time.

#### 6.4.11.6 Register 69h Current $\overline{P2\_PROCHOT}$

| Register Address | Read/Write | Register Name                    | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|----------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 69h              | R          | Current $\overline{P2\_PROCHOT}$ | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |

This is the value of the  $\overline{PROCHOT}$  percentage active time for Processor 2 at the end of each  $\overline{PROCHOT}$  monitoring interval as set by the  $\overline{PROCHOT}$  Time Interval register. Writing to this register does not effect the register contents, but does restart the capture cycle for both  $\overline{PROCHOT}$  channels (  $\overline{P1\_PROCHOT}$  and  $\overline{P2\_PROCHOT}$ ). A register value of one represents anything greater than 0% but less than 0.39% of active time.

| Register Value (Decimal) | Percentage Active Time |
|--------------------------|------------------------|
| 0                        | 0%                     |
| 1                        | 0.39%                  |
| 2                        | 0.78%                  |
| •                        | •                      |
| •                        | •                      |
| •                        | •                      |
| n                        | $n/256*100$            |
| 255                      | 99.60%                 |

#### 6.4.11.7 Register 6Ah Average $\overline{P2\_PROCHOT}$

| Register Address | Read/Write | Register Name                    | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|----------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 6Ah              | R          | Average $\overline{P2\_PROCHOT}$ | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |

This is the average percentage active time of  $\overline{P2\_PROCHOT}$ . It is the result of adding the contents of this register to the contents of the Current  $\overline{P2\_PROCHOT}$  register and dividing the result by 2. The update occurs at

the same time that the Current  $\overline{P2\_PROCHOT}$  register gets updated. A register value of one represents anything greater than 0% but less than 0.39% of active time.

#### 6.4.11.8 Register 6Bh Current GPI State

| Register Address | Read/Write | Register Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|---------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 6Bh              | R          | GPI State     | GPI7  | GPI6  | GP15  | GPI4  | GPI3  | GPI2  | GPI1  | GPI0  | 00h           |

| Bit | Name | Read/Write | Description                           |
|-----|------|------------|---------------------------------------|
| 0   | GPI0 | R          | 1 if GPIO_0 input is LOW, not latched |
| 1   | GPI1 | R          | 1 if GPIO_1 input is LOW, not latched |
| 2   | GPI2 | R          | 1 if GPIO_2 input is LOW, not latched |
| 3   | GPI3 | R          | 1 if GPIO_3 input is LOW, not latched |
| 4   | GPI4 | R          | 1 if GPIO_4 input is LOW, not latched |
| 5   | GPI5 | R          | 1 if GPIO_5 input is LOW, not latched |
| 6   | GPI6 | R          | 1 if GPIO_6 input is LOW, not latched |
| 7   | GPI7 | R          | 1 if GPIO_7 input is LOW, not latched |

#### 6.4.11.9 Register 6Ch P1\_VID

This register has four possible mappings described in the table. The mapping is determined by the VID mode as selected in the Special Function Control 2 register at address BDh. See the [Special Function Control 2](#) register description for further details.

| Register Address | Read/Write | Register Name | Bit 7                          | Bit 6   | Bit 5  | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|---------------|--------------------------------|---|--|-------|-------|-------|-------|-------|---------------|
| 6Ch              | R          | P1_VID        | RES (0)                        |   | P1_VID[5:0] for VRD 10 mode (functions same as LM93) |       |       |       |       | 00h   |               |
|                  |            |               | RES (0)                        | P1_VID[6:0] for VRD 10.2 Extended mode                              |  |       |       |       |       | 00h   |               |
|                  |            |               | RES (0)                        | P1_VID[6:0] for VRD 11 , Mode 1 (most commonly used mode for VRD11) |  |       |       |       |       |       | 00h           |
|                  |            |               | P1_VID[7:1] for VRD 11, Mode 2 |   |  |       |       |       |       |       | RES (0)       |

**Table 6-4. VRD 10 mode**

| Bit | Name        | Read/Write | Description  |
|-----|-------------|------------|--|
| 5:0 | P1_VID[5:0] | R          | Processor 1 VID status. Reports the current state of the P1_VID5 through P1_VID0 pins. This register will only be updated if P1_VID signals remain stable for at least 600 ns. |
| 7:6 | RES         | R          | Reserved and will always report 0.   |

**Table 6-5. VRD 10.2 Extended mode**

| Bit | Name        | Read/Write | Description  |
|-----|-------------|------------|--|
| 6:0 | P1_VID[6:0] | R          | Processor 1 VID status. Reports the current state of the P1_VID6 through P1_VID0 pins. This register will only be updated if P1_VID signals remain stable for at least 600 ns. |
| 7   | RES         | R          | Reserved and will always report 0.   |

**Table 6-6. VRD 11 Mode 1**

| Bit | Name        | Read/Write | Description  |
|-----|-------------|------------|--|
| 6:0 | P1_VID[6:0] | R          | Processor 1 VID status. This mode is the recommended mode for support of VRD11. Reports the current state of the P1_VID6 through P1_VID0 pins. This register will only be updated if P1_VID signals remain stable for at least 600 ns. |

**Table 6-6. VRD 11 Mode 1 (continued)**

| Bit | Name | Read/Write | Description                        |
|-----|------|------------|------------------------------------|
| 7   | RES  | R          | Reserved and will always report 0. |

**Table 6-7. VRD 11 Mode 2**

| Bit | Name        | Read/Write | Description  |
|-----|-------------|------------|--|
| 0   | RES         | R          | Reserved and will always report 0.   |
| 7:1 | P1_VID[7:1] | R          | Processor 1 VID status. This mode is supplied for future experimentation and will require additional hardware in order to support both VRD11 and VRD10 specifications.<br>Reports the current state of the P1_VID7 through P1_VID1 pins. This register will only be updated if P1_VID signals remain stable for at least 600 ns. |

**6.4.11.10 Register 6Dh P2\_VID**

This register has four possible mappings described in the table. The mapping is determined by the VID mode as selected in the Special Function Control 2 register at address BDh. See the [Special Function Control 2](#) register description for further details.

| Register Address | Read/Write | Register Name | Bit 7                          | Bit 6  | Bit 5  | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|---------------|--------------------------------|--|--|-------|-------|-------|-------|-------|---------------|
| 6Dh              | R          | P2_VID        | RES (0)                        |  | P2_VID[5:0] for VRD 10 mode (functions same as LM93) |       |       |       |       | 00h   |               |
|                  |            |               | RES (0)                        | P2_VID[6:0] for VRD 10.2 Extended mode                             |  |       |       |       |       | 00h   |               |
|                  |            |               | RES (0)                        | P2_VID[6:0] for VRD 11, Mode 1 (most commonly used mode for VRD11) |  |       |       |       |       | 00h   |               |
|                  |            |               | P2_VID[7:1] for VRD 11, Mode 2 |  |  |       |       |       |       |       | RES (0)       |

**Table 6-8. VRD 10 mode**

| Bit | Name        | Read/Write | Description   |
|-----|-------------|------------|---|
| 5:0 | P2_VID[5:0] | R          | Processor 2 VID status.<br>Reports the current state of the P2_VID5 through P2_VID0 pins. This register will only be updated if P2_VID signals remain stable for at least 600 ns. |
| 7:6 | RES         | R          | Reserved and will always report 0.  |

**Table 6-9. VRD 10.2 Extended mode**

| Bit | Name        | Read/Write | Description   |
|-----|-------------|------------|---|
| 6:0 | P2_VID[6:0] | R          | Processor 2 VID status.<br>Reports the current state of the P2_VID6 through P2_VID0 pins. This register will only be updated if P2_VID signals remain stable for at least 600 ns. |
| 7   | RES         | R          | Reserved and will always report 0.  |

**Table 6-10. VRD 11 Mode 1**

| Bit | Name        | Read/Write | Description   |
|-----|-------------|------------|---|
| 6:0 | P2_VID[6:0] | R          | Processor 2 VID status. This mode is the recommended mode for support of VRD11.<br>Reports the current state of the P2_VID6 through P2_VID0 pins. This register will only be updated if P2_VID signals remain stable for at least 600 ns. |
| 7   | RES         | R          | Reserved and will always report 0.  |

**Table 6-11. VRD 11 Mode 2**

| Bit | Name | Read/Write | Description                        |
|-----|------|------------|------------------------------------|
| 0   | RES  | R          | Reserved and will always report 0. |

**Table 6-11. VRD 11 Mode 2 (continued)**

| Bit | Name        | Read/Write | Description  |
|-----|-------------|------------|--|
| 7:1 | P2_VID[7:1] | R          | Processor 2 VID status. This mode is supplied for future experimentation and will require additional hardware in order to support both VRD11 and VRD10 specifications.<br>Reports the current state of the P2_VID7 through P2_VID1 pins. This register will only be updated if P2_VID signals remain stable for at least 600 ns. |

**6.4.11.11 Register 6E–75h Fan Tachometer Readings**

| Register Address | Read/Write | Register Name  | Bit 7       | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1     | Bit 0 | Default Value |     |
|------------------|------------|----------------|-------------|-------|-------|-------|-------|-------|-----------|-------|---------------|-----|
| 6Eh              | R          | Fan Tach 1 LSB | TACH1[5:0]  |       |       |       |       |       | T1ST[1:0] |       | 00h           |     |
| 6Fh              | R          | Fan Tach 1 MSB | TACH1[13:6] |       |       |       |       |       |           |       |               | 00h |
| 70h              | R          | Fan Tach 2 LSB | TACH2[5:0]  |       |       |       |       |       | T2ST[1:0] |       | 00h           |     |
| 71h              | R          | Fan Tach 2 MSB | TACH2[13:6] |       |       |       |       |       |           |       |               | 00h |
| 72h              | R          | Fan Tach 3 LSB | TACH3[5:0]  |       |       |       |       |       | T3ST[1:0] |       | 00h           |     |
| 73h              | R          | Fan Tach 3 MSB | TACH3[13:6] |       |       |       |       |       |           |       |               | 00h |
| 74h              | R          | Fan Tach 4 LSB | TACH4[5:0]  |       |       |       |       |       | T4ST[1:0] |       | 00h           |     |
| 75h              | R          | Fan Tach 4 MSB | TACH4[13:6] |       |       |       |       |       |           |       |               | 00h |

The 14-bit fan tach readings indicate the number of 22.5 kHz clock periods that occurred during two full periods of the tachometer input signal. Most fans produce two tachometer pulses per full revolution. These registers must be updated at least once every second.

The fan tachometer reading registers must always return an accurate fan tachometer measurement, even when a fan is disabled or non-functional. 3FFFh indicates that the fan is stalled, not spinning fast enough to measure, or the tachometer input is not connected to a valid signal.

If the pulses per revolution of the fan is known, the RPM can be calculated with the following equation:

$$RPM = 22500 \text{ cycles/sec} * 60 \text{ sec/min} * 2 \text{ pulses} / \text{COUNT cycles} / \text{PULSES\_PER\_REV}$$

where:

**PULSES\_PER\_REV** = the number of pulses that the fan produces per revolution

**COUNT** = The 14-bit value read from the tach register

| Bit | Name   | Read/Write | Description   |
|-----|--|------------|---|
| 1:0 | T1ST[1:0], T2ST[1:0], T3ST[1:0], T4ST[1:0]         | R          | Two bits for each tachometer reading that report the state of the fan control circuitry used to acquire a reading. See table below for further clarification. |
| 7:2 | TACH1[5:0], TACH2[5:0], TACH3[5:0], TACH4[5:0]     | R          | Least significant bit field of tachometer reading.  |
| 7:0 | TACH1[13:6], TACH2[13:6], TACH3[13:6], TACH4[13:6] | R          | Most significant bit field of tachometer reading.   |

| T1ST[1:0], T2ST[1:0], T3ST[1:0], or T4ST[1:0] | State of Fan Control Circuitry         |
|---|--|
| 00  | Normal Mode (Smart Tach Mode disabled) |

| T1ST[1:0], T2ST[1:0], T3ST[1:0], or T4ST[1:0] | State of Fan Control Circuitry                             |
|---|--|
| 01  | Reserved   |
| 10  | Smart Tach Mode 1, less accurate with most stable Fan RPM  |
| 11  | Smart Tach Mode 2, most accurate with least stable Fan RPM |

## 6.4.12 Limit Registers

### 6.4.12.1 Registers 78–7Fh Temperature Limit Registers

| Register Address | Read/Write | Register Name                      | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|------------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 78h              | R/W        | Processor 1 (Zone1) Low Temp       | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 80h           |
| 79h              | R/W        | Processor 1 (Zone1) High Temp      | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 80h           |
| 7Ah              | R/W        | Processor 2 (Zone2) Low Temp       | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 80h           |
| 7Bh              | R/W        | Processor 2 (Zone2) High Temp      | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 80h           |
| 7Ch              | R/W        | Internal (Zone3) Low Temp          | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 80h           |
| 7Dh              | R/W        | Internal (Zone3) High Temp         | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 80h           |
| 7Eh              | R/W        | External Digital (Zone4) Low Temp  | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 80h           |
| 7Fh              | R/W        | External Digital (Zone4) High Temp | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 80h           |

If an external temperature input or the internal temperature sensor either exceeds the value set in the high limit register or falls below the value set in the low limit register, the corresponding bit in the B\_ and H\_Error Status 1 register is set automatically by the LM94. For example, if the temperature read from the Remote1– and Remote1+ inputs exceeds the Processor (Zone1) High Temp register limit setting, the ZN1\_ERR bit in both B\_Error Status 1 and H\_Error Status 1 registers is set. The temperature limits in these registers is represented as 8 bit, 2's complement, signed numbers in Celsius.

If any high temp limit register is set to 80h then the B\_ and H\_Error Status register bit for that temperature channel is masked.

### 6.4.12.2 Registers 80–83h Fan Boost Temperature Registers

| Register Address | Read/Write | Register Name         | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|-----------------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 80h              | R/W        | Fan Boost Temp Zone 1 | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 3Ch           |

| Register Address | Read/Write | Register Name         | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|-----------------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 81h              | R/W        | Fan Boost Temp Zone 2 | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 3Ch           |
| 82h              | R/W        | Fan Boost Temp Zone 3 | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 23h           |
| 83h              | R/W        | Fan Boost Temp Zone 4 | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 23h           |

If any thermal zone exceeds the temperature set in the Fan Boost Limit register, both of the PWM outputs are set to 100%. The fan boost function takes precedence over low-resolution manual override. High-resolution manual override takes priority over the fan boost function. This is a safety feature that attempts to cool the system if there is a potentially catastrophic thermal event. If set to 7Fh and the fan control temperature resolution is 1°C, the feature is disabled.

Default = 60°C = 3Ch for zones 1 and 2

Default = 35°C = 23h for zones 3 and 4

The temperature has to fall the number of degrees specified in the Fan Boost Hysteresis registers, below this temperature to cause the PWM outputs to return to normal operation. The fan boost function can be disabled by setting the associated register to 80h.

#### 6.4.12.3 Register 84h Zone1, and Zone2 Hysteresis for Limit Comparisons

| Register Address | Read/Write | Register Name                           | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|---|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 84h              | R/W        | Limit Comparison Hysteresis (Zones 1/2) | HC2   |       |       |       | HC1   |       |       |       | 00h           |

| Bit | Name | R/W | Description  |
|-----|------|-----|--|
| 3:0 | HC1  | R/W | Sets the limit comparison hysteresis for zone 1 for both the High and Low limits. The hysteresis can be set from 0°C to 15°C and has 1°C resolution. |
| 7:4 | HC2  | R/W | Sets the limit comparison hysteresis for zone 2 for both the High and Low limits. The hysteresis can be set from 0°C to 15°C and has 1°C resolution. |

#### 6.4.12.4 Register 85h Zone3 and Zone4 Hysteresis for Limit Comparisons

| Register Address | Read/Write | Register Name                           | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|---|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 85h              | R/W        | Limit Comparison Hysteresis (Zones 3/4) | HC4   |       |       |       | HC3   |       |       |       | 00h           |

| Bit | Name | R/W | Description  |
|-----|------|-----|--|
| 3:0 | HC3  | R/W | Sets the limit comparison hysteresis for zone 3 for both the High and Low limits. The hysteresis can be set from 0°C to 15°C and has 1°C resolution. |

| Bit | Name | R/W | Description  |
|-----|------|-----|--|
| 7:4 | HC4  | R/W | Sets the limit comparison hysteresis for zone 4 for both the High and Low limits. The hysteresis can be set from 0°C to 15°C and has 1°C resolution. |

#### 6.4.12.5 Registers 8E–8Fh Zone 1b and Zone 2b Temperature Reading Adjustment Registers

| Register Address | Read/Write | Register Name       | Bit 7 | Bit 6 | Bit 5           | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|---------------------|-------|-------|-----------------|-------|-------|-------|-------|-------|---------------|
| 8Eh              | R/W        | Zone 1b Temp Adjust | RES   | RES   | Z1b_ADJUST[5:0] |       |       |       |       |       | 00h           |
| 8Fh              | R/W        | Zone 2b Temp Adjust | RES   | RES   | Z2b_ADJUST[5:0] |       |       |       |       |       | 00h           |

| Bit | Name                               | R/W | Description  |
|-----|------------------------------------|-----|--|
| 5:0 | Z1b_ADJUST[5:0] or Z2b_ADJUST[5:0] | R/W | 6-bit signed 2's complement offset adjustment. This value is added to zone 1b or zone 2b temperature measurements as they are made. All LM94 registers and functions behave as if the resulting temperature was the true measured temperature. This register allows offset adjustments from +31°C to –32°C in 1°C steps. |
| 7:6 | RES                                | R   | Reserved   |

#### 6.4.12.6 Registers 90–AFh Voltage Limit Registers

| Register Address | Read/Write | Register Name     | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|-------------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 90h              | R/W        | AD_IN1 Low Limit  | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| 91h              | R/W        | AD_IN1 High Limit | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | FFh           |
| 92h              | R/W        | AD_IN2 Low Limit  | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| 93h              | R/W        | AD_IN2 High Limit | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | FFh           |
| 94h              | R/W        | AD_IN3 Low Limit  | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| 95h              | R/W        | AD_IN3 High Limit | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | FFh           |
| 96h              | R/W        | AD_IN4 Low Limit  | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| 97h              | R/W        | AD_IN4 High Limit | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | FFh           |
| 98h              | R/W        | AD_IN5 Low Limit  | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| 99h              | R/W        | AD_IN5 High Limit | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | FFh           |
| 9Ah              | R/W        | AD_IN6 Low Limit  | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| 9Bh              | R/W        | AD_IN6 High Limit | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | FFh           |
| 9Ch              | R/W        | AD_IN7 Low Limit  | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| 9Dh              | R/W        | AD_IN7 High Limit | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | FFh           |
| 9Eh              | R/W        | AD_IN8 Low Limit  | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |

| Register Address | Read/Write | Register Name      | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|--------------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 9Fh              | R/W        | AD_IN8 High Limit  | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | FFh           |
| A0h              | R/W        | AD_IN9 Low Limit   | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| A1h              | R/W        | AD_IN9 High Limit  | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | FFh           |
| A2h              | R/W        | AD_IN10 Low Limit  | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| A3h              | R/W        | AD_IN10 High Limit | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | FFh           |
| A4h              | R/W        | AD_IN11 Low Limit  | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| A5h              | R/W        | AD_IN11 High Limit | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | FFh           |
| A6h              | R/W        | AD_IN12 Low Limit  | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| A7h              | R/W        | AD_IN12 High Limit | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | FFh           |
| A8h              | R/W        | AD_IN13 Low Limit  | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| A9h              | R/W        | AD_IN13 High Limit | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | FFh           |
| AAh              | R/W        | AD_IN14 Low Limit  | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| ABh              | R/W        | AD_IN14 High Limit | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | FFh           |
| ACh              | R/W        | AD_IN15 Low Limit  | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| ADh              | R/W        | AD_IN15 High Limit | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | FFh           |
| A Eh             | R/W        | AD_IN16 Low Limit  | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| AFh              | R/W        | AD_IN16 High Limit | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | FFh           |

FFh as the high limit acts as a mask for that voltage sensor and so prevents this channel from being able to set the associated error status bit in the B\_ or H\_ Error Status registers, for both high and low limit errors.

If a voltage input either exceeds the value set in the voltage high limit register or falls below the value set in the voltage low limit register, the corresponding bit is set automatically by the LM94 in the B\_ and H\_ Error Status registers.

#### 6.4.12.7 Register B0–B1h *PROCHOT* User Limit Registers

| Register Address | Read/Write | Register Name         | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|-----------------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| B0h              | R/W        | P1_PROCHOT User Limit | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | FFh           |
| B1h              | R/W        | P2_PROCHOT User Limit | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | FFh           |

These registers allow a user limit to be set for the  $\overline{\text{PROCHOT}}$  monitoring function. If the corresponding Current  $\text{Px\_PROCHOT}$  register exceeds this value, the PH1\_ERR or PH2\_ERR bit is set in the corresponding Host and BMC error status registers. A value of FFh acts as a mask and prevents the error status bits from being set.

| Register Value (Decimal) | Threshold Percentage |
|--------------------------|----------------------|
| 0                        | 0%                   |
| 1                        | 0.39%                |
| 2                        | 0.78%                |
| •                        | •                    |
| •                        | •                    |
| •                        | •                    |
| n                        | $n/256 \times 100$   |
| 255                      | 99.60%               |

#### 6.4.12.8 Register B2–B3h Dynamic Vccp Limit Offset Registers

| Register Address | Read/Write | Register Name       | Bit 7         | Bit 6 | Bit 5 | Bit 4 | Bit 3         | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|---------------------|---------------|-------|-------|-------|---------------|-------|-------|-------|---------------|
| B2h              | R/W        | Vccp1 Limit Offsets | UPPER_OFFSET1 |       |       |       | LOWER_OFFSET1 |       |       |       | 17h           |
| B3h              | R/W        | Vccp2 Limit Offsets | UPPER_OFFSET2 |       |       |       | LOWER_OFFSET2 |       |       |       | 17h           |

These offsets are used to determine the upper and lower limits of the dynamic Vccp window comparator. These offsets are added or subtracted from the value selected by the VID bits.

| LOWER_OFFSET1 or LOWER_OFFSET2 | Lower Offset |
|--------------------------------|--------------|
| 0h                             | 25 mV        |
| 1h                             | 50 mV        |
| 2h                             | 75 mV        |
| 3h                             | 100 mV       |
| --                             | --           |
| Ch                             | 325 mV       |
| Dh                             | 350 mV       |
| Eh                             | 375 mV       |
| Fh                             | 400 mV       |

| UPPER_OFFSET1 or<br>UPPER_OFFSET2 | Upper Offset |
|-----------------------------------|--------------|
| 0h                                | 12.5 mV      |
| 1h                                | 25 mV        |
| 2h                                | 37.5 mV      |
| 3h                                | 50 mV        |
| ~ ~                               | ~ ~          |
| Dh                                | 175 mV       |
| Eh                                | 187.5 mV     |
| Fh                                | 200 mV       |

**6.4.12.9 Register B4–BBh Fan Tach Limit Registers**

| Register Address | Read/Write | Register Name        | Bit 7         | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |     |
|------------------|------------|----------------------|---------------|-------|-------|-------|-------|-------|-------|-------|---------------|-----|
| B4h              | R/W        | Fan Tach 1 Limit LSB | TLIMIT1[5:0]  |       |       |       |       |       | RES   |       | FCh           |     |
| B5h              | R/W        | Fan Tach 1 Limit MSB | TLIMIT1[13:6] |       |       |       |       |       |       |       |               | FFh |
| B6h              | R/W        | Fan Tach 2 Limit LSB | TLIMIT2[5:0]  |       |       |       |       |       | RES   |       | FCh           |     |
| B7h              | R/W        | Fan Tach 2 Limit MSB | TLIMIT2[13:6] |       |       |       |       |       |       |       |               | FFh |
| B8h              | R/W        | Fan Tach 3 Limit LSB | TLIMIT3[5:0]  |       |       |       |       |       | RES   |       | FCh           |     |
| B9h              | R/W        | Fan Tach 3 Limit MSB | TLIMIT3[13:6] |       |       |       |       |       |       |       |               | FFh |
| BAh              | R/W        | Fan Tach 4 Limit LSB | TLIMIT4[5:0]  |       |       |       |       |       | RES   |       | FCh           |     |
| BBh              | R/W        | Fan Tach 4 Limit MSB | TLIMIT4[13:6] |       |       |       |       |       |       |       |               | FFh |

If a tachometer reading exceeds its limit (as defined by these registers) the corresponding bit is set in the Host and BMC Error Status registers. The fan tachometer readings can be associated with a particular PWM output, but the tach errors are not automatically masked when a PWM is at 0% or set to level that causes the fan RPM to be below the limit purposely. In order to prevent false errors, care needs to be taken to make sure that the Fan Tach Limits are properly set. Errors are never generated for a fan if its limit is set to 3FFFh.

## 6.4.13 Setup Registers

### 6.4.13.1 Register BCh Special Function Control 1 (Voltage Hysteresis and Fan Control Filter Enable)

| Register Address | Read/Write | Register Name              | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|----------------------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| BCh              | R/W        | Special Function Control 1 | RES   | FCFE2 | FCFE1 | LCFE2 | LCFE1 | VH    |       |       | 00h           |

| Bit | Name  | R/W | Description   |
|-----|-------|-----|---|
| 2:0 | VH    | R/W | Voltage hysteresis control. This determines the amount of hysteresis to be applied to all voltage limit comparisons. It applies to both high and low limits. One LSB equals one A/D count, so the actual voltage represented by one LSB depends on the voltage channel.                   |
| 3   | LCFE1 | R/W | Limit Comparison Filter Enable. Setting this bit causes limit comparisons for temperature zone 1a and 1b to use the filtered (spike smoothed) temperature instead of the unfiltered temperature.  |
| 4   | LCFE2 | R/W | Limit Comparison Filter Enable. Setting this bit causes limit comparisons for temperature zone 2a and 2b to use the filtered (spike smoothed) temperature instead of the unfiltered temperature.  |
| 5   | FCFE1 | R/W | Fan Control Filter Enable. Setting this bit causes fan control functions for zone 1a and 1b (including fan boost) to use the filtered (spike smoothed) temperature instead of the unfiltered temperature. This includes the PI Loop controller, LUT, and temperature fan boost functions. |
| 6   | FCFE2 | R/W | Fan Control Filter Enable. Setting this bit causes fan control functions for zone 2a and 2b (including fan boost) to use the filtered (spike smoothed) temperature instead of the unfiltered temperature. This includes the PI Loop controller, LUT, and temperature fan boost functions. |
| 7   | RES   | R   | Reserved  |

In order for the LCFE1, LCFE2, FCFE1 and FCFE2 bits to work correctly, the ZN1E and ZN2E bits in the Zones 1/2 Spike Smoothing Control register (at address C2h) should be cleared.

**Application Note:** If hysteresis for voltage limit comparisons is non-zero, special care needs to be taken when changing the voltage limit registers while a voltage error condition exists. If software relaxes the voltage limits in an attempt to prevent an error condition, it may be necessary to relax the limits by an amount greater than the hysteresis value and wait several milliseconds before attempting to clear the error status bit for the given voltage channel. Once the error status bit has been cleared, the desired limit(s) can be programmed.

### 6.4.13.2 Register BDh Special Function Control 2 (Smart Tach Mode Enable, Fan Control Temperature Resolution Control and VID Mode Select)

| Register Address | Read/Write | Register Name              | Bit 7         | Bit 6 | Bit 5   | Bit 4   | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|----------------------------|---------------|-------|---------|---------|-------|-------|-------|-------|---------------|
| BDh              | R/W        | Special Function Control 2 | VID_MODE[1:0] |       | LT34_RS | LT12_RS | STE4  | STE3  | STE2  | STE1  | 00h           |

| Bit | Name    | R/W | Description  |
|-----|---------|-----|--|
| 0   | STE1    | R/W | Enable Smart Tach for Tach 1   |
| 1   | STE2    | R/W | Enable Smart Tach for Tach 2   |
| 2   | STE3    | R/W | Enable Smart Tach for Tach 3   |
| 3   | STE4    | R/W | Enable Smart Tach for Tach 4   |
| 4   | LT12_RS | R/W | When this bit is set, the LUT1 and LUT2 fan controls will use 0.5°C. The resolution of the LUT offsets and hysteresis settings are affected by this bit. These bits apply to the fan control offset registers, fan control hysteresis registers, and boost hysteresis registers. |
| 5   | LT34_RS | R/W | When this bit is set, the LUT3 and LUT4 fan controls will use 0.5°C. The resolution of the LUT offsets and hysteresis settings are affected by this bit.   |

| Bit | Name          | R/W | Description   |
|-----|---------------|-----|---|
| 7:6 | VID_MODE[1:0] | R/W | These bits select the VID mode which determines how the VID code is handled by the P1_VID and P2_VID value registers and the dynamic V <sub>ccp</sub> monitoring. |

**Table 6-12. VID Mode Select Bit Description**

| VID_MODE[1:0] | VID Mode         | Comments   |
|---------------|------------------|--|
| 00            | VRD10            | Supports the VRD10 specification from Intel and is backwards compatible with the LM93 dynamic V <sub>ccp</sub> monitoring circuitry. This mode has a voltage range of 0.8375V to 1.600V with 12.5mV resolution and supports 6 VID bits/pins.   |
| 01            | VRD10.2 Extended | Supports the VRD10.2 Extended specification from Intel. This mode has a voltage range of 0.83125V to 1.600V with 6.25mV resolution and supports 7 VID bits/pins.   |
| 10            | VRD11 Mode 1     | Supports the VRD11 specification from Intel. This mode has a voltage range of 0.83125V to 1.600V with 6.25mV resolution and supports 7 VID bits/pins (VID6-VID0). It assumes VID7 is 0. This is the recommended mode of operation for support of VRD10 and VRD11 without requiring additional hardware.                            |
| 11            | VRD11 Mode 2     | Supports the VRD11 specification from Intel. This mode has a voltage range of 0.0375V to 1.600V with 12.5mV resolution and supports 7 VID bits/pins (VID7-VID1). It assumes VID0 is 0. This mode measures voltage levels below 0.83125V for VRD11, but will require additional hardware to simultaneously support VRD10 operation. |

**Application Note:** Enabling Smart Tach mode is not supported while either PWM output is configured for 22.5 kHz. The behavior of the part is undefined if this configuration is programmed. Register E0h Special Function TACH to PWM Binding must be setup when Smart Tach modes are enabled.

#### 6.4.13.3 Register BEh GPI/VID Level Control

| Register Address | Read/Write | Register Name         | Bit 7    | Bit 6    | Bit 5    | Bit 4    | Bit 3    | Bit 2    | Bit 1      | Bit 0      | Default Value |
|------------------|------------|-----------------------|----------|----------|----------|----------|----------|----------|------------|------------|---------------|
| BEh              | R/W        | GPI/VID Level Control | GPI7_LVL | GPI6_LVL | GPI5_LVL | GPI4_LVL | GPI9_LVL | GPI8_LVL | P2_VID_LVL | P1_VID_LVL | 00h           |

| Bit | Name       | R/W | Description  |
|-----|------------|-----|--|
| 0   | P1_VID_LVL | R/W | If set, P1_VIDx inputs use alternate lower V <sub>IH</sub> and V <sub>IL</sub> levels.                       |
| 1   | P2_VID_LVL | R/W | If set, P2_VIDx uses alternate lower V <sub>IH</sub> and V <sub>IL</sub> levels.                             |
| 2   | GPI8_LVL   | R/W | When in VRD10 mode, if set, GPI_8 input uses alternate lower V <sub>IH</sub> and V <sub>IL</sub> levels.     |
| 3   | GPI9_LVL   | R/W | When in VRD10 mode, if set, GPI_9 input will use alternate lower V <sub>IH</sub> and V <sub>IL</sub> levels. |
| 4   | GPI4_LVL   | R/W | If set, GPIO4 input will use alternate lower V <sub>IH</sub> and V <sub>IL</sub> levels                      |
| 5   | GPI5_LVL   | R/W | If set, GPIO5 input will use alternate lower V <sub>IH</sub> and V <sub>IL</sub> levels                      |
| 6   | GPI6_LVL   | R/W | If set, GPIO6 input will use alternate lower V <sub>IH</sub> and V <sub>IL</sub> levels                      |
| 7   | GPI7_LVL   | R/W | If set, GPIO7 input will use alternate lower V <sub>IH</sub> and V <sub>IL</sub> levels                      |

See the [Section 5.3](#) for exact V<sub>IH</sub> and V<sub>IL</sub> levels.

#### 6.4.13.4 Register BFh PWM Ramp Control

| Register Address | Read/Write | Register Name    | Bit 7   | Bit 6 | Bit 5 | Bit 4 | Bit 3    | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|------------------|---------|-------|-------|-------|----------|-------|-------|-------|---------------|
| BFh              | R/W        | PWM Ramp Control | PH_RAMP |       |       |       | VRD_RAMP |       |       |       | 00h           |

| Bit | Name     | R/W | Description  |
|-----|----------|-----|--|
| 3:0 | VRD_RAMP | R/W | Sets the time delay between ramp steps for the VRD <sub>x</sub> _HOT ramp up/ramp down PWM function. |

| Bit | Name    | R/W | Description  |
|-----|---------|-----|--|
| 7:4 | PH_RAMP | R/W | Sets the time delay between ramp steps for the $\overline{\text{Px\_PROCHOT}}$ ramp up/ramp down PWM function. |

If the time delay between steps is set to 0 ms, the PWM duty cycle goes immediately to 100% instead of ramping up gradually.

| VRD_RAMP or PH_RAMP | Time Delay between Ramp Steps |
|---------------------|-------------------------------|
| 0h                  | 0 ms                          |
| 1h                  | 50 ms                         |
| 2h                  | 100 ms                        |
| 3h                  | 150 ms                        |
| 4h                  | 200 ms                        |
| 5h                  | 250 ms                        |
| 6h                  | 300 ms                        |
| 7h                  | 350 ms                        |
| 8h                  | 400 ms                        |
| 9h                  | 450 ms                        |
| Ah                  | 500 ms                        |
| Bh                  | 550 ms                        |
| Ch                  | 600 ms                        |
| Dh                  | 650 ms                        |
| Eh                  | 700 ms                        |
| Fh                  | 750 ms                        |

#### 6.4.13.5 Register C0h Fan Boost Hysteresis (Zones 1/2)

| Register Address | Read/Write | Register Name                    | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|----------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| C0h              | R/W        | Fan Boost Hysteresis (Zones 1/2) | H2    |       |       |       | H1    |       |       |       | 44h           |

| Bit | Name | R/W | Description   |
|-----|------|-----|---|
| 3:0 | H1   | R/W | Sets the fan boost hysteresis for Zone 1a and 1b, has 1°C resolution. |
| 7:4 | H2   | R/W | Sets the fan boost hysteresis for zone 2a and 2b, has 1°C resolution. |

If the temperature zone is above fan boost temperature and then drops below the fan boost temperature, the following occurs: the PWM output remains at 100% until the temperature goes a certain amount below the fan boost temperature. These hysteresis registers control this amount and can be set anywhere from 0°C to 15°C (unsigned).

#### 6.4.13.6 Register C1h Fan Boost Hysteresis (Zones 3/4)

| Register Address | Read/Write | Register Name                    | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|----------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| C1h              | R/W        | Fan Boost Hysteresis (Zones 3/4) | H4    |       |       |       | H3    |       |       |       | 44h           |

| Bit | Name | R/W | Description  |
|-----|------|-----|--|
| 3:0 | H3   | R/W | Sets the fan boost hysteresis for zone 3 and has 1°C resolution. |
| 7:4 | H4   | R/W | Sets the fan boost hysteresis for zone 4 and has 1°C resolution. |

If the temperature zone is above fan boost temperature and then drops below the fan boost temperature, the following occurs: the PWM output remains at 100% until the temperature goes a certain amount below the fan boost temperature. These hysteresis registers control this amount and can be set anywhere from 0°C to 15°C (unsigned).

#### 6.4.13.7 Register C2h Zones 1/2 Spike Smoothing Control

| Register Address | Read/Write | Register Name                     | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|-----------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| C2h              | R/W        | Zones 1/2 Spike Smoothing Control | ZN2E  | ZN2   |       |       | ZN1E  | ZN1   |       |       | 00h           |

| Bit | Name | R/W | Description   |
|-----|------|-----|---|
| 2:0 | ZN1  | R/W | Configures the spike smoothing characteristics for zone 1a and 1b   |
| 3   | ZN1E | R/W | When set, the filtered temperature for zone 1a and 1b is used for both limit checking and auto-fan control instead of the unfiltered temperature. Even when this bit is cleared, the filtered temperature can be read by software from the filtered temperature register. |
| 6:4 | ZN2  | R/W | Configures the spike smoothing characteristics for zone 2a and 2b   |
| 7   | ZN2E | R/W | When set, the filtered temperature for zone 2a and 2b is used for both limit checking and auto-fan control instead of the unfiltered temperature. Even when this bit is cleared, the filtered temperature can be read by software from the filtered temperature register. |

If all the REMOTE1 or REMOTE2 pins are connected to a processor or chipset, instantaneous temperature spikes may be sampled by the LM94. If these spikes are not ignored, the PWM outputs may cause the fans to turn on prematurely and produce unpleasant noise. Also, false error events may occur. For this reason, any zone that is connected to a chipset or processor may need spike smoothing enabled. The spike smoothing provides additional filtering above and beyond any  $\Sigma\Delta$  A/D inherent averaging.

When spike smoothing is enabled, the temperature reading registers still reflect the current value of the temperature—not the filtered value. Only the filtered temperature registers reflect the filtered value.

| ZN1 or ZN2 | Spike Smoothed Over |
|------------|---------------------|
| 0h         | 11.8 seconds        |
| 1h         | 7.0 seconds         |
| 2h         | 4.4 seconds         |
| 3h         | 3.0 seconds         |
| 4h         | 1.6 seconds         |
| 5h         | 0.8 seconds         |
| 6h         | 0.6 seconds         |
| 7h         | 0.4 seconds         |

#### 6.4.13.8 Register C3h LUT 1/2 MinPWM and Hysteresis

| Register Address | Read/Write | Register Name                 | Bit 7    | Bit 6 | Bit 5 | Bit 4 | Bit 3       | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|-------------------------------|----------|-------|-------|-------|-------------|-------|-------|-------|---------------|
| C3h              | R/W        | LUT 1/2 MinPWM and Hysteresis | MinPWM12 |       |       |       | LUT_FC_TH12 |       |       |       | 00h           |

| Bit | Name        | R/W | Description  |
|-----|-------------|-----|--|
| 3:0 | LUT_FC_TH12 | R/W | This field sets the amount of hysteresis (in degrees C) that is used by the auto-fan control for LUT 1 and 2. This should be set greater than 0 to avoid unwanted oscillation between two steps in the look-up table. The resolution of this field is controlled by Special Function Control 2 register bit 4.   |
| 7:4 | MinPWM12    | R/W | This field determines the duty cycle that the auto-fan control requests for LUT 1 and 2 if the temperature for the given zone falls below the programmed base temperature for the assigned LUT. This field accepts 16 possible values 13 of which are mapped to duty cycles according the table in the Auto-Fan Control section <a href="#">Section 6.2.18.2</a> . |

#### 6.4.13.9 Register C4h LUT 3/4 MinPWM and Hysteresis

| Register Address | Read/Write | Register Name                 | Bit 7    | Bit 6 | Bit 5 | Bit 4 | Bit 3       | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|-------------------------------|----------|-------|-------|-------|-------------|-------|-------|-------|---------------|
| C4h              | R/W        | LUT 3/4 MinPWM and Hysteresis | MinPWM34 |       |       |       | LUT_FC_TH34 |       |       |       | 00h           |

| Bit | Name        | R/W | Description  |
|-----|-------------|-----|--|
| 3:0 | LUT_FC_TH34 | R/W | This field sets the amount of hysteresis (in degrees C) that is used by the auto-fan control for LUT 3 and 4. This should be set greater than 0 to avoid unwanted oscillation between two steps in the look-up table. The resolution of this field is controlled by Special Function Control 2 register bit 5.   |
| 7:4 | MinPWM34    | R/W | This field determines the duty cycle that the auto-fan control requests for LUT 3 and 4 if the temperature for the given zone falls below the programmed base temperature for the assigned LUT. This field accepts 16 possible values 13 of which are mapped to duty cycles according the table in the Auto-Fan Control section <a href="#">Section 6.2.18.2</a> . |

#### 6.4.13.10 Register C5h GPO

| Register Address | Read/Write | Register Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|---------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| C5h              | R/W        | GPO           | GPO7  | GPO6  | GPO5  | GPO4  | GPO3  | GPO2  | GPO1  | GPO0  | 00h           |

| Bit | Name | R/W | Description  |
|-----|------|-----|--|
| 0   | GPO0 | R/W | If set, GPIO_0 will be pulled low. If cleared, the output is not pulled low. This bit should be 0 if GPIO_0 is being used as an input. |
| 1   | GPO1 | R/W | If set, GPIO_1 will be pulled low. If cleared, the output is not pulled low. This bit should be 0 if GPIO_1 is being used as an input. |
| 2   | GPO2 | R/W | If set, GPIO_2 will be pulled low. If cleared, the output is not pulled low. This bit should be 0 if GPIO_2 is being used as an input. |
| 3   | GPO3 | R/W | If set, GPIO_3 will be pulled low. If cleared, the output is not pulled low. This bit should be 0 if GPIO_3 is being used as an input. |
| 4   | GPO4 | R/W | If set, GPIO_4 will be pulled low. If cleared, the output is not pulled low. This bit should be 0 if GPIO_4 is being used as an input. |

| Bit | Name | R/W | Description  |
|-----|------|-----|--|
| 5   | GPO5 | R/W | If set, GPIO_5 will be pulled low. If cleared, the output is not pulled low. This bit should be 0 if GPIO_5 is being used as an input. |
| 6   | GPO6 | R/W | If set, GPIO_6 will be pulled low. If cleared, the output is not pulled low. This bit should be 0 if GPIO_6 is being used as an input. |
| 7   | GPO7 | R/W | If set, GPIO_7 will be pulled low. If cleared, the output is not pulled low. This bit should be 0 if GPIO_7 is being used as an input. |

#### 6.4.13.11 Register C6h PROCHOT Control

| Register Address | Read/Write | Register Name                 | Bit 7    | Bit 6    | Bit 5       | Bit 4       | Bit 3  | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|-------------------------------|----------|----------|-------------|-------------|--------|-------|-------|-------|---------------|
| C6h              | R/W        | PROCHOT <sub>T</sub> Override | FORCE_P1 | FORCE_P2 | P2_VRD2_DIS | P1_VRD1_DIS | PHT_DC |       |       | 00h   |               |

| Bit | Name        | R/W | Description  |
|-----|-------------|-----|--|
| 3:0 | PHT_DC      | R/W | PROCHOT <sub>T</sub> duty cycle select.  |
| 4   | P1_VRD1_DIS | R/W | When this bit is set by software, P1_PROCHOT <sub>T</sub> will not be asserted when P1_VRD_HOT is asserted.                |
| 5   | P2_VRD2_DIS | R/W | When this bit is set by software, P2_PROCHOT <sub>T</sub> will not be asserted when P2_VRD_HOT is asserted.                |
| 6   | FORCE_P1    | R/W | When this is set by software, P1_PROCHOT <sub>T</sub> will be asserted by the LM94 with the duty cycle selected by PHT_DC. |
| 7   | FORCE_P2    | R/W | When this is set by software, P2_PROCHOT <sub>T</sub> will be asserted by the LM94 with the duty cycle selected by PHT_DC. |

Note that if the P1P2\_PROCHOT bit is set to short the P<sub>x</sub>\_PROCHOT pins together, both P<sub>x</sub>\_PROCHOT outputs will be driven together, even if only one of the FORCE\_P<sub>x</sub> bits is set.

The period of the PWM signal driven on P<sub>x</sub>\_PROCHOT is 3.56 ms (80 internal 22.5 kHz clocks). The asserted time can be increased in 5 clock increments. 5 clocks is about 220 μs and would represent 6.25% percent throttled.

Possible settings for PHT\_DC:

| PHT_DC | Asserted Period |
|--------|-----------------|
| 0h     | 5 clocks        |
| 1h     | 10 clocks       |
| 2h     | 15 clocks       |
| 3h     | 20 clocks       |
| 4h     | 25 clocks       |
| 5h     | 30 clocks       |
| 6h     | 35 clocks       |
| 7h     | 40 clocks       |
| 8h     | 45 clocks       |
| 9h     | 50 clocks       |
| Ah     | 55 clocks       |
| Bh     | 60 clocks       |
| Ch     | 65 clocks       |
| Dh     | 70 clocks       |
| Eh     | 75 clocks       |
| Fh     | 80 clocks       |

#### 6.4.13.12 Register C7h PROCHOT Time Interval

| Register Address | Read/Write | Register Name         | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|-----------------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| C7h              | R/W        | PROCHOT Time Interval | P2_TI |       |       |       | P1_TI |       |       |       | 11h           |

| Bit | Name  | R/W | Description   |
|-----|-------|-----|---|
| 3:0 | P1_TI | R/W | Sets the monitoring interval for $\overline{P1\_PROCHOT}$ |
| 7:4 | P2_TI | R/W | Sets the monitoring interval for $\overline{P2\_PROCHOT}$ |

Possible settings for P1\_TI and P2\_TI:

| P1_TI or P2_TI | Monitoring Time Interval (seconds) |
|----------------|------------------------------------|
| 0h             | 0.73                               |
| 1h             | 1.46                               |
| 2h             | 2.9                                |
| 3h             | 5.8                                |
| 4h             | 11.7                               |
| 5h             | 23.3                               |
| 6h             | 46.6                               |
| 7h             | 93.2                               |
| 8h             | 186                                |
| 9h             | 372                                |
| Ah–Fh          | Reserved                           |

Note that changing this value while  $\overline{PROCHOT}$  measurements are running may cause the monitoring circuit to produce a erroneous value. To avoid alerts and invalid B\_Px\_PROCHOT or B\_Px\_PROCHOT Error Status values, only change this value while the chip is programmed for S3 or S4/5.

#### 6.4.13.13 Register C8h PWM1 Control 1

| Register Address | Read/Write | Register Name  | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|----------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| C8h              | R/W        | PWM1 Control 1 | VRD2  | VRD1  | PH2   | PH1   | LUT4  | LUT3  | LUT2  | LUT1  | 00h           |

| Bit | Name | R/W | Description  |
|-----|------|-----|--|
| 0   | LUT1 | R/W | If set, PWM1 will be bound to LUT 1.                     |
| 1   | LUT2 | R/W | If set, PWM1 will be bound to LUT 2.                     |
| 2   | LUT3 | R/W | If set, PWM1 will be bound to LUT 3.                     |
| 3   | LUT4 | R/W | If set, PWM1 will be bound to LUT 4.                     |
| 4   | PH1  | R/W | If set, PWM1 will be bound to $\overline{P1\_PROCHOT}$ . |
| 5   | PH2  | R/W | If set, PWM1 will be bound to $\overline{P2\_PROCHOT}$ . |
| 6   | VRD1 | R/W | If set, PWM1 will be bound to $\overline{VRD1\_HOT1}$ .  |
| 7   | VRD2 | R/W | If set, PWM1 will be bound to $\overline{VRD1\_HOT2}$ .  |

This register can bind PWM1 to several different control sources. The temperature zones control the PWM duty cycle using the table lookup function. The  $\overline{Px\_PROCHOT}$  and  $\overline{VRDx\_HOT}$  inputs control the PWM using the

ramp up/ramp down functions. If multiple control sources are bound to PWM1, the largest duty cycle being requested will be used.

**6.4.13.14 Register C9h PWM1 Control 2**

| Register Address | Read/Write | Register Name  | Bit 7  | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|----------------|--------|-------|-------|-------|-------|-------|-------|-------|---------------|
| C9h              | R/W        | PWM1 Control 2 | OVR_DC |       |       |       | PPL   | EPPL  | INV   | OVR   | 00h           |

| Bit | Name   | R/W | Description  |
|-----|--------|-----|--|
| 0   | OVR    | R/W | When set, enables manual duty cycle override for PWM1.   |
| 1   | INV    | R/W | Invert PWM1 output. When 0, 100% duty cycle corresponds to the PWM output continuously HIGH. When 1, 100% duty cycle corresponds to the PWM output continuously LOW.   |
| 2   | EPPL   | R/W | Enable PROCHOT PWM1 lock. When set, this bit causes bound PROCHOT events on PWM1 to trigger PPL (bit [3]). When cleared, PPL never gets set.   |
| 3   | PPL    | R/W | PROCHOT PWM1 lock. When set, this bit indicates that PWM1 is currently being held at 100% because a bound PROCHOT event occurred while EPPL (bit [2]) was set. This bit is cleared by writing a zero. Clearing this bit allows the fans to return to normal operation. This bit is not locked by the LOCK bit in the LM94 Configuration register.  |
| 7:4 | OVR_DC | R/W | This field sets the duty cycle that will be used by PWM1 whenever manual low resolution override mode is active. This field accepts 16 possible values that are mapped to duty cycles according to the table in the <a href="#">Section 6.2.18</a> section. Whenever this register is read, it returns the duty cycle that is currently being used by PWM1 regardless of whether override mode is active or not. The value read may not match the last value written if another control source is requesting a greater duty cycle. This field always returns 0h when the PWM1 spin up cycle is active. |

**6.4.13.15 Register CAh PWM1 Control 3**

| Register Address | Read/Write | Register Name  | Bit 7       | Bit 6 | Bit 5 | Bit 4     | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|----------------|-------------|-------|-------|-----------|-------|-------|-------|-------|---------------|
| CAh              | R/W        | PWM1 Control 3 | SU_DUR[2:0] |       |       | SU_DUR[3] | SU_DC |       |       |       | 00h           |

| Bit | Name        | R/W | Description   |
|-----|-------------|-----|---|
| 3:0 | SU_DC       | R/W | This field sets the duty cycle that will be used whenever PWM1 experiences a Spin-Up cycle. This field accepts 16 possible values that are mapped to duty cycles according to the table in the <a href="#">Section 6.2.18.2</a> section. Setting this field to 0h will effectively disable Spin-Up. |
| 4   | SU_DUR[3]   | R/W | Most significant bit that sets the Spin-up duration for PWM1.   |
| 7:0 | SU_DUR[2:0] | R/W | Least significant bits that set the Spin-Up duration for PWM1 least significant bits.   |

Bits 7:4 configure the spin-up duration. When the duty cycle of PWM1 changes from zero to a non-zero value, the spin-up sequence is activated for the specified amount of time. The available settings are defined according to this table:

| SU_DUR[3] (Bit 4) | SU_DUR[2:0] (Bits[7:5]) | Spin-Up Time     |
|-------------------|-------------------------|------------------|
| 0                 | 0h                      | Spin-up disabled |
| 0                 | 1h                      | 100 ms           |
| 0                 | 2h                      | 250 ms           |
| 0                 | 3h                      | 400 ms           |
| 0                 | 4h                      | 700 ms           |
| 0                 | 5h                      | 1 s              |
| 0                 | 6h                      | 2 s              |

| SU_DUR[3] (Bit 4) | SU_DUR[2:0] (Bits[7:5]) | Spin-Up Time |
|-------------------|-------------------------|--------------|
| 0                 | 7h                      | 4 s          |
| 1                 | 0h                      | 6 s          |
| 1                 | 1h                      | 8 s          |
| 1                 | 2h                      | 10 s         |
| 1                 | 3h                      | 12 s         |
| 1                 | 4h                      | 14 s         |
| 1                 | 5h                      | 16 s         |
| 1                 | 6h                      | 18 s         |
| 1                 | 7h                      | 20 s         |

#### 6.4.13.16 Register CBh PWM1 Control 4

| Register Address | Read/Write | Register Name  | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3      | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|----------------|-------|-------|-------|-------|------------|-------|-------|-------|---------------|
| CBh              | R/W        | PWM1 Control 4 | RES   | RES   | RES   | RES   | HF_LUT_MAP | FREQ1 |       |       | 00h           |

| Bit | Name       | R/W | Description  |
|-----|------------|-----|--|
| 2:0 | FREQ1      | R/W | PWM1 frequency control. Setting this value controls the frequency of the PWM1 output according to the table below.   |
| 3   | HF_LUT_MAP | R/W | Selects between two different maps for the PWM duty cycle assignment in the LUT when the PWM frequency is set to 22.5kHz. All 4 LUTs, VRD ramp, PROCHOT ramp, spin-up and low-resolution override will be affected by this bit. When this bit is set the LUT duty cycle assignment will increment 6.25% steps starting at 25%. When this bit is cleared the duty cycle mapping will match the Low Frequency table. This bit has no effect when the PWM frequency is set to anything other than 22.5kHz and the low PWM frequency mapping will be used. |
| 7:4 | RES        | R   | Reserved   |

| FREQ1 | Frequency of PWM1 (Hz) |
|-------|------------------------|
| 0h    | 22500                  |
| 1h    | 96                     |
| 2h    | 84                     |
| 3h    | 72                     |
| 4h    | 60                     |
| 5h    | 48                     |
| 6h    | 36                     |
| 7h    | 12                     |

**Table 6-13. LUT 1-4 Duty Cycle Assignment with PWM Frequency=22.5kHz as Controlled by the HF\_LUT\_MAP bit.**

| LUT Duty Cycle Assignments when HF_LUT_MAP='0' |                | LUT Duty Cycle Assignments when HF_LUT_MAP='1'<br>(Low PWM Frequency Mapping) |                |
|--|----------------|---|----------------|
| LUT Step                                       | Duty Cycle (%) | LUT Step  | Duty Cycle (%) |
| 1  | 25             | 1   | 25             |
| 2  | 31.25          | 2   | 28.57          |
| 3  | 37.5           | 3   | 32.14          |
| 4  | 43.75          | 4   | 35.71          |
| 5  | 50             | 5   | 39.29          |
| 6  | 56.25          | 6   | 42.86          |
| 7  | 62.25          | 7   | 46.43          |

**Table 6-13. LUT 1-4 Duty Cycle Assignment with PWM Frequency=22.5kHz as Controlled by the HF\_LUT\_MAP bit. (continued)**

| LUT Duty Cycle Assignments when HF_LUT_MAP='0' |       |  | LUT Duty Cycle Assignments when HF_LUT_MAP='1'<br>(Low PWM Frequency Mapping) |       |  |
|--|-------|--|---|-------|--|
| 8  | 68.75 |  | 8   | 50    |  |
| 9  | 75    |  | 9   | 53.57 |  |
| 10   | 81.25 |  | 10  | 57.14 |  |
| 11   | 87.5  |  | 11  | 71.43 |  |
| 12   | 93.75 |  | 12  | 85.71 |  |
| 13   | 100   |  | 13  | 100   |  |

**6.4.13.17 Register CCh PWM2 Control 1**

| Register Address | Read/Write | Register Name  | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|----------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| CCh              | R/W        | PWM2 Control 1 | VRD2  | VRD1  | PH2   | PH1   | LUT4  | LUT3  | LUT2  | LUT1  | 00h           |

| Bit | Name | R/W | Description                               |
|-----|------|-----|---|
| 0   | LUT1 | R/W | If set, PWM2 will be bound to LUT 1.      |
| 1   | LUT2 | R/W | If set, PWM2 will be bound to LUT 2.      |
| 2   | LUT3 | R/W | If set, PWM2 will be bound to LUT 3.      |
| 3   | LUT4 | R/W | If set, PWM2 will be bound to LUT 4.      |
| 4   | PH1  | R/W | If set, PWM2 will be bound to P1_PROCHOT. |
| 5   | PH2  | R/W | If set, PWM2 will be bound to P2_PROCHOT. |
| 6   | VRD1 | R/W | If set, PWM2 will be bound to VRD1_HOT.   |
| 7   | VRD2 | R/W | If set, PWM2 will be bound to VRD2_HOT.   |

This register can bind PWM2 to several different control sources. The temperature zones control the PWM duty cycle using the table lookup function. The Px\_PROCHOT and VRDx\_HOT inputs control the PWM using the ramp up/ramp down functions. If multiple control sources are bound to PWM2, the largest duty cycle being requested will be used.

**6.4.13.18 Register CDh PWM2 Control 2**

| Register Address | Read/Write | Register Name  | Bit 7  | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|----------------|--------|-------|-------|-------|-------|-------|-------|-------|---------------|
| CDh              | R/W        | PWM2 Control 2 | OVR_DC |       |       |       | PPL   | EPPL  | INV   | OVR   | 00h           |

| Bit | Name | R/W | Description   |
|-----|------|-----|---|
| 0   | OVR  | R/W | When set, enables manual duty cycle override for PWM2.  |
| 1   | INV  | R/W | Invert PWM1 output. When 0, 100% duty cycle corresponds to the PWM output continuously HIGH. When 1, 100% duty cycle corresponds to the PWM output continuously LOW.  |
| 2   | EPPL | R/W | Enable PROCHOT PWM2 lock. When set, this bit causes bound PROCHOT events on PWM2 to trigger PPL (bit [3]). When cleared, PPL never gets set.  |
| 3   | PPL  | R/W | PROCHOT PWM2 lock. When set, this bit indicates that PWM2 is currently being held at 100% because a bound PROCHOT event occurred while EPPL (bit [2]) was set. This bit is cleared by writing a zero. Clearing this bit allows the fans to return to normal operation. This bit is not locked by the LOCK bit in the LM94 Configuration register. |

| Bit | Name   | R/W | Description   |
|-----|--------|-----|---|
| 7:4 | OVR_DC | R/W | This field sets the duty cycle that will be used by PWM2 whenever manual low resolution override mode is active. This field accepts 16 possible values that are mapped to duty cycles according the table in the <a href="#">Section 6.2.18</a> section. Whenever this register is read, it returns the duty cycle that is currently being used by PWM2 regardless of whether override mode is active or not. The value read may not match the last value written if another control source is requesting a greater duty cycle. This field always returns 0h when the PWM2 spin up cycle is active. |

#### 6.4.13.19 Register CEh PWM2 Control 3

| Register Address | Read/Write | Register Name  | Bit 7       | Bit 6 | Bit 5 | Bit 4     | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|----------------|-------------|-------|-------|-----------|-------|-------|-------|-------|---------------|
| CEh              | R/W        | PWM2 Control 3 | SU_DUR[2:0] |       |       | SU_DUR[3] |       | SU_DC |       |       | 00h           |

| Bit | Name        | R/W | Description  |
|-----|-------------|-----|--|
| 3:0 | SU_DC       | R/W | This field sets the duty cycle that used whenever PWM2 experiences a Spin-Up cycle. This field accepts 16 possible values that are mapped to duty cycles according the table in the Auto-Fan Control section <a href="#">Section 6.2.18.2</a> . Setting this field to 0h effectively disables Spin-Up. |
| 4   | SU_DUR[3]   | R/W | Most significant bit that sets the spin-up duration for PWM2   |
| 7:5 | SU_DUR[2:0] | R/W | Least significant bits that set the Spin-Up duration for PWM2.   |

Bits 7:4 configure the spin-up duration. When the duty cycle of PWM2 changes from zero to a non-zero value, the spin-up sequence is activated for the specified amount of time. The available settings are defined according to this table:

| SU_DUR[3] (Bit 4) | SU_DUR[2:0] (Bits[7:5]) | Spin-Up Time     |
|-------------------|-------------------------|------------------|
| 0                 | 0h                      | Spin-up disabled |
| 0                 | 1h                      | 100 ms           |
| 0                 | 2h                      | 250 ms           |
| 0                 | 3h                      | 400 ms           |
| 0                 | 4h                      | 700 ms           |
| 0                 | 5h                      | 1 s              |
| 0                 | 6h                      | 2 s              |
| 0                 | 7h                      | 4 s              |
| 1                 | 0h                      | 6 s              |
| 1                 | 1h                      | 8 s              |
| 1                 | 2h                      | 10 s             |
| 1                 | 3h                      | 12 s             |
| 1                 | 4h                      | 14 s             |
| 1                 | 5h                      | 16 s             |
| 1                 | 6h                      | 18 s             |
| 1                 | 7h                      | 20 s             |

#### 6.4.13.20 Register CFh PWM2 Control 4

| Register Address | Read/Write | Register Name  | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3      | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|----------------|-------|-------|-------|-------|------------|-------|-------|-------|---------------|
| CFh              | R/W        | PWM2 Control 4 | RES   | RES   | RES   | RES   | HF_LUT_MAP | FREQ2 |       |       | 00h           |

| Bit | Name       | R/W | Description   |
|-----|------------|-----|---|
| 2:0 | FREQ2      | R/W | PWM2 frequency control. Controls the frequency of the PWM2 output in the same fashion as FREQ1 in the PWM1 Control 4 register.  |
| 3   | HF_LUT_MAP | R/W | Selects between two different maps for the PWM duty cycle assignment in the LUT when the PWM frequency is set to 22.5kHz. All 4 LUTs, VRD ramp, PROCHOT ramp, spin-up, and low-resolution override will be affected by this bit. When this bit is cleared the LUT duty cycle assignment will increment 6.25% steps starting at 25%. When this bit is set the duty cycle mapping will match the Low Frequency table. This bit has no effect when the PWM frequency is set to anything other than 22.5kHz and the low PWM frequency mapping will be used. |
| 7:4 | RES        | R   | Reserved  |

| FREQ1 | Frequency of PWM1 (Hz) |
|-------|------------------------|
| 0h    | 22500                  |
| 1h    | 96                     |
| 2h    | 84                     |
| 3h    | 72                     |
| 4h    | 60                     |
| 5h    | 48                     |
| 6h    | 36                     |
| 7h    | 12                     |

**Table 6-14. LUT 1-4 Duty Cycle Assignment with PWM Frequency=22.5kHz as Controlled by the HF\_LUT\_MAP bit.**

| LUT Duty Cycle Assignments when HF_LUT_MAP='0' |                | LUT Duty Cycle Assignments when HF_LUT_MAP='1'<br>(Low PWM Frequency Mapping) |                |
|--|----------------|---|----------------|
| LUT Step                                       | Duty Cycle (%) | LUT Step  | Duty Cycle (%) |
| 1  | 25             | 1   | 25             |
| 2  | 31.25          | 2   | 28.57          |
| 3  | 37.5           | 3   | 32.14          |
| 4  | 43.75          | 4   | 35.71          |
| 5  | 50             | 5   | 39.29          |
| 6  | 56.25          | 6   | 42.86          |
| 7  | 62.25          | 7   | 46.43          |
| 8  | 68.75          | 8   | 50             |
| 9  | 75             | 9   | 53.57          |
| 10   | 81.25          | 10  | 57.14          |
| 11   | 87.5           | 11  | 71.43          |
| 12   | 93.75          | 12  | 85.71          |
| 13   | 100            | 13  | 100            |

#### 6.4.13.21 Register D0h–D3h LUT 1 to 4 Base Temperatures

| Register Address | Read/Write | Register Name          | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|------------------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| D0h              | R/W        | LUT 1 Base Temperature | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| D1h              | R/W        | LUT 2 Base Temperature | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| D2h              | R/W        | LUT 3 Base Temperature | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| D3h              | R/W        | LUT 4 Base Temperature | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |

The value in this register is used as the base in the temperature calculation for the auto fan control look-up table. These registers use the standard temperature format (8-bit signed data). The look-up table contains the temperature offsets. The offsets are added to the base temperature to determine the true temperature to be used for each table entry for auto fan control.

#### 6.4.13.22 Register D4h–DFh Lookup Table Steps—LUT 1/2 and LUT 3/4 Offset Temperature

| Register Address | Read/Write | Register Name       | Bit 7         | Bit 6 | Bit 5 | Bit 4 | Bit 3         | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|---------------------|---------------|-------|-------|-------|---------------|-------|-------|-------|---------------|
| D4h              | R/W        | Step 2 Temp Offset  | LUT3/4_STEP2  |       |       |       | LUT1/2_STEP2  |       |       |       | 00h           |
| D5h              | R/W        | Step 3 Temp Offset  | LUT3/4_STEP3  |       |       |       | LUT1/2_STEP3  |       |       |       | 00h           |
| D6h              | R/W        | Step 4 Temp Offset  | LUT3/4_STEP4  |       |       |       | LUT1/2_STEP4  |       |       |       | 00h           |
| D7h              | R/W        | Step 5 Temp Offset  | LUT3/4_STEP5  |       |       |       | LUT1/2_STEP5  |       |       |       | 00h           |
| D8h              | R/W        | Step 6 Temp Offset  | LUT3/4_STEP6  |       |       |       | LUT1/2_STEP6  |       |       |       | 00h           |
| D9h              | R/W        | Step 7 Temp Offset  | LUT3/4_STEP7  |       |       |       | LUT1/2_STEP7  |       |       |       | 00h           |
| DAh              | R/W        | Step 8 Temp Offset  | LUT3/4_STEP8  |       |       |       | LUT1/2_STEP8  |       |       |       | 00h           |
| DBh              | R/W        | Step 9 Temp Offset  | LUT3/4_STEP9  |       |       |       | LUT1/2_STEP9  |       |       |       | 00h           |
| DCh              | R/W        | Step 10 Temp Offset | LUT3/4_STEP10 |       |       |       | LUT1/2_STEP10 |       |       |       | 00h           |
| DDh              | R/W        | Step 11 Temp Offset | LUT3/4_STEP11 |       |       |       | LUT1/2_STEP11 |       |       |       | 00h           |

| Register Address | Read/Write | Register Name       | Bit 7         | Bit 6 | Bit 5 | Bit 4 | Bit 3         | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|---------------------|---------------|-------|-------|-------|---------------|-------|-------|-------|---------------|
| DEh              | R/W        | Step 12 Temp Offset | LUT3/4_STEP12 |       |       |       | LUT1/2_STEP12 |       |       |       | 00h           |
| DFh              | R/W        | Step 13 Temp Offset | LUT3/4_STEP13 |       |       |       | LUT1/2_STEP13 |       |       |       | 00h           |

There are two look up tables of 13 steps (12 offsets), one for LUT 1 and 2 the other for LUT 3 and 4. Each 8-bit offset register contains the offset temperature for LUT 1 and 2 as well as the offset temperature for LUT 3 and 4. The format for the offsets is a 4-bit unsigned value, and one LSB is either 1°C or 0.5°C. The offset resolution is controlled by LT34\_RS and LT12\_RS bits found in the Special Function Control 2 register (at address BDh). Therefore, the offset range is variable as well and is either 15°C to 0°C or 7.5°C to 0°C.

See the [Section 6.2.18](#) section for information on how the base temperature/lookup table should be used for controlling the PWM output(s).

#### 6.4.13.23 Register E0h Special Function TACH to PWM Binding

| Register Address | Read/Write | Register Name                        | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|--------------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| E0h              | R/W        | Special Function TACH to PWM Binding | T4P2  | T4P1  | T3P2  | T3P1  | T2P2  | T2P1  | T1P2  | T1P1  | 00h           |

| Bit | Name | R/W | Description                     |
|-----|------|-----|---------------------------------|
| 0   | T1P1 | R/W | If set, TACH1 is bound to PWM1. |
| 1   | T1P2 | R/W | If set, TACH1 is bound to PWM2. |
| 2   | T2P1 | R/W | If set, TACH2 is bound to PWM1. |
| 3   | T2P2 | R/W | If set, TACH2 is bound to PWM2. |
| 4   | T3P1 | R/W | If set, TACH3 is bound to PWM1. |
| 5   | T3P2 | R/W | If set, TACH3 is bound to PWM2. |
| 6   | T4P1 | R/W | If set, TACH4 is bound to PWM1. |
| 7   | T4P2 | R/W | If set, TACH4 is bound to PWM2. |

If a TACH channel is bound to a PWM channel, TACH errors on that channel are automatically masked when the bound PWM is at 0% duty cycle or performing spin-up. Behavior is undefined if a TACH channel is bound to both PWM outputs. This register must be setup when Smart Tach Mode is enabled in register BDh, Special Function Control 2, and when Tach Boost is enabled in register E1h, Tachometer Fan Boost Control.

#### 6.4.13.24 Register E1h Tachometer Fan Boost Control Register

| Register Address | Read/Write | Register Name          | Bit 7 | Bit 6 | Bit 5    | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|------------------------|-------|-------|----------|-------|-------|-------|-------|-------|---------------|
| E1h              | R/W        | Tach Fan Boost Control | RES   | TBS   | TBT[5:0] | 3Fh   |       |       |       |       |               |

| Lock | Bit | Name      | R/W | Description  |
|------|-----|-----------|-----|--|
| X    | 5:0 | TBT[5:0]] | R/W | TACH error fan boost enable timeout. Set to 63 (3Fh) to disable the TACH error fan boost feature (default). Values other than 63 enable the TACH error fan boost feature and set the timeout according to the following table. |

| Lock | Bit | Name | R/W | Description   |
|------|-----|------|-----|---|
|      | 6   | TBS  | R/W | TACH boost status: When set, this bit indicates that the TACH error boost has been triggered and is currently requesting 100% PWM. If bits [5:0] are configured for an infinite timeout, and the TACH error(s) have ceased, then writing a zero to this bit will un-trigger the TACH boost. If TACH error boost is disabled, this bit always returns a 0. |
|      | 7   | RES  | R   | Reserved  |

**Table 6-15. Timeout Assignments for TBT[5:0]**

| TBT[5:0] | Timeout/Function   |
|----------|--|
| 0        | 0  |
| 1        | 3  |
| .        | .  |
| .        | .  |
| .        | .  |
| N        | $N * 32 * 0.091 \text{ sec}$   |
| 60       | 175  |
| 61       | 178  |
| 62       | Infinite setting (software must clear bit 6 of this register to reset) |
| 63       | Disabled   |

**6.4.13.25 Register E2h LM94 Status Control**

| Register Address | Read/Write | Register Name       | Bit 7   | Bit 6    | Bit 5     | Bit 4   | Bit 3   | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|---------------------|---------|----------|-----------|---------|---------|-------|-------|-------|---------------|
| E2h              | R/W        | LM94 Status/Control | BMC_ERR | HOST_ERR | TACH_EDGE | GPI5_AM | GPI4_AM | ASF   | OVRID |       | 00h           |

| Lock     | Bit | Name      | R/W | Description   |
|----------|-----|-----------|-----|---|
|          | 0   | OVRID     | R/W | If this bit is set, all PWM outputs go to 100% duty cycle.  |
| <b>X</b> | 1   | ASF       | R/W | If this bit is set, BMC error registers support ASF, i.e. reset on read. When not in ASF mode, a write "1" is required to clear the bits in the BMC error status registers.   |
|          | 2   | GPI4_AM   | R/W | GPI4 Auto Mask Enable<br>If this bit is set, an error event on GPI4 causes all other error events to be masked.<br>The BMC Error Status registers do not reflect any new error events until the GPI4_ERR bit is cleared in the B_GPI Error Status register. The HOST Error Status registers do not reflect any new error events until the GPI4_ERR bit is cleared in the H_GPI Error Status register.<br>If a CPU_THERMTRIP signal is connected to GPIO4, this ensures that unwanted error events do not fire once CPU_THERMTRIP is asserted. |
|          | 3   | GP15_AM   | R/W | GPI5 Auto Mask Enable<br>This bit works exactly the same as GPI4_AM, but applies to GPI5.   |
|          | 5:4 | TACH_EDGE | R/W | This field determines what type of edges are used for measuring fan tach pulses. This effects all four tachometer inputs.   |
|          | 6   | HOST_ERR  | R   | This bit gets set if any error bit is set in any of the Host Error Status registers (H_).   |
|          | 7   | BMC_ERR   | R   | This bit gets set if any error bit is set in any of the BMC Error Status registers (B_). When this bit is set, ALERT are asserted if enabled.   |

| TACH_EDGE | Edge Type Used for Tachometer Measurements  |
|-----------|---|
| 0h        | Either rising or falling edges may be used. |
| 1h        | Rising edges only                           |
| 2h        | Falling edges only                          |

| TACH_EDGE | Edge Type Used for Tachometer Measurements |
|-----------|--|
| 3h        | Reserved                                   |

#### 6.4.13.26 Register E3h LM94 Configuration

| Register Address | Read/Write | Register Name      | Bit 7 | Bit 6 | Bit 5         | Bit 4        | Bit 3    | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|--------------------|-------|-------|---------------|--------------|----------|-------|-------|-------|---------------|
| E3h              | R/W        | LM94 Configuration | READY | RES   | ALERT_COMP_EN | P1P2_PROCHOT | ALERT_EN | GMSK  | LOCK  | START | 00h           |

| Lock | Bit | Name          | R/W | Description  |
|------|-----|---------------|-----|--|
| x    | 0   | START         | R/W | When this bit is 0, the LM94 operates in basic mode. <b>All</b> error events are masked. The auto fan control algorithm is disabled. Both PWMs are set to 0%. All monitoring functions are active and the value registers are updated. Once this bit is set, error events are no longer globally masked, and the auto-fan control algorithm is enabled. Fan boost uses the programmed values. It is expected that all limit and setup registers are set by BIOS or application software prior to setting this bit. |
| X    | 1   | LOCK          | R/W | Setting this bit locks all registers and register bits that are indicated as lockable. Lockable registers have an “x” in the <b>Lock</b> column of their description. This register is locked once it is set. This bit can only be cleared by an external device asserting $\overline{\text{RESET}}$ .   |
|      | 2   | GMSK          | R/W | Global Mask<br>When this bit is set by software, <b>all</b> error events are masked. Setting this bit does not effect any other mask registers or value registers.   |
|      | 3   | ALERT_EN      | R/W | When this bit is set, the $\overline{\text{ALERT}}$ output is enabled. If this bit is cleared, the $\overline{\text{ALERT}}$ output is disabled.   |
|      | 4   | P1P2_PROCHOT  | R/W | In some configurations it may be required to have both processors throttling at the same rate. When this bit is set, the LM94 connects P1_PROCHOT to P2_PROCHOT. If P1_PROCHOT and P2_PROCHOT are already shorted by some other means, this bit should NOT be set. Doing so would cause both PROCHOT signals to be stuck low until this bit is cleared.  |
|      | 5   | ALERT_COMP_EN | R/W | When this bit is set the ALERT output will function in the thermal comparator mode. In the thermal comparator mode ALERT will be asserted only for unmasked thermal error events. ALERT will be de-asserted immediately when the error event ceases.   |
|      | 6   | RES           | R/W | Reserved   |
|      | 7   | READY         | R   | The LM94 sets this bit automatically after valid data has been collected for all temperatures and voltages. Software should not use any temperature or voltage values until this bit has been set.   |

#### 6.4.14 Sleep State Control and Mask Registers

##### 6.4.14.1 Register E4h Sleep State Control

| Register Address | Read/Write | Register Name       | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|---------------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| E4h              | R/W        | Sleep State Control | RES   |       |       |       |       |       | SB    |       | 03h           |

| Bit | Name | R/W | Description  |
|-----|------|-----|--|
| 1:0 | SB   | R/W | Sleep State Control. Setting this field tells the LM94 which sleep state the system is in. Several error events are masked depending on the state of this field. |
| 7:2 | RES  | R   | Reserved   |

| SB | Description  |
|----|--|
| 00 | Sleep state = S0<br>Do not mask errors.  |
| 01 | Sleep state = S1<br>Mask errors according to S1 mask registers and standard S1 masking.  |
| 10 | Sleep state = S3<br>Mask errors according to S3 mask registers and standard S3 masking.  |
| 11 | Sleep state = S4/5<br>Mask errors according to S4/5 mask registers and standard S4/5 masking.<br>This mode is activated automatically if the <b>RESET</b> input is asserted. |

#### 6.4.14.2 Register E5h S1 GPI Mask

| Register Address | Read/Write | Register Name | Bit 7       | Bit 6       | Bit 5       | Bit 4       | Bit 3       | Bit 2       | Bit 1       | Bit 0       | Default Value |
|------------------|------------|---------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|---------------|
| E5h              | R/W        | S1 GPI Mask   | GPI7_S1_MSK | GPI6_S1_MSK | GPI5_S1_MSK | GPI4_S1_MSK | GPI3_S1_MSK | GPI2_S1_MSK | GPI1_S1_MSK | GPI0_S1_MSK | FFh           |

| Bit | Name        | R/W | Description                                       |
|-----|-------------|-----|---|
| 0   | GPI0_S1_MSK | R/W | If set, GPI0 errors are masked in S1 sleep state. |
| 1   | GPI1_S1_MSK | R/W | If set, GPI1 errors are masked in S1 sleep state. |
| 2   | GPI2_S1_MSK | R/W | If set, GPI2 errors are masked in S1 sleep state. |
| 3   | GPI3_S1_MSK | R/W | If set, GPI3 errors are masked in S1 sleep state. |
| 4   | GPI4_S1_MSK | R/W | If set, GPI4 errors are masked in S1 sleep state. |
| 5   | GPI5_S1_MSK | R/W | If set, GPI5 errors are masked in S1 sleep state. |
| 6   | GPI6_S1_MSK | R/W | If set, GPI6 errors are masked in S1 sleep state. |
| 7   | GPI7_S1_MSK | R/W | If set, GPI7 errors are masked in S1 sleep state. |

#### 6.4.14.3 Register E6h S1 Tach Mask

| Register Address | Read/Write | Register Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3        | Bit 2        | Bit 1        | Bit 0        | Default Value |
|------------------|------------|---------------|-------|-------|-------|-------|--------------|--------------|--------------|--------------|---------------|
| E6h              | R/W        | S1 Tach Mask  | RES   |       |       |       | TACH4_S1_MSK | TACH3_S1_MSK | TACH2_S1_MSK | TACH1_S1_MSK | 0Fh           |

| Bit | Name         | R/W | Description  |
|-----|--------------|-----|--|
| 0   | TACH1_S1_MSK | R/W | If set, Tach1 errors are masked in S1 sleep state. |
| 1   | TACH2_S1_MSK | R/W | If set, Tach2 errors are masked in S1 sleep state. |
| 2   | TACH3_S1_MSK | R/W | If set, Tach3 errors are masked in S1 sleep state. |
| 3   | TACH4_S1_MSK | R/W | If set, Tach4 errors are masked in S1 sleep state. |
| 7:4 | RES          | R   | Reserved   |

#### 6.4.14.4 Register E7h S3 GPI Mask

| Register Address | Read/Write | Register Name | Bit 7       | Bit 6       | Bit 5       | Bit 4       | Bit 3       | Bit 2       | Bit 1       | Bit 0       | Default Value |
|------------------|------------|---------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|---------------|
| E7h              | R/W        | S3 GPI Mask   | GPI7_S3_MSK | GPI6_S3_MSK | GPI5_S3_MSK | GPI4_S3_MSK | GPI3_S3_MSK | GPI2_S3_MSK | GPI1_S3_MSK | GPI0_S3_MSK | FFh           |

| Bit | Name        | R/W | Description                                       |
|-----|-------------|-----|---|
| 0   | GPI0_S3_MSK | R/W | If set, GPI0 errors are masked in S3 sleep state. |
| 1   | GPI1_S3_MSK | R/W | If set, GPI1 errors are masked in S3 sleep state. |
| 2   | GPI2_S3_MSK | R/W | If set, GPI2 errors are masked in S3 sleep state. |

| Bit | Name        | R/W | Description                                       |
|-----|-------------|-----|---|
| 3   | GPI3_S3_MSK | R/W | If set, GPI3 errors are masked in S3 sleep state. |
| 4   | GPI4_S3_MSK | R/W | If set, GPI4 errors are masked in S3 sleep state. |
| 5   | GPI5_S3_MSK | R/W | If set, GPI5 errors are masked in S3 sleep state. |
| 6   | GPI6_S3_MSK | R/W | If set, GPI6 errors are masked in S3 sleep state. |
| 7   | GPI7_S3_MSK | R/W | If set, GPI7 errors are masked in S3 sleep state. |

#### 6.4.14.5 Register E8h S3 Tach Mask

| Register Address | Read/Write | Register Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3        | Bit 2        | Bit 1        | Bit 0        | Default Value |
|------------------|------------|---------------|-------|-------|-------|-------|--------------|--------------|--------------|--------------|---------------|
| E8h              | R/W        | S3 Tach Mask  | RES   |       |       |       | TACH4_S3_MSK | TACH3_S3_MSK | TACH2_S3_MSK | TACH1_S3_MSK | 0Fh           |

| Bit | Name         | R/W | Description  |
|-----|--------------|-----|--|
| 0   | TACH1_S3_MSK | R/W | If set, Tach1 errors are masked in S3 sleep state. |
| 1   | TACH2_S3_MSK | R/W | If set, Tach2 errors are masked in S3 sleep state. |
| 2   | TACH3_S3_MSK | R/W | If set, Tach3 errors are masked in S3 sleep state. |
| 3   | TACH4_S3_MSK | R/W | If set, Tach4 errors are masked in S3 sleep state. |
| 7:4 | RES          | R   | Reserved   |

#### 6.4.14.6 Register E9h S3 Temperature/Voltage Mask

| Register Address | Read/Write | Register Name   | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3       | Bit 2        | Bit 1        | Bit 0        | Default Value |
|------------------|------------|-----------------|-------|-------|-------|-------|-------------|--------------|--------------|--------------|---------------|
| E9h              | R/W        | S3 Voltage Mask | RES   |       |       |       | TEMP_S3_MSK | AIN14_S3_MSK | AIN13_S3_MSK | AIN12_S3_MSK | 07h           |

| Bit | Name         | R/W | Description   |
|-----|--------------|-----|---|
| 0   | AIN12_S3_MSK | R/W | If set, AIN12 errors as masked in S3 sleep state.   |
| 1   | AIN13_S3_MSK | R/W | If set, AIN13 errors as masked in S3 sleep state.   |
| 2   | AIN14_S3_MSK | R/W | If set, AIN14 errors as masked in S3 sleep state.   |
| 3   | TEMP_S3_MSK  | R/W | If set, temperature errors and diode fault errors for zones 1 and 2 are masked in S3 sleep state. |
| 7:3 | RES          | R   | Reserved  |

#### 6.4.14.7 Register EAh S4/5 GPI Mask

| Register Address | Read/Write | Register Name | Bit 7         | Bit 6         | Bit 5         | Bit 4         | Bit 3         | Bit 2         | Bit 1         | Bit 0         | Default Value |
|------------------|------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
| EAh              | R/W        | S4/5 GPI Mask | GPI7_S4/5_MSK | GPI6_S4/5_MSK | GPI5_S4/5_MSK | GPI4_S4/5_MSK | GPI3_S4/5_MSK | GPI2_S4/5_MSK | GPI1_S4/5_MSK | GPI0_S4/5_MSK | FFh           |

| Bit | Name          | R/W | Description   |
|-----|---------------|-----|---|
| 0   | GPI0_S4/5_MSK | R/W | If set, GPI0 errors are masked in S4/5 sleep state. |
| 1   | GPI1_S4/5_MSK | R/W | If set, GPI1 errors are masked in S4/5 sleep state. |
| 2   | GPI2_S4/5_MSK | R/W | If set, GPI2 errors are masked in S4/5 sleep state. |
| 3   | GPI3_S4/5_MSK | R/W | If set, GPI3 errors are masked in S4/5 sleep state. |
| 4   | GPI4_S4/5_MSK | R/W | If set, GPI4 errors are masked in S4/5 sleep state. |
| 5   | GPI5_S4/5_MSK | R/W | If set, GPI5 errors are masked in S4/5 sleep state. |
| 6   | GPI6_S4/5_MSK | R/W | If set, GPI6 errors are masked in S4/5 sleep state. |

| Bit | Name          | R/W | Description   |
|-----|---------------|-----|---|
| 7   | GPI7_S4/5_MSK | R/W | If set, GPI7 errors are masked in S4/5 sleep state. |

#### 6.4.14.8 Register EBh S4/5 Temperature/Voltage Mask

| Register Address | Read/Write | Register Name     | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3         | Bit 2          | Bit 1          | Bit 0          | Default Value |
|------------------|------------|-------------------|-------|-------|-------|-------|---------------|----------------|----------------|----------------|---------------|
| EBh              | R/W        | S4/5 Voltage Mask | RES   |       |       |       | TEMP_S4/5_MSK | AIN14_S4/5_MSK | AIN13_S4/5_MSK | AIN12_S4/5_MSK | 07h           |

| Bit | Name           | R/W | Description   |
|-----|----------------|-----|---|
| 0   | AIN12_S4/5_MSK | R/W | If set, AIN12 errors as masked in S4/5 sleep state.   |
| 1   | AIN13_S4/5_MSK | R/W | If set, AIN13 errors as masked in S4/5 sleep state.   |
| 2   | AIN14_S4/5_MSK | R/W | If set, AIN14 errors as masked in S4/5 sleep state.   |
| 3   | TEMP_S4/5_MSK  | R/W | If set, temperature errors and diode fault errors for zones 1 and 2 are masked in S4/5 sleep state. |
| 7:3 | RES            | R   | Reserved  |

### 6.4.15 Other Mask Registers

#### 6.4.15.1 Register ECh GPI Error Mask

| Register Address | Read/Write | Register Name  | Bit 7    | Bit 6    | Bit 5    | Bit 4    | Bit 3    | Bit 2    | Bit 1    | Bit 0    | Default Value |
|------------------|------------|----------------|----------|----------|----------|----------|----------|----------|----------|----------|---------------|
| ECh              | R/W        | GPI Error Mask | GPI7_MSK | GPI6_MSK | GPI5_MSK | GPI4_MSK | GPI3_MSK | GPI2_MSK | GPI1_MSK | GPI0_MSK | FFh           |

| Bit | Name     | R/W | Description   |
|-----|----------|-----|---|
| 0   | GPI0_MSK | R/W | When this bit is set, GPI0 error events are masked. |
| 1   | GPI1_MSK | R/W | When this bit is set, GPI1 error events are masked. |
| 2   | GPI2_MSK | R/W | When this bit is set, GPI2 error events are masked. |
| 3   | GPI3_MSK | R/W | When this bit is set, GPI3 error events are masked. |
| 4   | GPI4_MSK | R/W | When this bit is set, GPI4 error events are masked. |
| 5   | GPI5_MSK | R/W | When this bit is set, GPI5 error events are masked. |
| 6   | GPI6_MSK | R/W | When this bit is set, GPI6 error events are masked. |
| 7   | GPI7_MSK | R/W | When this bit is set, GPI7 error events are masked. |

These bits mask the corresponding bits in the B\_ and H\_GPI Error Status Registers. They do not effect the GPI State register.

#### 6.4.15.2 Register EDh Miscellaneous Error Mask

| Register Address | Read/Write | Register Name            | Bit 7 | Bit 6 | Bit 5 | Bit 4      | Bit 3      | Bit 2     | Bit 1     | Bit 0    | Default Value |     |
|------------------|------------|--------------------------|-------|-------|-------|------------|------------|-----------|-----------|----------|---------------|-----|
| EDh              | R/W        | Miscellaneous Error Mask | RES   |       |       | DVccp2_MSK | DVccp1_MSK | SCSI2_MSK | SCSI1_MSK | VRD2_MSK | VRD1_MSK      | 3Fh |

| Bit | Name      | R/W | Description  |
|-----|-----------|-----|--|
| 0   | VRD1_MSK  | R/W | When this bit is set, $\overline{\text{VRD1\_HOT}}$ error events are masked. |
| 1   | VRD2_MSK  | R/W | When this bit is set, $\overline{\text{VRD2\_HOT}}$ error events are masked. |
| 2   | SCSI1_MSK | R/W | When this bit is set, $\overline{\text{GPI8}}$ error events are masked.      |
| 3   | SCSI2_MSK | R/W | When this bit is set, $\overline{\text{GPI9}}$ error events are masked.      |

| Bit | Name       | R/W | Description   |
|-----|------------|-----|---|
| 4   | DVccp1_MSK | R/W | When this bit is set, dynamic Vccp limit error events for AD_IN7 (CPU1) are masked. |
| 5   | DVccp2_MSK | R/W | When this bit is set, dynamic Vccp limit error events for AD_IN8 (CPU2) are masked. |
| 7:6 | RES        | R   | Reserved  |

#### 6.4.15.3 Register EE and EFh Zone 1a and Zone 2a Adjustment Register

| Register Address | Read/Write | Register Name  | Bit 7 | Bit 6 | Bit 5           | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|----------------|-------|-------|-----------------|-------|-------|-------|-------|-------|---------------|
| EEh              | R/W        | Zone 1a Adjust | RES   | RES   | Z1a_ADJUST[5:0] |       |       |       |       | 00h   |               |
| EFh              | R/W        | Zone 2a Adjust | RES   | RES   | Z2a_ADJUST[5:0] |       |       |       |       | 00h   |               |

| Bit | Name                               | R/W | Description   |
|-----|------------------------------------|-----|---|
| 5:0 | Z1a_ADJUST[5:0] or Z2a_ADJUST[5:0] | R/W | 6-bit signed 2's complement offset adjustment. This value is added to all zone 1a and 2a temperature measurements as they are made. All LM94 registers and functions behave as if the resulting temperature was the true measured temperature. This register allows offset adjustments from +31°C to -32°C in 1°C steps. The format is sign two's complement. |
| 7:6 | RES                                | R   | Reserved  |

## 7 Application and Implementation

### 7.1 Application Information

#### 7.1.1 Power On

The LM94 generates a power on reset signal on  $\overline{\text{RESET}}$  when power is applied for the first time to the part.

#### 7.1.2 Resets

Upon power up, the  $\overline{\text{RESET}}$  output is asserted when the voltage on the power supply crosses the power-on-reset threshold level (see the [Electrical Characteristics](#)). The  $\overline{\text{RESET}}$  output is open-drain and should be used with an external pull-up resistor connected to  $V_{DD}$ . Once the power on reset has completed, the  $\overline{\text{RESET}}$  pin becomes an input and 10  $\mu\text{s}$  after assertion of  $\overline{\text{RESET}}$  the LOCK bit in the LM94 Configuration register shall be cleared. In addition, 10  $\mu\text{s}$  after assertion of  $\overline{\text{RESET}}$  the sleep control register shall be automatically set to S4/S5. This causes several error events to be masked according to the S4/S5 masking definitions. Since the  $\overline{\text{RESET}}$  pin becomes an active input, it must not be left floating at any time as this may cause the LM94 to drift into S4/S5 and thus have unpredictable behavior.  $\overline{\text{RESET}}$  must be asserted for more than 4 $\mu\text{s}$  in order to ensure detection.

| Register Types              | Power On Reset | External Reset |
|-----------------------------|----------------|----------------|
| Factory regs                | x              |                |
| BMC Error Status regs       | x              |                |
| Host Error Status regs      | x              |                |
| Value regs                  |                |                |
| Limit regs                  | x              |                |
| Setup regs                  | x              |                |
| LM94 Configuration Lock Bit | x              | x              |
| LM94 Configuration GMSK Bit | x (reset)      |                |
| Sleep Mask                  | x              |                |
| Sleep State Control         |                | x              |
| Other Mask regs             | x              |                |

All other registers are not effected by power on reset or external reset.

#### 7.1.3 Address Selection

LM94 is designed to be used primarily in dual processor server systems that may require only one monitoring device.

If multiple LM94 devices are implemented in a system, they must have unique SMBus slave addresses. See the [Section 6.3.1.1](#) for more information.

The board designer may apply a 10 k $\Omega$  pull-down and/or pull-up resistors to ground and/or to 3.3V SB  $V_{DD}$  on the ADDR\_SEL pin. The LM94 is designed to work with resistors of 5% tolerance for the case where two resistors are required. Upon the first SMBus communication to the part, the LM94 assigns itself an SMBus address according to the ADDR\_SEL input.

| Address Select               | Board Implementation  | SMBus Address |
|------------------------------|---|---------------|
| less-than 10% of $V_{DD}$    | Pulled to ground through a 10 k $\Omega$ resistor             | 0101 100b     |
| $\approx V_{DD}/2$           | 10 k $\Omega$ (5%) Resistor to 3.3V SB $V_{DD}$ and to Ground | 0101 110b     |
| greater-than 90% of $V_{DD}$ | Pulled to 3.3V SB $V_{DD}$ through a 10 k $\Omega$ resistor   | 0101 101b     |

### 7.1.4 Device Setup

BIOS executes the following steps to configure the registers in the LM94. All steps may not be necessary if default values are acceptable.

Set limits and parameters (not necessarily in this order):

- Set up Fan control
- Set up PWM temperature bindings
- Set fan tach limits
- Set fan boost temperature and hysteresis
- Set the VRD\_HOT and PROCHOT PWM ramp control rate
- Enable Smart Tach Mode and Tachometer Input to PWM binding (required with PWM drive of fan ground or power pins)
- Set the temperature absolute limits
- Set the temperature hysteresis values
- Set temperature filtered or unfiltered usage
- Set the Zone Adjustment Offset temperature
- Set the PROCHOT override and time interval values
- Set the PROCHOT user limit
- Enable THERMTRIP masking of error events (if GPIO4 and GPIO5 are used as THERMTRIP inputs)
- Set voltage sensor limits and hysteresis
- Set the Dynamic Vccp offset limits
- Set the Sleep State control and mask registers
- Set Other Mask Registers (GPI Error, VRDx\_HOT, and Dynamic Vccp limit checking)
- Set start bit to select user values and unmask error events
- Set the sleep state to 0
- Set Lock bit to lock the limit and parameter registers (optional)

### 7.1.5 Round Robin Voltage/Temperature Conversion Cycle

The LM94 monitoring function is started as soon as the part is powered up. The LM94 performs a “round robin” sampling of the inputs, in the order shown below. Each cycle of the round robin is completed in less than 100 ms.

The results of the sampling and conversions can be found in the value registers and are available at any time.

| Channel # | Input        | Typical Assignment                         |
|-----------|--------------|--|
| 3         | Temp Zone 3  | Internal Temperature Reading               |
| 1         | Temp Zone 1a | Remote Diode 1a Temp Reading               |
|           | Temp Zone 1b | Remote Diode 1b Temp Reading (if selected) |
| 2         | Temp Zone 2a | Remote Diode 2a Temp Reading               |
|           | Temp Zone 2b | Remote Diode 2b Temp Reading (if selected) |
| 4         | AIN1         | +12V1 (if selected)                        |
| 5         | AIN2         | +12V2 (if selected)                        |
| 6         | AIN3         | +12V3                                      |
| 7         | AIN4         | FSB_Vtt                                    |
| 8         | AIN5         | 3GIO/PXH/MCH_Core                          |
| 9         | AIN6         | ICH_Core                                   |
| 10        | AIN7         | CPU_1Vccp                                  |
| 11        | AIN8         | CPU2_Vccp                                  |
| 12        | AIN9         | 3.3V                                       |
| 13        | AIN10        | +5V  |
| 14        | AIN11        | SCSI_Core                                  |
| 15        | AIN12        | Mem_Core                                   |

| Channel # | Input | Typical Assignment                  |
|-----------|-------|-------------------------------------|
| 16        | AIN13 | Mem_Vtt                             |
| 17        | AIN14 | GBIT_Core                           |
| 18        | AIN15 | -12V                                |
| 19        | AIN16 | 3.3V SB V <sub>DD</sub> Supply Rail |

### 7.1.6 Error Status Registers

The LM94 contains several error status registers for the BMC side, and duplicated error status registers for the Host side. These registers are used to reflect the state of all the possible error conditions that the LM94 monitors.

The BMC/Host Error Status registers hold a set bit until the event is cleared by software, even if the condition causing the error event goes away.

To clear a bit in the Error Status registers, a '1' has to be written to the specific bit that is required to be cleared. If the event that caused the error is no longer active then the bit is cleared.

Clearing a bit in a BMC Error Status register does not clear the corresponding bit in the Host Error Status register or vice versa.

#### 7.1.6.1 ASF Mode

Error Status registers function allow the LM94 to act as a legacy sensor (6.1.2 of ASF spec DSP0114 rev 2) and to easily connect to the SMBus of an ASF capable NIC chip.

The LM94 can be placed into ASF mode by setting the appropriate bit in the LM94 Status/Control register. Once this bit is set, the BMC Error Status registers become read-to-clear. Writing a '1' to clear a particular bit is also allowed in ASF mode. The Host Error Status registers are not effected by ASF mode.

### 7.1.7 Masking, Error Status and $\overline{\text{ALERT}}$

Masking is always applied to bits in the HOST and BMC Error Status registers. If an event is masked, the corresponding error bit in the HOST or BMC Error Status registers is prevented from ever being set. As a result, this prevents the event from ever causing  $\overline{\text{ALERT}}$  to be asserted. Masking an event does not clear its associated Error Status bit if it is currently set.

Voltage errors are masked by writing a high voltage limit value of FFh. This is the default high limit for all voltages.

Temperature errors are masked by writing a high temperature limit value of 80h. This is the default high limit for all temperatures. Masking a temperature channel masks both temperature errors and diode fault errors.

The GPI Mask register allows GPI errors to be masked. Any bits that are set in this register mask events for the corresponding GPIO\_x pin.

User  $\overline{\text{PROCHOT}}$  status is not really an error but it can be used to notify the user of processor throttling past a preset USER limit. A user limit of FFh acts as the mask for this register. Error bits associated with the predefined  $\overline{\text{PROCHOT}}$  thresholds cannot be masked. It is important to note though, that these error bits do not cause BMC\_ERR, HOST\_ERR, or  $\overline{\text{ALERT}}$  to be asserted under any condition.

Fan tach errors are masked if the tach limit for the given tach is set to FFh .

$\overline{\text{GPI}}$  errors and  $\overline{\text{VRDx\_HOT}}$  errors can be masked by setting the appropriate bit in the GPI and Miscellaneous Error Mask registers.

When the LM94 powers up, the  $\overline{\text{ALERT}}$  output is disabled. The  $\overline{\text{ALERT}}$  output can be enabled by setting the ALERT\_EN bit in the LM94 Configuration register.

In addition the manual masking options, the LM94 also masks some errors depending on the sleep state of the system. The sleep state of the system is communicated to the LM94 by writing to the Sleep State Control register. Some types of error events are always masked in certain sleep modes. Some types of error events are optionally masked in certain sleep modes if their sleep mask register bit is set. Refer to the [register descriptions](#) for more information.

### 7.1.8 Layout and Grounding

Analog components such as voltage dividers should be physically located as close as possible to the LM94. See [Section 8.2](#) for thermal diode layout recommendations.

The LM94 bypass capacitors, the parallel combination of 100 pF, 10 μF (electrolytic or tantalum) and 0.1 μF (ceramic) bypass capacitors must be connected between power pin (pin 39) and ground, and should be located as close as possible to the LM94. The 100 pF capacitor should be placed closest to the power pin.

## 7.2 Typical Application

Baseboard management of a dual processor server. Two LM94s may be required to manage a quad processor board. The system diagram below shows a dual processor server

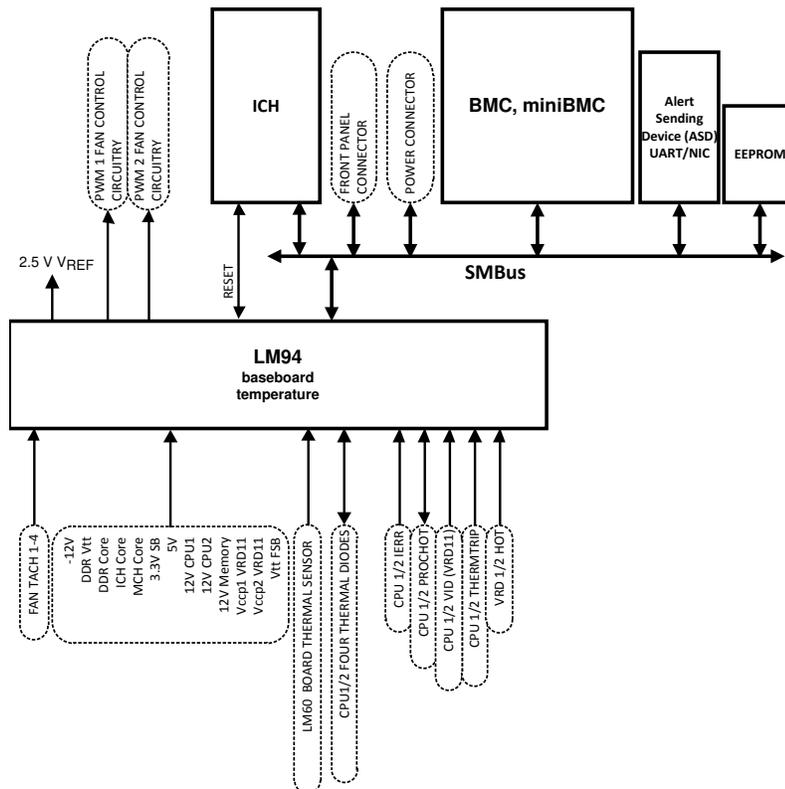


Figure 7-1. 2 Way Xeon Server Management

## 7.2.1 Thermal Diode Application

To measure temperature external to the LM94, use a remote discrete diode to sense the temperature of external objects or ambient air. The temperature of a discrete diode is affected, and often dominated, by the temperature of its leads.

Most silicon diodes do not lend themselves well to this application. It is recommended that a MMBT3904 transistor type base emitter junction be used with the collector tied to the base.

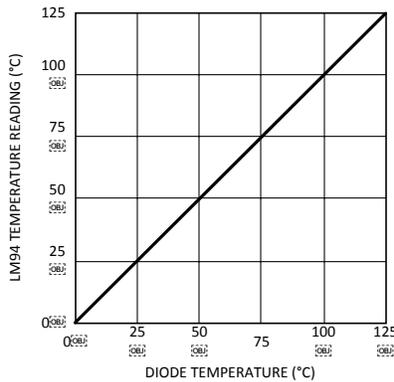


Figure 7-2. Thermal Diode Temperature vs. LM94 Temperature Reading

### 7.2.1.1 Diode Non-Ideality

#### 7.2.1.1.1 Diode Non-Ideality Factor Effect on Accuracy

When a transistor is connected as a diode, the following relationship holds for variables  $V_{BE}$ ,  $T$  and  $I_F$ :

$$I_F = I_S \times \left[ e^{\left( \frac{V_{BE}}{\eta \times V_t} \right)} - 1 \right] \quad (10)$$

where:

$$V_t = \frac{kT}{q} \quad (11)$$

- $q = 1.6 \times 10^{-19}$  Coulombs (the electron charge),
- $T$  = Absolute Temperature in Kelvin
- $k = 1.38 \times 10^{-23}$  joules/K (Boltzmann's constant),
- $\eta$  is the non-ideality factor of the process the diode is manufactured on,
- $I_S$  = Saturation Current and is process dependent,
- $I_F$  = Forward Current through the base emitter junction
- $V_{BE}$  = Base Emitter Voltage drop

In the active region, the -1 term is negligible and may be eliminated, yielding the following equation

$$I_F = I_S \left[ e^{\frac{V_{be}}{\eta V_t}} \right] \quad (12)$$

In Equation 12,  $\eta$  and  $I_S$  are dependant upon the process that was used in the fabrication of the particular diode. By forcing two currents with a well controlled ratio ( $I_{F2}/I_{F1}$ ) and measuring the resulting voltage difference, it is possible to eliminate the  $I_S$  term. Solving for the forward voltage difference yields the relationship:

$$\Delta V_{BE} = \eta \times \frac{k \times T}{q} \times \ln \left( \frac{I_{F2}}{I_{F1}} \right) \quad (13)$$

Solving Equation 13 for temperature yields:

$$T = \frac{\Delta V_{BE} \times q}{\eta \times k \times \ln \left( \frac{I_{F2}}{I_{F1}} \right)} \quad (14)$$

Equation 14 holds true when a diode connected transistor such as the MMBT3904 is used. When this “diode” equation is applied to an integrated diode such as a processor transistor with its collector tied to GND as shown in Figure 7-3 it will yield a wide non-ideality spread. This wide non-ideality spread is not due to true process variation but due to the fact that Equation 14 is an approximation.

TruTherm technology uses the transistor equation, Equation 15, which is a more accurate representation of the topology of the thermal diode found in an FPGA or processor.

$$T = \frac{\Delta V_{BE} \times q}{\eta \times k \times \ln \left( \frac{I_{C2}}{I_{C1}} \right)} \quad (15)$$

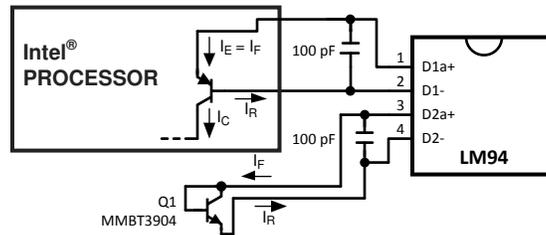


Figure 7-3. Thermal Diode Current Paths

TruTherm should only be enabled when measuring the temperature of a transistor integrated as shown in the processor of Figure 7-3, because Equation 15 only applies to this topology.

#### 7.2.1.1.2 Calculating Total System Accuracy

The voltage seen by the LM94 also includes the  $I_F R_S$  voltage drop of the series resistance. The non-ideality factor,  $\eta$ , is the only other parameter not accounted for and depends on the diode that is used for measurement. Since  $\Delta V_{BE}$  is proportional to both  $\eta$  and  $T$ , the variations in  $\eta$  cannot be distinguished from variations in temperature. Since the non-ideality factor is not controlled by the temperature sensor, it will directly add to the inaccuracy of the sensor. For the Pentium D processor on 65nm process, Intel specifies a +4.06%/–0.89% variation in  $\eta$  from part to part when the processor diode is measured by a circuit that assumes diode equation, Equation 14, as true. As an example, assume a temperature sensor has an accuracy specification of  $\pm 2.5^\circ\text{C}$  at a temperature of  $75^\circ\text{C}$  (348 Kelvin) and the processor diode has a non-ideality variation of +4.06%/–0.89%. The resulting system accuracy of the processor temperature being sensed will be:

$$T_{ACC} = \pm 2.5^\circ\text{C} + (+4.06\% \text{ of } 348 \text{ K}) = +16.6^\circ\text{C} \quad (16)$$

and

$$T_{ACC} = \pm 2.5^\circ\text{C} + (-0.89\% \text{ of } 348 \text{ K}) = -5.6^\circ\text{C} \quad (17)$$

TruTherm technology uses the transistor equation, [Equation 15](#), resulting in a non-ideality spread that truly reflects the process variation which is very small. The transistor equation non-ideality spread is  $\pm 0.4\%$  for the Pentium D processor on 65nm process. The resulting accuracy when using TruTherm technology improves to:

$$T_{ACC} = \pm 2.5^{\circ}\text{C} + (\pm 0.4\% \text{ of } 348 \text{ K}) = \pm 3.9^{\circ}\text{C} \quad (18)$$

The next error term to be discussed is that due to the series resistance of the thermal diode and printed circuit board traces. The thermal diode series resistance is specified on most processor data sheets. For the Pentium D processor on 65 nm process, this is specified at  $4.52\Omega$  typical. The LM94 accommodates the typical series resistance of the Pentium D processor on 90 nm process. The error that is not accounted for is the spread of the Pentium's series resistance, that is  $2.79\Omega$  to  $6.24\Omega$  or  $\pm 1.73\Omega$ . The equation to calculate the temperature error due to series resistance ( $T_{ER}$ ) for the LM94 is simply:

$$T_{ER} = R_{PCB} \times 0.62^{\circ}\text{C}/\Omega \quad (19)$$

Solving [Equation 19](#) for  $R_{PCB}$  equal to  $\pm 1.73\Omega$  results in the additional error due to the spread in the series resistance of  $\pm 1.07^{\circ}\text{C}$ . The spread in error cannot be canceled out, as it would require measuring each individual thermal diode device. This is quite difficult and impractical in a large volume production environment.

[Equation 19](#) can also be used to calculate the additional error caused by series resistance on the printed circuit board. Since the variation of the PCB series resistance is minimal, the bulk of the error term is always positive and can simply be cancelled out by subtracting it from the output readings of the LM94.

#### 7.2.1.1.3 Compensating for Different Non-Ideality

In order to compensate for the errors introduced by non-ideality, the temperature sensor is calibrated for a particular processor. Texas Instruments' temperature sensors are always calibrated to the typical non-ideality and series resistance of a given processor type. The LM94 is calibrated for two non-ideality factors and series resistance values thus supporting the MMBT3904 transistor and the Pentium D processor on 65nm process without the requirement for additional trims. For most accurate measurements TruTherm mode should be turned on when measuring the Pentium D processor on the 65nm process the error introduced by the false non-ideality spread (see [Section 7.2.1.1.1](#)). When a temperature sensor calibrated for a particular processor type is used with a different processor type, additional errors are introduced.

Temperature errors associated with non-ideality of different processor types may be reduced in a specific temperature range of concern through use of software calibration. Typical non-ideality specification differences cause a gain variation of the transfer function, therefore the center of the temperature range of interest should be the target temperature for calibration purposes. The following equation can be used to calculate the temperature correction factor ( $T_{CF}$ ) required to compensate for a target non-ideality differing from that supported by the LM94.

$$T_{CF} = [(\eta_S - \eta_{Processor}) \div \eta_S] \times (T_{CR} + 273 \text{ K}) \quad (20)$$

where

- $\eta_S$  = LM94 non-ideality for accuracy specification
- $\eta_T$  = target thermal diode typical non-ideality
- $T_{CR}$  = center of the temperature range of interest in  $^{\circ}\text{C}$

The correction factor of [Equation 20](#) should be directly added to the temperature reading produced by the LM94. For example when using the LM94, with the 3904 mode selected, to measure a AMD Athlon processor, with a typical non-ideality of 1.008, for a temperature range of  $60^{\circ}\text{C}$  to  $100^{\circ}\text{C}$  the correction factor would calculate to:

$$T_{CF} = [(1.003 - 1.008) \div 1.003] \times (80 + 273) = -1.75^{\circ}\text{C} \quad (21)$$

Therefore,  $1.75^{\circ}\text{C}$  should be subtracted from the temperature readings of the LM94 to compensate for the differing typical non-ideality target.

## 8 Layout

### 8.1 Recommended Implementation

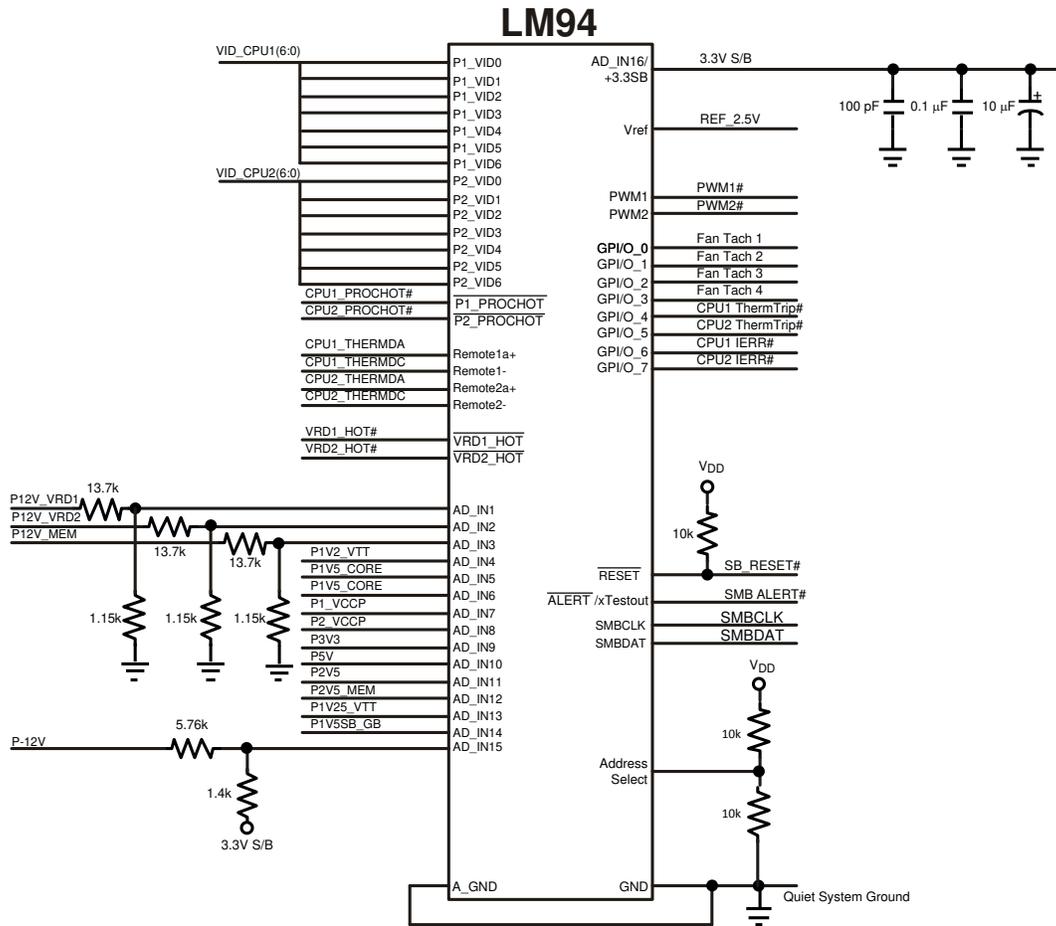
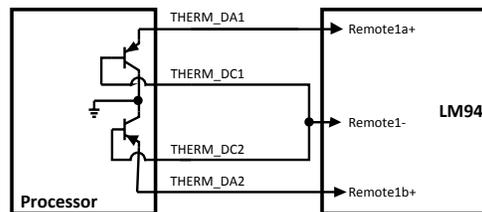


Figure 8-1. Recommended Implementation without Thermal Diode Connections



**Note:** 100 pF cap across each thermal diode is optional and should be placed close to the LM94, if used. The maximum capacitance between thermal diode pins is 300 pF.

Figure 8-2. Thermal Diode Recommended Implementation

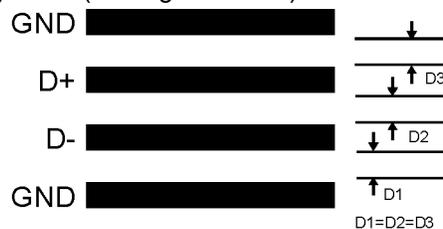
## 8.2 PCB Layout for Minimizing Noise

In the following guidelines, Remote+ and Remote -- refer to the REMOTE1a+, Remote 1b+, REMOTE1-, REMOTE2a+, Remote2b+ and REMOTE2- pins.

In a noisy environment, such as a power supply, layout considerations are very critical. Noise induced on traces running between the remote temperature diode sensor and the LM94 can cause temperature conversion errors.

The following guidelines should be followed:

1. Place a 0.1  $\mu\text{F}$  and 100 pF LM94 power bypass capacitors as close as possible to the  $V_{\text{DD}}$  pin, with the 100pF capacitor being the closest. Place 10  $\mu\text{F}$  capacitor in the near vicinity of the LM94 power pin.
2. Place a 100 pF capacitor as close as possible to the LM94 thermal diode Remote+ and Remote- pins. Make sure the traces to the 100 pF capacitor are matched and as short as possible. This capacitor is required to minimize high frequency noise error.
3. Thermal diodes that share one Remote- pin must have a separate trace from the LM94 Remote- pin run to each diode cathode. Do not "daisy chain" these connections.
4. Ideally, the LM94 should be placed within 10 cm of the thermal diode pins with the traces being as straight, short and identical as possible. Trace resistance of  $1\Omega$  can cause as much as  $1^\circ\text{C}$  of error.
5. Diode traces should be surrounded by a GND guard ring to either side, above and below, if possible. This GND guard should not be between the Remote+ and Remote- lines. In the event that noise does couple to the diode lines, it would be ideal if it is coupled to both identically, i.e. common mode. That is, equally to the Remote+ (D+) and Remote-(D-) lines. (See figure below):



**Figure 8-3. Recommended Diode Trace Layout**

6. Avoid routing diode traces in close proximity to any power supply switching or filtering inductors.
7. Avoid running diode traces close to or parallel to high speed digital and bus lines. Diode traces should be kept at least 2 cm apart from the high speed digital traces.
8. If it is necessary to cross high speed digital traces, the diode traces and the high speed digital traces should cross at a 90 degree angle.
9. The ideal place to connect the LM94's GND pin is as close as possible to the Processors GND associated with the sense diode. In the case of two processors pick a node in between the two that has the least noise.
10. Leakage current between Remote+ and GND should be kept to a minimum. Error in the diode temperature reading may reach  $0.4^\circ\text{C}$  with 30 nA of leakage current. Keeping the printed circuit board as clean as possible minimizes leakage current. The residue from some freeze spray can induce high leakage current.

## 9 Device and Documentation Support

### 9.1 Documentation Support

### 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 9.4 Trademarks

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### 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| <b>Changes from Revision C (March 2013) to Revision D (February 2024)</b>                              | <b>Page</b> |
|--|-------------|
| • Updated the numbering format for tables, figures, and cross-references throughout the document ..... | <b>1</b>    |

| <b>Changes from Revision B (July 2010) to Revision C (March 2013)</b> | <b>Page</b> |
|---|-------------|
| • Changed layout of National Data Sheet to TI format.....             | <b>13</b>   |

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable part number          | Status<br>(1) | Material type<br>(2) | Package   Pins   | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|--------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">LM94CIMT/NOPB</a>  | Obsolete      | Production           | TSSOP (DGG)   56 | -                     | -           | Call TI                              | Call TI                           | 0 to 100     | LM94CIMT            |
| <a href="#">LM94CIMTX/NOPB</a> | Active        | Production           | TSSOP (DGG)   56 | 1000   LARGE T&R      | Yes         | SN                                   | Level-2-260C-1 YEAR               | 0 to 100     | LM94CIMT            |
| LM94CIMTX/NOPB.A               | Active        | Production           | TSSOP (DGG)   56 | 1000   LARGE T&R      | Yes         | SN                                   | Level-2-260C-1 YEAR               | 0 to 100     | LM94CIMT            |

**(1) Status:** For more details on status, see our [product life cycle](#).

**(2) Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

**(3) RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

**(4) Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

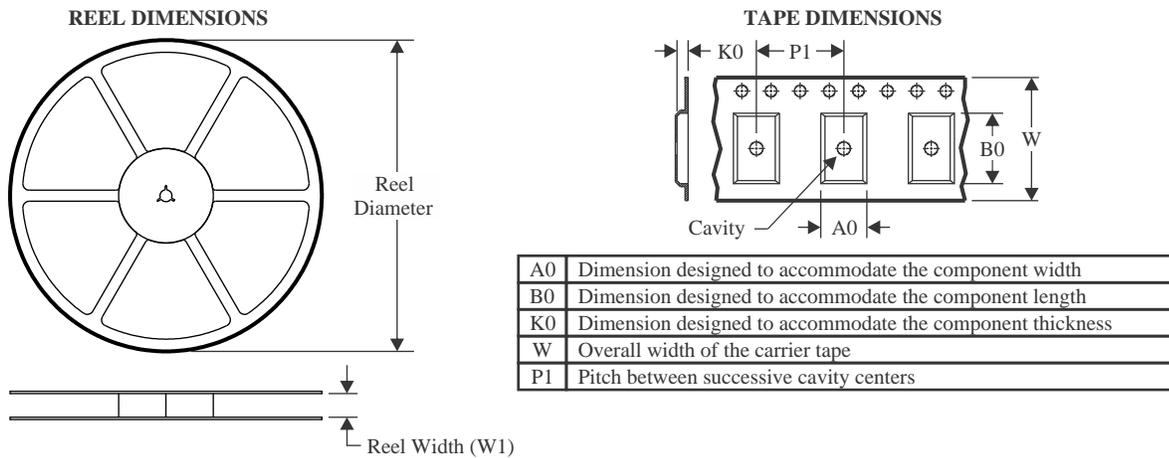
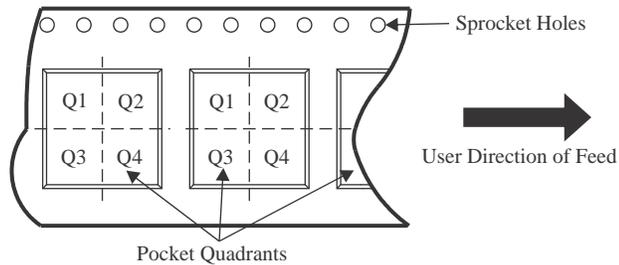
**(5) MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

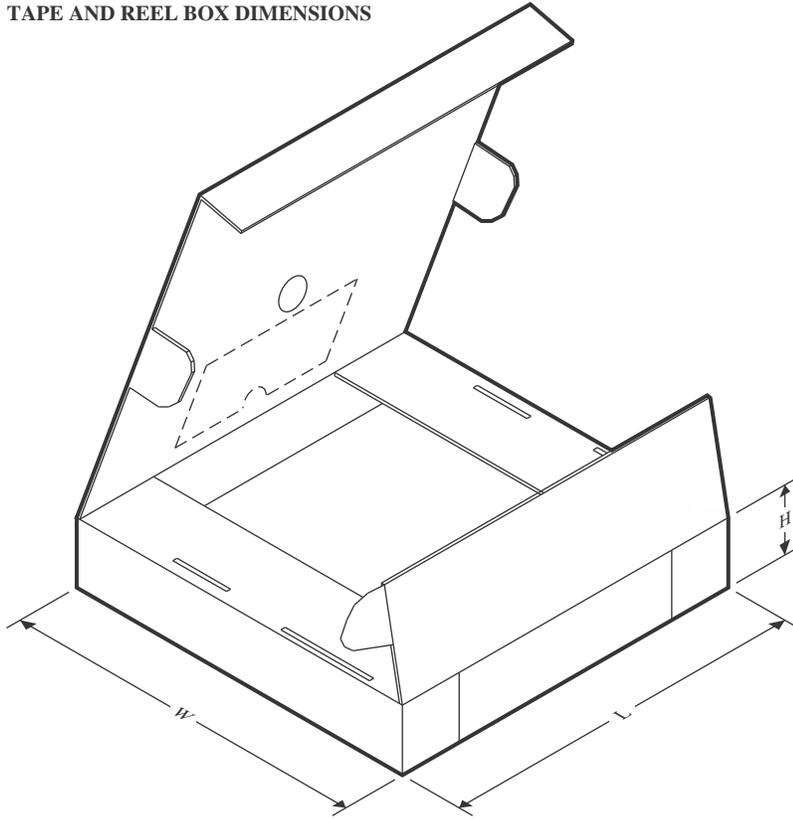
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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


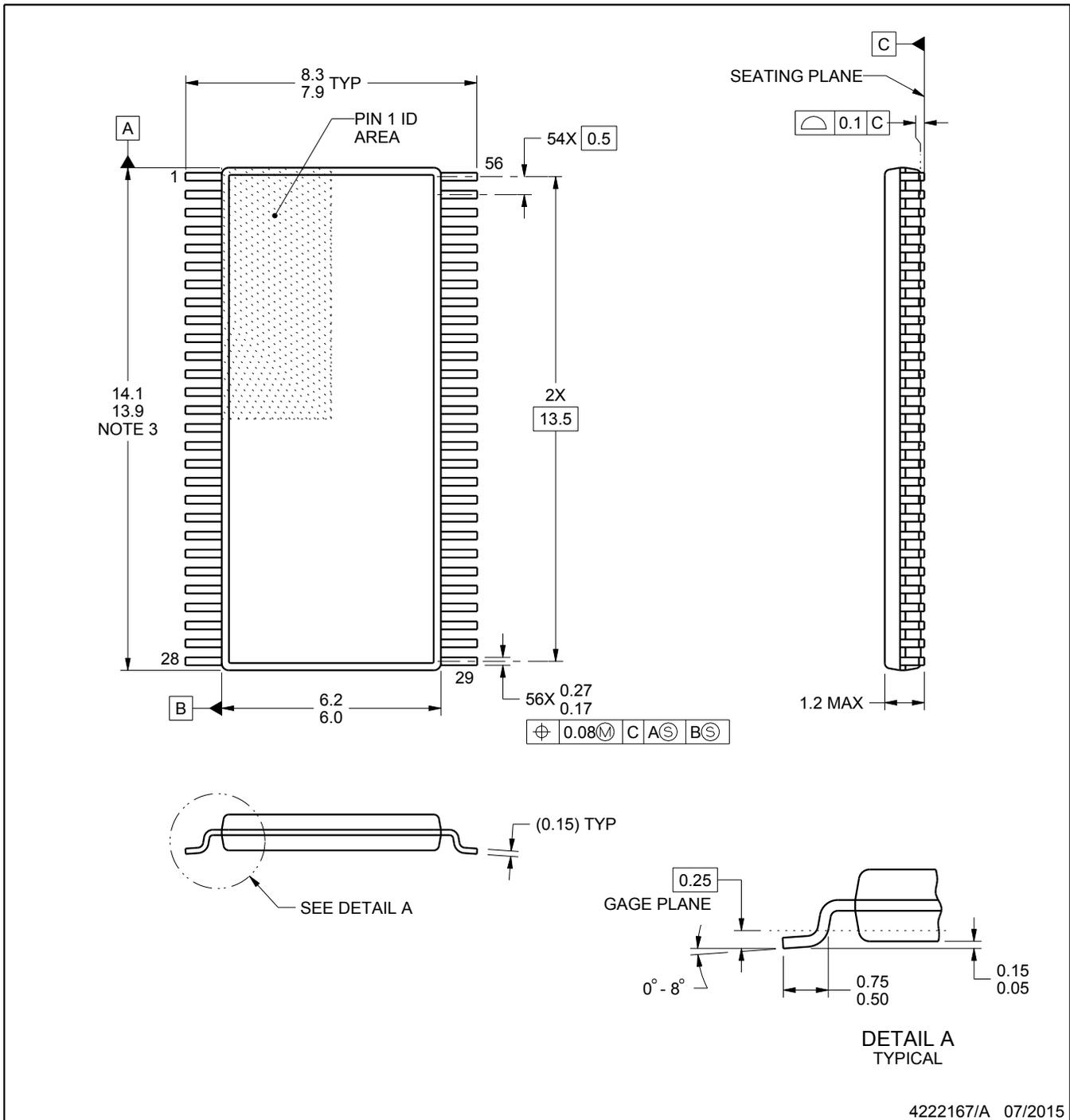
\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LM94CIMTX/NOPB | TSSOP        | DGG             | 56   | 1000 | 330.0              | 24.4               | 8.6     | 14.5    | 1.8     | 12.0    | 24.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LM94CIMTX/NOPB | TSSOP        | DGG             | 56   | 1000 | 356.0       | 356.0      | 45.0        |



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NOTES:

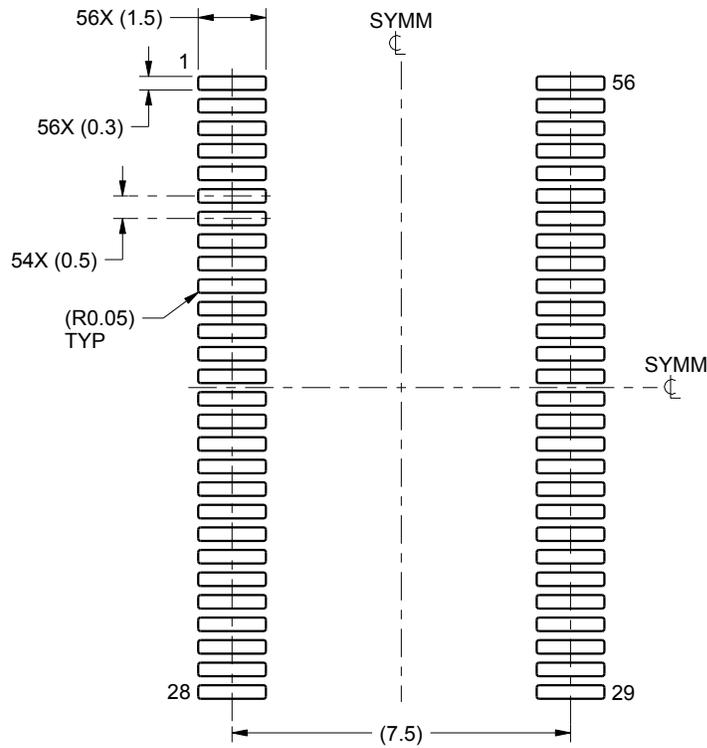
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

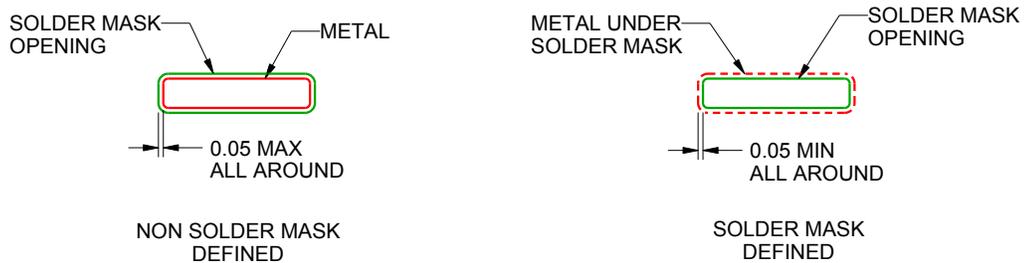
DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

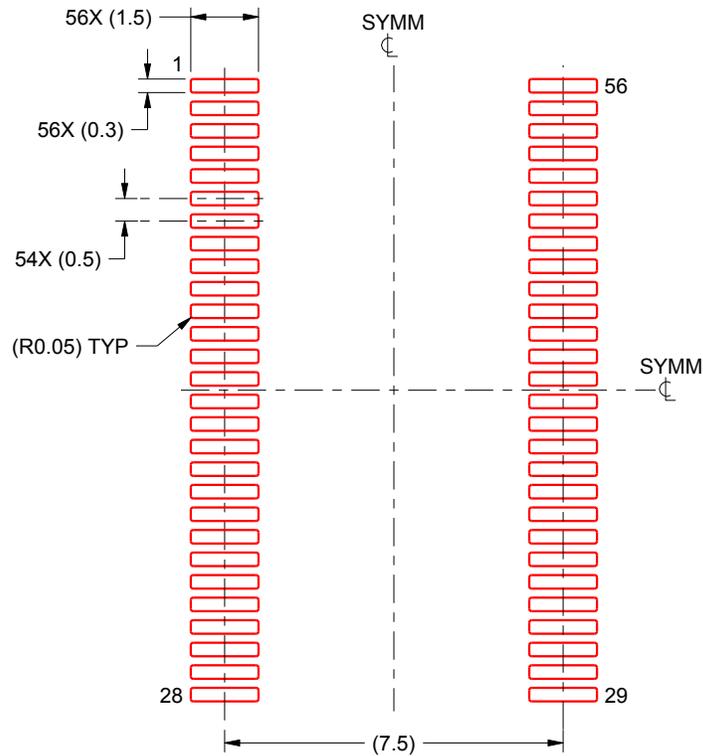
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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