LMD18200QML 2.4A, 55V H-Bridge

1 Features

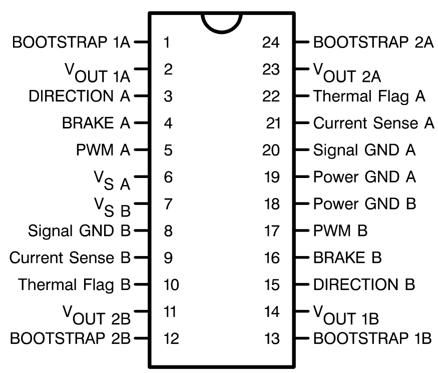
- Delivers up to 2.4A continuous output
- Operates at supply voltages up to 55V
- Low R_{DS}(On) typically 0.3Ω per switch
- TTL and CMOS compatible inputs
- No “shoot-through” current
- Thermal warning flag output at 145°C
- Thermal shutdown (outputs off) at 170°C
- Internal clamp diodes
- Shorted load protection
- Internal charge pump with external bootstrap capability

2 Applications

- DC and stepper motor drives
- Position and velocity servomechanisms
- Factory automation robots
- Numerically controlled machinery
- Computer printers and plotters

3 Description

The LMD18200 is a 2.4A H-Bridge designed for motion control applications. The device is built using a multi-technology process which combines bipolar and CMOS control circuitry with DMOS power devices on the same monolithic structure. Ideal for driving DC and stepper motors; the LMD18200 accommodates peak output currents up to 6A. An innovative circuit which facilitates low-loss sensing of the output current has been implemented.



24-Lead Dual-in-Line Package Top View See Package NAZ0024B

4 Functional Diagram

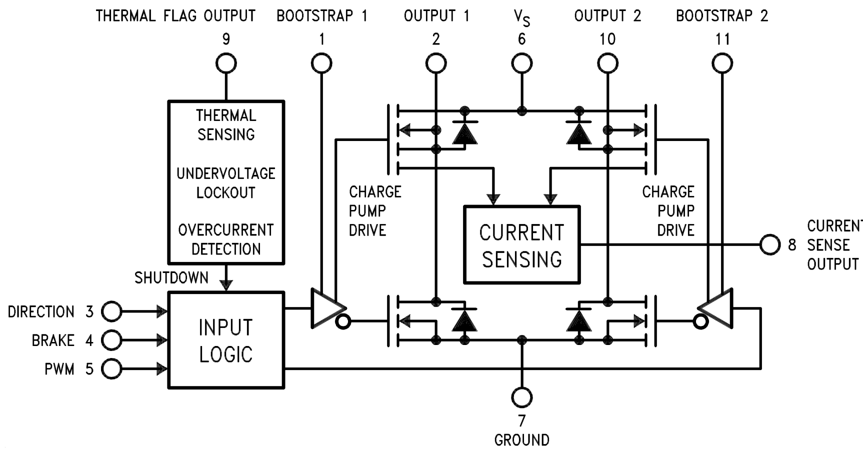


Figure 4-1. Functional Block Diagram of LMD18200

5 Absolute Maximum Ratings

See [(1)]

Total Supply Voltage (V_S, Pin 6 & 7)			60V
Voltage at Pins 3, 4, 5, 9, 10, 15, 16, 17, 21 and 22			12V
Voltage at Bootstrap Pins (Pins 1, 12, 13 and 24)			V_O +16V
Peak Output Current (200 mS)			6A
Continuous Output Current[(2)]			2.4A
Power Dissipation[(3)] [(4)]			25W
Power Dissipation (T_A = 25°C, Free Air)			3W
Junction Temperature (T_{Jmax})			150°C
Thermal Resistance	$R\theta_{JA}$	Junction-to-ambient thermal resistance	30.6°C/W
	$R\theta_{JC(top)}$	Junction-to-case (top) thermal resistance	6.6°C/W
	$R\theta_{JC(bottom)}$	Junction-to-case (bottom) thermal resistance	3.2°C/W
ESD Susceptibility[(5)]			1500V
Storage Temperature (T_{Stg})			−65°C ≤ T_A ≤ +150°C
Lead Temperature (Soldering, 10 sec.)			300°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For specified specifications and test conditions, see the Electrical Characteristics. The specified specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) See Section 11.1 for details regarding current limiting.
(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.
(4) The package material for these devices allows much improved heat transfer over our standard ceramic packages. In order to take full advantage of this improved heat transfer, heat sinking must be provided between the package base (directly beneath the die), and either metal traces on, or thermal vias through, the printed circuit board. Without this additional heat sinking, device power dissipation must be calculated using θ_{JA}, rather than θ_{JC}, thermal resistance. It must not be assumed that the device leads will provide substantial heat transfer out of the package, since the thermal resistance of the leadframe material is very poor, relative to the material of the package base. The stated θ_{JC} thermal resistance is for the package material only, and does not account for the additional thermal resistance between the package base and the printed circuit board. The user must determine the value of the additional thermal resistance and must combine this with the stated value for the package, to calculate the total allowed power dissipation for the device.
(5) Human-body model, 100 pF discharged through a 1.5 kΩ resistor. Except Bootstrap pins (pins 1, 12, 13 and 24) which are protected to 1000V of ESD.

6 Operating Ratings

See [(1)]

Junction Temperature, T_J	−55°C ≤ T_J ≤ +125°C
V_S Supply Voltage	+12V to +55V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For specified specifications and test conditions, see the Electrical Characteristics. The specified specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

7 Quality Conformance Inspection

Table 7-1. Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55
12	Settling time at	+25
13	Settling time at	+125
14	Settling time at	-55

8 LMD18200 Electrical Characteristics DC Parameters

The following conditions apply, unless otherwise specified. V_S = 42V

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
$R_{DS\ On}$	Switch On Resistance	Output current = 2.4A	See(1)		0.6	Ω	1
					0.7	Ω	2, 3
V_{Clamp}	Clamp Diode Forward Drop	Clamp current = 2.4A	See(1)		1.70	V	1, 2, 3
V_{IL}	Logic Low Input Voltage		See(3)	-0.1	0.8	V	1, 2, 3
I_{IL}	Logic Low Input Current	V_I = -0.1V	See(3)		-10	µA	1, 2, 3
V_{IH}	Logic High Input Voltage		See(3)	2.0	12	V	1, 2, 3
I_{IH}	Logic High Input Current	V_I = 12V	See(3)		10	µA	1, 2, 3
$I_{O\ Sense}$	Current Sense Output	I_O = 1A		250	500	µA	1
$I_{O\ Sense}$	Current Sense Output	I_O = 1A		225	525	µA	2, 3
$I_{LI\ Sense}$	Current Sense Linearity	1A ≤ I_O≤ 2.4A	See(2)	-20	20	%	1, 2, 3
	Undervoltage Lockout	Outputs turn Off		9.0	15	V	1, 2, 3
$I_{F\ Off}$	Flag Output Leakage	V_F = 12V			10	µA	1, 2, 3
I_S	Quiescent Supply Current	All Logic Inputs Low			25	mA	1, 2, 3

(1) Output currents are pulsed (Duty Cycle < 5%).
(2) Linearity is calculated relative to the current sense output value with 1A load.
(3) Pins 3, 4, 5, 15, 16 and 17

9 Typical Performance Characteristics

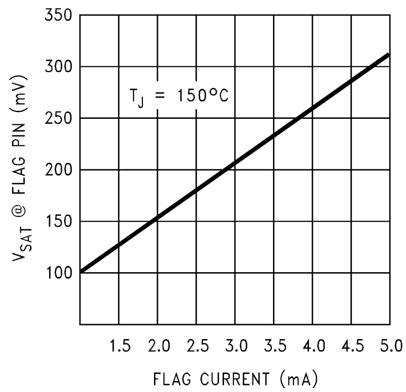


Figure 9-1. V_{Sat} vs Flag Current

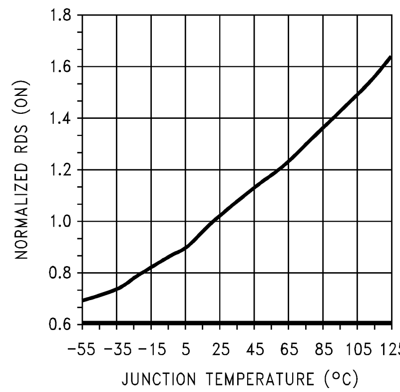


Figure 9-2. R_{DS}(On) vs Temperature

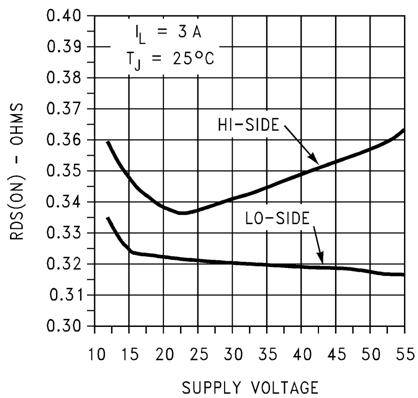


Figure 9-3. R_{DS}(On) vs Supply Voltage

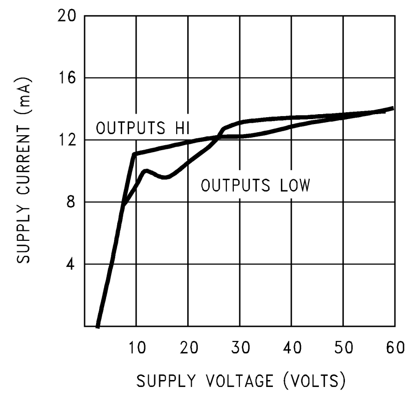


Figure 9-4. Supply Current vs Supply Voltage

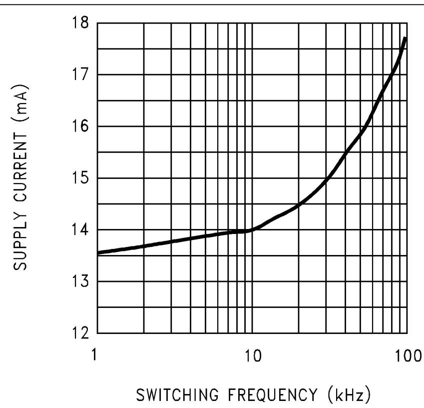


Figure 9-5. Supply Current vs Frequency (V_S = 42V)

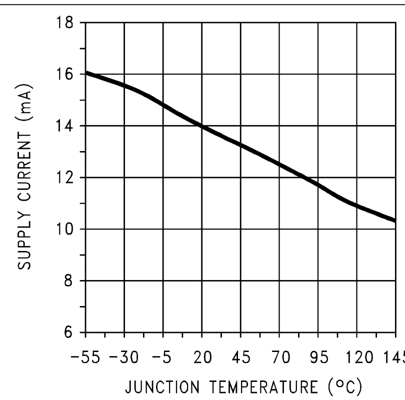


Figure 9-6. Supply Current vs Temperature (V_S = 42V)

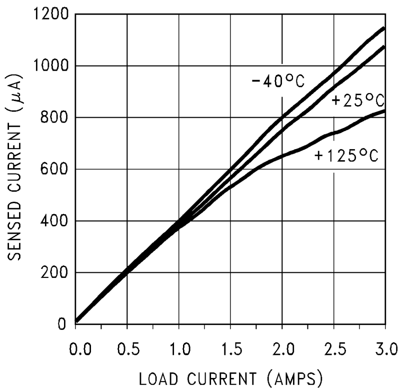


Figure 9-7. Current Sense Output vs Load Current

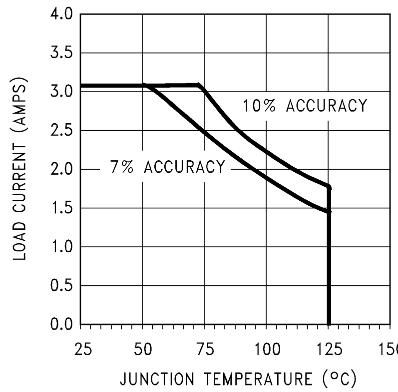
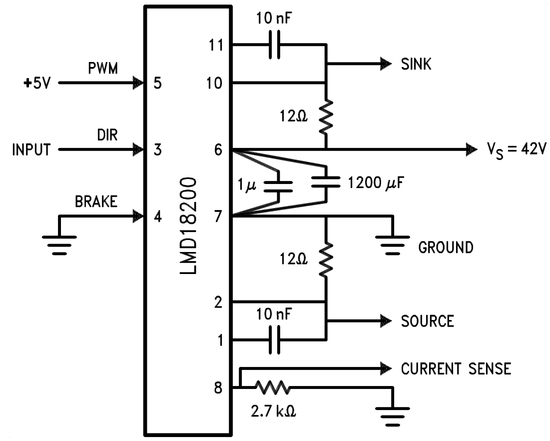
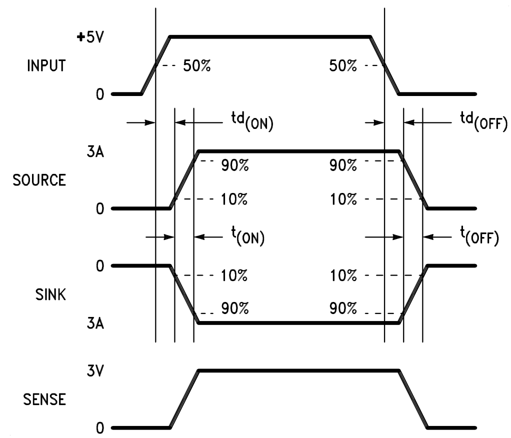


Figure 9-8. Current Sense Operating Region

10 Test Circuit



10.1 Switching Time Definitions



11 Pinout Description

(See 24-Lead Dual-in-Line Package Top View See Package NAZ0024B)

Pin 1, BOOTSTRAP 1 Input: Bootstrap capacitor pin for half H-bridge number 1. The recommended capacitor (10 nF) is connected between pins 1 and 2.

Pin 2, OUTPUT 1: Half H-bridge number 1 output.

Pin 3, DIRECTION Input: See Table 11-1. This input controls the direction of current flow between OUTPUT 1 and OUTPUT 2 (pins 2 and 10) and, therefore, the direction of rotation of a motor load.

Pin 4, BRAKE Input: See Table 11-1. This input is used to brake a motor by effectively shorting its terminals. When braking is desired, this input is taken to a logic high level and it is also necessary to apply logic high to PWM input, pin 5. The drivers that short the motor are determined by the logic level at the DIRECTION input (Pin 3): with Pin 3 logic high, both current sourcing output transistors are ON; with Pin 3 logic low, both current sinking output transistors are ON. All output transistors can be turned OFF by applying a logic high to Pin 4 and a logic low to PWM input Pin 5; in this case only a small bias current (approximately −1.5 mA) exists at each output pin.

Pin 5, PWM Input: See Table 11-1. How this input (and DIRECTION input, Pin 3) is used is determined by the format of the PWM Signal.

Pin 6, V_S Power Supply

Pin 7, GROUND Connection: This pin is the ground return, and is internally connected to the mounting tab.

Pin 8, CURRENT SENSE Output: This pin provides the sourcing current sensing output signal, which is typically 377 µA/A.

Pin 9, THERMAL FLAG Output: This pin provides the thermal warning flag output signal. Pin 9 becomes active-low at 145°C (junction temperature). However the chip will not shut itself down until 170°C is reached at the junction.

Pin 10, OUTPUT 2: Half H-bridge number 2 output.

Pin 11, BOOTSTRAP 2 Input: Bootstrap capacitor pin for Half H-bridge number 2. The recommended capacitor (10 nF) is connected between pins 10 and 11.

Table 11-1. Logic Truth Table

PWM	Dir	Brake	Active Output Drivers
H	H	L	Source 1, Sink 2
H	L	L	Sink 1, Source 2
L	X	L	Source 1, Source 2
H	H	H	Source 1, Source 2
H	L	H	Sink 1, Sink 2
L	X	H	None

11.1 Application Information

11.1.1 TYPES OF PWM SIGNALS

The LMD18200 readily interfaces with different forms of PWM signals. Use of the part with two of the more popular forms of PWM is described in the following paragraphs.

Simple, locked anti-phase PWM consists of a single, variable duty-cycle signal in which is encoded both direction and amplitude information (see Figure 11-1). A 50% duty-cycle PWM signal represents zero drive, since the net value of voltage (integrated over one period) delivered to the load is zero. For the LMD18200, the PWM signal drives the direction input (pin 3) and the PWM input (pin 5) is tied to logic high.

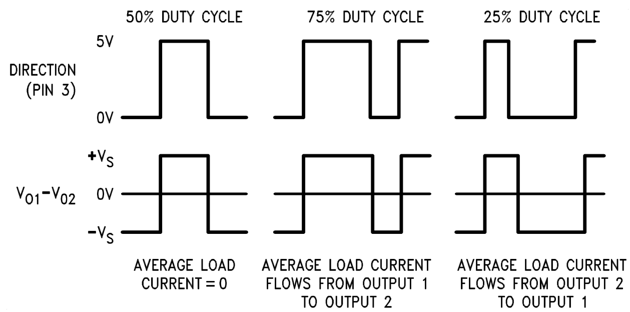


Figure 11-1. Locked Anti-Phase PWM Control

Sign/magnitude PWM consists of separate direction (sign) and amplitude (magnitude) signals (see Figure 11-2). The (absolute) magnitude signal is duty-cycle modulated, and the absence of a pulse signal (a continuous logic low level) represents zero drive. Current delivered to the load is proportional to pulse width. For the LMD18200, the DIRECTION input (pin 3) is driven by the sign signal and the PWM input (pin 5) is driven by the magnitude signal.

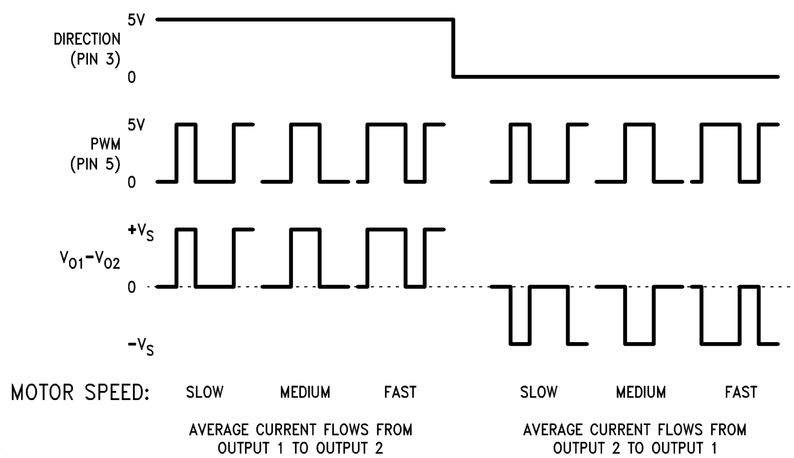


Figure 11-2. Sign/Magnitude PWM Control

11.1.2 SIGNAL TRANSITION REQUIREMENTS

To ensure proper internal logic performance, it is good practice to avoid aligning the falling and rising edges of input signals. A delay of at least 1 µsec should be incorporated between transitions of the Direction, Brake, and/or PWM input signals. A conservative approach is be sure there is at least 500ns delay between the end of the first transition and the beginning of the second transition. See Figure 11-3.

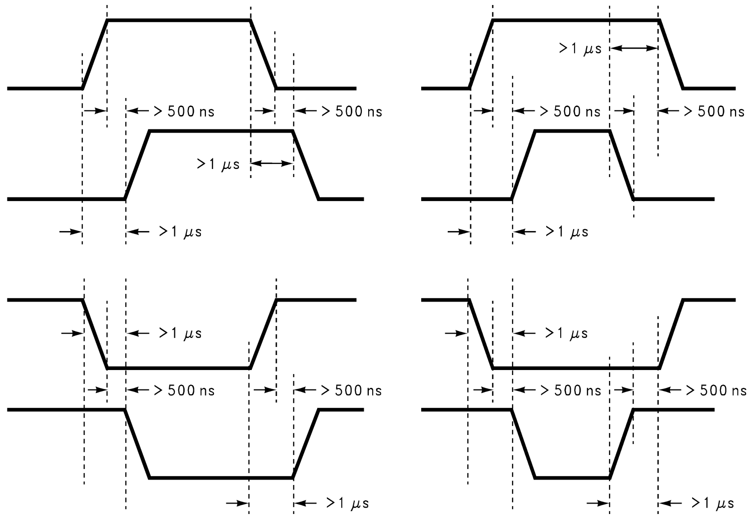


Figure 11-3. Transitions in Brake, Direction, or PWM Must Be Separated By At Least 1 µsec

11.1.3 USING THE CURRENT SENSE OUTPUT

The CURRENT SENSE output (pin 8) has a sensitivity of 377 µA per ampere of output current. For optimal accuracy and linearity of this signal, the value of voltage generating resistor between pin 8 and ground should be chosen to limit the maximum voltage developed at pin 8 to 5V, or less. The maximum voltage compliance is 12V.

It should be noted that the recirculating currents (free wheeling currents) are ignored by the current sense circuitry. Therefore, only the currents in the upper sourcing outputs are sensed.

11.1.4 USING THE THERMAL WARNING FLAG

The THERMAL FLAG output (pin 9) is an open collector transistor. This permits a wired OR connection of thermal warning flag outputs from multiple LMD18200's, and allows the user to set the logic high level of the output signal swing to match system requirements. This output typically drives the interrupt input of a system controller. The interrupt service routine would then be designed to take appropriate steps, such as reducing load currents or initiating an orderly system shutdown. The maximum voltage compliance on the flag pin is 12V.

11.1.5 SUPPLY BYPASSING

During switching transitions the levels of fast current changes experienced may cause troublesome voltage transients across system stray inductance.

It is normally necessary to bypass the supply rail with a high quality capacitor(s) connected as close as possible to the V_S Power Supply (Pin 6) and GROUND (Pin 7). A 1 µF high-frequency ceramic capacitor is recommended. Care should be taken to limit the transients on the supply pin below the Absolute Maximum Rating of the device. When operating the chip at supply voltages above 40V a voltage suppressor (transorb) such as P6KE62A is recommended from supply to ground. Typically the ceramic capacitor can be eliminated in the presence of the voltage suppressor. Note that when driving high load currents a greater amount of supply bypass capacitance (in general at least 100 µF per Amp of load current) is required to absorb the recirculating currents of the inductive loads.

11.1.6 CURRENT LIMITING

Current limiting protection circuitry has been incorporated into the design of the LMD18200. With any power device it is important to consider the effects of the substantial surge currents through the device that may occur as a result of shorted loads. The protection circuitry monitors this increase in current (the threshold is set to approximately 10 Amps) and shuts off the power device as quickly as possible in the event of an overload condition. In a typical motor driving application the most common overload faults are caused by shorted motor windings and locked rotors. Under these conditions the inductance of the motor (as well as any series inductance in the V_{CC} supply line) serves to reduce the magnitude of a current surge to a safe level for the

LMD18200. Once the device is shut down, the control circuitry will periodically try to turn the power device back on. This feature allows the immediate return to normal operation in the event that the fault condition has been removed. While the fault remains however, the device will cycle in and out of thermal shutdown. This can create voltage transients on the V_{CC} supply line and therefore proper supply bypassing techniques are required.

The most severe condition for any power device is a direct, hard-wired (“screwdriver”) long term short from an output to ground. This condition can generate a surge of current through the power device on the order of 15 Amps and require the die and package to dissipate up to 500 Watts of power for the short time required for the protection circuitry to shut off the power device. This energy can be destructive, particularly at higher operating voltages (>30V) so some precautions are in order. Proper heat sink design is essential and it is normally necessary to heat sink the V_{CC} supply pin (pin 6) with 1 square inch of copper on the PCB.

11.1.7 INTERNAL CHARGE PUMP AND USE OF BOOTSTRAP CAPACITORS

To turn on the high-side (sourcing) DMOS power devices, the gate of each device must be driven approximately 8V more positive than the supply voltage. To achieve this an internal charge pump is used to provide the gate drive voltage. As shown in Figure 11-4, an internal capacitor is alternately switched to ground and charged to about 14V, then switched to V supply thereby providing a gate drive voltage greater than V supply. This switching action is controlled by a continuously running internal 300 kHz oscillator. The rise time of this drive voltage is typically 20 µs which is suitable for operating frequencies up to 1 kHz.

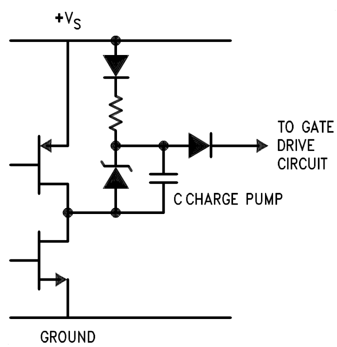


Figure 11-4. Internal Charge Pump Circuitry

For higher switching frequencies, the LMD18200 provides for the use of external bootstrap capacitors. The bootstrap principle is in essence a second charge pump whereby a large value capacitor is used which has enough energy to quickly charge the parasitic gate input capacitance of the power device resulting in much faster rise times. The switching action is accomplished by the power switches themselves Figure 11-5. External 10 nF capacitors, connected from the outputs to the bootstrap pins of each high-side switch provide typically less than 100 ns rise times allowing switching frequencies up to 500 kHz.

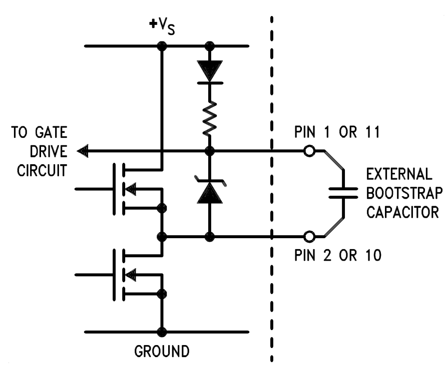


Figure 11-5. Bootstrap Circuitry

11.1.8 INTERNAL PROTECTION DIODES

A major consideration when switching current through inductive loads is protection of the switching power devices from the large voltage transients that occur. Each of the four switches in the LMD18200 have a built-in protection diode to clamp transient voltages exceeding the positive supply or ground to a safe diode voltage drop across the switch.

The reverse recovery characteristics of these diodes, once the transient has subsided, is important. These diodes must come out of conduction quickly and the power switches must be able to conduct the additional reverse recovery current of the diodes. The reverse recovery time of the diodes protecting the sourcing power devices is typically only 70 ns with a reverse recovery current of 1A when tested with a full 6A of forward current through the diode. For the sinking devices the recovery time is typically 100 ns with 4A of reverse current under the same conditions.

11.2 Typical Applications

11.2.1 FIXED OFF-TIME CONTROL

This circuit controls the current through the motor by applying an average voltage equal to zero to the motor terminals for a fixed period of time, whenever the current through the motor exceeds the commanded current. This action causes the motor current to vary slightly about an externally controlled average level. The duration of the Off-period is adjusted by the resistor and capacitor combination of the LM555. In this circuit the Sign/ Magnitude mode of operation is implemented (see Section 11.1.1).

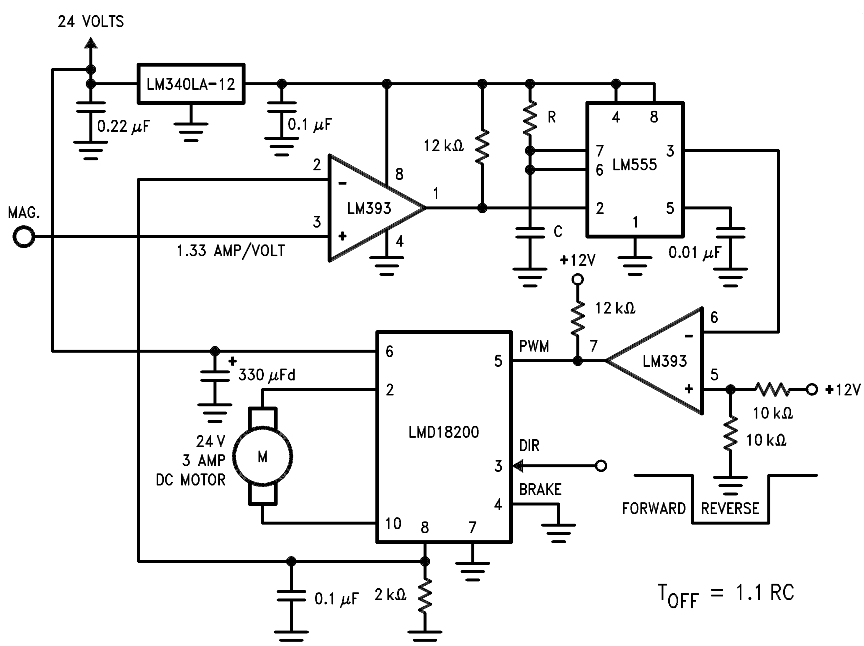


Figure 11-6. Fixed Off-Time Control

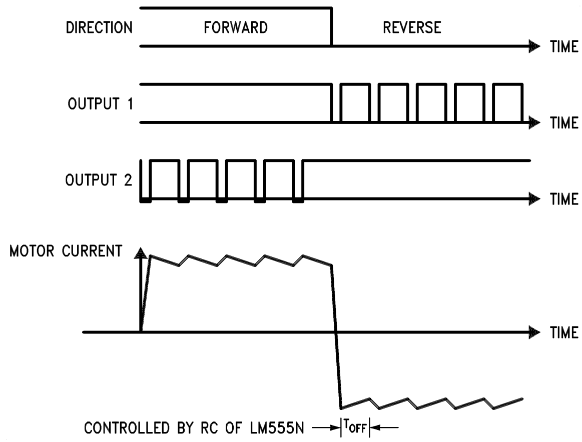


Figure 11-7. Switching Waveforms

11.2.2 TORQUE REGULATION

Locked Anti-Phase Control of a brushed DC motor. Current sense output of the LMD18200 provides load sensing. The LM3524D is a general purpose PWM controller. The relationship of peak motor current to adjustment voltage is shown in Figure 11-9.

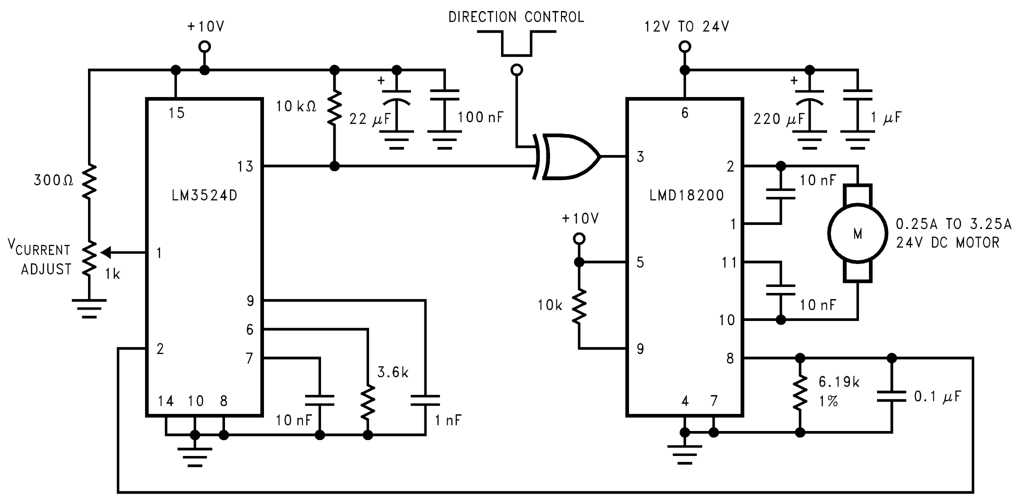


Figure 11-8. Locked Anti-Phase Control Regulates Torque

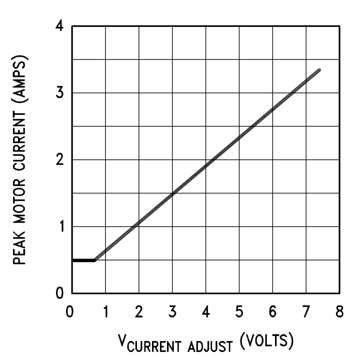


Figure 11-9. Peak Motor Current vs Adjustment Voltage

11.2.3 VELOCITY REGULATION

Utilizes tachometer output from the motor to sense motor speed for a locked anti-phase control loop. The relationship of motor speed to the speed adjustment control voltage is shown in Figure 11-11.

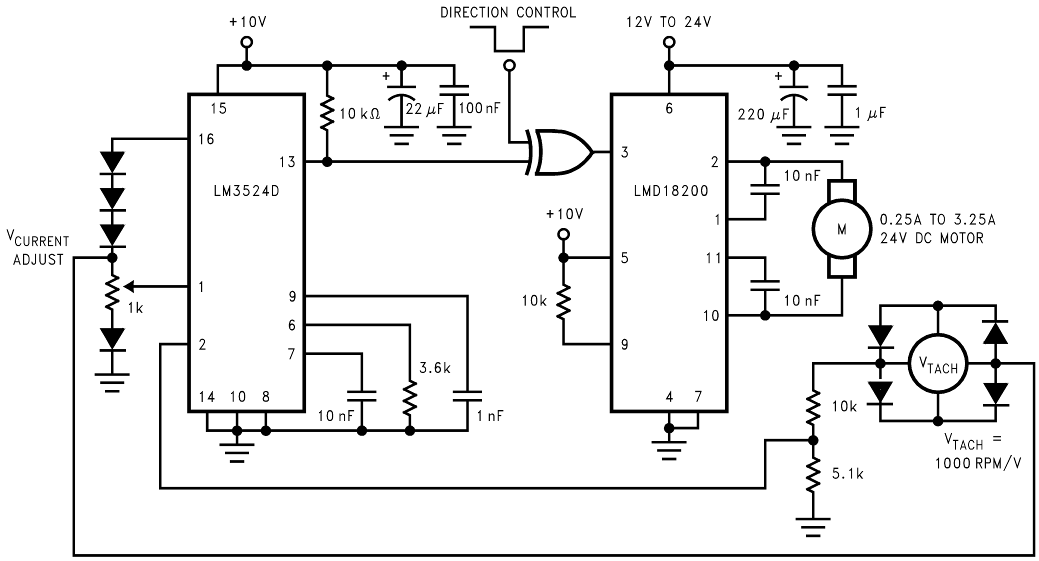


Figure 11-10. Regulate Velocity with Tachometer Feedback

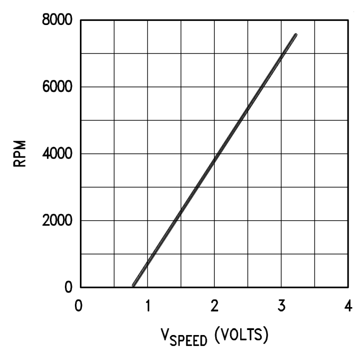


Figure 11-11. Motor Speed vs Control Voltage

12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Released	Revision	Section	Changes
11/30/2010	*	New Release, Corporate format	1 MDS data sheet converted into one Corp. data sheet format. The drift table was eliminated from the 883 section since it did not apply; MNLM18200-2-X Rev 1A1 will be archived.
04/18/2013	A	All	Changed layout of National Data Sheet to TI format.
9/18/2025	B	*Absolute Maximum Ratings*	Updated thermal resistance values
9/18/2025	B	All	Updated the numbering format for tables, figures, and cross-references throughout the document

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9232501MXA	Active	Production	CDIP SB (NAZ) | 24	15 | TUBE	No	Call TI	Call TI	-55 to 125	LMD18200-2D/883 5962-9232501MXA Q
LMD18200-2D/883	Active	Production	CDIP SB (NAZ) | 24	15 | TUBE	No	Call TI	Call TI	-55 to 125	LMD18200-2D/883 5962-9232501MXA Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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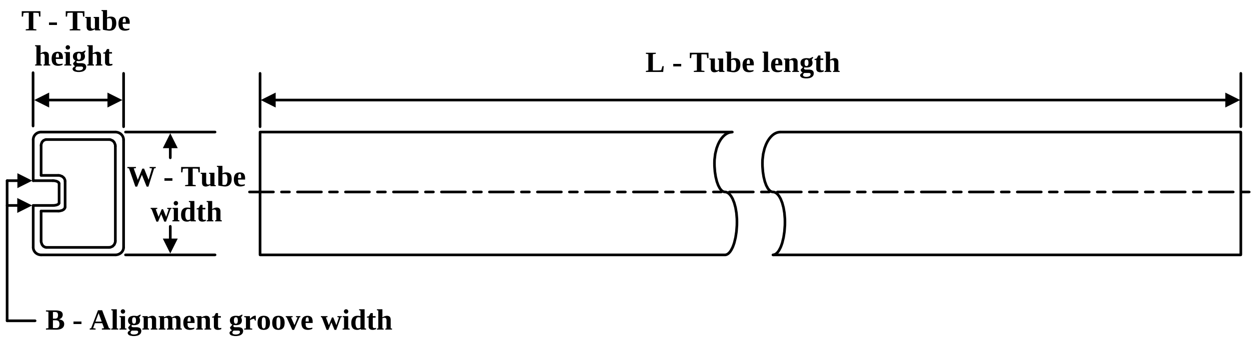
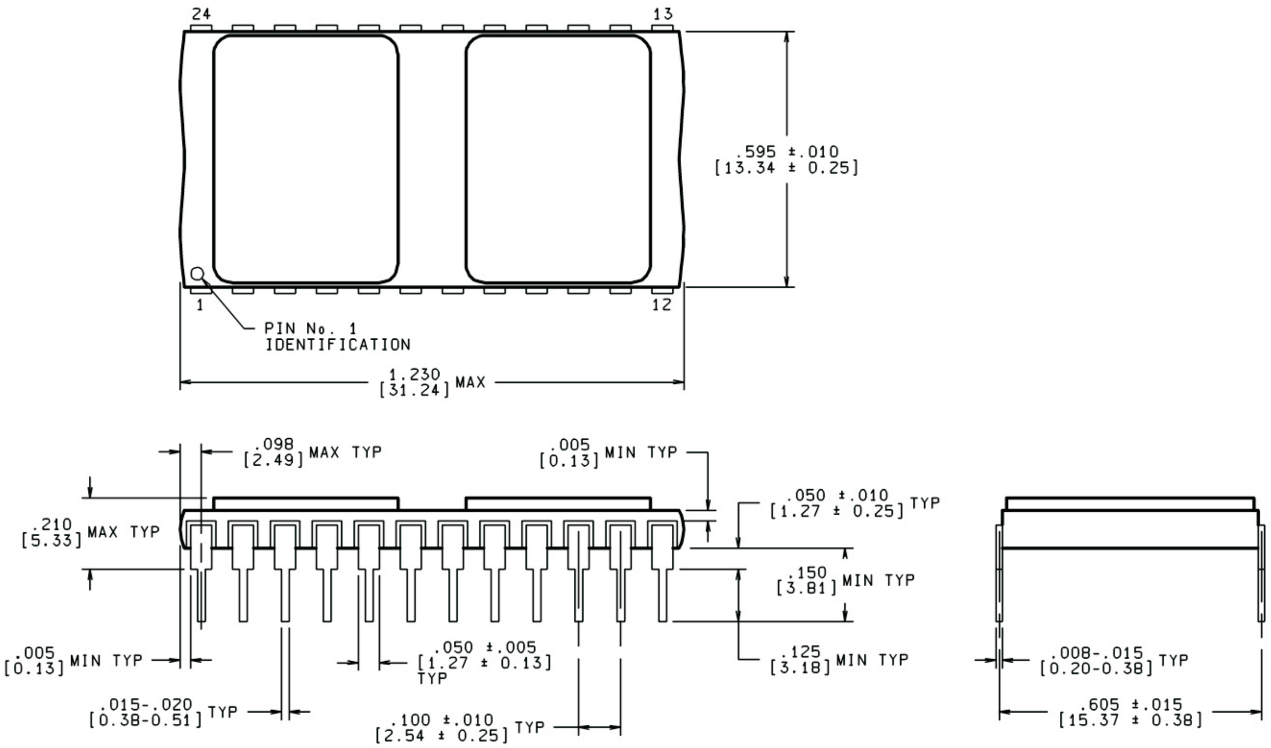
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9232501MXA	NAZ	CDIP SB	24	15	502	21	10668	11.05
LMD18200-2D/883	NAZ	CDIP SB	24	15	502	21	10668	11.05

NAZ0024B



CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

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