LMG1208 100V Dual Floating Gate Driver for MOSFET and GaN FET With Integrated Current Sense Amplifier

1 Features

- Dual floating gate driver
- 120V absolute maximum voltage on bootstrap supply (HB, LB) pins supporting 100V on the half-bridge
- 5A peak source and 6A peak sink current strength at 12V for silicon N-channel power FETs
- 3.5A peak source and 4.5A peak sink current strength at 5V for GaN FETs
- Wide supply operating voltage range: from 4.5V to 16V (18V absolute maximum)
- UVLO protection for VDD, HB-HS, and LB-LS supplies
- Single pulse width modulation (PWM) mode with resistor-programmable dead time
- Independent high-side (HS) and low-side (LS) logic inputs compatible with 3.3V and 5V logic levels
- Tri-state PWM input support
- Resistor programmable delay/dead time configuration in IIM and HSC modes
- Hybrid switched capacitor (HSC) converter mode support with integrated PWM logic
- Integrated low-offset high common-mode current sense amplifier
- Integrated synchronous bootstrap for floating high side driver supply
- Bootstrap control to prevent GaN FET overdrive
- 50V/ns dV/dt rating for all HS and LS referenced circuitry
- Switching parameters:
  - Maximum propagation delay times: 30ns
  - Maximum delay matching: 5ns
- Fully specified in –40°C to +150°C junction temperature range
- QFN-16 package (3mm × 3mm)

2 Applications

- 48V-12V IBC for server power supply
- Floating topologies
  - Hybrid switched capacitor converter
  - Three-level buck converter
- 48V to Vcore direct conversion topologies
- 800V to 48V/12V secondary side FET drive
- Half-bridge and full-bridge DC-DC converter for Telecom power
- Multiphase PWM DC-DC converters
- Audio class-D amplifiers

3 Description

The LMG1208 is a robust floating half-bridge gate driver designed to drive two N-channel MOSFETs or enhancement mode GaN FETs with an absolute maximum bootstrap voltage of 120V. The device has 4.5A peak source and 5.5A peak sink current capability at 12V, allowing the LMG1208 to drive large power MOSFETs with minimized switching losses during the transition through the Miller Plateau. The switching nodes (HS, LS pins) can handle negative transient voltage, which protects the two floating domains from inherent negative voltages caused by parasitic inductance and stray capacitance.

The device, configured using a MODE pin, operates a variety of modes, such as independent input (IIM), single PWM, HSC_HS (hybrid switched-capacitor converter high side responder), HSC_LS (hybrid switched-capacitor converter low side responder), and HI LI inversion, giving the user complete flexibility to adopt the device in numerous topologies. The LMG1208 integrates a high-voltage high common mode support differential current sense amplifier with transconductance gain of 5uA/mV that can be used for inductor DCR or shunt based current sensing.

The PWM inputs support tri-state logic and can be interfaced to 3.3V PWM controllers independent of the operating supply voltage (5V or 12V). The low-side and high-side gate driver paths are matched to 5ns between the turn on and turn off of each other and are controlled through the EN/INL and PWM/INH input pins respectively. User can program the dead time in the range of 8ns to 100ns in single PWM mode using resistor to ground on DT pin. Same DT pin introduces rising edge delay on incoming PWM signals allowing dead time insertion in IIM mode and HSC modes as well. On-chip 120V rated bootstrap synchronous FET eliminates the need to add discrete bootstrap diode for HB domain. Bootstrap charging is controlled to prevent the gate voltage from exceeding the GaN FET maximum gate-to-source voltage rating. Device integrates robust level shifters from VDD to (LB-LS) and VDD to (HB-HS) domains. Undervoltage lockout (UVLO) is provided for VDD and for both the high-side (HB-HS) and the low-side (LB-LS) driver supply which forces the outputs low if the drive voltage is below the specified threshold.

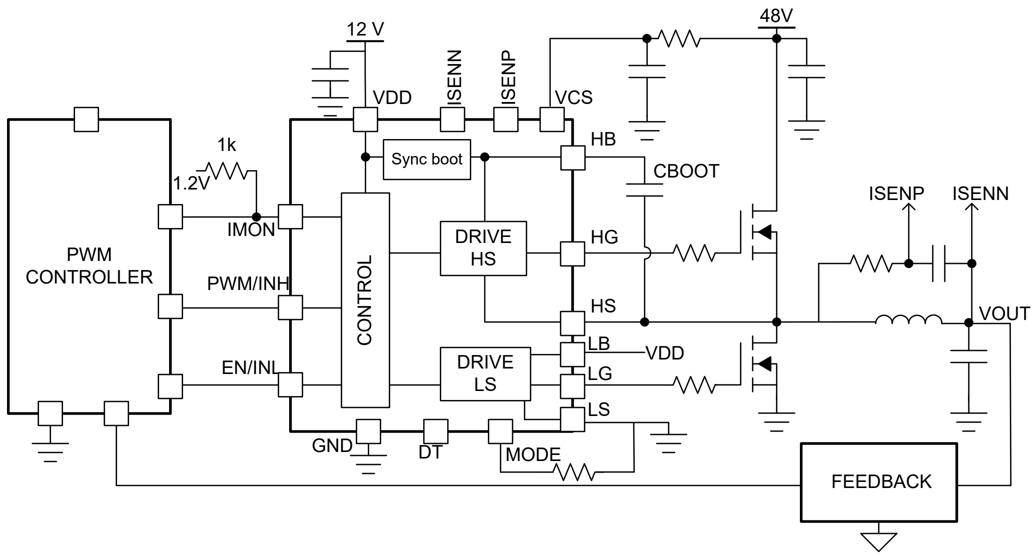
PRODUCT PREVIEW

PRODUCT PREVIEW

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LMG1208-1VEGR	VEG (WQFN, 16)	3mm × 3mm

(1) For all available packages, see the Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Application Diagram

Table of Contents

PRODUCT PREVIEW

PRODUCT PREVIEW

4 Pin Configuration and Functions

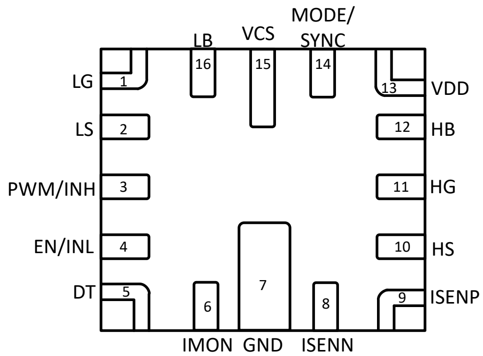


Figure 4-1. QFN Package 16-Pin WQFN Top View

Table 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	No.		
DT	5	I	Pin is with respect to GND. Programmable dead time or delay configuration pin. Put a resistor from this pin to GND. This programs dead time for single PWM mode. Controls rising turn-on delay for HI LI (IIM) mode and for HSC modes.
EN/INL	4	I	Pin is with respect to GND. In IIM mode, low side gate driver logic input. In single PWM mode, enables/disables both high side and low side gate drive. EN is active high.
GND	7	G	Analog logic ground.
HB	12	P	High side bootstrap supply voltage reference to HS pin
HG	11	O	High side FET driver output
HS	10	—	High side gate driver reference node.
IMON	6	O	Pin is with respect to GND. Current reporting output pin.
ISENN	8	I	Current sense, negative input pin. For inductor DCR sense, connect to other side of cap (output node).
ISENP	9	I	Current sense, positive pin. For inductor DCR sense, connect to center point of RC (in parallel to the external inductor).
LB	16	P	Low side bootstrap supply voltage reference to LS pin
LG	1	O	Low side FET driver output.
LS	2	-	Low side gate driver reference node.
PWM/INH	3	I	Pin is with respect to GND. In IIM mode, high side gate driver logic input. In single PWM mode, PWM input.
SYNC/MODE	14	I/O	Pin is with respect to GND. Mode configure with resistor to GND. Resistor value decides IIM, PWM, HSC_HS and HSC_LS mode. After power up and mode selection locked, this becomes SYNC output to drive PWM input to HSC responder device
VCS	15	P	Supply for internal current sense amplifier
VDD	13	P	Analog power supply for the device.

(1) G = Ground, I = Input, O = Output, P = Power, and I/O = Bidirectional

5 Specifications

5.1 Absolute Maximum Ratings

All voltages are with respect to GND (unless otherwise noted) See (1)

PARAMETER		MIN	MAX	UNIT
VDD	Maximum continuous supply voltage	-0.3	18	V
PWM/ INH, EN/INL to GND	PWM input pins continuous voltage	-0.3	8	V
	PWM input pins transient voltage, repetitive 100ns transients, ≤ 1Mhz frequency	-2	8	V
V_{LG}	Low side gate driver output voltage, continuous	V_{LS} - 0.3	V_{LB} + 0.3	V
	Low side gate driver output voltage, repetitive 100ns transients, ≤ 1Mhz frequency	V_{LS} - 2	V_{LB} + 0.3	V
V_{HG}	High side gate driver output voltage, continuous	V_{HS} - 0.3	V_{HB} + 0.3	V
	High side gate driver output voltage, repetitive 100ns transients, ≤ 1Mhz frequency	V_{HS} - 2	V_{HB} + 0.3	V
HS to GND (2)	Voltage on HS, continuous	-10	120	V
	Voltage on HS, repetitive 100ns transients, ≤ 1Mhz frequency	-20	120	V
LS to GND (2)	Voltage on LS, continuous	-10	120	V
	Voltage on LS, repetitive 100ns transients, ≤ 1Mhz frequency	-20	120	V
HB to GND (2)	Voltage on HB	-0.3	120	V
LB to GND (2)	Voltage on LB	-0.3	120	V
V_{HB-HS}, V_{LB-LS} (2)	Voltage on HB-HS, LB-LS	-0.3	18	V
DT, Mode to GND	Voltage on DT, MODE pin	-0.3	6	V
Sync to GND	Sync pin to GND	-0.3	8	V
V_{CS} to GND	Current sense amplifier supply pin voltage	-0.3	120	V
ISENP, ISENN to GND	Current sense amplifier input pins voltage	-0.3	40	V
ISENP-ISENN	Differential voltage across sense amplifier input pins	-0.3	5	V
IMON to GND	Current sense amplifier output pin voltage	-0.3	6	V
T_J	Junction Temperature	-40	175	°C
T_{stg}	Storage Temperature	-40	175	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All of these ratings apply simultaneously

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic Discharge	Human-body model (HBM), per ANSI/ ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

PRODUCT PREVIEW

PRODUCT PREVIEW

5.3 Recommended Operating Conditions

Unless otherwise noted, all voltages are with respect to GND

		MIN	NOM	MAX	UNIT
VCC : Silicon MOSFET usage		8	12	16	V
VCC : GaN FET usage		5	5.5	6	V
PWM/INH, EN/INL inputs		0		5.5	V
DT to GND	Dead time or turn-on delay resistor	1		100	kΩ
MODE to GND	Mode pin resistor to GND for various modes	0		120	kΩ
HB	Voltage on HB pin with respect to HS	V_{HS} + 4.5		V_{HS} + 16	V
LB	Voltage on LB pin with respect to LS	V_{LS} + 4.5		V_{LS} + 16	V
HS	Voltage on HS pin	$-V_{HB}$		100	V
LS	Voltage on LS pin	$-V_{LB}$		100	V
VCS	Current sense amplifier supply voltage	10		80	V
f_{MAX}	Maximum switching frequency (50% Duty Cycle)			2	MHz
HS, LS Slew with respect to[(1)]				50	V/ns
T_J	Operating junction temperature	-40		150	℃

(1) Determined through design and characterization. Not tested in production.

5.4 Thermal Information

THERMAL METRIC [(1)]		LMG1208 QFN 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	TBD	°C/W
$R_{\theta JC(Bot)}$	Junction-to-case (bottom) thermal resistance	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	TBD	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	TBD	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	TBD	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

Unless otherwise noted, no load on LG or HG, typical specifications are at 25℃; VDD and VCS across entire operating range unless otherwise noted [(1)]; Min/max limits apply for -40℃ ≤ T_J ≤150℃

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT PINS (PWM/INH, EN/INL)						
I_{PWMH}	PWM Sinking current	PWM pin = 5V, single PWM mode with EN = High OR HSC_LS mode OR HSC_HS mode OR HI LI mode OR HI LI inverted mode; VDD = 12V		1		mA
I_{PWML}	PWM sourcing current	PWM pin= 0V, single PWM mode with EN = High OR HSC_LS mode OR HSC_HS mode OR HI LI mode OR HI LI inverted mode; VDD = 12V		500		µA
I_{PWM_off}	PWM pin leakage current	Single PWM mode with EN = Low, PWM pin 5V or GND	-10		25	µA

Unless otherwise noted, no load on LG or HG, typical specifications are at 25℃; VDD and VCS across entire operating range unless otherwise noted (1); Min/max limits apply for -40℃ ≤ T_J ≤150℃

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{PWM_PU}	PWM pin pull-up resistance to internal 5V	PWM pin = 0V, single PWM mode with EN = High OR HSC_LS mode OR HSC_HS mode OR HI LI mode OR HI LI inverted mode; VDD = 12V		10		kΩ
R_{PWM_PD}	PWM pin pull-down resistance to GND	PWM pin= 5V, single PWM mode with EN = High OR HSC_LS mode OR HSC_HS mode OR HI LI mode OR HI LI inverted mode; VDD = 12V		5		kΩ
R_{INH_PD}, R_{INL_PD}	INH INL pin pull-down resistance to GND	HI LI mode OR HI LI inverted mode OR HI LI with boot disable, VDD = 12V	240	300	350	kΩ
V_{PWMH}	PWM Logic level high	single PWM mode with EN = High OR HSC_LS mode OR IIM mode OR HSC_HS mode, VDD = 12V	2.6		5.5	V
V_{PWML}	PWM Logic level low	single PWM mode with EN = High OR HSC_LS mode OR IIM mode OR HSC_HS mode, VDD = 12V	0		0.8	V
$V_{PWM\_Tristate}$	PWM tri-state window	single PWM mode with EN = High OR HSC_LS mode OR IIM mode OR HSC_HS mode, VDD = 12V	1		2.1	V
V_{PWM_3TV}	PWM pin Tri-state voltage	single PWM mode with EN = High OR HSC_LS mode OR IIM mode OR HSC_HS mode, VDD = 12V		1.5		V
V_{ENH}	High-Level Input Voltage Threshold	Rising Edge, EN buffer in single PWM mode, VDD = 12V		1.8	2.2	V
V_{ENL}	Low-Level Input Voltage Threshold	Falling Edge, EN buffer in single PWM mode, VDD = 12V	0.8	1.1		V
R_{EN_PD}	Input pull down resistance		250	300	350	kΩ
UNDER-VOLTAGE PROTECTION						
V_{VDDFET_THR}	VDD rising threshold for device to recognize Silicon MOSFET or GaN FET usage		6.8	7.3	7.8	V
V_{VDDFET_THF}	VDD falling threshold for device to recognize Silicon MOSFET or GaN FET usage		6.5	7	7.5	V
$V_{VDDFET\_TH\_HYS}$	VDD hysteresis for Silicon MOSFET or GaN FET detection			240		mV
V_{VDD_UVR}	V_{DD} Rising edge threshold for UVLO		3.9	4.2	4.5	V
V_{VDD_UVF}	V_{DD} Falling edge threshold for UVLO		3.7	3.9	4.2	V
$V_{VDD(UV\_hyst)}$	V_{DD} UVLO threshold hysteresis			300		mV
V_{HB_UVR}	HB Rising edge threshold for UVLO		3.3	3.7	4.2	V
V_{HB_UVF}	HB Falling edge threshold for UVLO		3.1	3.5	3.95	V
$V_{HB(UV\_hyst)}$	HB UVLO threshold hysteresis			200		mV
V_{LB_UVR}	LB Rising edge threshold for UVLO		3.3	3.7	4.2	V
V_{LB_UVF}	LB Falling edge threshold for UVLO		3.1	3.5	3.95	V
$V_{LB(UV\_hyst)}$	LB UVLO threshold hysteresis			200		mV
t_{PWRUP}	Power Up time (time after which PWM signals must be provided for power converter operation)				400	µs
SYNCHRONOUS BOOTSTRAP						

PRODUCT PREVIEW

PRODUCT PREVIEW

Unless otherwise noted, no load on LG or HG, typical specifications are at 25℃; VDD and VCS across entire operating range unless otherwise noted (1); Min/max limits apply for -40℃ ≤ T_J ≤150℃

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{DH\_BOOTFET}$	Forward voltage drop of synchronous boot switch (from VDD to HB)	I_{VDD-HB} = 5mA		25		mV
		I_{VDD-HB} = 50mA		250		mV
t_{SS1}	HB power up time	VDD = 5V, C_{BOOT} = 100nF, LI = toggling@300khz, HS = GND		4		µs
t_{SS1}	HB power up time	C_{BOOT} = 1 µF, LI = toggling@300khz, HS = GND		27		µs
t_{SS2}	HB power up time	VDD = 12V, C_{BOOT} = 100nF, LI = toggling@300khz, HS = GND		5		µs
t_{SS2}	HB power up time	VDD = 12V, C_{BOOT} = 1 µF, LI = toggling@300khz, HS = GND		34		µs
I_R	Reverse bias leakage of boot switch	V_{HB} = 100V, VDD=12V		0.1		µA
SUPPLY CURRENTS						
I_{DD_IIM}	VDD Quiescent Current	LI = HI = 0V, VDD = HB = LB = 12V, GND= HS = LS; IIM Mode, DT float		1.4	1.6	mA
		LI = HI = 0V, VDD = HB = LB = 5V, GND= HS = LS; IIM Mode, DT float		1.1	1.3	mA
I_{DDO_IIM}	Total VDD Operating Current (includes bootstrap current)	HI LI 50% duty square wave (0 to 5V amplitude), Fsw=500khz, VDD = LB = 12V, GND = LS = HS; IIM Mode, DT float, HB-HS cap = 1uF		3	3.5	mA
		HI LI 50% duty square wave (0 to 5V amplitude), Fsw=500khz, VDD = LB = 5V, GND= HS = LS; IIM Mode, DT float, HB-HS cap = 1uF		2.2	2.6	mA
I_{HB_IIM}	HB Quiescent Current	LI = HI = 0V, VDD = LB = 12V, GND= LS; IIM Mode, DT float, Apply HB-HS externally 12V		0.3	0.4	mA
		LI = HI = 0V, VDD = LB = 5V, GND= LS; IIM Mode, DT float, Apply HB-HS externally 5V		0.2	0.3	mA
I_{HBO_IIM}	HB Operating Current	HI 50% duty square wave (0 to 5V amplitude), Fsw=500khz, VDD = LB = 12V, GND= LS; IIM Mode, DT float, LI = low, Apply HB-HS externally 5V		0.8	1	mA
		HI 50% duty square wave (0 to 5V amplitude), Fsw=500khz, LI low, VDD = LB = 5V, GND= LS; IIM Mode, DT float,Apply HB-HS externally 5V		0.5	0.6	mA
I_{DD_PWM}	VDD Quiescent Current	Single PWM mode, PWM pin= floating, EN= 0V, R_{DT} = 6k, VDD = HB = LB = 12V, GND= HS = LS		1.7	2	mA
		Single PWM mode, PWM pin= floating, EN= 0V, R_{DT} = 100k, VDD = HB = LB = 12V, GND= HS = LS		1.7	1.9	mA
I_{DD_PWM}	VDD Quiescent Current	Single PWM mode, PWM pin= floating, EN= 5V, R_{DT} = 6k, VDD = HB = LB = 5V, GND= HS = LS		1.7	2.2	mA
		Single PWM mode, PWM pin= floating, EN= 5V, R_{DT} = 100k, VDD = HB = LB = 5V, GND= HS = LS		1.7	2.1	mA

Unless otherwise noted, no load on LG or HG, typical specifications are at 25℃; VDD and VCS across entire operating range unless otherwise noted (1); Min/max limits apply for -40℃ ≤ T_J ≤150℃

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DDO_PWM}	Total VDD Operating Current (includes bootstrap current)	Single PWM mode, PWM = 500khz square wave 50% duty 0-5V amplitude, EN = 5V, R_{DT} = 20k, VDD = LB = 12V, GND= HS = LS, HB-HS boot cap 1uF		3.5	4	mA
I_{HB_PWM}	HB Quiescent Current	Single PWM mode, PWM pin= floating, EN= 0V, VDD = LB = 12V, GND= LS, Apply HB-HS externally 12V		0.3	0.4	mA
		Single PWM mode, PWM pin= floating, EN= 5V, VDD = LB = 5V, GND= LS,Apply HB-HS externally 5V		0.3	0.4	mA
I_{HBO_PWM}	HB Operating Current	Single PWM mode, PWM = 500khz square wave 50% duty 0-5V amplitude, EN = 5V, VDD = LB = 12V, GND= LS, Apply HB-HS externally 12V		0.8	1	mA
DEAD TIME_DELAY CONTROL						
t_{delay_1k}	Rising edge delay for 1k DT resistor	HI LI IIM mode or HSC_LS mode Or HSC_HS mode, delay inserted in PWM_HS, PWM_LS and in PWM_responder rising edge; R_{DT} = 1kΩ	6	9	13	ns
t_{delay_6k}	Rising edge delay for 6k DT resistor	HI LI IIM mode or HSC_LS mode Or HSC_HS mode, delay inserted in PWM_HS, PWM_LS and in PWM_responder rising edge; R_{DT} = 6kΩ	9	12	15	ns
t_{delay_center}	Center point rising edge delay	HI LI IIM mode or HSC_LS mode Or HSC_HS mode, delay inserted in PWM_HS, PWM_LS and in PWM_responder rising edge; R_{DT} = 50kΩ	40	49	56	ns
t_{delay_max}	Maximum rising edge delay	HI LI IIM mode or HSC_LS mode Or HSC_HS mode, delay inserted in PWM_HS, PWM_LS and in PWM_responder rising edge; R_{DT} = 100kΩ	80	95	108	ns
t_{dead_1k}	Dead time for 1k DT resistor	Single PWM mode; Dead time inserted between HG rising and LG falling edge/ HG falling and LG rising edge; R_{DT} = 1kΩ	6	9	13	ns
t_{dead_6k}	Dead time for 6k DT resistor	Single PWM mode; Dead time inserted between HG rising and LG falling edge/ HG falling and LG rising edge; R_{DT} = 6kΩ	9	12	15	ns
t_{dead_center}	Center point dead time	Single PWM mode; Dead time inserted between HG rising and LG falling edge/ HG falling and LG rising edge; R_{DT} = 50kΩ	40	49	56	ns
t_{dead_max}	Maximum dead time	Single PWM mode; Dead time inserted between HG rising and LG falling edge/ HG falling and LG rising edge; R_{DT} = 100kΩ	80	95	108	ns
	Bypass internal delay (no delay inserted)	DT pin floated; not applicable to single PWM mode		0		ns
SYNC OUTPUT BUFFER						

PRODUCT PREVIEW

PRODUCT PREVIEW

Unless otherwise noted, no load on LG or HG, typical specifications are at 25℃; VDD and VCS across entire operating range unless otherwise noted (1); Min/max limits apply for -40℃ ≤ T_J ≤150℃

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High level output voltage	I_{OH} = -4mA (Vcc is internal 5V rail)	4.2	4.8		V
V_{OL}	Low level output voltage	I_{OL} = 4 mA		0.2	0.3	V
t_{PLH}, t_{PHL}	Propagation delay (HSC_HS mode)	Device in HSC_HS mode ; 180k || 10pF Sync output buffer load; Measured from 50% of incoming PWM on INL to 50% of Sync PWM output		4	9	ns
PWD	Pulse width distortion |t_{PHL}-t_{PLH}|				2	ns
t_{PLH}, t_{PHL}	Propagation delay (HSC_LS mode)	Device in HSC_LS mode ; 54k || 10pF Sync output buffer load; Measured from 50% of incoming PWM on INH to 50% of Sync PWM output		4	9	ns
PWD	Pulse width distortion |t_{PHL}-t_{PLH}|				2	ns
t_{PLH_P2P}, t_{PHL_P2P}	Part-to-part Propagation delay variation, HSC_HS mode	T_J = 125℃, HSC_HS Prop delay setup			TBD	ns
t_{PLH_P2P}, t_{PHL_P2P}	Part-to-part Propagation delay variation, HSC_LS mode	T_J = 125℃, HSC_LS Prop delay setup			TBD	ns
t_r	Output signal rise	10pF cap load on sync output pin; Measured from 10% to 90% for t_r and 90% to 10% for t_f		2	3	ns
t_f	Output signal fall time			1	2	ns
MODE						
$R_{MODE\_HILI\_INV}$	Resistor from MODE pin to GND for HI LI inverted mode setting		0		1.5	kΩ
R_{MODE_HILI}	Resistor from MODE pin to GND for HI LI (IIM) mode setting		3.6	4.02	4.4	kΩ
R_{MODE_PWM}	Resistor from MODE pin to GND for single PWM mode setting		14.3	15.8	17.3	kΩ
$R_{MODE\_HSC\_LS}$	Resistor from MODE pin to GND for HSC_LS mode setting		50	54	60	kΩ
$R_{MODE\_HSC\_HS}$	Resistor from MODE pin to GND for HSC_HS mode setting		165	180	190	kΩ
$R_{MODE\_HILI\_BD}$	Resistor from MODE pin to GND for HI LI (IIM) mode with boot disable			Float		
DCR CURRENT SENSE						
Vos	Input offset voltage	T_J = 40℃ to 110℃, Output CM = 1.2V, VCS = 48V, VICM = 12V			0.5	mV
I_{B1}	Input leakage current: ISENP terminal	T_J = 40℃ to 110℃			100	nA
I_{B2}	Input leakage current: ISENN terminal	T_J = 40℃ to 110℃			200	µA
V_{ICM}	Input common mode voltage at amplifier inputs	ISENP, ISENN terminals	0		35	V
V_{IDM}	Input differential voltage at amplifier inputs	ISENP-ISENN	-150		150	mV
I_{OUT_IMON}	Output current capability	IMON terminal	-750		750	µA
V_{OUT_IMON}	Output voltage range	IMON terminal	0.5		4	V
BW	3dB Bandwidth of the current sense amplifier		5			Mhz
A_I	Transconductance gain of amplifier	Average Vin = 30mV, VCS = 48V, VICM = 12V, 40℃ to 110℃	4.9	5	5.1	µA/mV
A_I	Transconductance gain of amplifier	Average Vin = 60mV, VCS = 48V, VICM = 12V, 40℃ to 110℃	4.9	5	5.1	µA/mV
VCS	Current sense amplifier supply voltage		10		80	V

Unless otherwise noted, no load on LG or HG, typical specifications are at 25℃; VDD and VCS across entire operating range unless otherwise noted (1); Min/max limits apply for -40℃ ≤ T_J ≤150℃

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CS}	Current consumption from VCS terminal	VCS terminal, DCR sensed with 500khz changing current waveform, VCS pin voltage = 60V			300	µA
LG GATE DRIVER						
V_{OL_LG}	Low-Level output voltage	I_{LG} = 100mA sink; LB = VDD = 5V or 12V, LS = GND		0.05	0.1	V
V_{OH_LG}	High-Level output voltage	I_{LG} = 100mA source; LB = VDD = 5V or 12V, LS = GND; V_{OH_LG} = VDD - V_{LG}		0.1	0.15	V
I_{OH_LG}	Peak Pull-up source current	V_{LG} = 0V, LB = VDD = 12V, LS = GND		5		A
		V_{LG} = 0V, LB = VDD = 5V, LS = GND		3.5		A
I_{OL_LG}	Peak Pull-down sink current	V_{LG} = 12V, LB = VDD = 12V, LS = GND		6		A
		V_{LG} = 5V, LB = VDD = 5V, LS = GND		4.5		A
HG GATE DRIVER						
V_{OL_HG}	Low-Level output voltage	I_{HG} = 100mA sink; HB = VDD = 5V or 12V, HS = GND		0.05	0.1	V
V_{OH_HG}	High-Level output voltage	I_{HG} = 100mA source; HB = VDD = 5V or 12V, HS = GND V_{OH_HG} = VDD - V_{HG}		0.1	0.15	V
I_{OH_HG}	Peak Pull-up source current	V_{HG} = 0V, HB = VDD = 12V, HS = GND		5		A
		V_{HG} = 0V, HB = VDD = 5V, HS = GND		3.5		A
I_{OL_HG}	Peak Pull-down sink current	V_{HG} = 12V, HB = VDD = 12V, HS = GND		6		A
		V_{HG} = 5V, HB = VDD = 5V, HS = GND		4.5		A

(1) Parameters that show only a typical value are determined by design and may not be tested in production

5.6 Swiching Characteristics

V_{DD} = V_{HB} = V_{LB} = 12V OR 5.5V, V_{HS} = V_{LS} = GND = 0V; Unless otherwise specified, No load on LG or HG; typical specifications are at 25℃ (1); -40℃ ≤ T_J ≤150℃

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PROPAGATON DELAYS_IIM mode						
t_{PDINL_F}	LG Turn-off propagation delay	INL = high to low, VDD = 12V, DT float	18	25	32	ns
		INL = high to low, VDD = 5.5V, DT float	18	24	29	ns
t_{PDINL_R}	LG Turn-on propagation delay	INL = low to high, VDD = 12V, DT float	20	28	36	ns
		INL = low to high, VDD = 5.5V, DT float	20	26	33	ns
t_{PDINH_F}	HG Turn-off propagation delay	INH = high to low, VDD = 12V, DT float	18	25	32	ns
		INH = high to low, VDD = 5.5V, DT float	18	24	29	ns

PRODUCT PREVIEW

$V_{DD} = V_{HB} = V_{LB}$ = 12V OR 5.5V, $V_{HS} = V_{LS}$ = GND = 0V; Unless otherwise specified, No load on LG or HG; typical specifications are at 25℃ [(1)]; -40℃ ≤ T_J ≤150℃

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PDINH_R}	HG Turn-on propagation delay	INH = low to high, VDD = 12V, DT float	20	28	36	ns
		INH = low to high, VDD = 5.5V, DT float	20	26	33	ns
t_{IIM_MON}	Propagation delay matching	125℃		2	4	ns
		-40℃ to 150℃		2	4.5	ns
t_{IIM_MOFF}	Propagation delay matching	125℃		2	4	ns
		-40℃ to 150℃		2	4.5	ns
PROPAGATION DELAYS_PWM MODE						
t_{PD_PWMF}	Turn-off propagation delay	EN=5V, R_{DT} = 1k (min allowed), VDD = 12V, PWM falling to HG falling delay	18	25	32	ns
		EN=5V, R_{DT} = 1k (min allowed), VDD = 5.5V, PWM falling to HG falling delay	18	24	29	ns
t_{PD_PWMR}	Turn-on propagation delay	EN=5V, R_{DT} = 1k (min allowed), VDD = 12V, PWM rising to LG falling delay	18	25	32	ns
		EN=5V, R_{DT} = 1k (min allowed), VDD = 5.5V, PWM rising to LG falling delay	18	24	29	ns
$t_{PD\_PWM\_M}$	Propagation delay matching	125℃, EN=5V, R_{DT} = 1k (min allowed), $\lvert t_{PD\_PWMF} - t_{PD\_PWMR} \rvert$ for LG or HG		10	15	ns
		-40℃ to 150℃, EN=5V, R_{DT} = 1k (min allowed), $\lvert t_{PD\_PWMF} - t_{PD\_PWMR} \rvert$ for LG or HG		10	15	ns
OUTPUT RISE/FALL TIME						
t_{RISE1}	LG/HG Output rise time	C_{load} on LG/HG = 1nF, VDD = HB = LB = 12V, GND = HS = LS = 0V, 10% to 90% of LG/HG		5	7	ns
		C_{load} on LG/HG = 1nF, VDD = HB = LB = 5.5V, GND = HS = LS = 0V, 10% to 90% of LG/HG		12	18	ns
t_{RISE2}		C_{load} on LG/HG = 100nF, VDD = HB = LB = 12V, GND = HS = LS = 0V, 10% to 90% of LG/HG		300	440	ns
		C_{load} on LG/HG = 100nF, VDD = HB = LB = 5.5V, GND = HS = LS = 0V, 10% to 90% of LG/HG		280	390	ns
t_{FALL1}	LG/HG Output fall time	C_{load} on LG/HG = 1nF, VDD = HB = LB = 12V, GND = HS = LS = 0V, 90% to 10% of LG/HG		4	6	ns
		C_{load} on LG/HG = 1nF, VDD = HB = LB = 5.5V, GND = HS = LS = 0V, 90% to 10% of LG/HG		3	5	ns
t_{FALL2}		C_{load} on LG/HG = 100nF, VDD = HB = LB = 12V, GND = HS = LS = 0V, 90% to 10% of LG/HG		240	340	ns
		C_{load} on LG/HG = 100nF, VDD = HB = LB = 5.5V, GND = HS = LS = 0V, 90% to 10% of LG/HG		150	250	ns
MISCELLANEOUS						

V_{DD} = V_{HB} = V_{LB} = 12V OR 5.5V, V_{HS} = V_{LS} = GND = 0V; Unless otherwise specified, No load on LG or HG; typical specifications are at 25℃ (1); -40℃ ≤ T_J ≤150℃

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{3HT}	Tri-state Shutdown Hold-Off Time	single PWM mode with EN = High OR HSC_LS mode OR HSC_HS mode OR IIM mode	20	28	43	ns
t_{3SD1}	Tri-state High Side FET Shutdown Propagation Delay	Includes tristate hold-off time; single PWM mode with EN = High OR HSC_LS mode OR HSC_HS mode OR IIM mode;	30	40	60	ns
t_{3SD2}	Tri-state low Side FET Shutdown Propagation Delay	Includes tristate hold-off time; single PWM mode with EN = High OR HSC_LS mode OR HSC_HS mode OR IIM mode;	30	40	60	ns
t_{3RD1}	Tri-state Recovery Propagation Delay for High side FET	single PWM mode with EN = High OR HSC_LS mode OR HSC_HS mode OR IIM mode;	20	28	35	ns
t_{3RD2}	Tri-state Recovery Propagation Delay for low side FET	single PWM mode with EN = High OR HSC_LS mode OR HSC_HS mode OR IIM mode;	20	28	35	ns
t_{EN_R}	EN rising to HG rising propagation delay	PWM = 5V	20	28	35	ns
t_{EN_F}	EN falling to HG falling propagation delay	PWM = 5V	15	20	25	ns

(1) Parameters that show only a typical value are determined by design and may not be tested in production

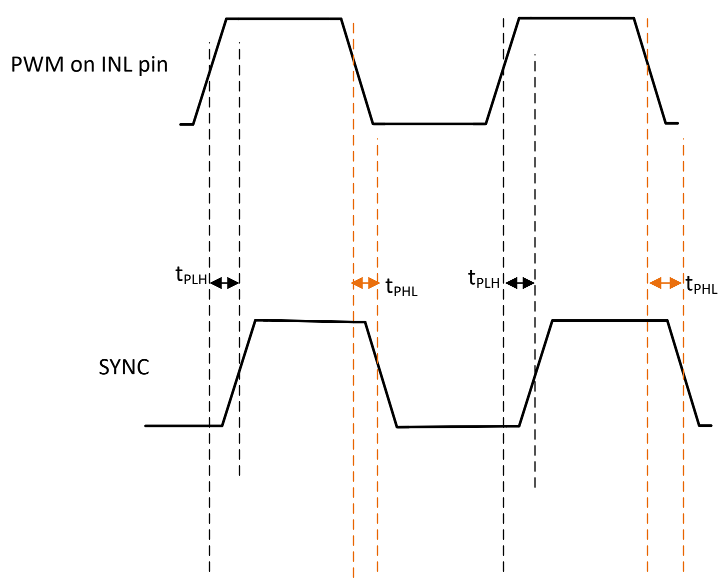


Figure 5-1. SYNC Timing HSC_HS Mode

PRODUCT PREVIEW

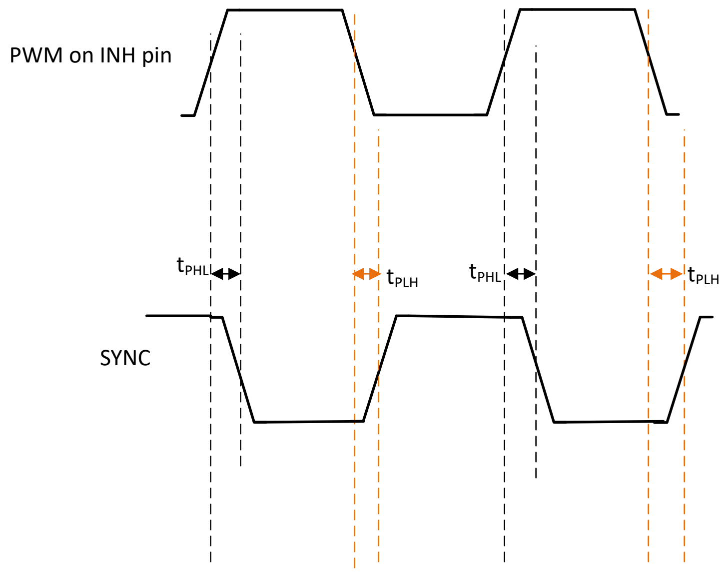
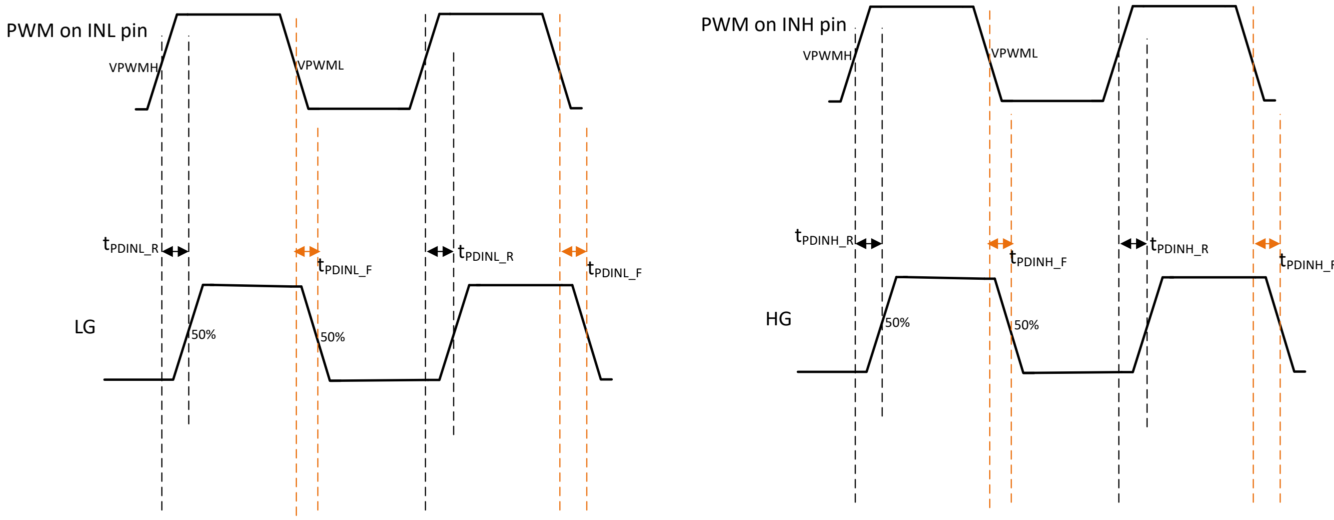


Figure 5-2. SYNC Timing HSC_LS Mode

PRODUCT PREVIEW



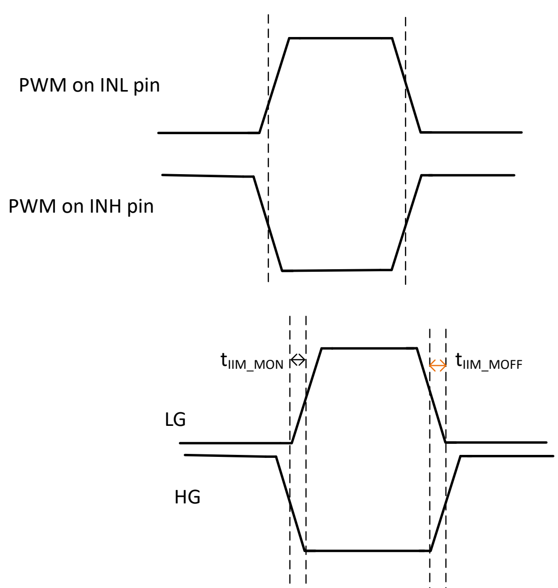


Figure 5-3. IIM Mode Timing

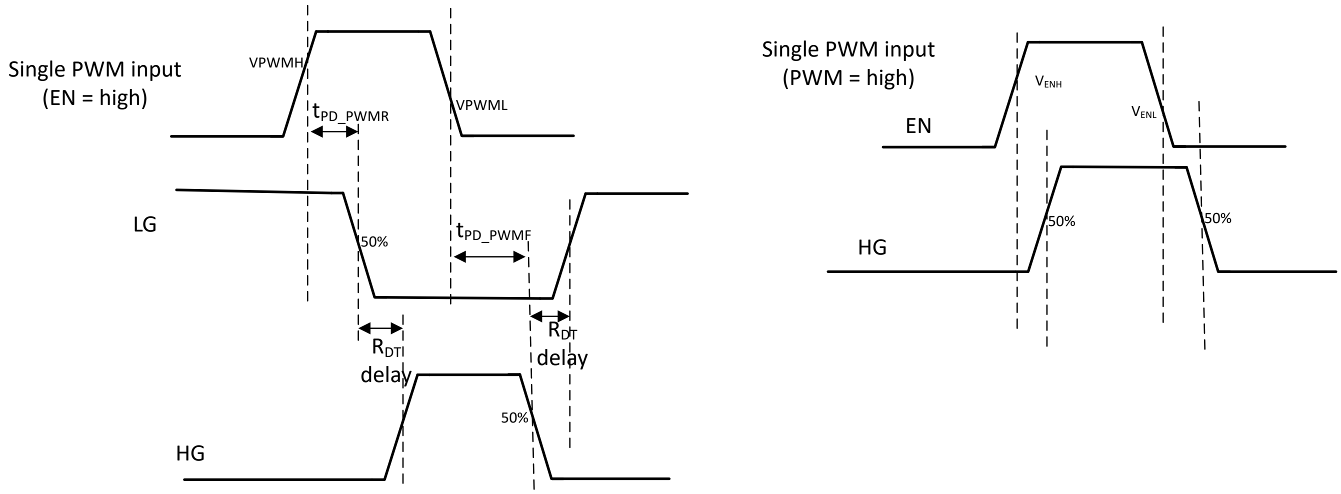


Figure 5-4. Single PWM Mode Timing

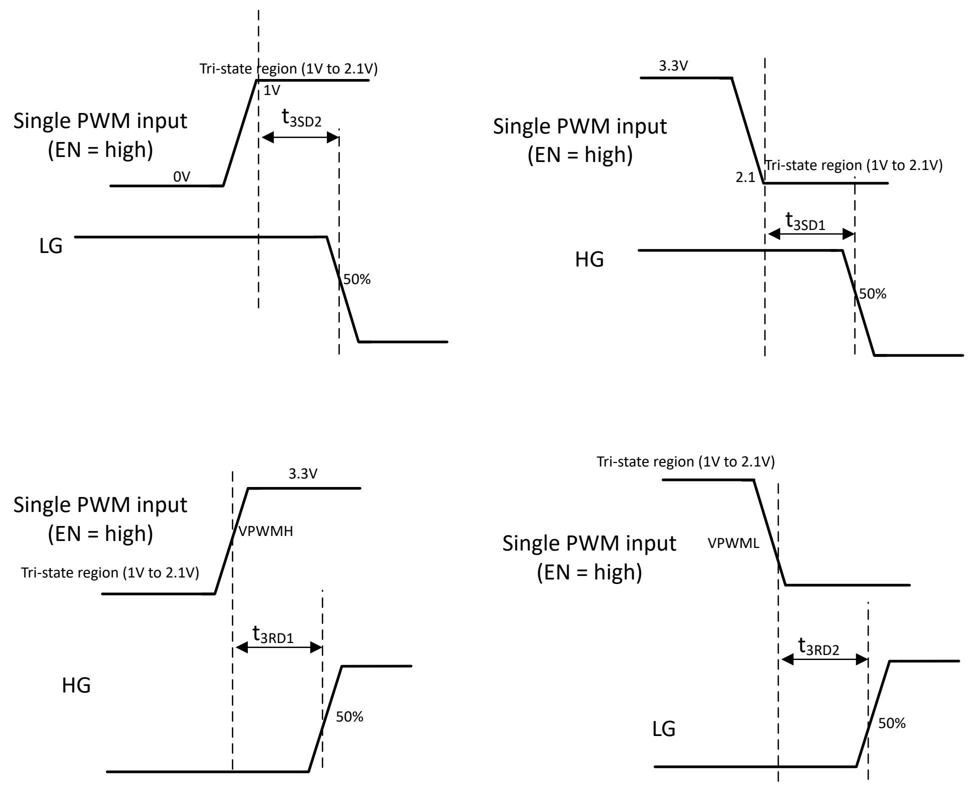


Figure 5-5. Tristate Timing

6 Detailed Description

6.1 Overview

The LMG1208 is a floating half-bridge gate driver designed to drive N-channel MOSFETs or e-mode GaN FETs in a half-bridge configuration. The device features two input buffers, the functionality of the input buffers is dependent on the operating mode of the device set by the MODE pin. The device incorporates the PWM logic needed to drive six FET HSC converter from two incoming PWMs. DT pin configures the dead time in single PWM mode between the turn-on and turn-off transitions of the high-side and low-side FET. In all the other operating modes of the device, the DT delays the rising edge of all the PWMs, thereby inserting dead time. The floating high-side driver and low side driver is capable of operating with HB/LB voltages up to 120V, with respect to GND. A 120V synchronous bootstrap FET is integrated in the LMG1208 device to charge the high-side (HB-HS) gate drive bootstrap capacitor. Integrated robust level shifters from VDD domain to HB/LB domains are capable to operate at high speed (> 2Mhz) while consuming low power and providing clean level transitions from the control logic (VDD) domain to the floating gate drivers in HB/LB domains. Undervoltage lockout (UVLO) is provided on all three power rails: VDD, HB-HS, and LB-LS.

The LMG1208 integrates a high-voltage precise current sense amplifier that can be used for current sensing using shunt resistor or using inductor DCR method. The transconductance amplifier supports input common-mode voltage up to 35V and can be used for peak current mode control or current balancing between multiple phases. The high-side gate driver is referenced to the switch node (HS), and the low-side driver is referenced to LS. The LMG1208 floating domains provides the flexibility to the user to configure the device in synchronous buck or boost configurations by connecting LB to VDD, LS to GND on the PCB. Whereas for floating topologies such as Hybrid switched-capacitor (HSC) converter, HB and LB domains can be the gate drive domains for top and middle FETs respectively, while VDD can be the gate drive domain for the bottom FET in HSC stack.

PRODUCT PREVIEW

Table 6-1. LMG1208 Highlights

FEATURE	BENEFIT
3A peak source and 4A peak sink current at VDD = 5V for GaN FETs, 4.5A peak source and 5.5A peak sink current at VDD = 12V for Silicon MOSFETs	High peak current capable of driving large power FETs with minimal power loss (fast-drive capability at Miller plateau)
Switch nodes HS/LS and gate driver output pins HG/LG can sustain negative transients	Increased robustness and ability to handle undershoot and overshoot because of the PCB parasitics
120V internal synchronous boot FET to charge HB domain while LB domain completely floating	Balance between integration and cost to target various topologies such as Buck, Boost, HSC, Three Level buck, and so forth
Precise low-offset current sense amplifier	Reduces BOM cost and PCB space compared to other regular half-bridge gate drivers where current sensing uses external amplifier
32ns maximum propagation delay with 5ns maximum delay mismatch	Best-in-class switching characteristics to reduce dead time losses and enable fast closed loop response
MODE functionality	Provides flexibility to the end application for configuring the device in different modes such as IIM (independent input mode), single PWM, HSC_HS (hybrid switched capacitor converter with high side responder), HSC_LS (hybrid switched capacitor converter with low side responder) and IIM inverted modes.
Dead time configuration via the DT pin	For multiphase applications where single PWM is used per phase, dead time between high side FET and low side FET can be easily set by DT resistor to GND to avoid cross-conduction of the FETs. Even if the controller has the capability to provide two independent PWMs, DT can be used to insert dead time by shifting the rising edge of the incoming PWM- useful for applications such as HSC converter.
HSC PWM logic	48V-12V Multiphase HSC converter (total 6 FETs per HSC block) can be driven with only 2 incoming PWMs per HSC block.
Tri-state input buffers	Tri-state functionality can be used to turn-off the FET in fault conditions and also ensures the FET remains off at start-up where some controllers have mid-rail bias on PWM controller outputs after power-up.

6.2 Functional Block Diagram

Figure 6-1 shows the functional block diagram of the LMG1208 device. The device integrates:

- Synchronous bootstrap supply for HB-HS domain
- Gate driver for HB and LB domain
- Input buffer, PWM logic and control, dead time, and mode configuration block
- Sync output buffer (useful in hybrid switched capacitor topology implementation)
- Level shifters from VDD to HB-HS and to LB-LS domains
- Current sense amplifier

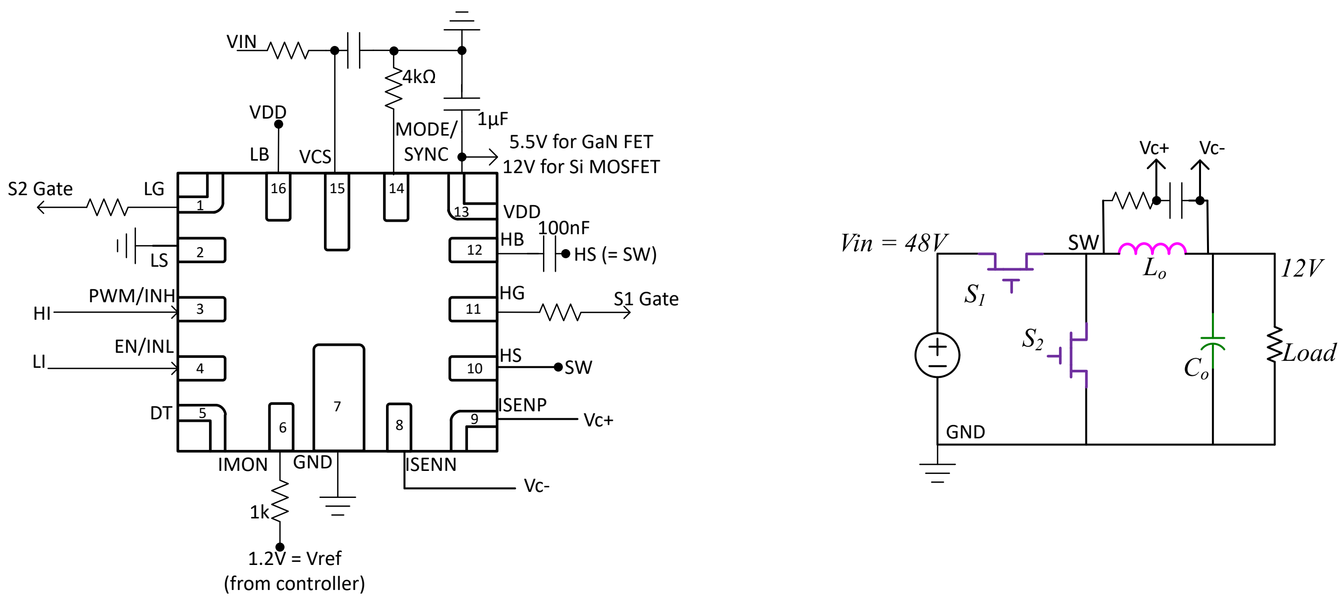


Figure 6-1. LMG1208 Functional Block Diagram

6.3 Feature Description

6.3.1 Input Buffer Stages

The LMG1208 has 2 input buffers. PWM/INH terminal is buffer1 and controls the input to gate drive in HB-HS domain. EN/LI terminal is buffer2 and controls the input to gate drive in LB-LS domain. The inputs are 3.3V and 5V logic level compatible, independent of the supply voltage VCC. The resistor structure of these 2 input pins is controlled by the device depending on the operational mode of the device (configured through the MODE resistor to GND). Both the input buffers run on internally generated supply rail 5V (typical) when the device is used for Silicon MOSFET drive and VDD supply can be anywhere from 8V to 16V. For GaN FET usage, since VDD rail is from 5V to 6V, input buffers run directly on VDD supply.

Input buffer supports 2-state thresholds or 3-state (also called tri-state logic) thresholds depending on the operating mode as detailed in Table 6-4. Below is a generic table for a 2 state input buffer and a tri-state input buffer:

Table 6-2. 2 State Input Buffer

Input Voltage Level	Description
0V to 0.8V	Device considers as logic low
2.2V and above	Device considers as logic high

Table 6-3. Tri-State Input Buffer

Input Voltage Level	Description
0V to 0.8V	Device considers as logic low

Table 6-3. Tri-State Input Buffer (continued)

Input Voltage Level	Description
1V to 2.1V	Device considers as tri-state region if signal dwells in this voltage range for more than tristate hold-off time (t_{3HT})
2.6V and beyond	Device considers as logic high

INH and INL are interchangeably referred to as HI and LI respectively throughout the data sheet. See below table for the Input buffer logic:

Table 6-4. Input Buffer Logic

MODE	Tri-state PWM input support	PWM/INH (buffer1)	EN/ INL(Buffer2)	Buffer1 Input configuration	Buffer2 Input configuration
HI LI inverted	Yes for both (buffer1 and buffer2)	INH	INL	300kΩ pull-down resistor to GND	300kΩ pull-down resistor to GND
HI LI	Yes for both (buffer1 and buffer2)	INH	INL	300kΩ pull-down resistor to GND	300kΩ pull-down resistor to GND
Single PWM	Yes only for buffer1; Buffer2 is 2-state	PWM	EN	10kΩ pull-up resistor to internal 5V rail, 5kΩ pull-down resistor to GND	300kΩ pull-down resistor to GND
HSC_LS	Yes for both (buffer1 and buffer2)	PWM1	PWM2	10kΩ pull-up resistor to internal 5V rail, 5kΩ pull-down resistor to GND	10kΩ pull-up resistor to internal 5V rail, 5kΩ pull-down resistor to GND
HSC_HS	Yes for both (buffer1 and buffer2)	PWM1	PWM2	10kΩ pull-up resistor to internal 5V rail, 5kΩ pull-down resistor to GND	10kΩ pull-up resistor to internal 5V rail, 5kΩ pull-down resistor to GND
HI LI with boot disable	Yes for both (buffer1 and buffer2)	INH	INL	300kΩ pull-down resistor to GND	300kΩ pull-down resistor to GND

6.3.2 Enable (Applicable Only to Single PWM Mode)

The device has an enable (EN) pin which is only applicable in single PWM mode. The gate driver outputs (HG and LG) are active only if the EN pin voltage is above the threshold voltage. Outputs are held low if the EN pin is left floating or pulled-down to ground. An internal 300kΩ resistor pulls the EN pin to GND. Thus, leaving the EN pin floating disables both the gate drive signals. Externally pulling EN pin to ground also disables both the gate drive.

Table 6-5. Single PWM Mode With EN Function

EN	PWM	HG	LG
L	x	Low	Low
H	L	Low	High
H	H	High	Low
H	Float	Low	Low
H	Driven to Tri-state range (from 1V to 2.1V)	Low	Low

6.3.3 MODE Configuration

The LMG1208 has a MODE pin which configures the device in various operational modes. User can put a resistor from MODE pin to GND- see MODE section under Section 5.5 for resistor values. Depending on the end application and the power converter topology, MODE provides the flexibility to the LMG1208 to be used in multiple configurations.

MODE resistor cannot be changed dynamically in an application. MODE has internal current source to detect the value of the resistor connected. At the startup, MODE is sampled and device locks the operational mode. Post-that, in HSC_HS and HSC_LS modes, this terminal becomes SYNC output buffer. MODE also configures the type of input buffer and resistor structure on both the input buffers. See SYNC Output Buffer for more details.

Below function table describes the operational modes of LMG1208.

Table 6-6. MODE Setting

R_{MODE}	Operational mode	Description
Short to GND	HI LI inverted	Device inverts both the incoming PWMs on INH (HI) and INL (LI) pins. Useful for applications where some FETs (in specific topology) are to be driven in complementary fashion.
4kΩ	HI LI	Regular use case for, for example, buck or boost converter where PWM controller provides 2 incoming PWMs.
15.8kΩ	Single PWM	Device takes in single PWM and generates complementary PWM. Useful for multiphase applications where the PWM controller is only able to provide single PWM for one half-bridge phase.
54kΩ	HSC LS	Useful for Hybrid switched capacitor converter. Device takes in two incoming PWMs from the controller and generates third PWM and drives SYNC output buffer according to this third PWM. See applications section for HSC topology implementation.
180kΩ	HSC_HS	
Float (Open)	HI LI with boot disable	Internal bootstrap path (from VDD to HB) is disabled to provide flexibility to generate bootstrap externally on PCB.

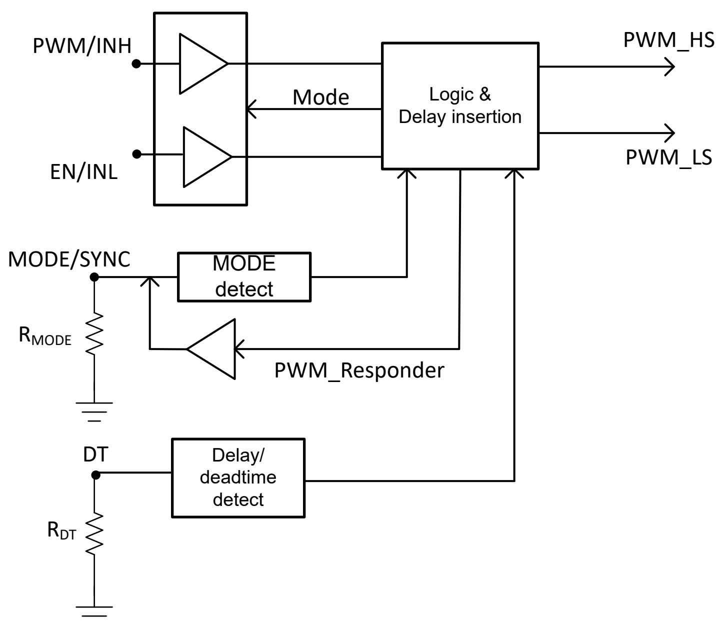


Figure 6-2. MODE

6.3.4 SYNC Output Buffer

The LMG1208 integrates a PWM output buffer, called a SYNC. This is useful to control the responder LMG1208 driver in HSC_HS and HSC_LS modes. SYNC runs on the same supply rail as the two input buffers. SYNC is only applicable to HSC_HS and HSC_LS modes. In all other operational modes, SYNC output buffer is disabled internally. See Integrated PWM Logic for the encoding used in the device to generate the SYNC output.

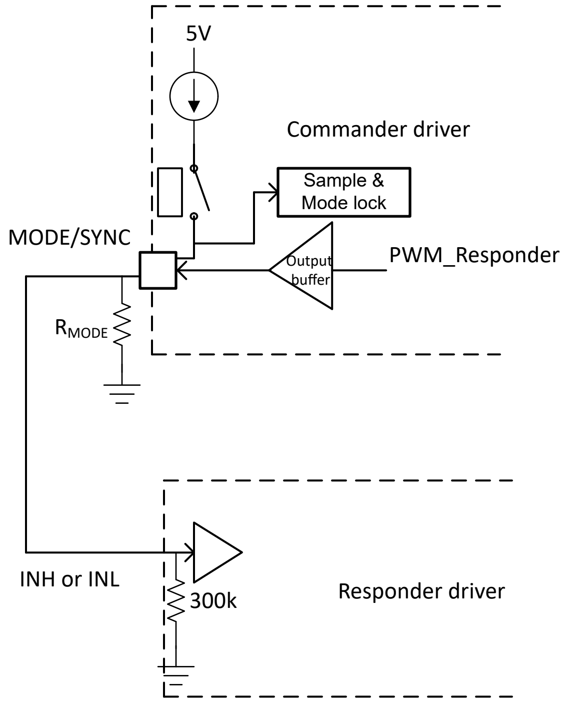


Figure 6-3. SYNC

6.3.5 Integrated PWM Logic

The LMG1208 integrates PWM logic as shown in the table below. Based on the MODE configuration, this integrated logic decides PWM_HS (PWM for gate driver in HB-HS domain), PWM_LS (PWM for gate driver in LB-LS domain) and PWM_Responder as the input to the SYNC output buffer.

Table 6-7. PWM Logic

MODE	PWM_LS	PWM_HS	PWM_Responder	Description
HI LI inverted	$\overline{INL}$	$\overline{INH}$	Disabled	Device inverts the incoming PWM on INH and INL pins. If any incoming PWM is in tri-state window for more than tri-state hold-off time, device makes the corresponding PWM output low
HI LI	INL	INH	Disabled	Device is transparent to the incoming PWMs on INH INL pins. If any incoming PWM is in tri-state window for more than tri-state hold-off time, device makes the corresponding PWM output low
Single PWM	$\overline{INH}$	INH	Disabled	Device generates complementary PWM for PWM_LS using incoming PWM on INH pin. If incoming single PWM is in tri-state window for more than the tri-state hold-off time, device makes both the PWM_HS and PWM_LS low
HSC_LS	INH AND $\overline{INL}$	INL	$\overline{INH}$	Device in this mode needs to drive top and middle FET of HSC stack, and sends PWM_responder for bottom FET on Sync output buffer. If any incoming PWM (on INH INL pins) is in tri-state window for more than tri-state hold-off time, device makes PWM_HS, PWM_LS and PWM_responder all low.
HSC_HS	$\overline{INH}$	INH AND $\overline{INL}$	INL	Device in this mode needs to drive bottom and middle FET of HSC stack, and sends PWM_responder for top FET on Sync output buffer. If any incoming PWM (on INH INL pins) is in tri-state window for more than tristate hold-off time, device makes PWM_HS, PWM_LS and PWM_responder all low.
HI LI with boot disable	INL	INH	Disabled	Device is transparent to the incoming PWMs on INH INL pins. If any incoming PWM is in tri-state window for more than tristate hold-off time, device makes the corresponding PWM output low.

6.3.6 Undervoltage Lockout (UVLO)

Both the high-side and the low-side driver stages as well as the controlled side supply domain VDD include UVLO protection circuitry. Protection circuitry monitors the supply voltage (VDD) and the bootstrap capacitor voltage (V_{HB} to V_{HS}, and V_{LB} to V_{LS}). The UVLO circuit inhibits the gate drive output until sufficient supply voltage is available to turn on the external FETs. The built-in UVLO hysteresis prevents chattering during supply voltage variations. When the supply voltage is applied to the VDD pin of the device, both the outputs are held low until VDD exceeds the UVLO threshold. Any UVLO condition in the bootstrap supply domain (V_{HB}–V_{HS}) or (V_{LB}–V_{LS}) disables only the corresponding gate drive output HG or LG respectively. See below for the supply function table:

Table 6-8. Supply Function

VDD	V(LB-LS)	V(HB-HS)	INH	INL	HG	LG
<VDD_UVR	x	x	x	x	Low	Low
>VDD_UVR	<LB_UVR	<HB_UVR	x	x	Low	Low
>VDD_UVR	<LB_UVR	>HB_UVR	High	x	High	Low
>VDD_UVR	<LB_UVR	>HB_UVR	Low	x	Low	Low
>VDD_UVR	>LB_UVR	<HB_UVR	x	High	Low	High
>VDD_UVR	>LB_UVR	<HB_UVR	x	Low	Low	Low
>VDD_UVR	>LB_UVR	>HB_UVR	High	Low	High	Low
>VDD_UVR	>LB_UVR	>HB_UVR	Low	High	Low	High
>VDD_UVR	>LB_UVR	>HB_UVR	Low	Low	Low	Low
>VDD_UVR	>LB_UVR	>HB_UVR	High	High	High	High

6.3.7 Level Shifter

The level shift circuit is the interface between the logic inputs in the VDD domain, which are referenced to GND, to the high-side or the low-side driver stage which are referenced to the switch nodes HS pin and LS pin respectively. The level shift allows the control of the HG/LG outputs. The device is designed to keep the delay introduced by the level shifter as low as possible to provide excellent propagation delay characteristic and delay matching between the low-side driver output and the high-side driver output. Low delay matching allows the power converter to operate with less dead time. The reduction in dead time is important in applications to achieve high power conversion efficiency. Additionally the level shifter circuit is optimized to provide excellent common mode transient immunity, particularly applicable to GaN FET based power converters where switch node rise and fall times are made fast to reduce switching losses.

6.3.8 Synchronous Bootstrap

The synchronous bootstrap path necessary to generate the high-side driver bias (HB-HS) is included in the LMG1208 driver. LB-LS remains floating and supply for this domain is generated on the PCB depending on the topology. The internal boot FET is connected between VDD and HB. With the external capacitor connected between the HB and the HS pins, the V_{HB} capacitor charge is refreshed every switching cycle when HS transitions to ground. The boot FET provides fast recovery times, low resistance, and enough voltage rating margin to allow for efficient and reliable bootstrap operation.

The boot path from VDD to HS gets enabled when all the below conditions are met:

1. VDD is in proper operating voltage range (> UVLO rising threshold).
2. LI is high.
3. HS has transitioned to close to GND potential.

Buck converter example with LMG1208 shows application schematic example buck converter with LMG1208. Since low side FET (S2) is referenced to GND, LB can be shorted to VDD and LS can be shorted to GND on PCB. Internal bootstrap is used for high-side FET S1 since source of S1 is referenced to SW node. HS of LMG1208 is shorted to SW on PCB.

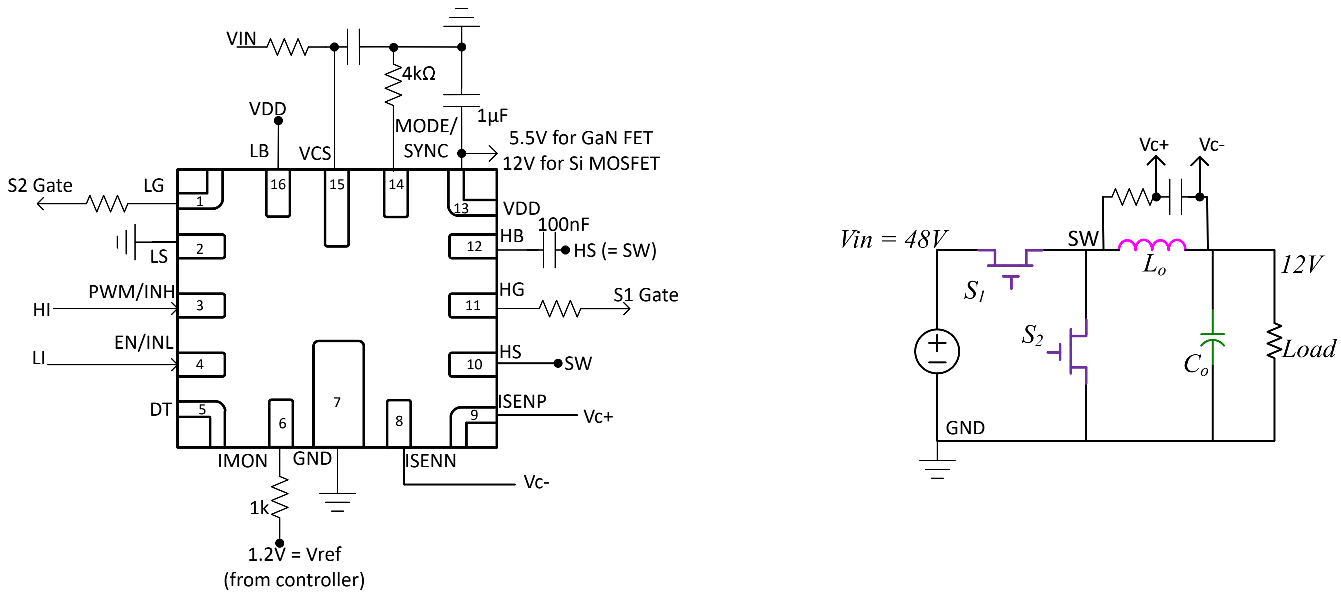


Figure 6-4. Buck converter example with LMG1208

Bootstrap Charging Path shows bootstrap charging path from VDD to HB. For buck converter, Switch is low side FET which completes the path between HS and GND. Low side FET in buck conducts current from source (GND in Figure 6-5) to drain (HS in Figure 6-5). When low side FET is ON, voltage difference across source-to-drain terminals is load Current (I_L) × Rdson, with source at higher potential than drain.

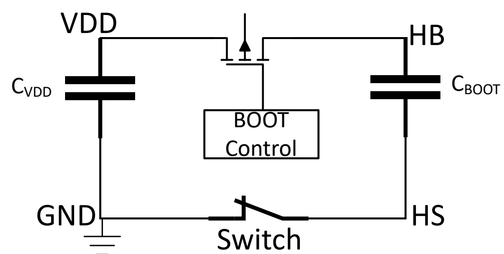


Figure 6-5. Bootstrap Charging Path

$$V(VDD - GND) - V_{DH\_BOOTFET} - V(HB - HS) + I_L \times Rdson = 0 \quad (1)$$

$$\text{Bootstrap supply voltage } V(HB - HS) = VDD - V_{DH\_BOOTFET} + I_L \times Rdson \quad (2)$$

GaN FET third quadrant drop (VSD when VGS = 0V) is usually from 1.5V to 2.5V. The LMG1208 verifies that GaN FET drive supply generated from bootstrap does not overcharge due to GaN FET third quadrant by enabling the VDD to HB boot path only when LI is high, for example, when the low side FET is ON with VGS = high.

6.3.9 Output Gate drivers

The output gate driver stages are the interface to the power MOSFETs or GaN FETs in the power train. High slew rate, low resistance, and high peak current capability of both output drivers allow for efficient switching of the external FETs. The low-side output stage is referenced from LB to LS and the high side is referenced from HB to HS. The device output stages feature a pull-up structure which delivers the highest peak source current when it is most needed: during the Miller plateau region of the power switch turn on transition. User can use external resistor between HG/LG and gate of the external FET to control the turn the slew rate of the FET on and off.

PRODUCT PREVIEW

6.3.10 Negative Voltage Transients

In most applications, the body diode of the external low-side power MOSFET clamps the HS node to ground. In some situations, board capacitance and inductance cause the HS node to transiently swing several volts below ground, before the body diode of the external low-side MOSFET clamps this swing. The HS pin in the device can swing below ground, as long as the specifications in the data sheet are not violated.

Verify that the HB to HS operating voltage is within the recommended operating conditions during DC and transient conditions. Generally, when HS swings negative, HB follows HS instantaneously and therefore the HB to HS voltage does not significantly overshoot.

Establish that HS/LS is always at a lower potential than HG/LG respectively. Pulling HG/LG more negative than specified conditions can activate parasitic transistors which can result in excessive current flow from the HB/LB supply. Excessive current flow can result in damage to the device.

Low ESR bypass capacitors from HB to HS, from VDD to GND and from LB-LS are essential for proper operation of the gate driver device. Place the capacitor very close to the device terminals to minimize series inductance. The peak currents from LG and HG can be quite large. Avoid any series inductance with the bypass capacitor for reliable operation.

Based on application board design and other operating parameters, along with HS/LS pins, other pins such as INH and INL input pins can also transiently swing below ground. To accommodate such operating conditions, the input pins of the device are capable of handling an absolute maximum of –2V. Based on the layout and other design constraints, sometimes the outputs, HG and LG, can also undergo transient voltages for short durations. Therefore, the device handles –2V transients with less than 100ns duration on the HG and LG output pins.

6.3.11 Dead Time/Delay Pin

The LMG1208 integrates a delay block to insert dead time to the incoming PWMs to make-sure no shoot-through (also called as cross-conduction) of the external FETs happens. DT terminal can be connected by a resistor to GND. Device detects the resistor and converts to an equivalent rising edge delay from 8ns to 100ns (typical) range. If dead time is managed from the PWM controller, DT pin can be floated to bypass this delay block and device is transparent to the incoming PWMs.

For single PWM mode, LMG1208 generates complementary PWM and same delay block is used to insert dead time between the rising edge of PWM_HS and falling edge of PWM_LS and vice versa. For all the other modes, rising edge of the PWM_HS, PWM_LS and PWM_responder (only applicable to HSC_HS and HSC_LS modes) is shifted by R_{DT} equivalent delay. See Figure 6-2 for the symbol names used in this section. Thus, LMG1208 DT feature is beneficial even if PWM controller is providing 2 independent PWMs with minimal or no dead time.

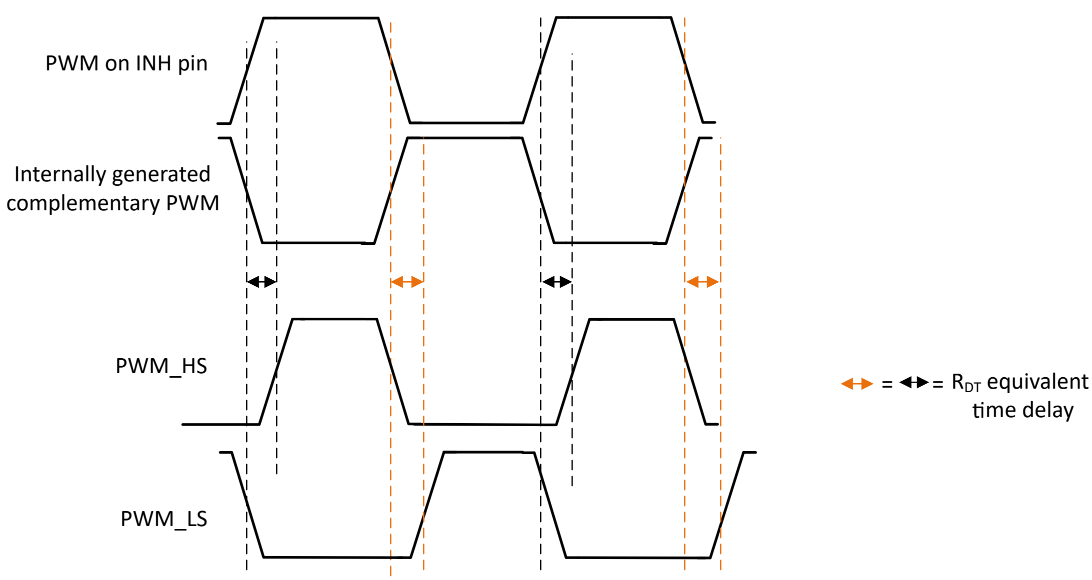


Figure 6-6. Single PWM Mode With Dead Time

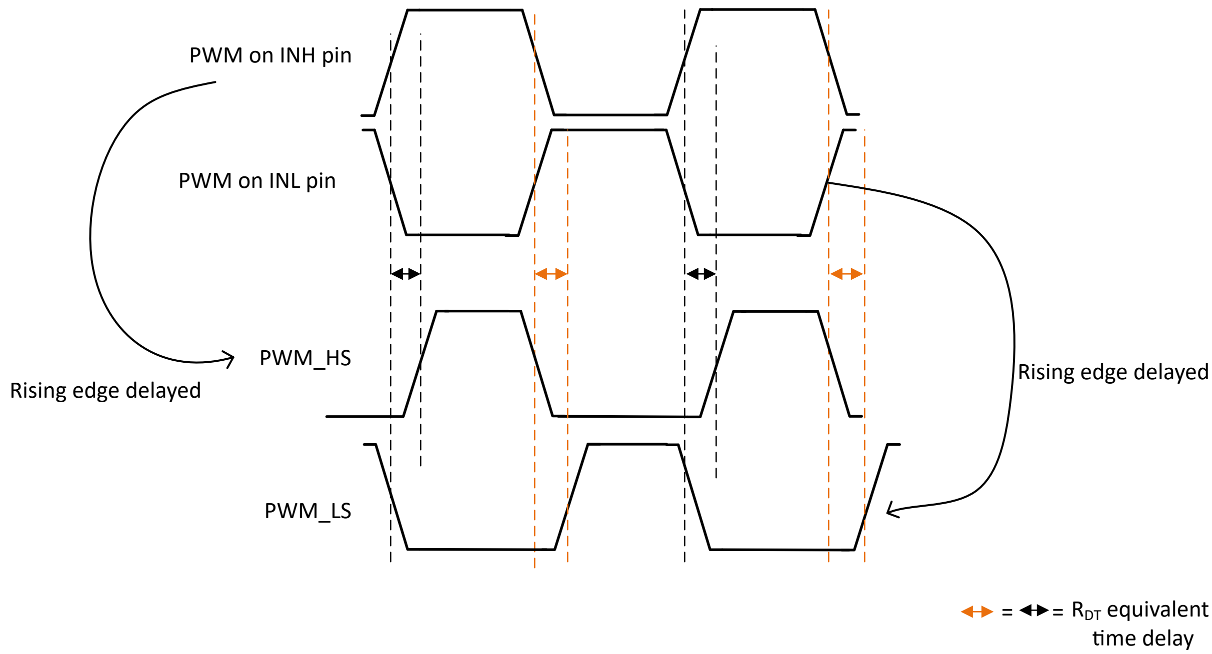


Figure 6-7. HI LI mode With Rising Edge Delay

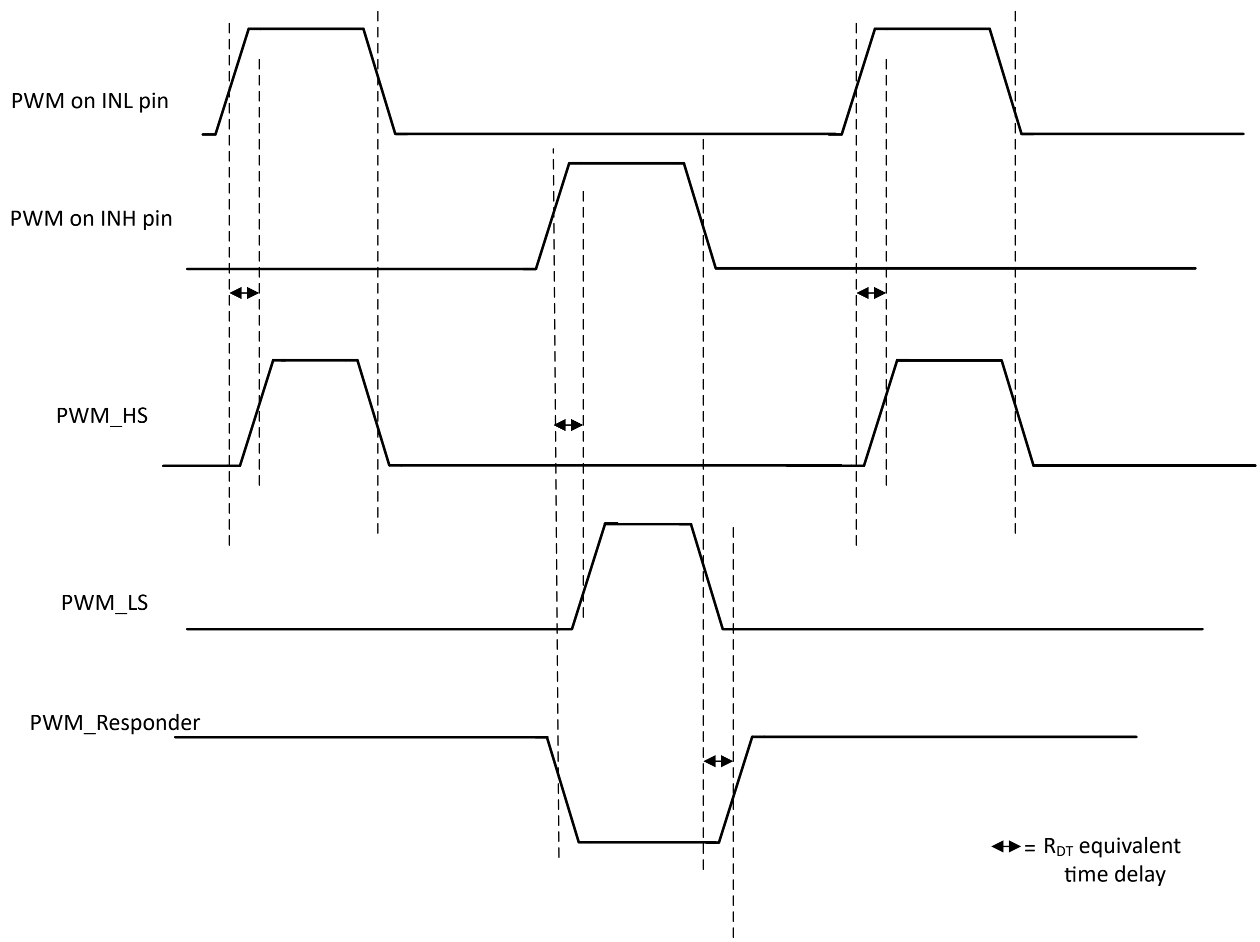


Figure 6-8. HSC_LS Mode With Rising Edge Delay

6.3.12 Current Sense Amplifier

The LMG1208 features a trans-conductance amplifier with integrated high precision current sense. ISENP and ISENN terminals take in the differential input voltage and output IMON is the current output (with internal gain of 5μA/mV). The integrated amplifier first stage is powered by high input supply voltage VCS that can be tied to VIN of the power converter. Amplifier inputs have high common mode rejection and can tolerate up to 35V of common mode. The amplifier supports inductor DCR sense and shunt resistor sense and IMON can be used for current mode control, current balancing between multiple phases and over-current protection. Main features of the integrated current sense amplifier are low offset (< 500μV), low input leakage, large input differential range (± 150mV), and high bandwidth (5Mhz) which helps to eliminate any external current sensing amplifier on the PCB- saving cost and PCB space and reducing component count. To process the output current IMON, use an external resistor R_{REF} and reference voltage V_{REF}.

For inductor DCR sense, recommended resistor and capacitor values can be calculated from below equation

$$\left(\frac{L}{R_{DCR}}\right) = R_{EXT} \times C_{EXT} \tag{3}$$

where

- L = power converter inductor value
- R_{DCR} = DC resistance from inductor data sheet

If external RC is chosen as per above equation, then voltage across capacitor is reflected by below equation:

$$I_L \times R_{DCR} = V_{C+} - V_{C-} = V_{CEXT} \tag{4}$$

where

- I_L = inductor current (includes DC and ripple component)

Voltage at output terminal IMON is governed by below equation:

$$V_{IMON} = V_{CEXT} \times Gain \times R_{REF} + V_{REF} \tag{5}$$

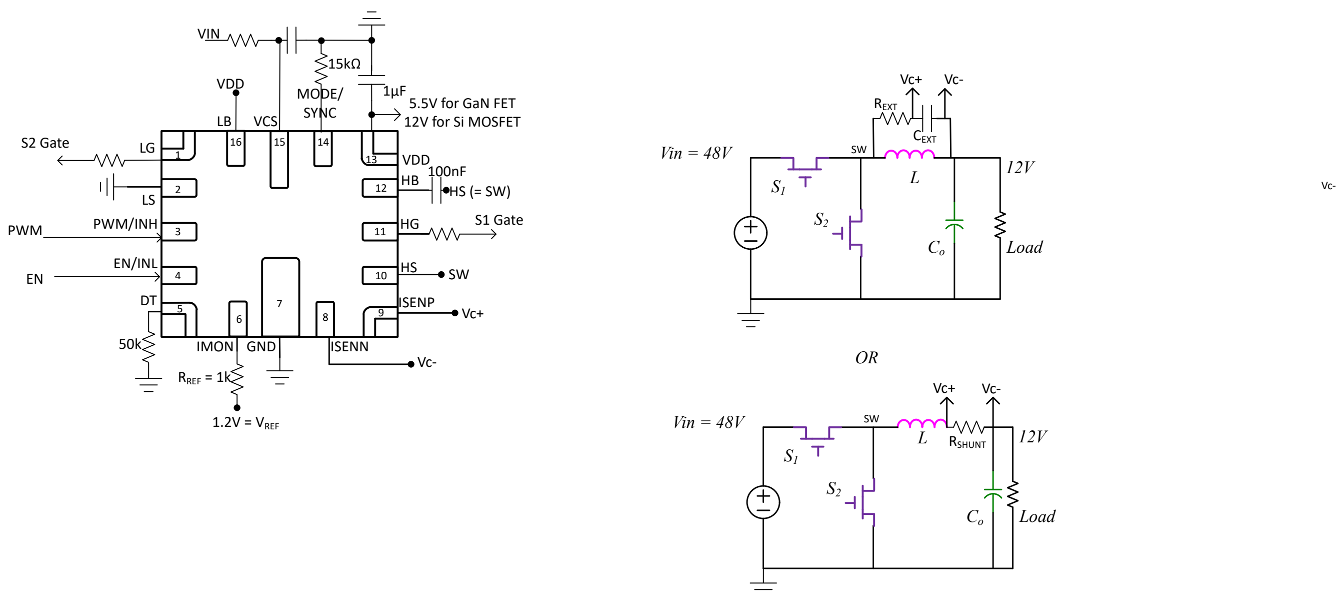


Figure 6-9. Single PWM Mode With Current Sensing

6.4 Device Functional Modes

When the device is enabled, the device operates in normal mode or UVLO mode. See Section 6.3.6 for more information on UVLO operational mode. In normal mode when the VDD, V(HB–HS) and V(LB-LS) are above UVLO threshold, the output stage is dependent on the states PWM/INH and EN/INL pins and R_{MODE} value. Single PWM mode function table is provided in Single PWM Mode With EN Function.

Table 6-9. HI LI Mode, HI LI With Boot Disable Mode Functional Table

INH	INL	HG	LG
L	L	L	L
L	H	L	H
H	L	H	L
H	H	H	H
Tri-state	H	L	H
Tri-state	L	L	L
H	Tri-state	H	L
L	Tri-state	L	L

Table 6-10. HI LI Inverted Mode Functional Table

INH	INL	HG	LG
L	L	H	H
L	H	H	L
H	L	L	H
H	H	L	L
Tri-state	H	L	L
Tri-state	L	L	H
H	Tri-state	L	L
L	Tri-state	H	L

Table 6-11. HSC_HS Mode Functional Table

INH	INL	HG	LG	SYNC
L	L	L	H	L
L	H	L	H	H
H	L	H	L	L
H	H	L	L	H
Tri-state	x	L	L	L
x	Tri-state	L	L	L

Table 6-12. HSC_LS Mode Functional Table

INH	INL	HG	LG	SYNC
L	L	L	L	H
L	H	H	L	H
H	L	L	H	L
H	H	H	L	L
Tri-state	x	L	L	L
x	Tri-state	L	L	L

PRODUCT PREVIEW

PRODUCT PREVIEW

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

To enable fast switching of power devices and reduce associated switching power losses, a powerful gate driver is used between the PWM output of controllers and the gates of the power semiconductor devices. Gate drivers are indispensable when it is impossible for the PWM controller to directly drive the gates of the switching devices. With the advent of digital power, this situation is frequently encountered because the PWM signal from the digital controller is often a 3.3V logic signal which cannot effectively turn on a power switch. Level shifting circuitry is needed to boost the 3.3V signal to the gate-drive voltage (such as 12V for silicon MOSFET) to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN/PNP bipolar transistors in totem-pole arrangement, as emitter follower configurations, prove inadequate with digital power because they lack level-shifting capability. Gate drivers effectively combine both the level-shifting and buffer-drive functions. Gate drivers also find other needs, such as minimizing the effect of high-frequency switching noise, by locating the high-current driver physically close to the power switch, and controlling floating power-device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses from the controller into the driver.

7.2 Typical Application

The LMG1208 is a versatile floating half bridge gate driver and can be used in multiple power converter topology implementation. Three examples are shown below.

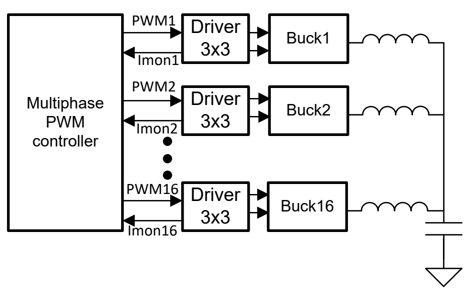


Figure 7-1. LMG1208 in 16 Phase Buck (using Single PWM Mode of LMG1208)

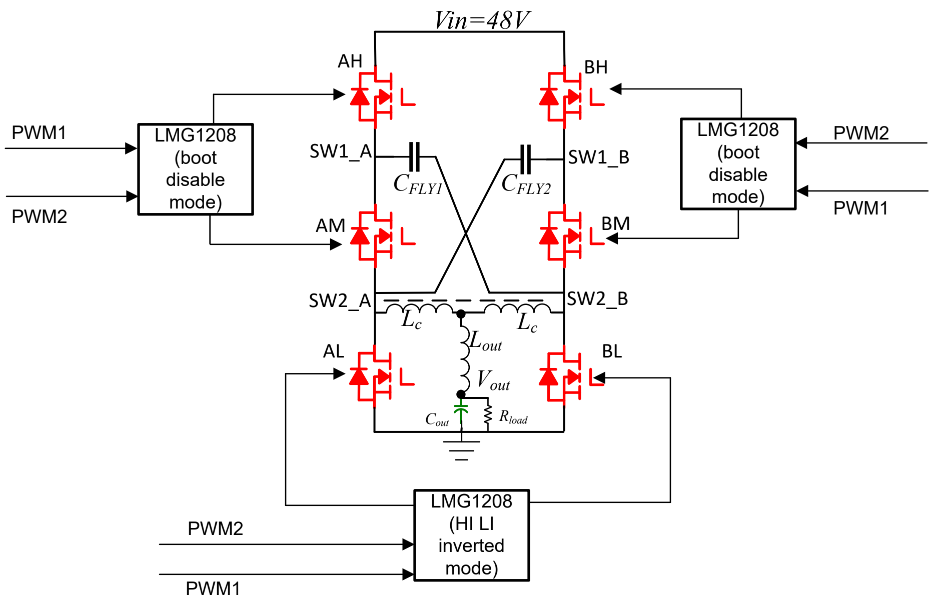


Figure 7-2. LMG1208 in Hybrid Switched Capacitor Converter (Using HI LI With Boot Disable Mode of LMG1208)

PRODUCT PREVIEW

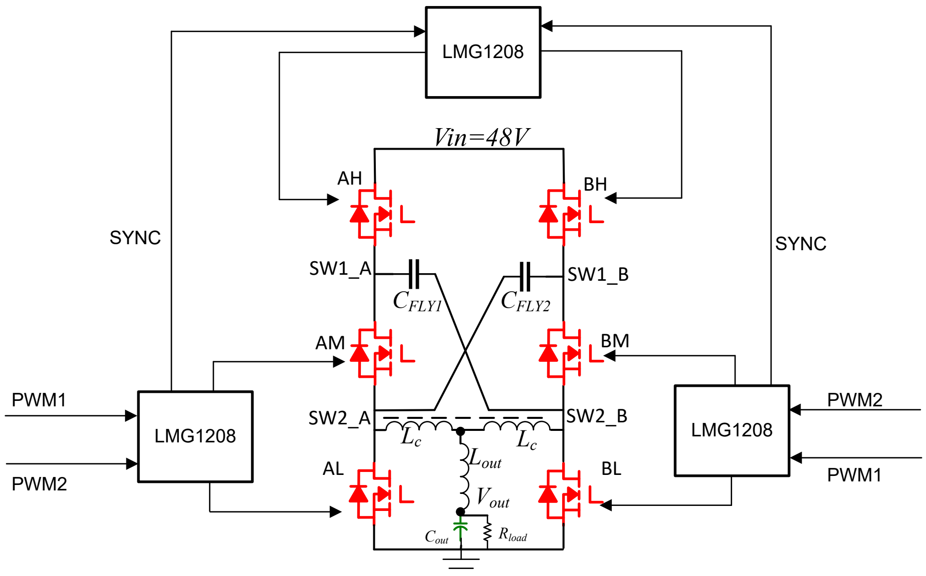


Figure 7-3. LMG1208 in Hybrid Switched Capacitor Converter (Using HSC_HS Mode of LMG1208)

Detailed application schematic of HSC_HS implementation is shown in Figure 7-4. Use three drivers (U1, U2, U3) to implement the six FET HSC topology. HSC topology comprises of two cross-coupled arms A and B with switched capacitors denoted by C_{FLY1} and C_{FLY2}. Arm A consists of tree FETs AH, AM and AL. Similarly, arm B consists of three FETs BH, BM and BL. L_C is tightly coupled inductor with 1:1 turns ratio to provide 4:1 step down of VIN. L_{OUT} regulates the V_{OUT} to 12V. U1 and U2 are in HSC_HS mode, while U3 is in HI LI with boot disable mode. Since middle and bottom FET turn-on in complementary fashion, internal bootstrap from VDD to HB is used to drive middle FET in both arms A and B. Also, AH and AM turn-on in complementary fashion, bootstrap for top FET drive (AH and BH) is generated on PCB using Schottky diodes D1 and D2, while internal boot path for U3 is kept disabled using MODE pin.

See the example of AH and AM FETs. AH FET is driven from LB-LS domain of U3 driver. When middle FET AM turns on, bootstrap path from HB1 to SW2_A gets completed via path HB1- D1 - LB - boot cap - LS - SW1_A - via AM - SW2_A - HS. Similarly for arm B, bootstrap path for top FET gets completed via path HB2- D2 - HB - boot cap - HS - SW1_B - via BM - SW2_B - HS.

Take precaution with voltage-clamping the bootstrap supplies LB-LS and HB-HS for U3 on PCB using zener in case FETs used in the topology are GaN FETs. GaN FETs have to be driven with regulated 5V. If gate-source of GaN FET crosses 6V, there are gate reliability issues which can damage the GaN FET. Third quadrant drop of GaN FET is 1.5V-2.5V, when middle FET (AM or BM) goes to third quadrant, there is a possibility to charge boot caps across LB-LS and HB-HS to higher than 6V because this discrete bootstrap path from D1 and D2 is always ON unlike using internal bootstrap built in LMG1208 which is a synchronous bootstrap FET and is controlled by the device.

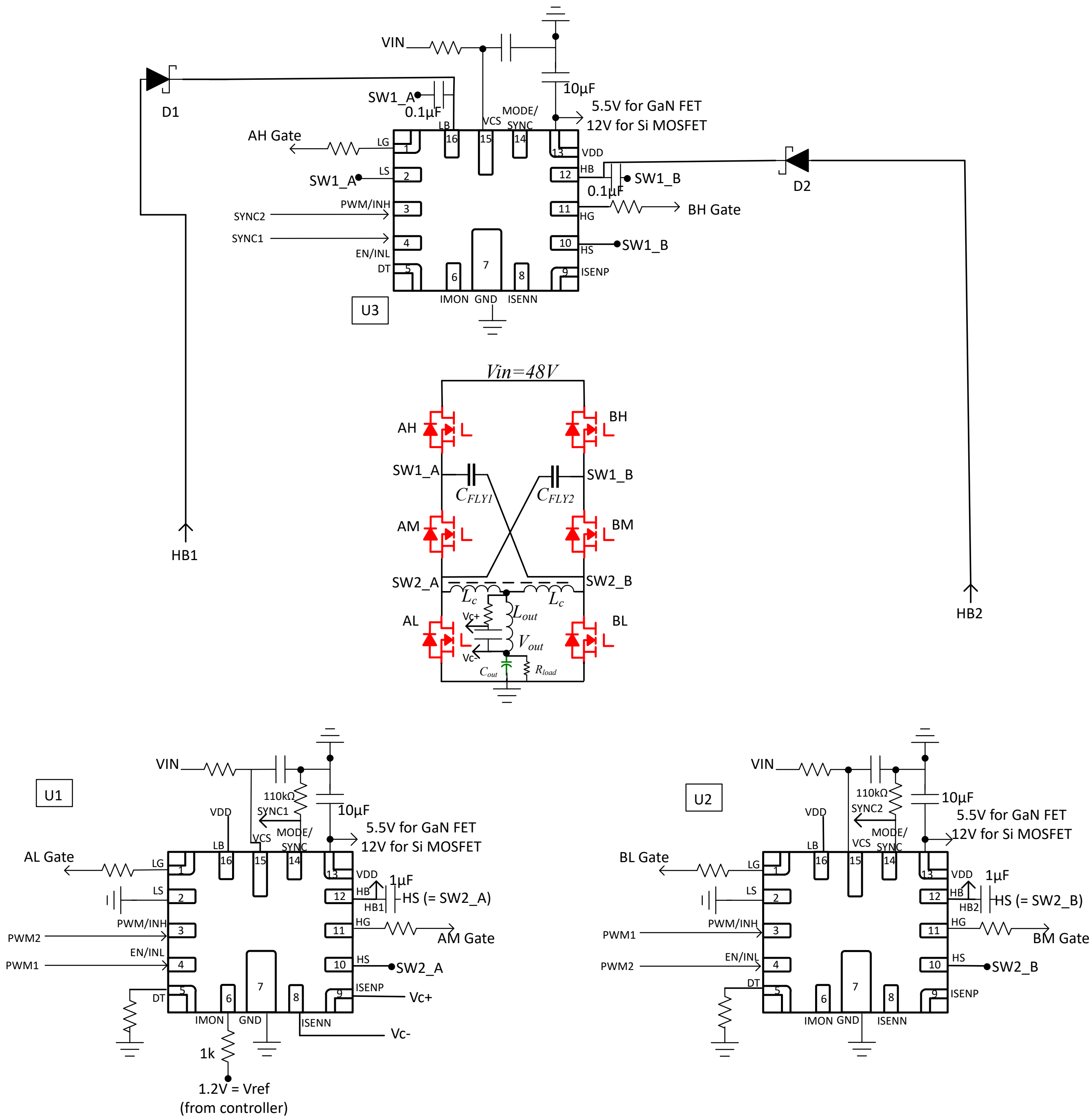


Figure 7-4. LMG1208 Typical Application Diagram in HSC_HS Configuration

Figure 7-5 shows steady state waveforms of PWM1, PWM2, and six gate drives for Vin = 60V, VOUT = 12V.

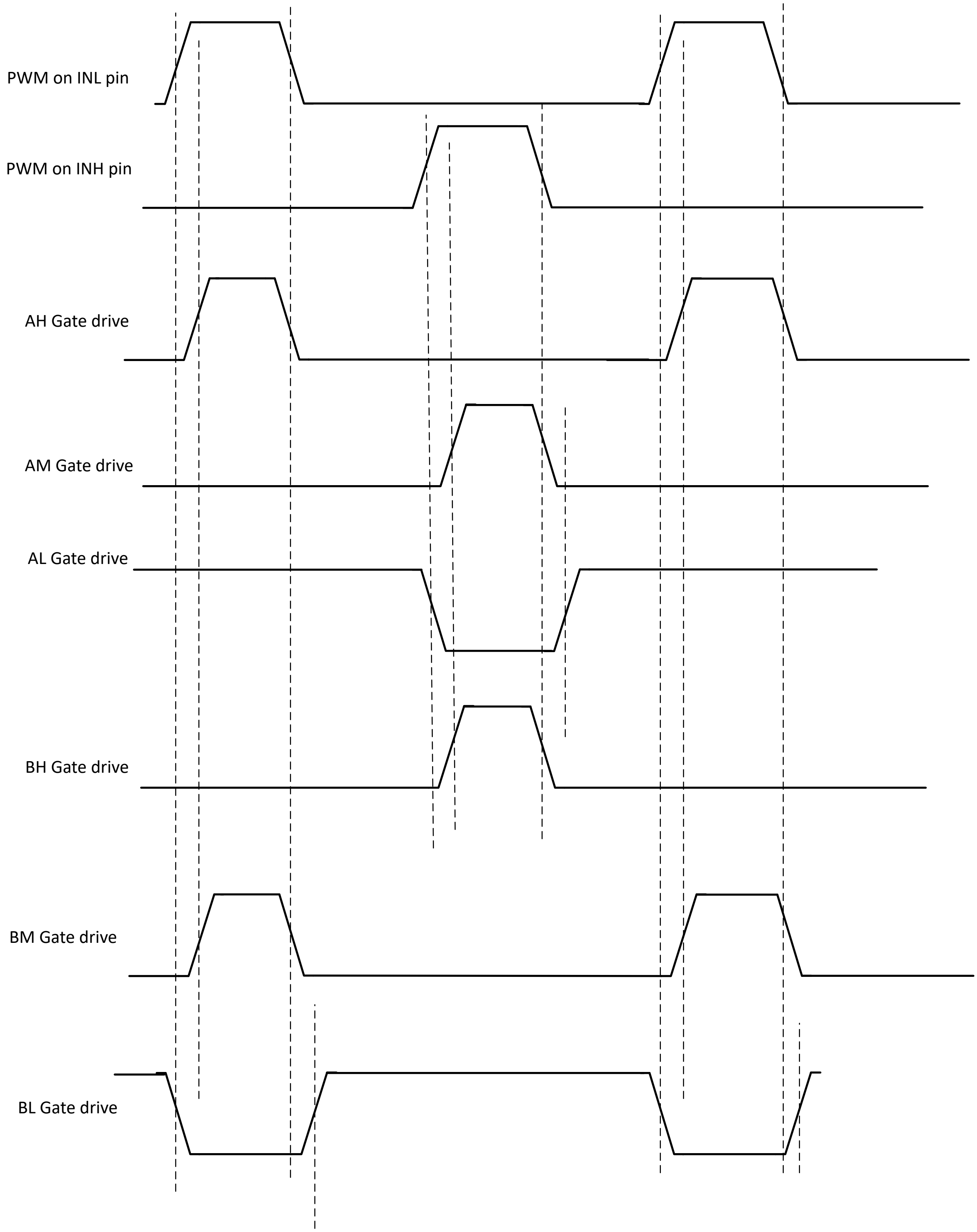


Figure 7-5. HSC Waveforms for Duty Cycle < 0.5

Figure 7-6 shows steady state waveforms of PWM1, PWM2, and six gate drives for Vin = 40V, VOUT = 12V.

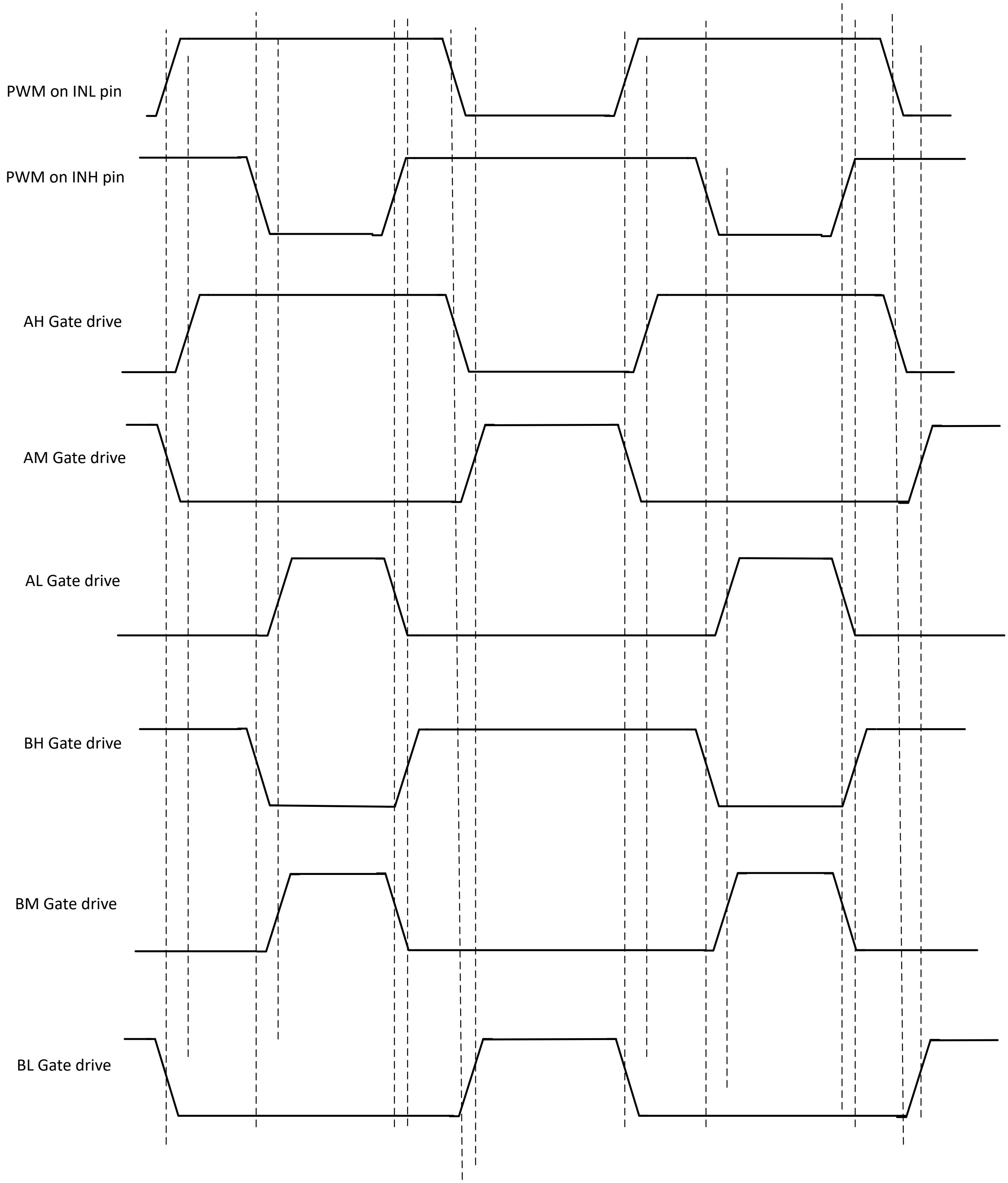


Figure 7-6. HSC Waveforms for Duty Cycle > 0.5

7.2.1 Design Requirements

For this design example, use the parameters listed in Table 7-1.

PRODUCT PREVIEW

Table 7-1. Design Specifications

DESIGN PARAMETER	EXAMPLE VALUE
Supply voltage, Silicon MOSFET usage, VDD	12V
Supply voltage, GaN FET usage, VDD	5V or 5.5V
VIN, HSC Converter main supply voltage	40V - 60V
VOUT of HSC converter	12V
IOUT of HSC converter	125A
Operating frequency	200kHz

7.2.2 Detailed Design Procedure

7.2.2.1 V_{DD} Bias Supply Voltage

Verify that the bias supply voltage applied to the VDD pin of the device does not exceed the values listed in Section 5.5. However, different power switches require different voltage levels applied at the gate terminals for effective turnon and turnoff. With a wide operating range from 4.5V to 16V, the device can be used to drive a variety of power switches, such as Si MOSFETs, and wide-bandgap power semiconductors GaN FETs.

7.2.2.2 Peak Source and Sink Currents

Verify that the switching speed of the power switch during turnon and turnoff is as fast as possible to minimize switching power losses. Confirm that the gate driver device provides the required peak current for achieving the targeted switching speeds with the targeted power FET. The system requirement for the switching speed is typically described in terms of the slew rate of the drain-to-source voltage of the power FET (such as dV_{DS}/dt). In inductive hard-switching application, reducing switching power losses is critical. When the drain-to-source voltage swing occurs, the Miller charge of the power FET (Q_{GD} parameter in the FET data sheet) is supplied by the peak current of gate driver. According to power FET inductive switching mechanism, the gate-to-source voltage of the power FET at this time is the Miller plateau voltage, which is typically slightly higher than the threshold voltage of the power MOSFET, $V_{GS(TH)}$.

To achieve the targeted dV_{DS}/dt, verify that the gate driver provides the Q_{GD} charge in T_{SW} time or less; confirm that a peak current of Q_{GD}/T_{SW} or higher is provided by the gate driver. Extra gate drive current capability provides additional flexibility to insert external gate resistors and fine tune the switching speed for efficiency versus EMI optimizations.

However, in practical designs, the parasitic trace inductance in the gate drive circuit of the PCB has a definitive role to play on the power MOSFET switching speed. The effect of the trace inductance is to limit the dI/dt of the output current pulse of the gate driver. Thus, placing the gate driver device very close to the power FET and designing a tight gate drive-loop with minimal PCB trace inductance is important to realize the full peak-current capability of the gate driver.

7.2.2.3 Power Dissipation

Power dissipation of the gate driver has various portions such as switching gate charge loss, internal bias, bootstrap conduction loss and FET gate leakage.

When no external gate resistor is employed between the driver and FET, switching power is completely dissipated inside the driver package. With the use of external gate-drive resistors, the internal resistance of driver and external gate resistor share power dissipation.

7.2.3 Application Curves: Buck Converter

A 48V-12V buck converter is made using LMG1208 and Silicon MOSFET. The operating conditions are listed below:

- Load current = 10A
- Inductor = 4.7µH

- Switching frequency = 200kHz
- DT pin used to insert dead time, R_{DT} = 100kΩ
- Inductor DCR method is used and fed to ISENP, ISENN terminals, while maintaining VCS = 48V
- IMON pin is biased through the 1kΩ resistor and 1.2V VREF as shown in application diagram.

7.3 Power Supply Recommendations

The bias supply voltage range for which the device is recommended to operate is from 4.5V to 17V. The lower end of this range is governed by the internal undervoltage-lockout (UVLO) protection feature on the V_{DD} pin supply circuit blocks. Whenever the driver is in UVLO condition when the V_{DD} pin voltage is below the V_{VDD_UVR} supply start threshold, this feature holds the outputs HG/LG low, regardless of the status of the inputs. The upper end of this range is driven by the 18V absolute maximum voltage rating of the V_{DD} pin of the device (which is a stress rating). Keeping a 2V margin to allow for transient voltage spikes, the maximum recommended voltage for the V_{DD} pin is 16V. The UVLO protection feature also involves a hysteresis function, which means that when the V_{DD} pin bias voltage has exceeded the threshold voltage and device begins to operate, and if the voltage drops, then the device continues to deliver normal functionality unless the voltage drop exceeds the hysteresis specification $V_{VDD(UV\_hys)}$. It is recommended to keep VDD between 5V to 6V for GaN FET usage, and between 8V-15V for Silicon MOSFET usage. Device has internal threshold $V_{DDFET\_THR/F}$ below which device internal rail (on which input buffer INH/INL and output buffer SYNC) is shorted to VDD, and beyond which internal rail is shorted to internally generated supply 5V (typical).

The quiescent current consumed by the internal circuit blocks of the device is supplied through the VDD-GND, HB-HS and LB-LS supplies. Ensure that a local bypass capacitor is provided between the V_{DD} and GND pins, between HB-HS and LB-LS pins and located as close to the device as possible for the purpose of decoupling. A low-ESR, ceramic surface-mount capacitor is required. TI recommends using a capacitor in the range 0.1µF to 10µF for the 3 supplies- value depending on exact power converter topology.

7.4 Layout

7.4.1 Layout Guidelines

To improve the switching characteristics and efficiency of a design, follow the layout rules.

- Position the driver as close as possible to the power FETs.
- Position the V_{DD} – V_{GND}, V_{HB} − V_{HS} and V_{LB} − V_{LS} (bootstrap) capacitors as close as possible to the device.
- Pay close attention to the HS and LS traces. These trace from the driver go directly to the source of the power FET, but must not be in the high current path of the FET drain or source current.
- For systems using multiple LMG1208 devices, TI recommends locating the dedicated decoupling capacitors at VDD, HB-HS and LB-LS pins for each device.
- Take care to avoid placing VDD traces close to LG, HS, LS and HG signals.
- Use wide traces for LG and HG closely following the associated LS or HS traces.
- Use as least two or more vias if the driver outputs or SW node is routed from one layer to another. For GND, the number of vias must be a consideration of the thermal pad requirements, as well as parasitic inductance.
- Avoid INL and INH (driver input) going close to the HS/LS nodes or any other high dV/dT traces that can induce significant noise into the relatively high impedance leads.

A poor layout can cause a significant drop in efficiency or system malfunction and can lead to decreased reliability of the whole system.

PRODUCT PREVIEW

8 Device and Documentation Support

8.1 Device Support

8.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

8.2 Documentation Support

8.2.1 Related Documentation

- Texas Instruments, *PowerPAD™ Made Easy* application note
- Texas Instruments, *PowerPAD™ Thermally Enhanced Package* application note

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

PowerPAD™ and TI E2E™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
March 2026	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PRODUCT PREVIEW

PRODUCT PREVIEW

10.1 Package Option Addendum

Packaging Information

Orderable Device	Status(1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan(2)	Lead/Ball Finish(6)	MSL Peak Temp(3)	Op Temp (°C)	Device Marking(4) (5)
LMG1208-1VEGR	PREVIEW	WQFN	VEG	16					–40 to 150°C	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

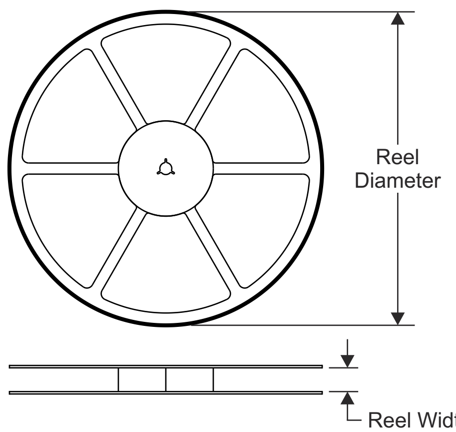
(5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

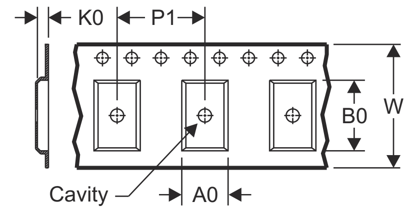
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

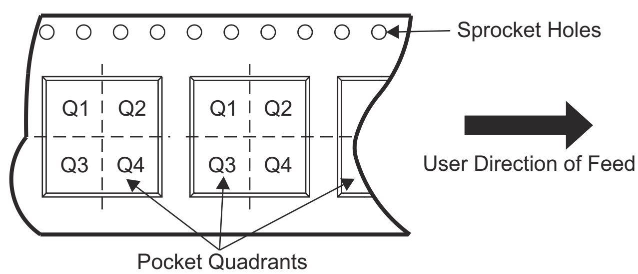
10.2 Tape and Reel Information





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

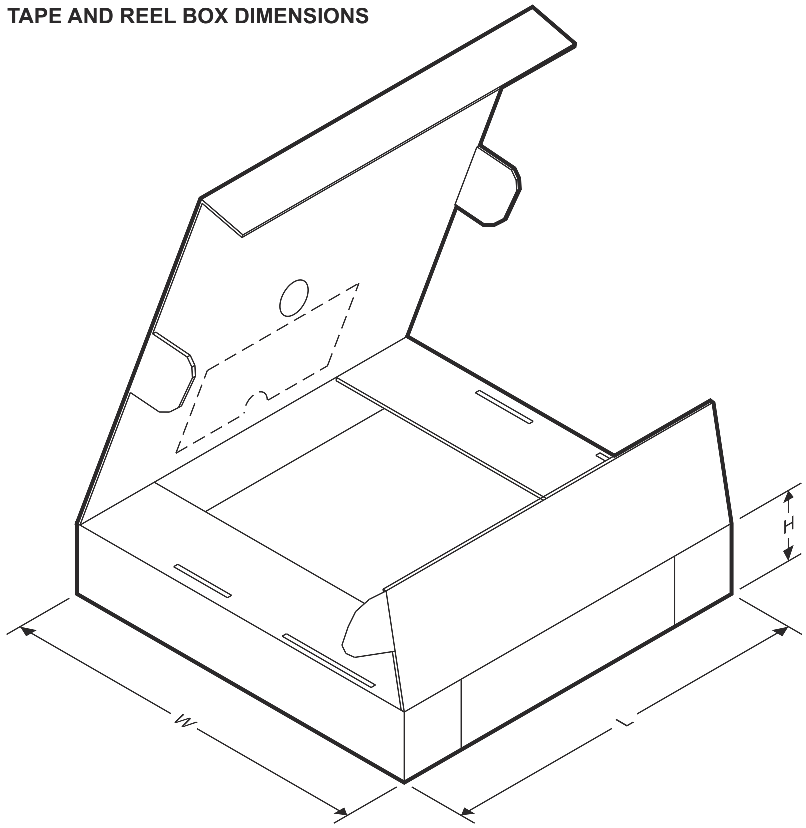
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMG1208-1VEGR	WQFN	VEG	16									

PRODUCT PREVIEW

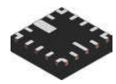
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMG1208-1VEGR	WQFN	VEG	16				

10.3 Mechanical Data

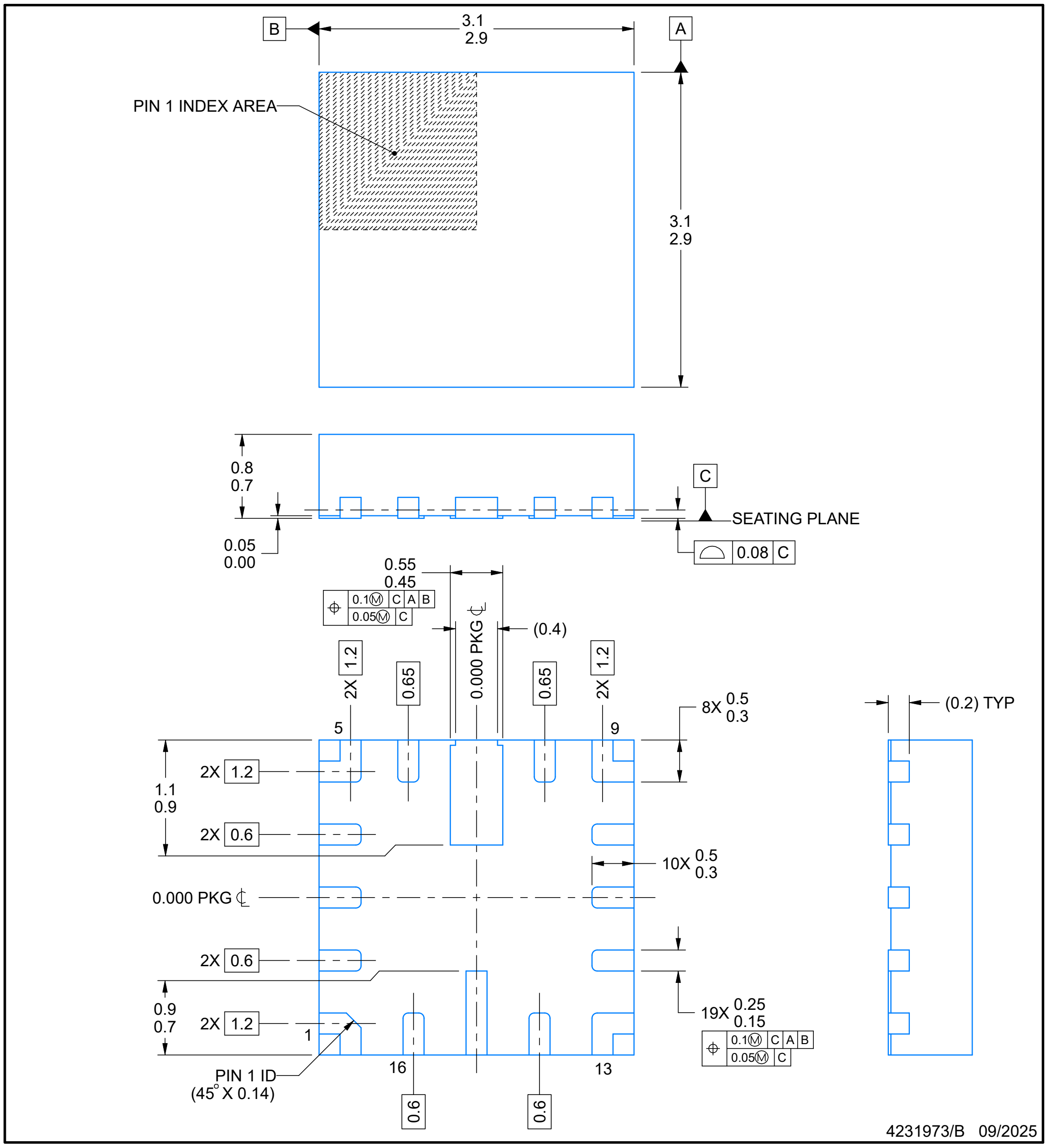
PACKAGE OUTLINE



VEG0016A

WQFN-HR - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

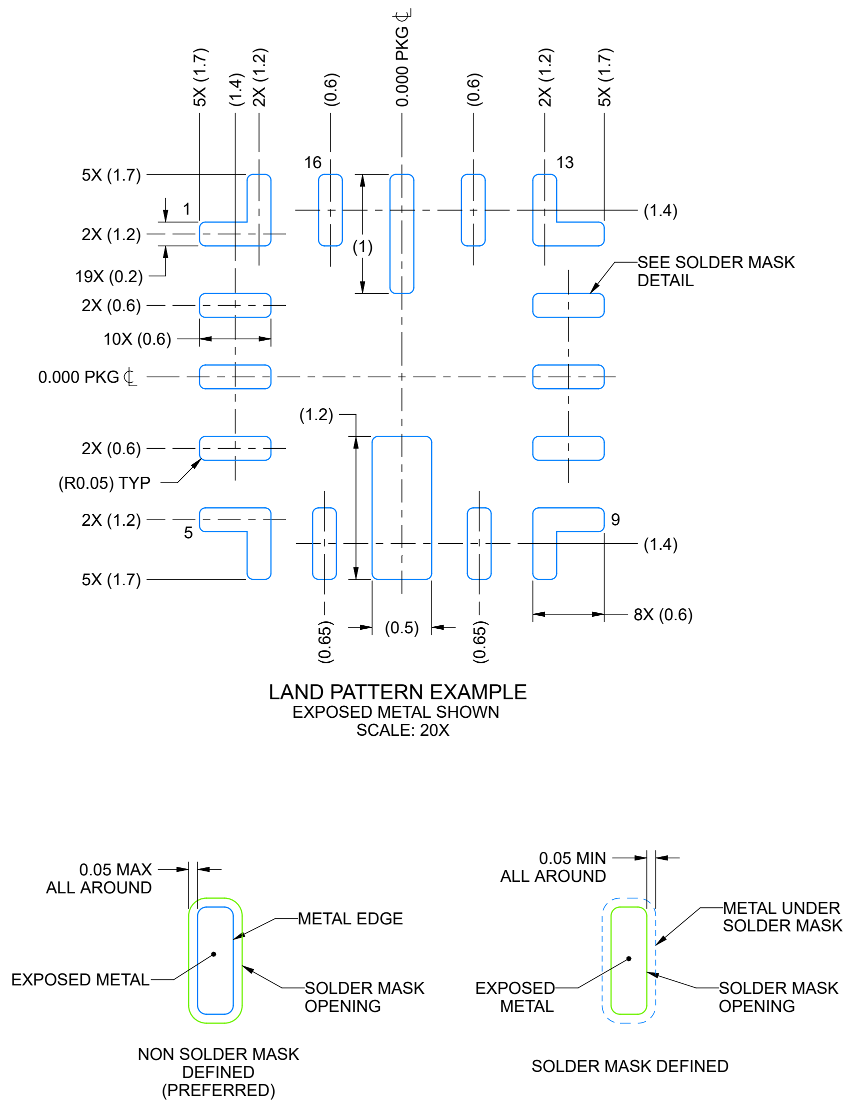
PRODUCT PREVIEW

EXAMPLE BOARD LAYOUT

VEG0016A

WQFN-HR - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

SOLDER MASK DETAILS

4231973/B 09/2025

NOTES: (continued)

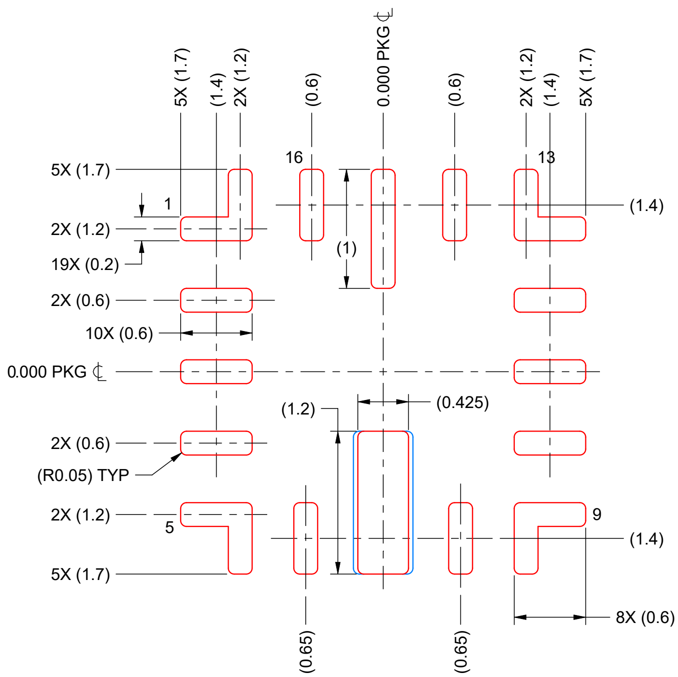
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

VEG0016A

WQFN-HR - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PAD 7: 85%

4231973/B 09/2025

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

www.ti.com

PRODUCT PREVIEW