

# LP5866 6 × 18 LED Matrix Driver with 8-Bit Analog and 8-/16-Bit PWM Dimming

## 1 Features

- LED matrix topology:
  - 18 constant current sinks with 6 scan switches for 108 LED dots
  - Configurable for 1 to 6 scan switches
- Operating voltage range:
  - $V_{CC}/V_{LED}$  range: 2.7V to 5.5V
  - Logic pins compatible with 1.8V, 3.3V, and 5V
- 18 constant current sinks with high precision:
  - 0.1mA – 50mA per current sink when  $V_{CC} \geq 3.3V$
  - Device-to-device error:  $\pm 3\%$  when channel current = 50mA
  - Channel-to-channel error:  $\pm 3\%$  when channel current = 50mA
  - Phase-shift for balanced transient power
- Ultra-low power consumption:
  - Shutdown mode:  $I_{CC} \leq 1\mu A$  when EN = Low
  - Standby mode:  $I_{CC} \leq 10\mu A$  (15 $\mu A$  for LP5866MDBT) when EN = High and CHIP\_EN = 0 (data retained)
  - Active mode:  $I_{CC} = 4.3mA$  (typ.) when channel current = 5mA
- Flexible dimming options:
  - Individual ON, OFF control for each LED dot
  - Analog dimming (current gain control)
    - Global 3-bit Maximum Current (MC) setting for all LED dots
    - 3 groups of 7-bit Color Current (CC) setting for red, green, and blue
    - Individual 8-bit Dot Current (DC) setting for each LED dot
  - PWM dimming with audible-noise-free frequency
    - Global 8-bit PWM dimming for all LED dots
    - 3 programmable groups of 8-bit PWM dimming for LED dot arbitrary mapping
    - Individual 8-bit or 16-bit PWM dimming for each LED dot
- Full addressable SRAM to minimize data traffic
- Individual LED dot open and short detection
- Deghosting and low brightness compensation
- Interface options:
  - 1MHz (max.) I<sup>2</sup>C interface when IFS = Low
  - 12MHz (max.) SPI interface when IFS = High

## 2 Applications

- LED animation and indication for:
  - Keyboard, mouse, and gaming accessories
  - Major and smart home appliances

- Smart speaker, wired and wireless speaker
- Audio mixer, DJ equipment, and broadcast
- Access equipment, switches, and servers
- Constant current sinks for optical module

## 3 Description

Electronic devices are becoming smarter, requiring to use larger quantity of LEDs for animation and indication purpose. A high-performance LED matrix driver is required to improve user experience with small solution size.

The **LP586x devices** are a family of high performance LED matrix drivers. The device integrates 18 constant current sinks with N (N = 1/2/4/6/8/11) switching MOSFETs to support N × 18 LED dots or N × 6 RGB LEDs. The LP5866 integrates 6 MOSFETs for up to 108 LED dots or 36 RGB LEDs.

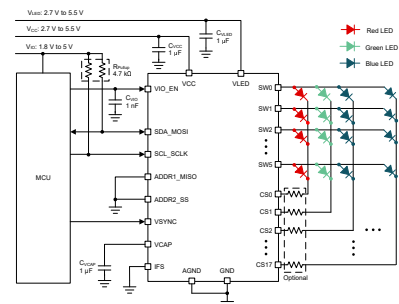
The LP5866 supports both analog dimming and PWM dimming methods. For analog dimming, each LED dot can be adjusted with 256 steps. For PWM dimming, the integrated 8-bit or 16-bit configurable PWM generators enable smooth and audible-noise-free dimming control. Each LED dot can also be arbitrarily mapped into 8-bit group PWM to achieve dimming control together.

The LP5866 device implements full addressable SRAM to minimize the data traffic. The ghost-cancellation circuitry is integrated to eliminate both upside and downside ghosting. The LP5866 also supports LED open and short detection functions. Both 1MHz (maximum) I<sup>2</sup>C and 12MHz (maximum) SPI are available in LP5866.

### Device Information

PART NUMBER	PACKAGE <sup>(1)</sup>	BODY SIZE (NOM)
LP5866	VQFN (40)	5.00mm × 5.00mm
	TSSOP (38)	9.70mm × 4.40mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.



**Simplified Schematic**



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## 4 Device Comparison

PART NUMBER	MATERIAL	LED DOT NUMBER	PACKAGE <sup>(2)</sup>	SOFTWARE COMPATIBLE
LP5861	LP5861RSMR	18 × 1 = 18	VQFN-32	Yes
LP5862	LP5862RSMR	18 × 2 = 36	VQFN-32	
	LP5862DBTR		TSSOP-38	
LP5864	LP5864RSMR	18 × 4 = 72	VQFN-32	
	LP5864MRSMR <sup>(1)</sup>			
LP5866	LP5866RKPR	18 × 6 = 108	VQFN-40	
	LP5866DBTR		TSSOP-38	
	LP5866MDBTR <sup>(1)</sup>			
LP5868	LP5868RKPR	18 × 8 = 144	VQFN-40	
LP5860	LP5860RKPR	18 × 11 = 198	VQFN-40	
	LP5860MRKPR <sup>(1)</sup>			

- (1) Extended temperature devices, supporting –55°C to approximately 125°C operating ambient temperature.  
(2) The same packages are hardware compatible.

## 5 Pin Configuration and Functions

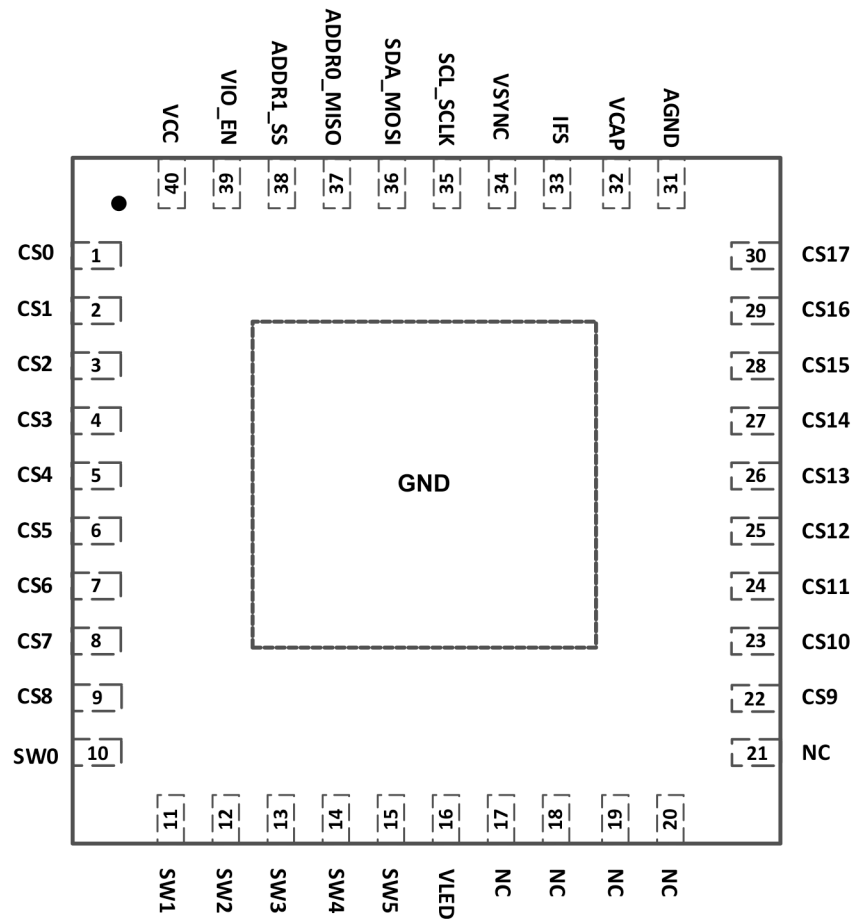
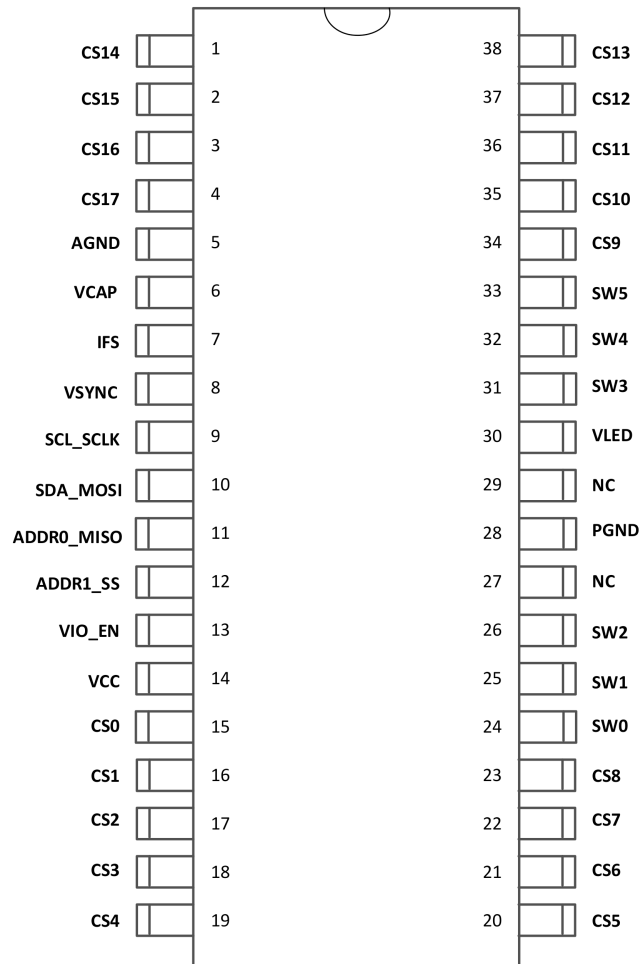


Figure 5-1. LP5866 RKP Package 40-Pin VQFN With Exposed Thermal Pad Top View



**Figure 5-2. LP5866 DBT Package 38-Pin TSSOP Top View**

**Table 5-1. Pin Functions**

PIN			I/O	DESCRIPTION
NAME	VQFN NO.	TSSOP NO.		
CS0	1	15	O	Current sink 0. If not used, this pin must be left floating.
CS1	2	16	O	Current sink 1. If not used, this pin must be left floating.
CS2	3	17	O	Current sink 2. If not used, this pin must be left floating.
CS3	4	18	O	Current sink 3. If not used, this pin must be left floating.
CS4	5	19	O	Current sink 4. If not used, this pin must be left floating.
CS5	6	20	O	Current sink 5. If not used, this pin must be left floating.
CS6	7	21	O	Current sink 6. If not used, this pin must be left floating.
CS7	8	22	O	Current sink 7. If not used, this pin must be left floating.
CS8	9	23	O	Current sink 8. If not used, this pin must be left floating.
SW0	10	24	O	High-side PMOS switch output for scan line 0. If not used, this pin must be left floating.
SW1	11	25	O	High-side PMOS switch output for scan line 1. If not used, this pin must be left floating.
SW2	12	26	O	High-side PMOS switch output for scan line 2. If not used, this pin must be left floating.
SW3	13	31	O	High-side PMOS switch output for scan line 3. If not used, this pin must be left floating.
SW4	14	32	O	High-side PMOS switch output for scan line 4. If not used, this pin must be left floating.
SW5	15	33	O	High-side PMOS switch output for scan line 5. If not used, this pin must be left floating.

**Table 5-1. Pin Functions (continued)**

PIN			I/O	DESCRIPTION
NAME	VQFN NO.	TSSOP NO.		
VLED	16	30	Power	Power input for high-side switches
NC	17, 18, 19, 20, 21	27, 29	–	No internal connection
CS9	22	34	O	Current sink 9. If not used, this pin must be left floating.
CS10	23	35	O	Current sink 10. If not used, this pin must be left floating.
CS11	24	36	O	Current sink 11. If not used, this pin must be left floating.
CS12	25	37	O	Current sink 12. If not used, this pin must be left floating.
CS13	26	38	O	Current sink 13. If not used, this pin must be left floating.
CS14	27	1	O	Current sink 14. If not used, this pin must be left floating.
CS15	28	2	O	Current sink 15. If not used, this pin must be left floating.
CS16	29	3	O	Current sink 16. If not used, this pin must be left floating.
CS17	30	4	O	Current sink 17. If not used, this pin must be left floating.
AGND	31	5	Ground	Analog ground. Must be connected to exposed thermal pad and common ground plane.
VCAP	32	6	O	Internal LDO output. A 1- $\mu$ F capacitor must be connected between this pin with GND. Place the capacitor as close to the device as possible.
IFS	33	7	I	Interface type select. I <sup>2</sup> C is selected when IFS is low. SPI is selected when IFS is high. A resistor must be connected between VIO and this pin.
VSYNC	34	8	I	External synchronize signal for display mode 2 and mode 3
SCL_SCLK	35	9	I	I <sup>2</sup> C clock input or SPI clock input. Pull up to VIO when configured as I <sup>2</sup> C.
SDA_MOSI	36	10	I/O	I <sup>2</sup> C data input or SPI leader output follower input. Pull up to VIO when configured as I <sup>2</sup> C.
ADDR0_MISO	37	11	I/O	I <sup>2</sup> C address select 0 or SPI leader input follower output
ADDR1_SS	38	12	I	I <sup>2</sup> C address select 1 or SPI follower select
VIO_EN	39	13	Power,I	Power supply for digital circuits and chip enable. A 1-nF capacitor must be connected between this pin with GND and be placed as close to the device as possible.
VCC	40	14	Power	Power supply for device. A 1- $\mu$ F capacitor must be connected between this pin with GND and be placed as close to the device as possible.
GND	Exposed Thermal Pad	/	Ground	Must be connected to AGND and common ground plane

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Voltage on V <sub>CC</sub> / V <sub>LED</sub> / V <sub>IO</sub> / EN / CS / SW / SDA / SCL / SCLK / MOSI / MISO / SS / ADDR0 / ADDR1 / VSYNC / IFS		-0.3	6	V
Voltage on VCAP		-0.3	2	V
T <sub>J</sub>	Junction temperature	-55	150	°C
T <sub>stg</sub>	Storage temperature	-65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins <sup>(1)</sup>	±3000	V
		Charged device model (CDM), per ANSI/ESDA/ JEDEC JS-002, all pins <sup>(2)</sup>	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input voltage on V <sub>CC</sub>	Supply voltage	2.7		5.5	V
Input voltage on V <sub>LED</sub>	LED supply voltage	2.7		5.5	V
Input voltage on V <sub>IO_EN</sub>		1.65		5.5	V
Voltage on SDA / SCL / SCLK / MOSI / MISO / SS / ADDR <sub>x</sub> / VSYNC / IFS				V <sub>IO</sub>	V
T <sub>A</sub>	Operating ambient temperature	-40		85	°C
T <sub>A</sub>	Operating ambient temperature, LP5866MDBT	-55		125	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		LP5866, LP5866M		UNIT
		RKP (VQFN)	DBT (TSSOP)	
		40 Pins	38 Pins	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	31.4	67.0	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	22.9	20.1	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	12.0	27.4	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.3	1.0	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	12.0	27.0	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	3.5	n/a	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

$V_{CC} = 3.3\text{ V}$ ,  $V_{LED} = 3.8\text{ V}$ ,  $V_{IO} = 1.8\text{ V}$  and  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$  ( $T_A = -55\text{ }^\circ\text{C}$  to  $+125\text{ }^\circ\text{C}$  for LP5866MDBT); Typical values are at  $T_A = 25\text{ }^\circ\text{C}$  (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Power supplies</b>						
$V_{CC}$	Device supply voltage		2.7		5.5	V
$V_{UVR}$	Undervoltage restart	$V_{CC}$ rising, Test mode			2.5	V
$V_{UVF}$	Undervoltage shutdown	$V_{CC}$ falling, Test mode	1.9			V
$V_{UV\_HYS}$	Undervoltage shutdown hysteresis			0.3		V
$V_{CAP}$	Internal LDO output	$V_{CC} = 2.7\text{ V}$ to $5.5\text{ V}$		1.78		V
$I_{CC}$	Shutdown supply current $I_{SHUTDOWN}$	$V_{EN} = 0\text{ V}$ , $CHIP\_EN = 0$ (bit), measure the total current from $V_{CC}$ and $V_{LED}$		0.1	1	$\mu\text{A}$
	Standby supply current $I_{STANDBY}$	$V_{EN} = 3.3\text{ V}$ , $CHIP\_EN = 0$ (bit), measure the total current from $V_{CC}$ and $V_{LED}$		5.5	10	$\mu\text{A}$
		$V_{EN} = 3.3\text{ V}$ , $CHIP\_EN = 0$ (bit), measure the total current from $V_{CC}$ and $V_{LED}$ , LP5866MDBT			5.5	15
	Active mode supply current $I_{NORMAL}$	$V_{EN} = 3.3\text{ V}$ , $CHIP\_EN = 1$ (bit), all channels $I_{OUT} = 5\text{ mA}$ ( $MC = 1$ , $CC = 127$ , $DC = 256$ ), measure the current from $V_{CC}$		4.3	6	$\text{mA}$
$V_{LED}$	LED supply voltage		2.7		5.5	V
$V_{VIO}$	VIO supply voltage		1.65		5.5	V
$I_{VIO}$	VIO supply current	Interface idle			5	$\mu\text{A}$
<b>Output Stages</b>						
$I_{CS}$	Constant current sink output range (CS0 – CS17)	$2.7 \leq V_{CC} < 3.3\text{ V}$ , PWM = 100%	0.1		40	$\text{mA}$
		$V_{CC} \geq 3.3\text{ V}$ PWM = 100%	0.1		50	$\text{mA}$
$I_{LKG}$	Leakage current (CS0 – CS17)	channels off, up_degghost = 0, $V_{CS} = 5\text{ V}$		0.1	1	$\mu\text{A}$
$I_{ERR\_DD}$	Device to device current error, $I_{ERR\_DD} = (I_{AVE} - I_{SET}) / I_{SET} \times 100\%$	All channels ON. Current set to 0.1 mA. $MC = 0$ $CC = 42$ $DC = 25$ PWM = 100%	-7		7	%
		All channels ON. Current set to 1 mA. $MC = 2$ $CC = 127$ $DC = 25$ PWM = 100%	-5		5	%
		All channels ON. Current set to 10 mA. $MC = 2$ $CC = 127$ $DC = 255$ PWM = 100%	-3.5		3.5	%
		All channels ON. Current set to 25 mA. $MC = 7$ $CC = 64$ $DC = 255$ PWM = 100%	-3.5		3.5	%
		All channels ON. Current set to 50 mA. $MC = 7$ $CC = 127$ $DC = 255$ PWM = 100%	-3		3	%
$I_{ERR\_CC}$	Channel to channel current error, $I_{ERR\_CC} = (I_{OUTX} - I_{AVE}) / I_{AVE} \times 100\%$	All channels ON. Current set to 0.1 mA. $MC = 0$ $CC = 42$ $DC = 25$ PWM = 100%	-5.5		5.5	%
		All channels ON. Current set to 1 mA. $MC = 2$ $CC = 127$ $DC = 25$ PWM = 100%	-5		5	%
		All channels ON. Current set to 10 mA. $MC = 2$ $CC = 127$ $DC = 255$ PWM = 100%	-4		4	%
		All channels ON. Current set to 25 mA. $MC = 7$ $CC = 64$ $DC = 255$ PWM = 100%	-3.5		3.5	%
		All channels ON. Current set to 50 mA. $MC = 7$ $CC = 127$ $DC = 255$ PWM = 100%	-3		3	%
$f_{PWM}$	LED PWM frequency	PWM_Fre = 1, PWM = 100%		62.5		KHz
		PWM_Fre = 0, PWM = 100%		125		KHz



## 6.5 Electrical Characteristics (continued)

$V_{CC} = 3.3\text{ V}$ ,  $V_{LED} = 3.8\text{ V}$ ,  $V_{IO} = 1.8\text{ V}$  and  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$  ( $T_A = -55\text{ }^\circ\text{C}$  to  $+125\text{ }^\circ\text{C}$  for LP5866MDBT); Typical values are at  $T_A = 25\text{ }^\circ\text{C}$  (unless otherwise specified)

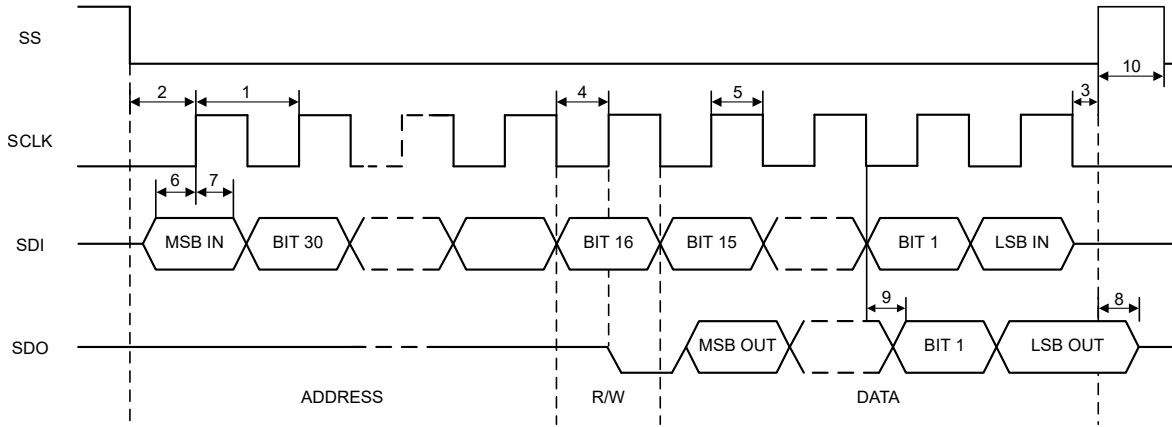
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{SAT}$	Output saturation voltage	$I_{OUT} = 50\text{ mA}$ , decreasing output voltage, when the LED current has dropped 5%			0.45	V
		$I_{OUT} = 30\text{ mA}$ , decreasing output voltage, when the LED current has dropped 5%			0.4	V
		$I_{OUT} = 10\text{ mA}$ , decreasing output voltage, when the LED current has dropped 5%			0.35	V
$R_{SW}$	High-side PMOS ON resistance	$V_{LED} = 2.7\text{ V}$ , $I_{SW} = 200\text{ mA}$		450		m $\Omega$
		$V_{LED} = 3.8\text{ V}$ , $I_{SW} = 200\text{ mA}$		380		m $\Omega$
		$V_{LED} = 5\text{ V}$ , $I_{SW} = 200\text{ mA}$		310		m $\Omega$
<b>Logic Interfaces</b>						
$V_{LOGIC\_IL}$	Low-level input voltage, SDA, SCL, SCLK, MOSI, SS, ADDR <sub>x</sub> , VSYNC, IFS			$0.3 \times V_{IO}$		V
$V_{LOGIC\_IH}$	High-level input voltage, SDA, SCL, SCLK, MOSI, SS, ADDR <sub>x</sub> , VSYNC, IFS		$0.7 \times V_{IO}$			V
$V_{EN\_IL}$	Low-level input voltage of EN			0.4		V
$V_{EN\_IH}$	High-level input voltage of EN	When $V_{CAP}$ powered up	1.4			V
$I_{LOGIC\_I}$	Input current, SDA, SCL, SCLK, MOSI, SS, ADDR <sub>x</sub>		-1		1	$\mu\text{A}$
$V_{LOGIC\_OL}$	Low-level output voltage, SDA, MISO	$I_{PULLUP} = 3\text{ mA}$			0.4	V
$V_{LOGIC\_OH}$	High-level output voltage, MISO	$I_{PULLUP} = -3\text{ mA}$	$0.7 \times V_{IO}$			V
<b>Protection Circuits</b>						
$V_{LOD\_TH}$	Thershold for channel open detection			0.25		V
$V_{LSD\_TH}$	Thershold for channel short detection			$V_{LED} - 1$		V
$T_{TSD}$	Thermal-shutdown junction temperature			150		$^\circ\text{C}$
$T_{HYS}$	Thermal shutdown temperature hysteresis			15		$^\circ\text{C}$

## 6.6 Timing Requirements

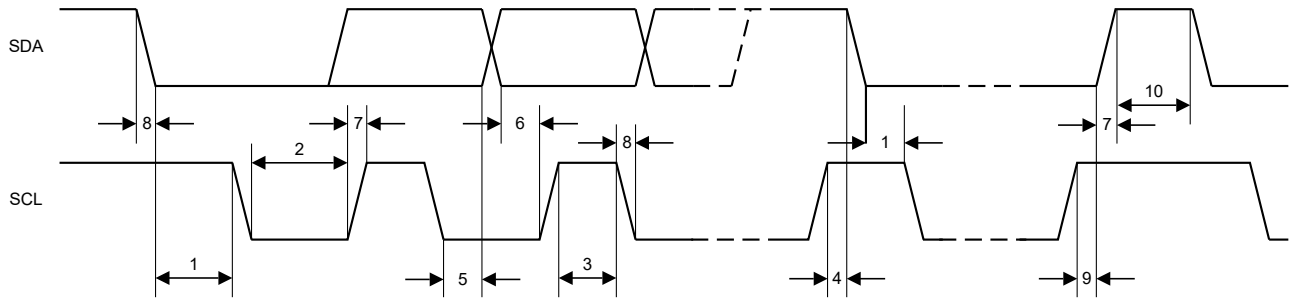
		MIN	NOM	MAX	UNIT
<b>MISC. Timing Requirements</b>					
$f_{OSC}$	Internal oscillator frequency		31.2		MHz
$f_{OSC\_ERR}$	Device to device oscillator frequency error	-3%		3%	
$t_{POR\_H}$	Wait time from UVLO disactive to device NORMAL			500	$\mu\text{s}$
$t_{CHIP\_EN}$	Wait time from setting Chip_EN (Register) =1 to device NORMAL			100	$\mu\text{s}$
$t_{RISE}$	LED output rise time		10		ns
$t_{FALL}$	LED output fall time		15		ns
$t_{VSYNC\_H}$	The minimum high-level pulse width of VSYNC	200			$\mu\text{s}$
<b>SPI timing requirements</b>					
$f_{SCLK}$	SPI Clock frequency			12	MHz
1	Cycle time	83.3			ns
2	SS active lead-time	50			ns
3	SS active leg time	50			ns
4	SS inactive time	50			ns

## 6.6 Timing Requirements (continued)

		MIN	NOM	MAX	UNIT
5	SCLK low time	36			ns
6	SCLK high time	36			ns
7	MOSI set-up time	20			ns
8	MOSI hold time	20			ns
9	MISO disable time			30	ns
10	MISO data valid time			35	ns
C <sub>b</sub>	Bus capacitance	5		40	pF
<b>I<sup>2</sup>C standard mode timing requirements</b>					
<b>I<sup>2</sup>C fast mode timing requirements</b>					
f <sub>SCL</sub>	I <sup>2</sup> C clock frequency	0		400	KHz
1	Hold time (repeated) START condition	0.6			μs
2	Clock low time	1.3			μs
3	Clock high time	0.6			μs
4	Setup time for a repeated START condition	0.6			μs
5	Data hold time	0			μs
6	Data setup time	100			ns
7	Rise time of SDA and SCL			300	ns
8	Fall time of SDA and SCL			300	ns
9	Setup time for STOP condition	0.6			μs
10	Bus free time between a STOP and a START condition	1.3			μs
<b>I<sup>2</sup>C fast mode plus timing requirements</b>					
f <sub>SCL</sub>	I <sup>2</sup> C clock frequency	0		1000	KHz
1	Hold time (repeated) START condition	0.26			μs
2	Clock low time	0.5			μs
3	Clock high time	0.26			μs
4	Setup time for a repeated START condition	0.26			μs
5	Data hold time	0			μs
6	Data setup time	50			ns
7	Rise time of SDA and SCL			120	ns
8	Fall time of SDA and SCL			120	ns
9	Setup time for STOP condition	0.26			μs
10	Bus free time between a STOP and a START condition	0.5			μs



**Figure 6-1. SPI Timing Parameters**



**Figure 6-2. I<sup>2</sup>C Timing Parameters**

## 6.7 Typical Characteristics

Unless specified otherwise, typical characteristics apply over the full ambient temperature range ( $-40^{\circ}\text{C} < T_A < +85^{\circ}\text{C}$ ),  $V_{CC} = 3.3\text{V}$ ,  $V_{IO} = 3.3$ ,  $V_{LED} = 5\text{V}$ ,  $I_{LED\_Peak} = 50\text{mA}$ ,  $C_{VLED} = 1\mu\text{F}$ ,  $C_{VCC} = 1\mu\text{F}$

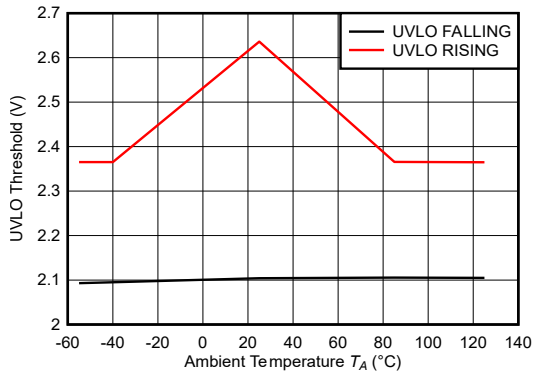


Figure 6-3. V<sub>CC</sub> UVLO Rising and Falling Thresholds

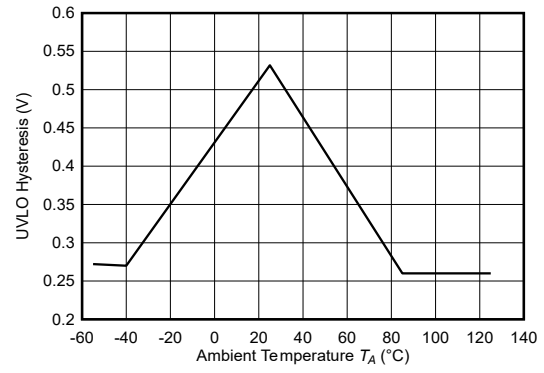


Figure 6-4. V<sub>CC</sub> UVLO Hysteresis

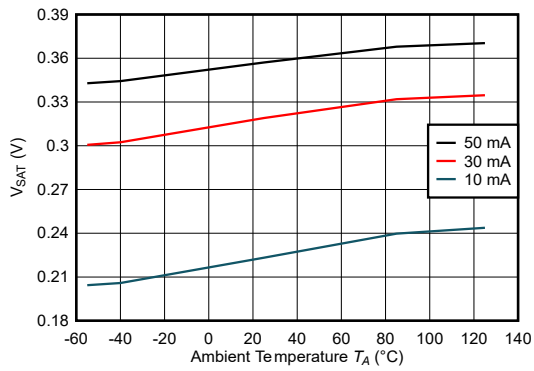


Figure 6-5. V<sub>SAT</sub> vs Temperature

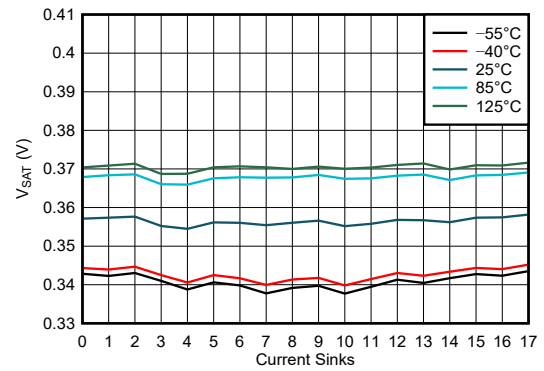


Figure 6-6. V<sub>SAT</sub> vs Current Sinks (50mA)

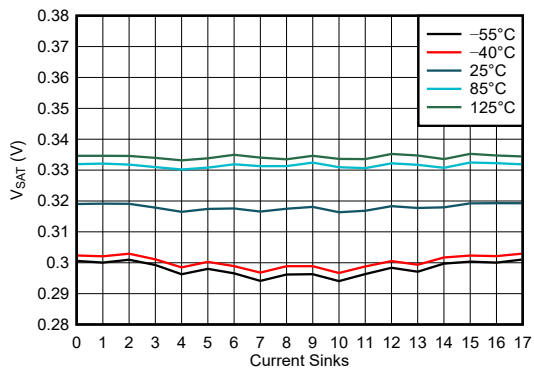


Figure 6-7. V<sub>SAT</sub> vs Current Sinks (30mA)

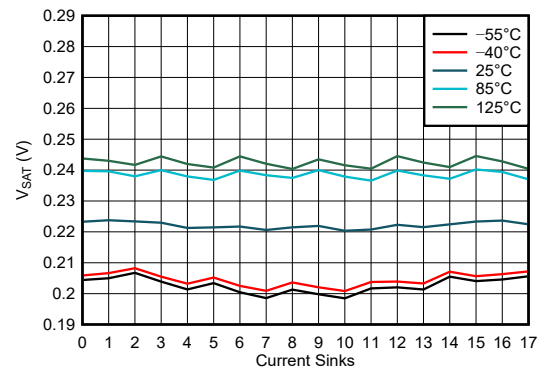
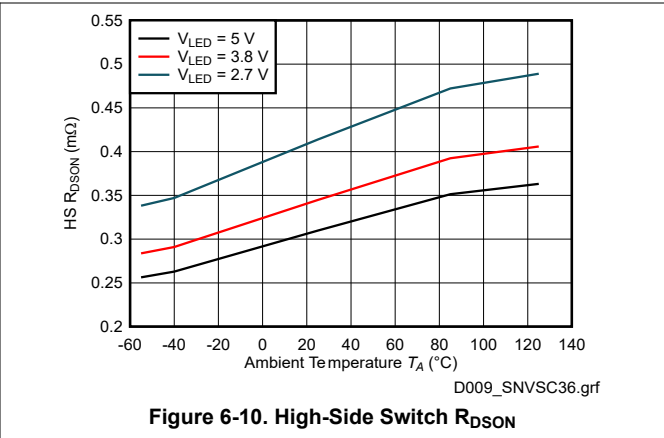
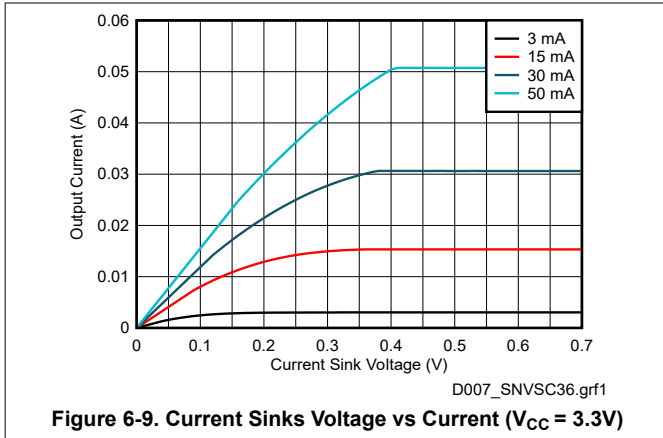


Figure 6-8. V<sub>SAT</sub> vs Current Sinks (10mA)

### 6.7 Typical Characteristics (continued)

Unless specified otherwise, typical characteristics apply over the full ambient temperature range ( $-40^{\circ}\text{C} < T_A < +85^{\circ}\text{C}$ ),  $V_{CC} = 3.3\text{V}$ ,  $V_{IO} = 3.3$ ,  $V_{LED} = 5\text{V}$ ,  $I_{LED\_Peak} = 50\text{mA}$ ,  $C_{VLED} = 1\mu\text{F}$ ,  $C_{VCC} = 1\mu\text{F}$



## 7 Detailed Description

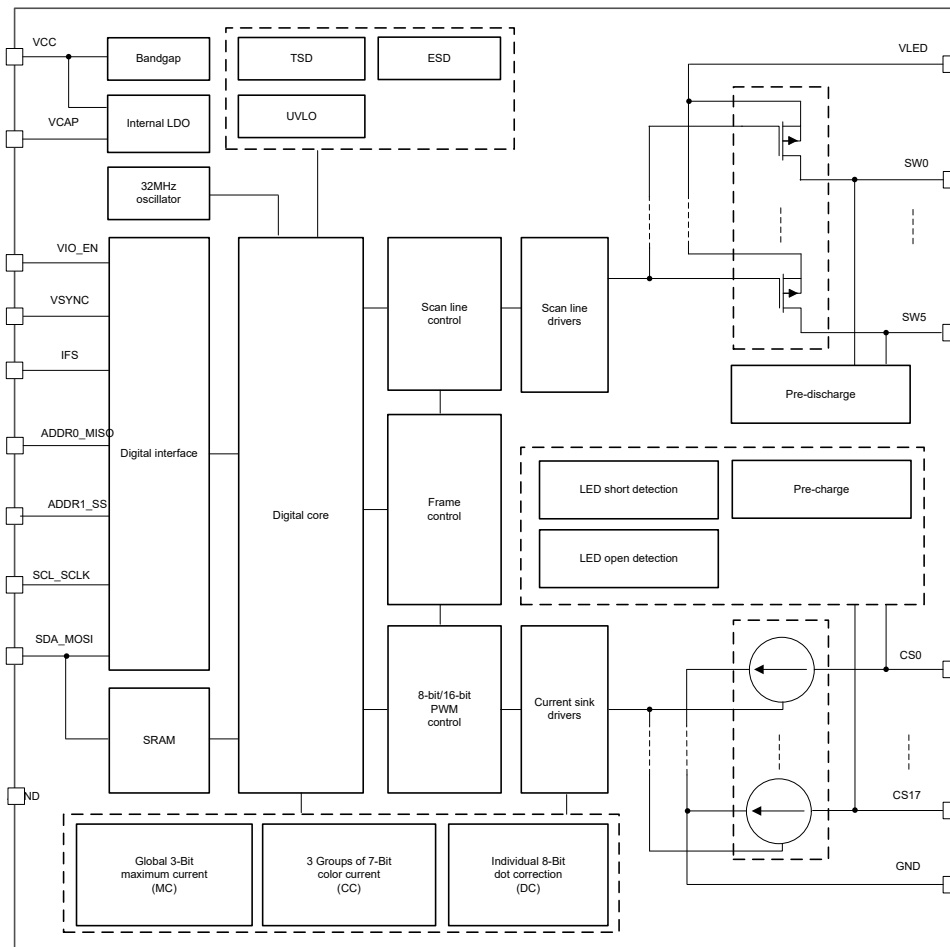
### 7.1 Overview

The LP5866 is an 6 × 18 LED matrix driver. The device integrates 6 switching FETs with 18 constant current sinks. One LP5866 device can drive up to 108 LED dots or 36 RGB pixels by using time-multiplexing matrix scheme.

The LP5866 supports both analog dimming and PWM dimming methods. For analog dimming, the current gain of each individual LED dot can be adjusted with 256 steps through 8-bits dot correction. For PWM dimming, the integrated 8-bits or 16-bits configurable, > 20kHz PWM generators for each LED dot enable smooth, vivid animation effects without audible noise. Each LED can also be mapped into a 8-bits group PWM to achieve the group control with minimum data traffic.

The LP5866 device implements full addressable SRAM. The device supports entire SRAM data refresh and partial SRAM data update on demand to minimize the data traffic. The LP5866 implements the ghost cancellation circuit to eliminate both upside and downside ghosting. The LP5866 also uses low brightness compensation technology to support high density LED pixels. Both 1MHz (maximum) I<sup>2</sup>C and 12MHz (maximum) SPI interfaces are available in the LP5866.

### 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 Time-Multiplexing Matrix

The LP5866 device uses time-multiplexing matrix scheme to support up to 108 LED dots with one chip. The device integrates 18 current sinks with 6 scan lines to drive  $18 \times 6 = 108$  LED dots or  $6 \times 6 = 36$  RGB pixels. In matrix control scheme, the device scans from Line 0 to Line 5 sequentially as shown in Figure 7-1. Current gain and PWM duty registers are programmable for each LED dot to support individual analog and PWM dimming.

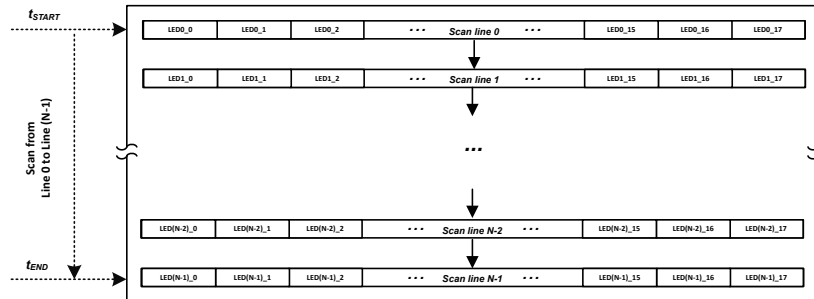


Figure 7-1. Scan Line Control Scheme

There are 6 high-side p-channel MOSFETs (PMOS) integrated in LP5866 device. Users can flexibly set the active scan numbers from 1 to 6 by configuring the 'Max\_Line\_Num' in Dev\_initial register. The time-multiplexing matrix timing sequence follows the Figure 7-2.

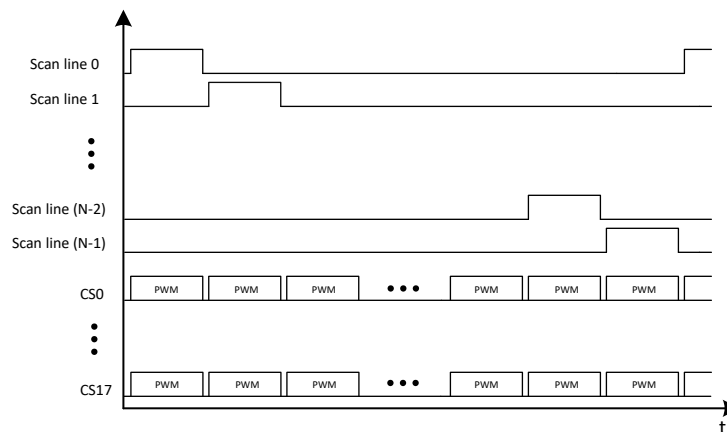


Figure 7-2. Time-Multiplexing Matrix Timing Sequence

One cycle time of the line switching can be calculated as below:

$$t_{\text{line\_switch}} = t_{\text{PWM}} + t_{\text{SW\_BLK}} + 2 \times t_{\text{phase\_shift}} \quad (1)$$

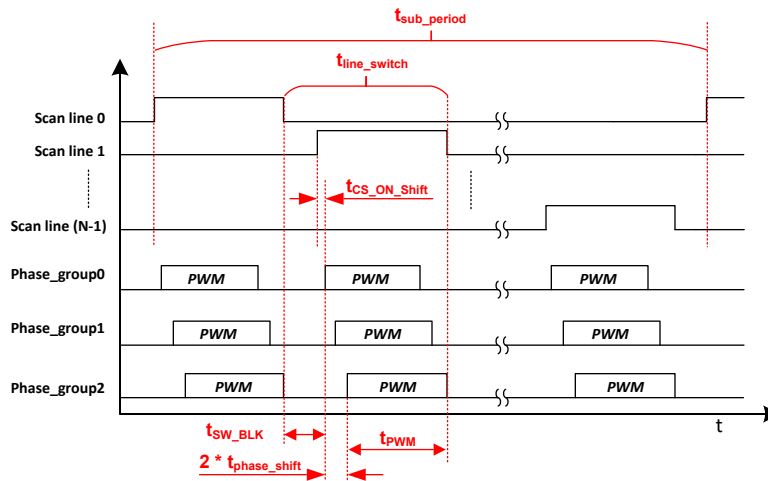
- $t_{\text{PWM}}$  is the current sink active time, which equals to 8 us (PWM frequency set at 125 kHz) or 16 us (PWM frequency set at 62.5 kHz) by configuring 'PWM\_Fre' in Dev\_initial register.
- $t_{\text{SW\_BLK}}$  is the switch blank time, which equals to 1 us or 0.5 us by configuring 'SW\_BLK' in Dev\_config1 register.
- $t_{\text{phase\_shift}}$  is the PWM phase shift time, which equal to 0 or 125 ns by configuring 'PWM\_Phase\_Shift' in Dev\_config1 register.

Total display time for one complete sub-period is  $t_{\text{sub\_period}}$  and it can be calculated by the following equation:

$$t_{\text{sub\_period}} = t_{\text{line\_switch}} \times \text{Scan\_line\#} \quad (2)$$

- Scan\_line# is the scan line number determined by 'Max\_Line\_Num' in Dev\_initial register.

The time-multiplexing matrix scheme time diagram is shown in [Figure 7-3](#). The  $t_{CS\_ON\_Shift}$  is the current sink turning on shift by configuring 'CS\_ON\_Shift' bit in Dev\_config1 register.



**Figure 7-3. Time-Multiplexing Matrix Timing Diagram**

The LP5866 device implements deghosting and low brightness compensation to remove the side effects of matrix topology:

- **Deghosting:** Both upside deghosting and downside deghosting are implemented to eliminate the LED unexpected weak turn-on.
  - Upside\_deghosting: discharge each scan line during its off state. By configuring the 'Up\_Deghost' in Dev\_config3 register, the LP5866 discharges and clamps the scan line switch to a certain voltage.
  - Downside\_deghosting: pre-charge each current sink voltage during its OFF state. The deghosting capability can be adjusted through the 'Down\_Deghost' in Dev\_config3 register.
- **Low Brightness Compensation:** three groups compensation are implemented to overcome the color-shift and non-uniformity in low brightness conditions. The compensation capability can be through 'Comp\_Group1', 'Comp\_Group2', and 'Comp\_Group3' in Dev\_config2 register.
  - Compensation\_group 1: CS0, CS3, CS6, CS9, CS12, CS15.
  - Compensation\_group 2: CS1, CS4, CS7, CS10, CS13, CS16.
  - Compensation\_group 3: CS2, CS5, CS8, CS11, CS14, CS17.

### 7.3.2 Analog Dimming (Current Gain Control)

Analog dimming of LP5866 is achieved by configuring the current gain control. There are several methods to control the current gain of each LED.

- Global 3-bits Maximum Current (MC) setting without external resistor
- 3 groups of 7-bits Color Current (CC) setting
- Individual 8-bit Dot Current (DC) setting

#### Global 3-Bits Maximum Current (MC) Setting

The MC is used to set the maximum current  $I_{OUT\_MAX}$  for each current sink and this current is the maximum peak current for each LED dot. The MC can be set with 3 bits (8 steps) from 3 mA to 50 mA. When the device is powered on, the MC data is set to default value, which is 15 mA.

For data refresh [Mode 1](#), MC data is effective immediately after new data is updated. For [Mode 2](#) and [Mode 3](#), to avoid unexpected MC data change during high speed data refreshing, MC data must be changed when all channels are off and new MC data is only be updated when the 'Chip\_EN' bit in Chip\_en register is set to 0, and after the 'Chip\_EN' returns to 1, the new MC data is effective. 'Down\_Deghost' and 'Up\_Deghost' in Dev\_config3 work in the similar way with MC.



**Table 7-1. Maximum Current (MC) Register Setting**

3-BITS MAXIMUM_CURRENT REGISTER		I <sub>OUT_MAX</sub>
Binary	Decimal	mA
000	0	3
001	1	5
010	2	10
011 (default)	3 (default)	15 (default)
100	4	20
101	5	30
110	6	40
111	7	50

### 3 Groups of 7-Bits Color Current (CC) Setting

The LP5866 device can adjust the output current of three color groups separately. For each color, the device has 7-bits data in 'CC\_Group1', 'CC\_Group2', and 'CC\_Group3'. Thus, all color group currents can be adjusted in 128 steps from 0% to 100% of the maximum output current, I<sub>OUT\_MAX</sub>.

The 18 current sinks have fixed mapping to the three color groups:

- CC-Group 1: CS0, CS3, CS6, CS9, CS12, CS15.
- CC-Group 2: CS1, CS4, CS7, CS10, CS13, CS16.
- CC-Group 3: CS2, CS5, CS8, CS11, CS14, CS17.

**Table 7-2. 3 Groups of 7-bits Color Current (CC) Setting**

7-BITS CC_GROUP1/CC_GROUP2/CC_GROUP3 REGISTER		RATIO OF OUTPUT CURRENT TO I <sub>OUT_MAX</sub>
Binary	Decimal	%
000 0000	0	0
000 0001	1	0.79
000 0010	2	1.57
---	---	---
100 0000 (default)	64 (default)	50.4 (default)
---	---	---
111 1101	125	98.4
111 1110	126	99.2
111 1111	127	100

### Individual 8-bit Dot Current (DC) Setting

The LP5866 can individually adjust the output current of each LED by using dot current function through DC setting. The device allows the brightness deviations of the LEDs to adjusted be individually. Each output DC is programmed with a 8-bit depth, so the value can be adjusted with 256 steps within the range from 0% to 100% of (I<sub>OUT\_MAX</sub> × CC/127).

**Table 7-3. Individual 8-bit Dot Current (DC) Setting**

8-BIT DC REGISTER		RATIO OF OUTPUT CURRENT TO I <sub>OUT_MAX</sub> × CC/127
Binary	Decimal	%
0000 0000	0	0
0000 0001	1	0.39
0000 0010	2	0.78
---	---	---
1000 0000 (default)	128 (default)	50.2 (default)

**Table 7-3. Individual 8-bit Dot Current (DC) Setting (continued)**

8-BIT DC REGISTER		RATIO OF OUTPUT CURRENT TO $I_{OUT\_MAX} \times CC/127$
Binary	Decimal	%
---	---	---
1111 1101	253	99.2
1111 1110	254	99.6
1111 1111	255	100

In summary, the current gain of each current sink can be calculated as below:

$$I_{OUT} \text{ (mA)} = I_{OUT\_MAX} \times (CC/127) \times (DC/255) \quad (3)$$

For time-multiplexing scan scheme, if the scan number is N, each LED dot average current  $I_{AVG}$  is shown as below:

$$I_{AVG} \text{ (mA)} = I_{OUT} / N = I_{OUT\_MAX} \times (CC/127) \times (DC/255) / N \quad (4)$$

### 7.3.3 PWM Dimming

There are several methods to control the PWM duty cycle of each LED dot.

- **Individual 8-bit / 16-bit PWM for Each LED Dot**

Every LED has an individual 8-bit or 16-bit PWM register that is used to change the LED brightness by PWM duty. The LP5866 uses an enhanced spectrum PWM (ES-PWM) algorithm to achieve 16-bit depth with high refresh rate, which can avoid flicker under a high speed camera. Comparing with conventional 8-bit PWM, 16-bit PWM can help to achieve ultimate high dimming resolution in LED animation applications.

- **3 Programmable Groups of 8-bit PWM Dimming**

The group PWM Control is used to select LEDs into 1 to 3 groups where each group has a separate register for duty cycle control. Every LED has 2-bit selection in LED\_DOT\_GROUP Registers (x = 0, 1, ... , 29.) to select whether it belongs to one of the three groups or not:

- 00: not a member of any group
- 01: member of group 1
- 10: member of group 2
- 11: member of group 3

- **8-bit PWM for Global Dimming**

The Global PWM Control function affects all LEDs simultaneously.

The final PWM duty cycle can be calculated as below:

$$PWM\_Final(8 \text{ bit}) = PWM\_Individual(8 \text{ bit}) \times PWM\_Group(8 \text{ bit}) \times PWM\_Global(8\text{-bit}) \quad (5)$$

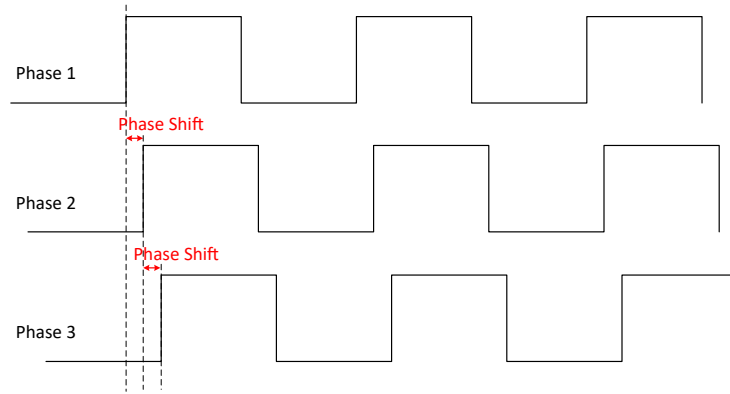
$$PWM\_Final(16 \text{ bit}) = PWM\_Individual(16 \text{ bit}) \times PWM\_Group(8 \text{ bit}) \times PWM\_Global(8\text{-bit}) \quad (6)$$

The LP5866 supports 125-kHz or 62.5-kHz PWM output frequency. The PWM frequency is selected by configuring the 'PWM\_Fre' in Dev\_initial register. An internal 31.2-MHz oscillator is used for generating PWM outputs. The high-accuracy design of the oscillator ( $f_{OSC\_ERR} \leq \pm 2\%$ ) enables a better synchronization if multiple LP5866 devices are connected together.

A PWM phase-shifting scheme is implemented in each current sink to avoid the current overshoot when turning on simultaneously. As the LED drivers are not activated simultaneously, the peak load current from the pre-stage power supply is significantly decreased. This scheme also reduces input-current ripple and ceramic-capacitor audible ringing. LED drivers are grouped into three different phases. By configuring the 'PWM\_Phase\_Shift' in

Dev\_config1 register, which is default off, the LP5866 supports  $t_{\text{phase\_shift}} = 125\text{-ns}$  shifting time shown in Figure 7-4.

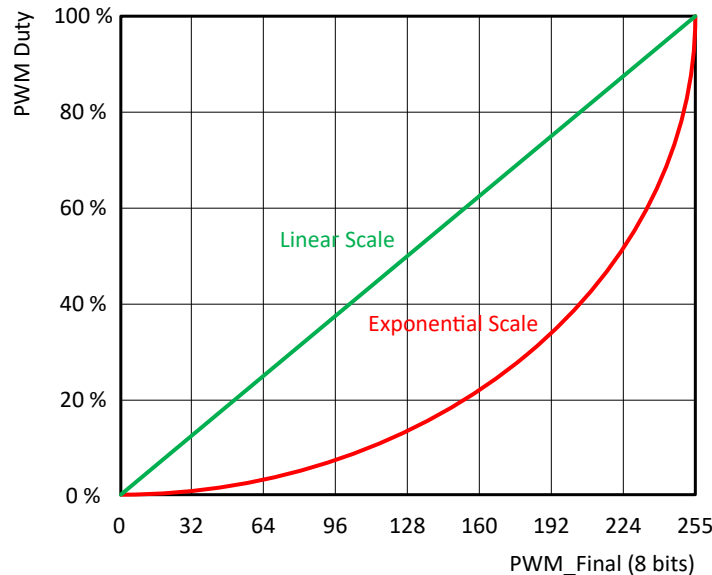
- Phase 1: CS0, CS3, CS6, CS9, CS12, CS15.
- Phase 2: CS1, CS4, CS7, CS10, CS13, CS16.
- Phase 3: CS2, CS5, CS8, CS11, CS14, CS17.



**Figure 7-4. Phase Shift**

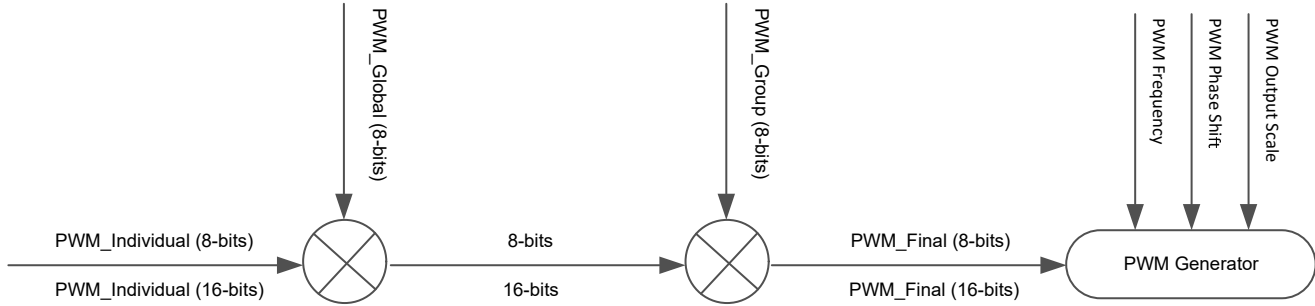
To avoid high current sinks output ripple during line switching, current sinks can be configured to turn on with 1 clock delay (62.5 ns or 31.25 ns according to the PWM frequency) after lines turn on, as shown in Figure 7-3. This function can be configured by 'CS\_ON\_Shift' in Dev\_config1 register.

The LP5866 allows users to configure the dimming scale either exponentially (Gamma Correction) or linearly through the 'PWM\_Scale\_Mode' in Dev\_config1 register. If a human-eye-friendly dimming curve is desired, using the internal fixed exponential scale is an easy approach. If a special dimming curve is desired, TI recommends using the linear scale with software correction. The LP5866 supports both linear and exponential dimming curves under 8-bit and 16-bit PWM depth. Figure 7-5 is an example of 8-bit PWM depth.



**Figure 7-5. Linear and Exponential Dimming Curves**

In summary, Figure 7-6 illustrates the PWM control method:



**Figure 7-6. PWM Control Scheme**

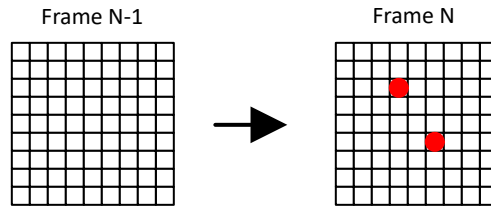
**7.3.4 ON and OFF Control**

The LP5866 device supports the individual ON and OFF control of each LED. For indication purpose, users can turn on and off the LED directly by writing 1-bit ON and OFF data to the corresponding Dot\_onoffx (x = 0, 1, ... , 17) register.

**7.3.5 Data Refresh Mode**

The LP5866 supports three data refresh modes: Mode 1, Mode 2, and Mode 3, by configuring 'Data\_Ref\_Mode' in Dev\_initial register.

**Mode 1:** 8-bit PWM data without VSYNC command. Data is sent out for display instantly after received. With Mode 1, users can refresh the corresponding dot data, only instead of updating the whole SRAM. It is called 'on demand data refresh', which can save the total data volume effectively. As shown in Figure 7-7, the red LED dots can be refreshed after sending the corresponding data while the others kept the same with last frame.

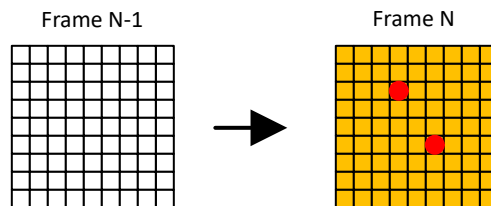


**Figure 7-7. On Demand Data Refresh – Mode 1**

**Mode 2:** 8-bit PWM data with VSYNC command. Data is held and sent out simultaneously by frame after receiving the VSYNC command.

**Mode 3:** 16-bit PWM data with VSYNC command. Data is held and sent out simultaneously by frame after receiving the VSYNC command.

Frame control is implemented in Mode 2 and Mode 3. Instead of refreshing the output instantly after data is received (Mode 1), the device holds the data and refreshes the whole frame data by a fixed frame rate,  $f_{VSYNC}$ . Usually, 24Hz, 50Hz, 60Hz, 120Hz or even higher frame rate is selected to achieve vivid animation effects. Whole SRAM Data Refresh is shown in Figure 7-8, a new frame is updated after receiving the VSYNC command.



**Figure 7-8. Whole SRAM Data Refresh**

Comparing with Mode 1, Mode 2 and Mode 3 provide a better synchronization when multiple LP5866 devices used together. A high-level pulse width longer than  $t_{\text{SYNC\_H}}$  is required at the beginning of each VSYNC frame. Figure 7-9 shows the VSYNC connections and Figure 7-10 shows the timing requirements.

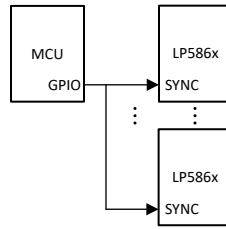


Figure 7-9. Multiple Devices Sync

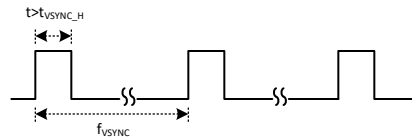


Figure 7-10. VSYNC Timing

Table 8-4 is the summary of the three data refresh modes.

Table 7-4. Data Refresh Mode

MODE TYPE	PWM RESOLUTION	PWM OUTPUT	EXTERNAL VSYNC
Mode 1	8 Bits	Data update instantly	No
Mode 2	8 Bits	Data update by frame	Yes
Mode 3	16 Bits		

### 7.3.6 Full Addressable SRAM

SRAM is implemented inside the LP5866 device to support data writing and reading at the same time.

Although data refresh mechanisms are not the same for Mode 1 and Mode 2, and Mode 3, the data writing and reading follow the same method. Users can update partial of the SRAM data only or the whole SRAM page simultaneously. The LP5866 supports auto-increment function to minimize data traffic and increase data transfer efficiency.

Please note that 16-bit PWM (Mode 3) and 8-bit PWM (Mode 1 and Mode 2) are assigned with different SRAM addresses.

### 7.3.7 Protections and Diagnostics

#### LED Open Detection

The LP5866 includes LED open detection (LOD) for the fault caused by any opened LED dot. The threshold for LED open is 0.25V typical. LED open detection is only performed when PWM  $\geq$  25 (Mode 1 and Mode 2) or PWM  $\geq$  6400 (Mode 3) and voltage on CS<sub>n</sub> is detected lower than open threshold for continuously 4 sub-periods.

Figure 7-11 shows the detection circuit of LOD function. When open fault is detected, 'Global\_LOD' bit in Fault\_state register is set to 1 and detailed fault state for each LED is also monitored in register Dot\_lodx (x = 0, 1, ..., 17). All open fault indicator bits can be cleared by setting LOD\_clear = 0Fh after the open condition is removed.

LOD removal function can be enabled by setting 'LOD\_removal' bit in Dev\_config2 register to 1. This function turns off the current sink of the open channel when scanning to the line where the opened LED is included.

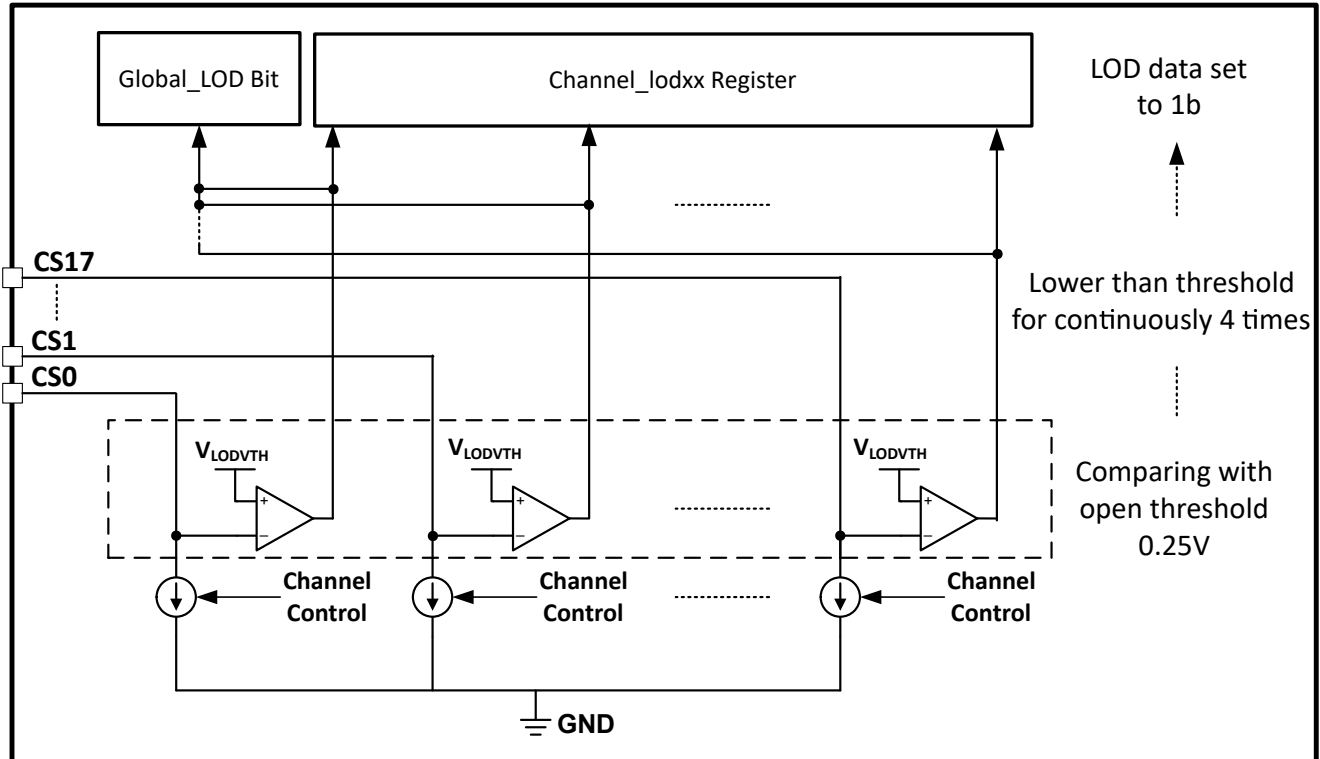


Figure 7-11. LOD Circuits

### LED Short Detection

The LP5866 includes LED short detection (LSD) for the fault caused by any shorted LED. Threshold for channel short is  $(V_{LED} - 1) V$  typical. LED short detection only performed when  $PWM \geq 25$  (Mode 1 and Mode 2) or  $PWM \geq 6400$  (Mode 3) and voltage on CSn is detected higher than short threshold for continuously 4 sub-periods. As there is parasitic capacitance for the current sink, to make sure the LSD result is correct, TI recommends to set the LED current higher than 0.5mA.

Figure 7-12 shows the detection circuit of LSD function. When short fault is detected, 'Global\_LSD bit' in Fault\_state register is set to 1 and detailed fault state for every channel can also be monitored in register Dot\_Isdx ( $x = 0, 1, \dots, 17$ ). All short fault indicator bits can be cleared by setting LSD\_clear = 0Fh after the short condition is removed.

LSD removal function can be enabled by setting 'LSD\_removal' bit in Dev\_config2 register to 1. This function turns off the upside deghosting function of the scan line where short LED is included.

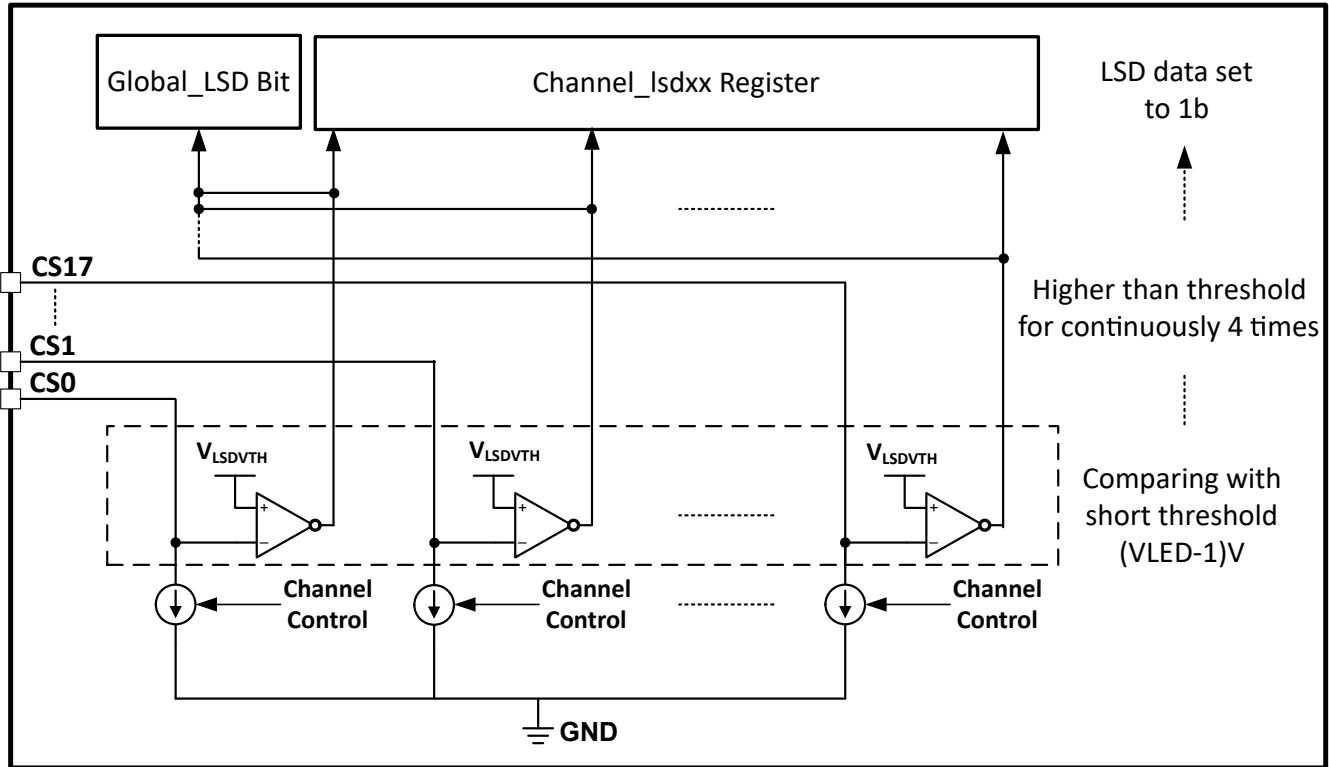


Figure 7-12. LSD Circuit

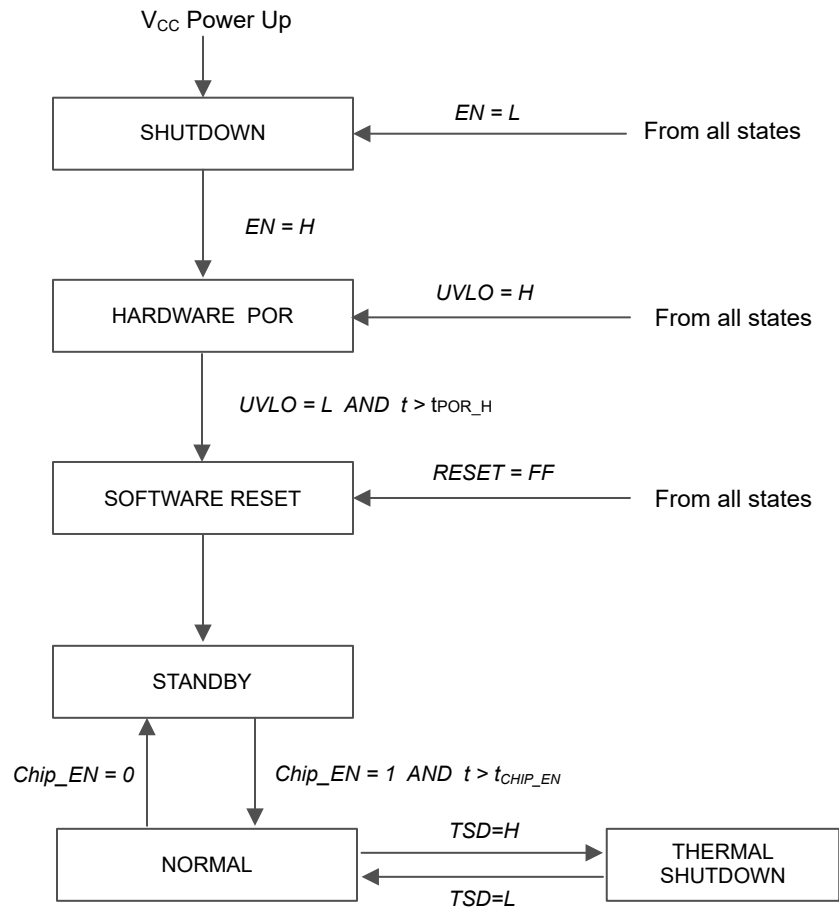
### Thermal Shutdown

The LP5866 device implements thermal shutdown mechanism to protect the device from damage due to overheating. When the junction temperature rises to 160°C (typical) and above, the device switches into shutdown mode. The LP5866 exits thermal shutdown when the junction temperature of the device drops to 145°C (typical) and below.

### UVLO (Undervoltage Lockout)

The LP5866 has an internal comparator that monitors the voltage at VCC. When VCC is below  $V_{UVF}$ , reset is active and the LP5866 enters INITIALIZATION state.

## 7.4 Device Functional Modes



**Figure 7-13. Device Functional Modes**

- Shutdown: The device enters into shutdown mode from all states on VCC power up or EN pin is low.
- Hardware POR: The device enters into hardware POR when Enable pin is high or VCC fall under  $V_{UVF}$  causing UVLO = H from all states.
- Software reset: The device enters into software reset mode when VCC rise higher than  $V_{UVR}$  with the time  $t > t_{POR\_H}$ . In this mode, all the registers are reset. Entry can also be from any state when the RESET (register) = FFh or UVLO is low.
- Standby: The device enters the standby mode when Chip\_EN (register) = 0. In this mode, the device enters into low power mode, but the I<sup>2</sup>C/SPI are still available for Chip\_EN only and the register data is retained.
- Normal: The device enters the normal mode when 'Chip\_EN' = 1 with the time  $t > t_{CHIP\_EN}$ .
- Thermal shutdown: The device automatically enters the thermal shutdown mode when the junction temperature exceeds 160°C (typical). If the junction temperature decreases below 145°C (typical), the device returns to the normal mode.



## 7.5 Programming

### Interface Selection

The LP5866 supports two communication interfaces: I<sup>2</sup>C and SPI. If IFS is high, it enters into SPI mode. If IFS is low, it enters into I<sup>2</sup>C mode.

**Table 7-5. Interface Selection**

INTERFACE TYPE	ENTRY CONDITION
I <sup>2</sup> C	IFS = Low
SPI	IFS = High

### I<sup>2</sup>C Interface

The LP5866 is compatible with I<sup>2</sup>C standard specification. the device supports both fast mode (400kHz maximum) and fast plus mode (1MHz maximum).

#### I<sup>2</sup>C Data Transactions

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when clock signal is LOW. START and STOP conditions classify the beginning and the end of the data transfer session. A START condition is defined as the SDA signal transitioning from HIGH to LOW while SCL line is HIGH. A STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The bus leader always generates START and STOP conditions. The bus is considered to be busy after a START condition and free after a STOP condition. During data transmission, the bus leader can generate repeated START conditions. First START and repeated START conditions are functionally equivalent.

Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the leader. The leader releases the SDA line (HIGH) during the acknowledge clock pulse. The device pulls down the SDA line during the 9<sup>th</sup> clock pulse, signifying an acknowledge. The device generates an acknowledge after each byte has been received.

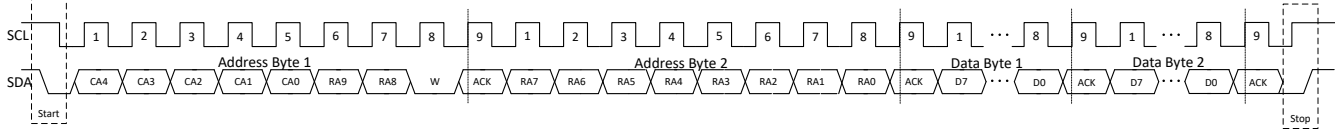
There is one exception to the acknowledge after every byte rule. When the leader is the receiver, it must indicate to the transmitter an end of data by not acknowledging (*negative acknowledge*) the last byte clocked out of the follower. This negative acknowledge still includes the acknowledge clock pulse (generated by the leader), but the SDA line is not pulled down.

#### I<sup>2</sup>C Data Format

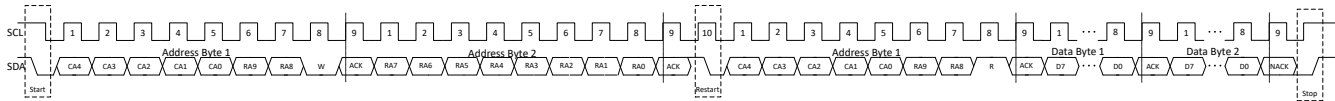
The address and data bits are transmitted MSB first with 8-bits length format in each cycle. Each transmission is started with Address Byte 1, which are divided into 5-bits of the chip address, 2 higher bits of the register address, and 1 read and write bit. The other 8 lower bits of register address are put in Address Byte 2. The device supports both independent mode and broadcast mode. The auto-increment feature allows writing and reading several consecutive registers within one transmission. If not consecutive, a new transmission must be started.

**Table 7-6. I<sup>2</sup>C Data Format**

Address Byte 1	Chip Address					Register Address		R/W
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Independent	1	0	0	ADDR1	ADDR0	9 <sup>th</sup> bit	8 <sup>th</sup> bit	R: 1 W: 0
Broadcast	1	0	1	0	1			
Address Byte 2	Register Address							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	7 <sup>th</sup> bit	6 <sup>th</sup> bit	5 <sup>th</sup> bit	4 <sup>th</sup> bit	3 <sup>th</sup> bit	2 <sup>th</sup> bit	1 <sup>th</sup> bit	0 <sup>th</sup> bit



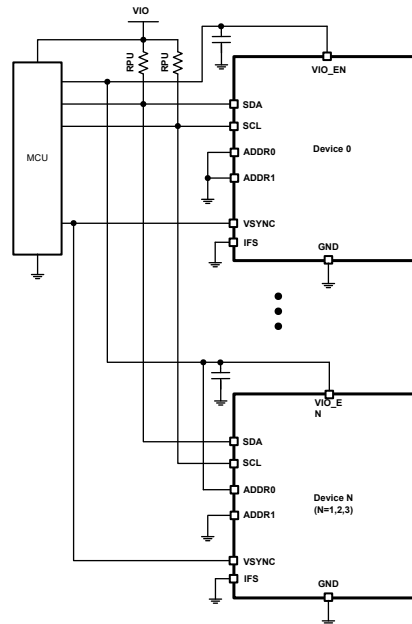
**Figure 7-14. I<sup>2</sup>C Write Timing**



**Figure 7-15. I<sup>2</sup>C Read Timing**

**Multiple Devices Connection**

The LP5866 enters into I<sup>2</sup>C mode if IFS is connected to GND. The ADDR0/1 pin is used to select the unique I<sup>2</sup>C follower address for each device. The SCL and SDA lines must each have a pullup resistor (4.7KΩ for 400kHz, 2KΩ for 1MHz) placed somewhere on the line and remain HIGH even when the bus is idle. VIO\_EN can either be connected with VIO power supply or GPIO. TI suggests to put one 1nF cap as closer to VIO\_EN pin as possible. Up to four LP5866 follower devices can share the same I<sup>2</sup>C bus by the different ADDR configurations.



**Figure 7-16. I<sup>2</sup>C Multiple Devices Connection**

**SPI Interface**

The LP5866 is compatible with SPI serial-bus specification, and it operates as a follower. The maximum frequency supported by LP5866 is 12MHz.

**SPI Data Transactions**

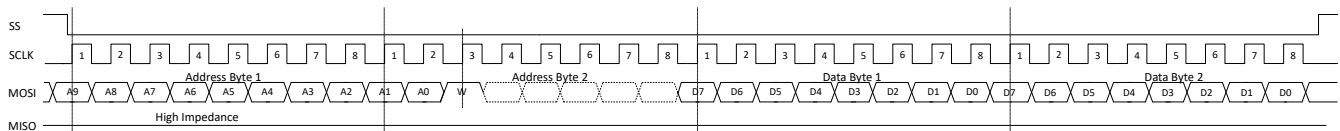
MISO output is normally in a high impedance state. When the follower-select pin SS for the device is active (low) the MISO output is pulled low for read only. During write cycle MISO stays in high-impedance state. The follower-select signal SS must be low during the cycle transmission. SS resets the interface when high. Data is clocked in on the rising edge of the SCLK clock signal, while data is clocked out on the falling edge of SCLK.

**SPI Data Format**

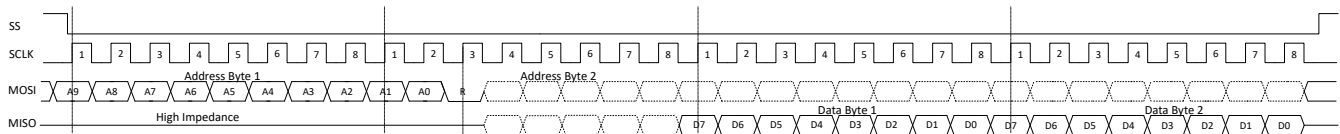
The address and data bits are transmitted MSB first with 8-bits length format in each cycle. Each transmission is started with Address Byte 1, which contains 8 higher bits of the register address. The Address Byte 2 is started with 2 lower bits of the register address and 1 read and write bit. The auto-increment feature allows writing and reading several consecutive registers within one transmission. If not consecutive, a new transmission must be started.

**Table 7-7. SPI Data Format**

Address Byte 1	Register Address								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
	9 <sup>th</sup> bit	8 <sup>th</sup> bit	7 <sup>th</sup> bit	6 <sup>th</sup> bit	5 <sup>th</sup> bit	4 <sup>th</sup> bit	3 <sup>th</sup> bit	2 <sup>th</sup> bit	
Address Byte 2	Register Address								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
	1 <sup>th</sup> bit	0 <sup>th</sup> bit	R: 0 W: 1	Don't Care					



**Figure 7-17. SPI Write Timing**



**Figure 7-18. SPI Read Timing**

**Multiple Devices Connection**

The device enters into SPI mode if IFS is pulled high to VIO through a pullup resistor (4.7KΩ recommended). VIO\_EN can either be connected with VIO power supply or GPIO. TI suggests to put one 1nF cap as closer to VIO\_EN pin as possible. In SPI mode host can address as many devices as there are follower select pins on host.

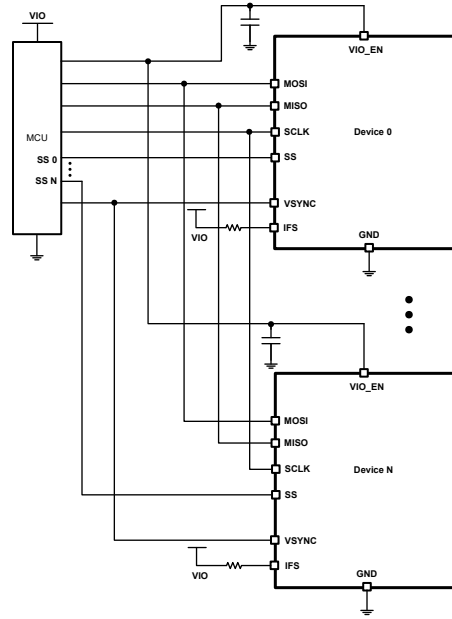


Figure 7-19. SPI Multiple Devices Connection

### 7.6 Register Maps

This section provides a summary of the register maps. For detailed register functions and descriptions, please refer to [LP5866 11x18 LED Matrix Driver Register Maps](#).

Table 7-8. Register Section, Block Access Type Codes

Access Type	Code	Description
<b>Read Type</b>		
R	R	Read
RC	R C	Read to Clear
R-0	R -0	Read Returns 0s
<b>Write Type</b>		
W	W	Write
W0CP	W 0C P	W 0 to clear Requires privileged access
Reset or Default Value		
-n		Value after reset or the default value

Register Acronym	Address	Type	D7	D6	D5	D4	D3	D2	D1	D0	Default
Chip_en	000h	R/W	Reserved							Chip_EN	00h
Dev_initial	001h	R/W	Reserved	Max_Line_Num				Data_Ref_Mode		PWM_Fre	5Eh
Dev_config1	002h	R/W	Reserved	Reserved	Reserved	Reserved	SW_BLK	PWM_Scale_Mode	PWM_Phase_Shift	CS_ON_Shift	00h
Dev_config2	003h	R/W	Comp_Group3		Comp_Group2		Comp_Group1		LOD_remove	LSD_remove	00h
Dev_config3	004h	R/W	Down_Deghost		Up_Deghost		Maximum_Current			Up_Deghost_enable	47h

<b>Global_bri</b>	005h	R/W	PWM_Global								FFh	
<b>Group0_bri</b>	006h	R/W	PWM_Group1								FFh	
<b>Group1_bri</b>	007h	R/W	PWM_Group2								FFh	
<b>Group2_bri</b>	008h	R/W	PWM_Group3								FFh	
<b>R_current_set</b>	009h	R/W	Reserved	CC_Group1							40h	
<b>G_current_set</b>	00Ah	R/W	Reserved	CC_Group2							40h	
<b>B_current_set</b>	00Bh	R/W	Reserved	CC_Group3							40h	
<b>Dot_grp_sel0</b>	00Ch	R/W	Dot L0-CS3 group		Dot L0-CS2 group		Dot L0-CS1 group		Dot L0-CS0 group		00h	
<b>Dot_grp_sel1</b>	00Dh	R/W	Dot L0-CS7 group		Dot L0-CS6 group		Dot L0-CS5 group		Dot L0-CS4 group		00h	
<b>Dot_grp_sel2</b>	00Eh	R/W	Dot L0-CS11 group		Dot L0-CS10 group		Dot L0-CS9 group		Dot L0-CS8 group		00h	
<b>Dot_grp_sel3</b>	00Fh	R/W	Dot L0-CS15 group		Dot L0-CS14 group		Dot L0-CS13 group		Dot L0-CS12 group		00h	
<b>Dot_grp_sel4</b>	010h	R/W	Reserved				Dot L0-CS17 group		Dot L0-CS16 group		00h	
<b>Dot_grp_sel5</b>	011h	R/W	Dot L1-CS3 group		Dot L1-CS2 group		Dot L1-CS1 group		Dot L1-CS0 group		00h	
<b>Dot_grp_sel6</b>	012h	R/W	Dot L1-CS7 group		Dot L1-CS6 group		Dot L1-CS5 group		Dot L1-CS4 group		00h	
<b>Dot_grp_sel7</b>	013h	R/W	Dot L1-CS11 group		Dot L1-CS10 group		Dot L1-CS9 group		Dot L1-CS8 group		00h	
<b>Dot_grp_sel8</b>	014h	R/W	Dot L1-CS15 group		Dot L1-CS14 group		Dot L1-CS13 group		Dot L1-CS12 group		00h	
<b>Dot_grp_sel9</b>	015h	R/W	Reserved				Dot L1-CS17 group		Dot L1-CS16 group		00h	
<b>Dot_grp_sel10</b>	016h	R/W	Dot L2-CS3 group		Dot L2-CS2 group		Dot L2-CS1 group		Dot L2-CS0 group		00h	
<b>Dot_grp_sel11</b>	017h	R/W	Dot L2-CS7 group		Dot L2-CS6 group		Dot L2-CS5 group		Dot L2-CS4 group		00h	
<b>Dot_grp_sel12</b>	018h	R/W	Dot L2-CS11 group		Dot L2-CS10 group		Dot L2-CS9 group		Dot L2-CS8 group		00h	
<b>Dot_grp_sel13</b>	019h	R/W	Dot L2-CS15 group		Dot L2-CS14 group		Dot L2-CS13 group		Dot L2-CS12 group		00h	
<b>Dot_grp_sel14</b>	01Ah	R/W	Reserved				Dot L2-CS17 group		Dot L2-CS16 group		00h	
<b>Dot_grp_sel15</b>	01Bh	R/W	Dot L3-CS3 group		Dot L3-CS2 group		Dot L3-CS1 group		Dot L3-CS0 group		00h	
<b>Dot_grp_sel16</b>	01Ch	R/W	Dot L3-CS7 group		Dot L3-CS6 group		Dot L3-CS5 group		Dot L3-CS4 group		00h	
<b>Dot_grp_sel17</b>	01Dh	R/W	Dot L3-CS11 group		Dot L3-CS10 group		Dot L3-CS9 group		Dot L3-CS8 group		00h	
<b>Dot_grp_sel18</b>	01Eh	R/W	Dot L3-CS15 group		Dot L3-CS14 group		Dot L3-CS13 group		Dot L3-CS12 group		00h	
<b>Dot_grp_sel19</b>	01Fh	R/W	Reserved				Dot L3-CS17 group		Dot L3-CS16 group		00h	
<b>Dot_grp_sel20</b>	020h	R/W	Dot L4-CS3 group		Dot L4-CS2 group		Dot L4-CS1 group		Dot L4-CS0 group		00h	
<b>Dot_grp_sel21</b>	021h	R/W	Dot L4-CS7 group		Dot L4-CS6 group		Dot L4-CS5 group		Dot L4-CS4 group		00h	
<b>Dot_grp_sel22</b>	022h	R/W	Dot L4-CS11 group		Dot L4-CS10 group		Dot L4-CS9 group		Dot L4-CS8 group		00h	
<b>Dot_grp_sel23</b>	023h	R/W	Dot L4-CS15 group		Dot L4-CS14 group		Dot L4-CS13 group		Dot L4-CS12 group		00h	
<b>Dot_grp_sel24</b>	024h	R/W	Reserved				Dot L4-CS17 group		Dot L4-CS16 group		00h	
<b>Dot_grp_sel25</b>	025h	R/W	Dot L5-CS3 group		Dot L5-CS2 group		Dot L5-CS1 group		Dot L5-CS0 group		00h	
<b>Dot_grp_sel26</b>	026h	R/W	Dot L5-CS7 group		Dot L5-CS6 group		Dot L5-CS5 group		Dot L5-CS4 group		00h	
<b>Dot_grp_sel27</b>	027h	R/W	Dot L5-CS11 group		Dot L5-CS10 group		Dot L5-CS9 group		Dot L5-CS8 group		00h	
<b>Dot_grp_sel28</b>	028h	R/W	Dot L5-CS15 group		Dot L5-CS14 group		Dot L5-CS13 group		Dot L5-CS12 group		00h	
<b>Dot_grp_sel29</b>	029h	R/W	Reserved				Dot L5-CS17 group		Dot L5-CS16 group		00h	
<b>Dot_onoff0</b>	043h	R/W	Dot L0-CS7 onoff	Dot L0-CS6 onoff	Dot L0-CS5 onoff	Dot L0-CS4 onoff	Dot L0-CS3 onoff	Dot L0-CS2 onoff	Dot L0-CS1 onoff	Dot L0-CS0 onoff	FFh	
<b>Dot_onoff1</b>	044h	R/W	Dot L0-CS15 onoff	Dot L0-CS14 onoff	Dot L0-CS13 onoff	Dot L0-CS12 onoff	Dot L0-CS11 onoff	Dot L0-CS10 onoff	Dot L0-CS9 onoff	Dot L0-CS8 onoff	FFh	
<b>Dot_onoff2</b>	045h	R/W	Reserved							Dot L0-CS17 onoff	Dot L0-CS16 onoff	03h
<b>Dot_onoff3</b>	046h	R/W	Dot L1-CS7 onoff	Dot L1-CS6 onoff	Dot L1-CS5 onoff	Dot L1-CS4 onoff	Dot L1-CS3 onoff	Dot L1-CS2 onoff	Dot L1-CS1 onoff	Dot L1-CS0 onoff	FFh	
<b>Dot_onoff4</b>	047h	R/W	Dot L1-CS15 onoff	Dot L1-CS14 onoff	Dot L1-CS13 onoff	Dot L1-CS12 onoff	Dot L1-CS11 onoff	Dot L1-CS10 onoff	Dot L1-CS9 onoff	Dot L1-CS8 onoff	FFh	

<b>Dot_onoff5</b>	048h	R/W	Reserved						Dot L1- CS17 onoff	Dot L1- CS16 onoff	03h
<b>Dot_onoff6</b>	049h	R/W	Dot L2- CS7 onoff	Dot L2- CS6 onoff	Dot L2- CS5 onoff	Dot L2- CS4 onoff	Dot L2- CS3 onoff	Dot L2- CS2 onoff	Dot L2- CS1 onoff	Dot L2- CS0 onoff	FFh
<b>Dot_onoff7</b>	04Ah	R/W	Dot L2- CS15 onoff	Dot L2- CS14 onoff	Dot L2- CS13 onoff	Dot L2- CS12 onoff	Dot L2- CS11 onoff	Dot L2- CS10 onoff	Dot L2- CS9 onoff	Dot L2- CS8 onoff	FFh
<b>Dot_onoff8</b>	04Bh	R/W	Reserved						Dot L2- CS17 onoff	Dot L2- CS16 onoff	03h
<b>Dot_onoff9</b>	04Ch	R/W	Dot L3- CS7 onoff	Dot L3- CS6 onoff	Dot L3- CS5 onoff	Dot L3- CS4 onoff	Dot L3- CS3 onoff	Dot L3- CS2 onoff	Dot L3- CS1 onoff	Dot L3- CS0 onoff	FFh
<b>Dot_onoff10</b>	04Dh	R/W	Dot L3- CS15 onoff	Dot L3- CS14 onoff	Dot L3- CS13 onoff	Dot L3- CS12 onoff	Dot L3- CS11 onoff	Dot L3- CS10 onoff	Dot L3- CS9 onoff	Dot L3- CS8 onoff	FFh
<b>Dot_onoff11</b>	04Eh	R/W	Reserved						Dot L3- CS17 onoff	Dot L3- CS16 onoff	03h
<b>Dot_onoff12</b>	04Fh	R/W	Dot L4- CS7 onoff	Dot L4- CS6 onoff	Dot L4- CS5 onoff	Dot L4- CS4 onoff	Dot L4- CS3 onoff	Dot L4- CS2 onoff	Dot L4- CS1 onoff	Dot L4- CS0 onoff	FFh
<b>Dot_onoff13</b>	050h	R/W	Dot L4- CS15 onoff	Dot L4- CS14 onoff	Dot L4- CS13 onoff	Dot L4- CS12 onoff	Dot L4- CS11 onoff	Dot L4- CS10 onoff	Dot L4- CS9 onoff	Dot L4- CS8 onoff	FFh
<b>Dot_onoff14</b>	051h	R/W	Reserved						Dot L4- CS17 onoff	Dot L4- CS16 onoff	03h
<b>Dot_onoff15</b>	052h	R/W	Dot L5- CS7 onoff	Dot L5- CS6 onoff	Dot L5- CS5 onoff	Dot L5- CS4 onoff	Dot L5- CS3 onoff	Dot L5- CS2 onoff	Dot L5- CS1 onoff	Dot L5- CS0 onoff	FFh
<b>Dot_onoff16</b>	053h	R/W	Dot L5- CS15 onoff	Dot L5- CS14 onoff	Dot L5- CS13 onoff	Dot L5- CS12 onoff	Dot L5- CS11 onoff	Dot L5- CS10 onoff	Dot L5- CS9 onoff	Dot L5- CS8 onoff	FFh
<b>Dot_onoff17</b>	054h	R/W	Reserved						Dot L5- CS17 onoff	Dot L5- CS16 onoff	03h
<b>Fault_state</b>	064h	R	Reserved						Global_L OD	Global_L SD	00h
<b>Dot_lod0</b>	065h	R	Dot L0- CS7 LOD	Dot L0- CS6 LOD	Dot L0- CS5 LOD	Dot L0- CS4 LOD	Dot L0- CS3 LOD	Dot L0- CS2 LOD	Dot L0- CS1 LOD	Dot L0- CS0 LOD	00h
<b>Dot_lod1</b>	066h	R	Dot L0- CS15 LOD	Dot L0- CS14 LOD	Dot L0- CS13 LOD	Dot L0- CS12 LOD	Dot L0- CS11 LOD	Dot L0- CS10 LOD	Dot L0- CS9 LOD	Dot L0- CS8 LOD	00h
<b>Dot_lod2</b>	067h	R	Reserved						Dot L0- CS17 LOD	Dot L0- CS16 LOD	00h
<b>Dot_lod3</b>	068h	R	Dot L1- CS7 LOD	Dot L1- CS6 LOD	Dot L1- CS5 LOD	Dot L1- CS4 LOD	Dot L1- CS3 LOD	Dot L1- CS2 LOD	Dot L1- CS1 LOD	Dot L1- CS0 LOD	00h
<b>Dot_lod4</b>	069h	R	Dot L1- CS15 LOD	Dot L1- CS14 LOD	Dot L1- CS13 LOD	Dot L1- CS12 LOD	Dot L1- CS11 LOD	Dot L1- CS10 LOD	Dot L1- CS9 LOD	Dot L1- CS8 LOD	00h
<b>Dot_lod5</b>	06Ah	R	Reserved						Dot L1- CS17 LOD	Dot L1- CS16 LOD	00h
<b>Dot_lod6</b>	06Bh	R	Dot L2- CS7 LOD	Dot L2- CS6 LOD	Dot L2- CS5 LOD	Dot L2- CS4 LOD	Dot L2- CS3 LOD	Dot L2- CS2 LOD	Dot L2- CS1 LOD	Dot L2- CS0 LOD	00h
<b>Dot_lod7</b>	06Ch	R	Dot L2- CS15 LOD	Dot L2- CS14 LOD	Dot L2- CS13 LOD	Dot L2- CS12 LOD	Dot L2- CS11 LOD	Dot L2- CS10 LOD	Dot L2- CS9 LOD	Dot L2- CS8 LOD	00h

<b>Dot_lod8</b>	06Dh	R	Reserved							Dot L2- CS17 LOD	Dot L2- CS16 LOD	00h
<b>Dot_lod9</b>	06Eh	R	Dot L3- CS7 LOD	Dot L3- CS6 LOD	Dot L3- CS5 LOD	Dot L3- CS4 LOD	Dot L3- CS3 LOD	Dot L3- CS2 LOD	Dot L3- CS1 LOD	Dot L3- CS0 LOD	00h	
<b>Dot_lod10</b>	06Fh	R	Dot L3- CS15 LOD	Dot L3- CS14 LOD	Dot L3- CS13 LOD	Dot L3- CS12 LOD	Dot L3- CS11 LOD	Dot L3- CS10 LOD	Dot L3- CS9 LOD	Dot L3- CS8 LOD	00h	
<b>Dot_lod11</b>	070h	R	Reserved							Dot L3- CS17 LOD	Dot L3- CS16 LOD	00h
<b>Dot_lod12</b>	071h	R	Dot L4- CS7 LOD	Dot L4- CS6 LOD	Dot L4- CS5 LOD	Dot L4- CS4 LOD	Dot L4- CS3 LOD	Dot L4- CS2 LOD	Dot L4- CS1 LOD	Dot L4- CS0 LOD	00h	
<b>Dot_lod13</b>	072h	R	Dot L4- CS15 LOD	Dot L4- CS14 LOD	Dot L4- CS13 LOD	Dot L4- CS12 LOD	Dot L4- CS11 LOD	Dot L4- CS10 LOD	Dot L4- CS9 LOD	Dot L4- CS8 LOD	00h	
<b>Dot_lod14</b>	073h	R	Reserved							Dot L4- CS17 LOD	Dot L4- CS16 LOD	00h
<b>Dot_lod15</b>	074h	R	Dot L5- CS7 LOD	Dot L5- CS6 LOD	Dot L5- CS5 LOD	Dot L5- CS4 LOD	Dot L5- CS3 LOD	Dot L5- CS2 LOD	Dot L5- CS1 LOD	Dot L5- CS0 LOD	00h	
<b>Dot_lod16</b>	075h	R	Dot L5- CS15 LOD	Dot L5- CS14 LOD	Dot L5- CS13 LOD	Dot L5- CS12 LOD	Dot L5- CS11 LOD	Dot L5- CS10 LOD	Dot L5- CS9 LOD	Dot L5- CS8 LOD	00h	
<b>Dot_lsd0</b>	086h	R	Dot L0- CS7 LSD	Dot L0- CS6 LSD	Dot L0- CS5 LSD	Dot L0- CS4 LSD	Dot L0- CS3 LSD	Dot L0- CS2 LSD	Dot L0- CS1 LSD	Dot L0- CS0 LSD	00h	
<b>Dot_lsd1</b>	087h	R	Dot L0- CS15 LSD	Dot L0- CS14 LSD	Dot L0- CS13 LSD	Dot L0- CS12 LSD	Dot L0- CS11 LSD	Dot L0- CS10 LSD	Dot L0- CS9 LSD	Dot L0- CS8 LSD	00h	
<b>Dot_lsd2</b>	088h	R	Reserved							Dot L0- CS17 LSD	Dot L0- CS16 LSD	00h
<b>Dot_lsd3</b>	089h	R	Dot L1- CS7 LSD	Dot L1- CS6 LSD	Dot L1- CS5 LSD	Dot L1- CS4 LSD	Dot L1- CS3 LSD	Dot L1- CS2 LSD	Dot L1- CS1 LSD	Dot L1- CS0 LSD	00h	
<b>Dot_lsd4</b>	08Ah	R	Dot L1- CS15 LSD	Dot L1- CS14 LSD	Dot L1- CS13 LSD	Dot L1- CS12 LSD	Dot L1- CS11 LSD	Dot L1- CS10 LSD	Dot L1- CS9 LSD	Dot L1- CS8 LSD	00h	
<b>Dot_lsd5</b>	08Bh	R	Reserved							Dot L1- CS17 LSD	Dot L1- CS16 LSD	00h
<b>Dot_lsd6</b>	08Ch	R	Dot L2- CS7 LSD	Dot L2- CS6 LSD	Dot L2- CS5 LSD	Dot L2- CS4 LSD	Dot L2- CS3 LSD	Dot L2- CS2 LSD	Dot L2- CS1 LSD	Dot L2- CS0 LSD	00h	
<b>Dot_lsd7</b>	08Dh	R	Dot L2- CS15 LSD	Dot L2- CS14 LSD	Dot L2- CS13 LSD	Dot L2- CS12 LSD	Dot L2- CS11 LSD	Dot L2- CS10 LSD	Dot L2- CS9 LSD	Dot L2- CS8 LSD	00h	
<b>Dot_lsd8</b>	08Eh	R	Reserved							Dot L2- CS17 LSD	Dot L2- CS16 LSD	00h
<b>Dot_lsd9</b>	08Fh	R	Dot L3- CS7 LSD	Dot L3- CS6 LSD	Dot L3- CS5 LSD	Dot L3- CS4 LSD	Dot L3- CS3 LSD	Dot L3- CS2 LSD	Dot L3- CS1 LSD	Dot L3- CS0 LSD	00h	
<b>Dot_lsd10</b>	090h	R	Dot L3- CS15 LSD	Dot L3- CS14 LSD	Dot L3- CS13 LSD	Dot L3- CS12 LSD	Dot L3- CS11 LSD	Dot L3- CS10 LSD	Dot L3- CS9 LSD	Dot L3- CS8 LSD	00h	
<b>Dot_lsd11</b>	091h	R	Reserved							Dot L3- CS17 LSD	Dot L3- CS16 LSD	00h
<b>Dot_lsd12</b>	092h	R	Dot L4- CS7 LSD	Dot L4- CS6 LSD	Dot L4- CS5 LSD	Dot L4- CS4 LSD	Dot L4- CS3 LSD	Dot L4- CS2 LSD	Dot L4- CS1 LSD	Dot L4- CS0 LSD	00h	

<b>Dot_Isd13</b>	093h	R	Dot L4- CS15 LSD	Dot L4- CS14 LSD	Dot L4- CS13 LSD	Dot L4- CS12 LSD	Dot L4- CS11 LSD	Dot L4- CS10 LSD	Dot L4- CS9 LSD	Dot L4- CS8 LSD	00h
<b>Dot_Isd14</b>	094h	R	Reserved						Dot L4- CS17 LSD	Dot L4- CS16 LSD	00h
<b>Dot_Isd15</b>	095h	R	Dot L5- CS7 LSD	Dot L5- CS6 LSD	Dot L5- CS5 LSD	Dot L5- CS4 LSD	Dot L5- CS3 LSD	Dot L5- CS2 LSD	Dot L5- CS1 LSD	Dot L5- CS0 LSD	00h
<b>Dot_Isd16</b>	096h	R	Dot L5- CS15 LSD	Dot L5- CS14 LSD	Dot L5- CS13 LSD	Dot L5- CS12 LSD	Dot L5- CS11 LSD	Dot L5- CS10 LSD	Dot L5- CS9 LSD	Dot L5- CS8 LSD	00h
<b>Dot_Isd17</b>	097h	R	Reserved						Dot L5- CS17 LSD	Dot L5- CS16 LSD	00h
<b>LOD_clear</b>	0A7h	W	Reserved				LOD_Clear				00h
<b>LSD_clear</b>	0A8h	W	Reserved				LSD_Clear				00h
<b>Reset</b>	0A9h	W	Reset								00h
<b>DC0</b>	100h	R/W	LED dot current setting for Dot L0-CS0								80h
<b>DC1</b>	101h	R/W	LED dot current setting for Dot L0-CS1								80h
<b>DC2</b>	102h	R/W	LED dot current setting for Dot L0-CS2								80h
<b>DC3</b>	103h	R/W	LED dot current setting for Dot L0-CS3								80h
<b>DC4</b>	104h	R/W	LED dot current setting for Dot L0-CS4								80h
<b>DC5</b>	105h	R/W	LED dot current setting for Dot L0-CS5								80h
<b>DC6</b>	106h	R/W	LED dot current setting for Dot L0-CS6								80h
<b>DC7</b>	107h	R/W	LED dot current setting for Dot L0-CS7								80h
<b>DC8</b>	108h	R/W	LED dot current setting for Dot L0-CS8								80h
<b>DC9</b>	109h	R/W	LED dot current setting for Dot L0-CS9								80h
<b>DC10</b>	10Ah	R/W	LED dot current setting for Dot L0-CS10								80h
<b>DC11</b>	10Bh	R/W	LED dot current setting for Dot L0-CS11								80h
<b>DC12</b>	10Ch	R/W	LED dot current setting for Dot L0-CS12								80h
<b>DC13</b>	10Dh	R/W	LED dot current setting for Dot L0-CS13								80h
<b>DC14</b>	10Eh	R/W	LED dot current setting for Dot L0-CS14								80h
<b>DC15</b>	10Fh	R/W	LED dot current setting for Dot L0-CS15								80h
<b>DC16</b>	110h	R/W	LED dot current setting for Dot L0-CS16								80h
<b>DC17</b>	111h	R/W	LED dot current setting for Dot L0-CS17								80h
<b>DC18</b>	112h	R/W	LED dot current setting for Dot L1-CS0								80h
<b>DC19</b>	113h	R/W	LED dot current setting for Dot L1-CS1								80h
<b>DC20</b>	114h	R/W	LED dot current setting for Dot L1-CS2								80h
<b>DC21</b>	115h	R/W	LED dot current setting for Dot L1-CS3								80h
<b>DC22</b>	116h	R/W	LED dot current setting for Dot L1-CS4								80h
<b>DC23</b>	117h	R/W	LED dot current setting for Dot L1-CS5								80h
<b>DC24</b>	118h	R/W	LED dot current setting for Dot L1-CS6								80h
<b>DC25</b>	119h	R/W	LED dot current setting for Dot L1-CS7								80h
<b>DC26</b>	11Ah	R/W	LED dot current setting for Dot L1-CS8								80h
<b>DC27</b>	11Bh	R/W	LED dot current setting for Dot L1-CS9								80h
<b>DC28</b>	11Ch	R/W	LED dot current setting for Dot L1-CS10								80h
<b>DC29</b>	11Dh	R/W	LED dot current setting for Dot L1-CS11								80h
<b>DC30</b>	11Eh	R/W	LED dot current setting for Dot L1-CS12								80h
<b>DC31</b>	11Fh	R/W	LED dot current setting for Dot L1-CS13								80h
<b>DC32</b>	120h	R/W	LED dot current setting for Dot L1-CS14								80h



DC33	121h	R/W	LED dot current setting for Dot L1-CS15	80h
DC34	122h	R/W	LED dot current setting for Dot L1-CS16	80h
DC35	123h	R/W	LED dot current setting for Dot L1-CS17	80h
DC36	124h	R/W	LED dot current setting for Dot L2-CS0	80h
DC37	125h	R/W	LED dot current setting for Dot L2-CS1	80h
DC38	126h	R/W	LED dot current setting for Dot L2-CS2	80h
DC39	127h	R/W	LED dot current setting for Dot L2-CS3	80h
DC40	128h	R/W	LED dot current setting for Dot L2-CS4	80h
DC41	129h	R/W	LED dot current setting for Dot L2-CS5	80h
DC42	12Ah	R/W	LED dot current setting for Dot L2-CS6	80h
DC43	12Bh	R/W	LED dot current setting for Dot L2-CS7	80h
DC44	12Ch	R/W	LED dot current setting for Dot L2-CS8	80h
DC45	12Dh	R/W	LED dot current setting for Dot L2-CS9	80h
DC46	12Eh	R/W	LED dot current setting for Dot L2-CS10	80h
DC47	12Fh	R/W	LED dot current setting for Dot L2-CS11	80h
DC48	130h	R/W	LED dot current setting for Dot L2-CS12	80h
DC49	131h	R/W	LED dot current setting for Dot L2-CS13	80h
DC50	132h	R/W	LED dot current setting for Dot L2-CS14	80h
DC51	133h	R/W	LED dot current setting for Dot L2-CS15	80h
DC52	134h	R/W	LED dot current setting for Dot L2-CS16	80h
DC53	135h	R/W	LED dot current setting for Dot L2-CS17	80h
DC54	136h	R/W	LED dot current setting for Dot L3-CS0	80h
DC55	137h	R/W	LED dot current setting for Dot L3-CS1	80h
DC56	138h	R/W	LED dot current setting for Dot L3-CS2	80h
DC57	139h	R/W	LED dot current setting for Dot L3-CS3	80h
DC58	13Ah	R/W	LED dot current setting for Dot L3-CS4	80h
DC59	13Bh	R/W	LED dot current setting for Dot L3-CS5	80h
DC60	13Ch	R/W	LED dot current setting for Dot L3-CS6	80h
DC61	13Dh	R/W	LED dot current setting for Dot L3-CS7	80h
DC62	13Eh	R/W	LED dot current setting for Dot L3-CS8	80h
DC63	13Fh	R/W	LED dot current setting for Dot L3-CS9	80h
DC64	140h	R/W	LED dot current setting for Dot L3-CS10	80h
DC65	141h	R/W	LED dot current setting for Dot L3-CS11	80h
DC66	142h	R/W	LED dot current setting for Dot L3-CS12	80h
DC67	143h	R/W	LED dot current setting for Dot L3-CS13	80h
DC68	144h	R/W	LED dot current setting for Dot L3-CS14	80h
DC69	145h	R/W	LED dot current setting for Dot L3-CS15	80h
DC70	146h	R/W	LED dot current setting for Dot L3-CS16	80h
DC71	147h	R/W	LED dot current setting for Dot L3-CS17	80h
DC72	148h	R/W	LED dot current setting for Dot L4-CS0	80h
DC73	149h	R/W	LED dot current setting for Dot L4-CS1	80h
DC74	14Ah	R/W	LED dot current setting for Dot L4-CS2	80h
DC75	14Bh	R/W	LED dot current setting for Dot L4-CS3	80h
DC76	14Ch	R/W	LED dot current setting for Dot L4-CS4	80h
DC77	14Dh	R/W	LED dot current setting for Dot L4-CS5	80h
DC78	14Eh	R/W	LED dot current setting for Dot L4-CS6	80h
DC79	14Fh	R/W	LED dot current setting for Dot L4-CS7	80h

<b>DC80</b>	150h	R/W	LED dot current setting for Dot L4-CS8	80h
<b>DC81</b>	151h	R/W	LED dot current setting for Dot L4-CS9	80h
<b>DC82</b>	152h	R/W	LED dot current setting for Dot L4-CS10	80h
<b>DC83</b>	153h	R/W	LED dot current setting for Dot L4-CS11	80h
<b>DC84</b>	154h	R/W	LED dot current setting for Dot L4-CS12	80h
<b>DC85</b>	155h	R/W	LED dot current setting for Dot L4-CS13	80h
<b>DC86</b>	156h	R/W	LED dot current setting for Dot L4-CS14	80h
<b>DC87</b>	157h	R/W	LED dot current setting for Dot L4-CS15	80h
<b>DC88</b>	158h	R/W	LED dot current setting for Dot L4-CS16	80h
<b>DC89</b>	159h	R/W	LED dot current setting for Dot L4-CS17	80h
<b>DC90</b>	15Ah	R/W	LED dot current setting for Dot L5-CS0	80h
<b>DC91</b>	15Bh	R/W	LED dot current setting for Dot L5-CS1	80h
<b>DC92</b>	15Ch	R/W	LED dot current setting for Dot L5-CS2	80h
<b>DC93</b>	15Dh	R/W	LED dot current setting for Dot L5-CS3	80h
<b>DC94</b>	15Eh	R/W	LED dot current setting for Dot L5-CS4	80h
<b>DC95</b>	15Fh	R/W	LED dot current setting for Dot L5-CS5	80h
<b>DC96</b>	160h	R/W	LED dot current setting for Dot L5-CS6	80h
<b>DC97</b>	161h	R/W	LED dot current setting for Dot L5-CS7	80h
<b>DC98</b>	162h	R/W	LED dot current setting for Dot L5-CS8	80h
<b>DC99</b>	163h	R/W	LED dot current setting for Dot L5-CS9	80h
<b>DC100</b>	164h	R/W	LED dot current setting for Dot L5-CS10	80h
<b>DC101</b>	165h	R/W	LED dot current setting for Dot L5-CS11	80h
<b>DC102</b>	166h	R/W	LED dot current setting for Dot L5-CS12	80h
<b>DC103</b>	167h	R/W	LED dot current setting for Dot L5-CS13	80h
<b>DC104</b>	168h	R/W	LED dot current setting for Dot L5-CS14	80h
<b>DC105</b>	169h	R/W	LED dot current setting for Dot L5-CS15	80h
<b>DC106</b>	16Ah	R/W	LED dot current setting for Dot L5-CS16	80h
<b>DC107</b>	16Bh	R/W	LED dot current setting for Dot L5-CS17	80h
<b>pwm_bri0</b>	200h	R/W	8-bits PWM for Dot L0-CS0 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS0	00h
<b>pwm_bri1</b>	201h	R/W	8-bits PWM for Dot L0-CS1 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS0	00h
<b>pwm_bri2</b>	202h	R/W	8-bits PWM for Dot L0-CS2 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS1	00h
<b>pwm_bri3</b>	203h	R/W	8-bits PWM for Dot L0-CS3 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS1	00h
<b>pwm_bri4</b>	204h	R/W	8-bits PWM for Dot L0-CS4 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS2	00h
<b>pwm_bri5</b>	205h	R/W	8-bits PWM for Dot L0-CS5 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS2	00h
<b>pwm_bri6</b>	206h	R/W	8-bits PWM for Dot L0-CS6 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS3	00h
<b>pwm_bri7</b>	207h	R/W	8-bits PWM for Dot L0-CS7 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS3	00h
<b>pwm_bri8</b>	208h	R/W	8-bits PWM for Dot L0-CS8 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS4	00h
<b>pwm_bri9</b>	209h	R/W	8-bits PWM for Dot L0-CS9 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS4	00h
<b>pwm_bri10</b>	20Ah	R/W	8-bits PWM for Dot L0-CS10 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS5	00h
<b>pwm_bri11</b>	20Bh	R/W	8-bits PWM for Dot L0-CS11 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS5	00h
<b>pwm_bri12</b>	20Ch	R/W	8-bits PWM for Dot L0-CS12 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS6	00h
<b>pwm_bri13</b>	20Dh	R/W	8-bits PWM for Dot L0-CS13 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS6	00h
<b>pwm_bri14</b>	20Eh	R/W	8-bits PWM for Dot L0-CS14 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS7	00h
<b>pwm_bri15</b>	20Fh	R/W	8-bits PWM for Dot L0-CS15 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS7	00h
<b>pwm_bri16</b>	210h	R/W	8-bits PWM for Dot L0-CS16 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS8	00h
<b>pwm_bri17</b>	211h	R/W	8-bits PWM for Dot L0-CS17 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS8	00h
<b>pwm_bri18</b>	212h	R/W	8-bits PWM for Dot L1-CS0 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS9	00h

pwm_bri19	213h	R/W	8-bits PWM for Dot L1-CS1 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS9	00h
pwm_bri20	214h	R/W	8-bits PWM for Dot L1-CS2 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS10	00h
pwm_bri21	215h	R/W	8-bits PWM for Dot L1-CS3 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS10	00h
pwm_bri22	216h	R/W	8-bits PWM for Dot L1-CS4 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS11	00h
pwm_bri23	217h	R/W	8-bits PWM for Dot L1-CS5 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS11	00h
pwm_bri24	218h	R/W	8-bits PWM for Dot L1-CS6 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS12	00h
pwm_bri25	219h	R/W	8-bits PWM for Dot L1-CS7 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS12	00h
pwm_bri26	21Ah	R/W	8-bits PWM for Dot L1-CS8 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS13	00h
pwm_bri27	21Bh	R/W	8-bits PWM for Dot L1-CS9 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS13	00h
pwm_bri28	21Ch	R/W	8-bits PWM for Dot L1-CS10 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS14	00h
pwm_bri29	21Dh	R/W	8-bits PWM for Dot L1-CS11 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS14	00h
pwm_bri30	21Eh	R/W	8-bits PWM for Dot L1-CS12 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS15	00h
pwm_bri31	21Fh	R/W	8-bits PWM for Dot L1-CS13 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS15	00h
pwm_bri32	220h	R/W	8-bits PWM for Dot L1-CS14 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS16	00h
pwm_bri33	221h	R/W	8-bits PWM for Dot L1-CS15 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS16	00h
pwm_bri34	222h	R/W	8-bits PWM for Dot L1-CS16 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS17	00h
pwm_bri35	223h	R/W	8-bits PWM for Dot L1-CS17 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS17	00h
pwm_bri36	224h	R/W	8-bits PWM for Dot L2-CS0 OR 16-bits PWM lower 8 bits [7:0] for Dot L1-CS0	00h
pwm_bri37	225h	R/W	8-bits PWM for Dot L2-CS1 OR 16-bits PWM higher 8 bits [15:8] for Dot L1-CS0	00h
pwm_bri38	226h	R/W	8-bits PWM for Dot L2-CS2 OR 16-bits PWM lower 8 bits [7:0] for Dot L1-CS1	00h
pwm_bri39	227h	R/W	8-bits PWM for Dot L2-CS3 OR 16-bits PWM higher 8 bits [15:8] for Dot L1-CS1	00h
pwm_bri40	228h	R/W	8-bits PWM for Dot L2-CS4 OR 16-bits PWM lower 8 bits [7:0] for Dot L1-CS2	00h
pwm_bri41	229h	R/W	8-bits PWM for Dot L2-CS5 OR 16-bits PWM higher 8 bits [15:8] for Dot L1-CS2	00h
pwm_bri42	22Ah	R/W	8-bits PWM for Dot L2-CS6 OR 16-bits PWM lower 8 bits [7:0] for Dot L1-CS3	00h
pwm_bri43	22Bh	R/W	8-bits PWM for Dot L2-CS7 OR 16-bits PWM higher 8 bits [15:8] for Dot L1-CS3	00h
pwm_bri44	22Ch	R/W	8-bits PWM for Dot L2-CS8 OR 16-bits PWM lower 8 bits [7:0] for Dot L1-CS4	00h
pwm_bri45	22Dh	R/W	8-bits PWM for Dot L2-CS9 OR 16-bits PWM higher 8 bits [15:8] for Dot L1-CS4	00h
pwm_bri46	22Eh	R/W	8-bits PWM for Dot L2-CS10 OR 16-bits PWM lower 8 bits [7:0] for Dot L1-CS5	00h
pwm_bri47	22Fh	R/W	8-bits PWM for Dot L2-CS11 OR 16-bits PWM higher 8 bits [15:8] for Dot L1-CS5	00h
pwm_bri48	230h	R/W	8-bits PWM for Dot L2-CS12 OR 16-bits PWM lower 8 bits [7:0] for Dot L1-CS6	00h
pwm_bri49	231h	R/W	8-bits PWM for Dot L2-CS13 OR 16-bits PWM higher 8 bits [15:8] for Dot L1-CS6	00h
pwm_bri50	232h	R/W	8-bits PWM for Dot L2-CS14 OR 16-bits PWM lower 8 bits [7:0] for Dot L1-CS7	00h
pwm_bri51	233h	R/W	8-bits PWM for Dot L2-CS15 OR 16-bits PWM higher 8 bits [15:8] for Dot L1-CS7	00h
pwm_bri52	234h	R/W	8-bits PWM for Dot L2-CS16 OR 16-bits PWM lower 8 bits [7:0] for Dot L1-CS8	00h
pwm_bri53	235h	R/W	8-bits PWM for Dot L2-CS17 OR 16-bits PWM higher 8 bits [15:8] for Dot L1-CS8	00h
pwm_bri54	236h	R/W	8-bits PWM for Dot L3-CS0 OR 16-bits PWM lower 8 bits [7:0] for Dot L1-CS9	00h
pwm_bri55	237h	R/W	8-bits PWM for Dot L3-CS1 OR 16-bits PWM higher 8 bits [15:8] for Dot L1-CS9	00h
pwm_bri56	238h	R/W	8-bits PWM for Dot L3-CS2 OR 16-bits PWM lower 8 bits [7:0] for Dot L1-CS10	00h
pwm_bri57	239h	R/W	8-bits PWM for Dot L3-CS3 OR 16-bits PWM higher 8 bits [15:8] for Dot L1-CS10	00h
pwm_bri58	23Ah	R/W	8-bits PWM for Dot L3-CS4 OR 16-bits PWM lower 8 bits [7:0] for Dot L1-CS11	00h
pwm_bri59	23Bh	R/W	8-bits PWM for Dot L3-CS5 OR 16-bits PWM higher 8 bits [15:8] for Dot L1-CS11	00h
pwm_bri60	23Ch	R/W	8-bits PWM for Dot L3-CS6 OR 16-bits PWM lower 8 bits [7:0] for Dot L1-CS12	00h
pwm_bri61	23Dh	R/W	8-bits PWM for Dot L3-CS7 OR 16-bits PWM higher 8 bits [15:8] for Dot L1-CS12	00h
pwm_bri62	23Eh	R/W	8-bits PWM for Dot L3-CS8 OR 16-bits PWM lower 8 bits [7:0] for Dot L1-CS13	00h
pwm_bri63	23Fh	R/W	8-bits PWM for Dot L3-CS9 OR 16-bits PWM higher 8 bits [15:8] for Dot L1-CS13	00h
pwm_bri64	240h	R/W	8-bits PWM for Dot L3-CS10 OR 16-bits PWM lower 8 bits [7:0] for Dot L1-CS14	00h
pwm_bri65	241h	R/W	8-bits PWM for Dot L3-CS11 OR 16-bits PWM higher 8 bits [15:8] for Dot L1-CS14	00h

<b>pwm_bri66</b>	242h	R/W	8-bits PWM for Dot L3-CS12 OR 16-bits PWM lower 8 bits [7:0] for Dot L1-CS15	00h
<b>pwm_bri67</b>	243h	R/W	8-bits PWM for Dot L3-CS13 OR 16-bits PWM higher 8 bits [15:8] for Dot L1-CS15	00h
<b>pwm_bri68</b>	244h	R/W	8-bits PWM for Dot L3-CS14 OR 16-bits PWM lower 8 bits [7:0] for Dot L1-CS16	00h
<b>pwm_bri69</b>	245h	R/W	8-bits PWM for Dot L3-CS15 OR 16-bits PWM higher 8 bits [15:8] for Dot L1-CS16	00h
<b>pwm_bri70</b>	246h	R/W	8-bits PWM for Dot L3-CS16 OR 16-bits PWM lower 8 bits [7:0] for Dot L1-CS17	00h
<b>pwm_bri71</b>	247h	R/W	8-bits PWM for Dot L3-CS17 OR 16-bits PWM higher 8 bits [15:8] for Dot L1-CS17	00h
<b>pwm_bri72</b>	248h	R/W	8-bits PWM for Dot L4-CS0 OR 16-bits PWM lower 8 bits [7:0] for Dot L2-CS0	00h
<b>pwm_bri73</b>	249h	R/W	8-bits PWM for Dot L4-CS1 OR 16-bits PWM higher 8 bits [15:8] for Dot L2-CS0	00h
<b>pwm_bri74</b>	24Ah	R/W	8-bits PWM for Dot L4-CS2 OR 16-bits PWM lower 8 bits [7:0] for Dot L2-CS1	00h
<b>pwm_bri75</b>	24Bh	R/W	8-bits PWM for Dot L4-CS3 OR 16-bits PWM higher 8 bits [15:8] for Dot L2-CS1	00h
<b>pwm_bri76</b>	24Ch	R/W	8-bits PWM for Dot L4-CS4 OR 16-bits PWM lower 8 bits [7:0] for Dot L2-CS2	00h
<b>pwm_bri77</b>	24Dh	R/W	8-bits PWM for Dot L4-CS5 OR 16-bits PWM higher 8 bits [15:8] for Dot L2-CS2	00h
<b>pwm_bri78</b>	24Eh	R/W	8-bits PWM for Dot L4-CS6 OR 16-bits PWM lower 8 bits [7:0] for Dot L2-CS3	00h
<b>pwm_bri79</b>	24Fh	R/W	8-bits PWM for Dot L4-CS7 OR 16-bits PWM higher 8 bits [15:8] for Dot L2-CS3	00h
<b>pwm_bri80</b>	250h	R/W	8-bits PWM for Dot L4-CS8 OR 16-bits PWM lower 8 bits [7:0] for Dot L2-CS4	00h
<b>pwm_bri81</b>	251h	R/W	8-bits PWM for Dot L4-CS9 OR 16-bits PWM higher 8 bits [15:8] for Dot L2-CS4	00h
<b>pwm_bri82</b>	252h	R/W	8-bits PWM for Dot L4-CS10 OR 16-bits PWM lower 8 bits [7:0] for Dot L2-CS5	00h
<b>pwm_bri83</b>	253h	R/W	8-bits PWM for Dot L4-CS11 OR 16-bits PWM higher 8 bits [15:8] for Dot L2-CS5	00h
<b>pwm_bri84</b>	254h	R/W	8-bits PWM for Dot L4-CS12 OR 16-bits PWM lower 8 bits [7:0] for Dot L2-CS6	00h
<b>pwm_bri85</b>	255h	R/W	8-bits PWM for Dot L4-CS13 OR 16-bits PWM higher 8 bits [15:8] for Dot L2-CS6	00h
<b>pwm_bri86</b>	256h	R/W	8-bits PWM for Dot L4-CS14 OR 16-bits PWM lower 8 bits [7:0] for Dot L2-CS7	00h
<b>pwm_bri87</b>	257h	R/W	8-bits PWM for Dot L4-CS15 OR 16-bits PWM higher 8 bits [15:8] for Dot L2-CS7	00h
<b>pwm_bri88</b>	258h	R/W	8-bits PWM for Dot L4-CS16 OR 16-bits PWM lower 8 bits [7:0] for Dot L2-CS8	00h
<b>pwm_bri89</b>	259h	R/W	8-bits PWM for Dot L4-CS17 OR 16-bits PWM higher 8 bits [15:8] for Dot L2-CS8	00h
<b>pwm_bri90</b>	25Ah	R/W	8-bits PWM for Dot L5-CS0 OR 16-bits PWM lower 8 bits [7:0] for Dot L2-CS9	00h
<b>pwm_bri91</b>	25Bh	R/W	8-bits PWM for Dot L5-CS1 OR 16-bits PWM higher 8 bits [15:8] for Dot L2-CS9	00h
<b>pwm_bri92</b>	25Ch	R/W	8-bits PWM for Dot L5-CS2 OR 16-bits PWM lower 8 bits [7:0] for Dot L2-CS10	00h
<b>pwm_bri93</b>	25Dh	R/W	8-bits PWM for Dot L5-CS3 OR 16-bits PWM higher 8 bits [15:8] for Dot L2-CS10	00h
<b>pwm_bri94</b>	25Eh	R/W	8-bits PWM for Dot L5-CS4 OR 16-bits PWM lower 8 bits [7:0] for Dot L2-CS11	00h
<b>pwm_bri95</b>	25Fh	R/W	8-bits PWM for Dot L5-CS5 OR 16-bits PWM higher 8 bits [15:8] for Dot L2-CS11	00h
<b>pwm_bri96</b>	260h	R/W	8-bits PWM for Dot L5-CS6 OR 16-bits PWM lower 8 bits [7:0] for Dot L2-CS12	00h
<b>pwm_bri97</b>	261h	R/W	8-bits PWM for Dot L5-CS7 OR 16-bits PWM higher 8 bits [15:8] for Dot L2-CS12	00h
<b>pwm_bri98</b>	262h	R/W	8-bits PWM for Dot L5-CS8 OR 16-bits PWM lower 8 bits [7:0] for Dot L2-CS13	00h
<b>pwm_bri99</b>	263h	R/W	8-bits PWM for Dot L5-CS9 OR 16-bits PWM higher 8 bits [15:8] for Dot L2-CS13	00h
<b>pwm_bri100</b>	264h	R/W	8-bits PWM for Dot L5-CS10 OR 16-bits PWM lower 8 bits [7:0] for Dot L2-CS14	00h
<b>pwm_bri101</b>	265h	R/W	8-bits PWM for Dot L5-CS11 OR 16-bits PWM higher 8 bits [15:8] for Dot L2-CS14	00h
<b>pwm_bri102</b>	266h	R/W	8-bits PWM for Dot L5-CS12 OR 16-bits PWM lower 8 bits [7:0] for Dot L2-CS15	00h
<b>pwm_bri103</b>	267h	R/W	8-bits PWM for Dot L5-CS13 OR 16-bits PWM higher 8 bits [15:8] for Dot L2-CS15	00h
<b>pwm_bri104</b>	268h	R/W	8-bits PWM for Dot L5-CS14 OR 16-bits PWM lower 8 bits [7:0] for Dot L2-CS16	00h
<b>pwm_bri105</b>	269h	R/W	8-bits PWM for Dot L5-CS15 OR 16-bits PWM higher 8 bits [15:8] for Dot L2-CS16	00h
<b>pwm_bri106</b>	26Ah	R/W	8-bits PWM for Dot L5-CS16 OR 16-bits PWM lower 8 bits [7:0] for Dot L2-CS17	00h
<b>pwm_bri107</b>	26Bh	R/W	8-bits PWM for Dot L5-CS17 OR 16-bits PWM higher 8 bits [15:8] for Dot L2-CS17	00h
<b>pwm_bri108</b>	26Ch	R/W	16-bits PWM lower 8 bits [7:0] for Dot L3-CS0	00h
<b>pwm_bri109</b>	26Dh	R/W	16-bits PWM higher 8 bits [15:8] for Dot L3-CS0	00h
<b>pwm_bri110</b>	26Eh	R/W	16-bits PWM lower 8 bits [7:0] for Dot L3-CS1	00h
<b>pwm_bri111</b>	26Fh	R/W	16-bits PWM higher 8 bits [15:8] for Dot L3-CS1	00h
<b>pwm_bri112</b>	270h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L3-CS2	00h

<b>pwm_bri113</b>	271h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L3-CS2	00h
<b>pwm_bri114</b>	272h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L3-CS3	00h
<b>pwm_bri115</b>	273h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L3-CS3	00h
<b>pwm_bri116</b>	274h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L3-CS4	00h
<b>pwm_bri117</b>	275h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L3-CS4	00h
<b>pwm_bri118</b>	276h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L3-CS5	00h
<b>pwm_bri119</b>	277h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L3-CS5	00h
<b>pwm_bri120</b>	278h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L3-CS6	00h
<b>pwm_bri121</b>	279h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L3-CS6	00h
<b>pwm_bri122</b>	27Ah	R/W	16-bits PWM lower 8 bits [7:0] for Dot L3-CS7	00h
<b>pwm_bri123</b>	27Bh	R/W	16-bits PWM higher 8 bits [15:8] for Dot L3-CS7	00h
<b>pwm_bri124</b>	27Ch	R/W	16-bits PWM lower 8 bits [7:0] for Dot L3-CS8	00h
<b>pwm_bri125</b>	27Dh	R/W	16-bits PWM higher 8 bits [15:8] for Dot L3-CS8	00h
<b>pwm_bri126</b>	27Eh	R/W	16-bits PWM lower 8 bits [7:0] for Dot L3-CS9	00h
<b>pwm_bri127</b>	27Fh	R/W	16-bits PWM higher 8 bits [15:8] for Dot L3-CS9	00h
<b>pwm_bri128</b>	280h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L3-CS10	00h
<b>pwm_bri129</b>	281h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L3-CS10	00h
<b>pwm_bri130</b>	282h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L3-CS11	00h
<b>pwm_bri131</b>	283h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L3-CS11	00h
<b>pwm_bri132</b>	284h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L3-CS12	00h
<b>pwm_bri133</b>	285h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L3-CS12	00h
<b>pwm_bri134</b>	286h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L3-CS13	00h
<b>pwm_bri135</b>	287h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L3-CS13	00h
<b>pwm_bri136</b>	288h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L3-CS14	00h
<b>pwm_bri137</b>	289h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L3-CS14	00h
<b>pwm_bri138</b>	28Ah	R/W	16-bits PWM lower 8 bits [7:0] for Dot L3-CS15	00h
<b>pwm_bri139</b>	28Bh	R/W	16-bits PWM higher 8 bits [15:8] for Dot L3-CS15	00h
<b>pwm_bri140</b>	28Ch	R/W	16-bits PWM lower 8 bits [7:0] for Dot L3-CS16	00h
<b>pwm_bri141</b>	28Dh	R/W	16-bits PWM higher 8 bits [15:8] for Dot L3-CS16	00h
<b>pwm_bri142</b>	28Eh	R/W	16-bits PWM lower 8 bits [7:0] for Dot L3-CS17	00h
<b>pwm_bri143</b>	28Fh	R/W	16-bits PWM higher 8 bits [15:8] for Dot L3-CS17	00h
<b>pwm_bri144</b>	290h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L4-CS0	00h
<b>pwm_bri145</b>	291h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L4-CS0	00h
<b>pwm_bri146</b>	292h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L4-CS1	00h
<b>pwm_bri147</b>	293h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L4-CS1	00h
<b>pwm_bri148</b>	294h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L4-CS2	00h
<b>pwm_bri149</b>	295h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L4-CS2	00h
<b>pwm_bri150</b>	296h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L4-CS3	00h
<b>pwm_bri151</b>	297h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L4-CS3	00h
<b>pwm_bri152</b>	298h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L4-CS4	00h
<b>pwm_bri153</b>	299h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L4-CS4	00h
<b>pwm_bri154</b>	29Ah	R/W	16-bits PWM lower 8 bits [7:0] for Dot L4-CS5	00h
<b>pwm_bri155</b>	29Bh	R/W	16-bits PWM higher 8 bits [15:8] for Dot L4-CS5	00h
<b>pwm_bri156</b>	29Ch	R/W	16-bits PWM lower 8 bits [7:0] for Dot L4-CS6	00h
<b>pwm_bri157</b>	29Dh	R/W	16-bits PWM higher 8 bits [15:8] for Dot L4-CS6	00h
<b>pwm_bri158</b>	29Eh	R/W	16-bits PWM lower 8 bits [7:0] for Dot L4-CS7	00h
<b>pwm_bri159</b>	29Fh	R/W	16-bits PWM higher 8 bits [15:8] for Dot L4-CS7	00h



<b>pwm_bri160</b>	2A0h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L4-CS8	00h
<b>pwm_bri161</b>	2A1h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L4-CS8	00h
<b>pwm_bri162</b>	2A2h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L4-CS9	00h
<b>pwm_bri163</b>	2A3h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L4-CS9	00h
<b>pwm_bri164</b>	2A4h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L4-CS10	00h
<b>pwm_bri165</b>	2A5h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L4-CS10	00h
<b>pwm_bri166</b>	2A6h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L4-CS11	00h
<b>pwm_bri167</b>	2A7h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L4-CS11	00h
<b>pwm_bri168</b>	2A8h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L4-CS12	00h
<b>pwm_bri169</b>	2A9h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L4-CS12	00h
<b>pwm_bri170</b>	2AAh	R/W	16-bits PWM lower 8 bits [7:0] for Dot L4-CS13	00h
<b>pwm_bri171</b>	2ABh	R/W	16-bits PWM higher 8 bits [15:8] for Dot L4-CS13	00h
<b>pwm_bri172</b>	2ACh	R/W	16-bits PWM lower 8 bits [7:0] for Dot L4-CS14	00h
<b>pwm_bri173</b>	2ADh	R/W	16-bits PWM higher 8 bits [15:8] for Dot L4-CS14	00h
<b>pwm_bri174</b>	2AEh	R/W	16-bits PWM lower 8 bits [7:0] for Dot L4-CS15	00h
<b>pwm_bri175</b>	2AFh	R/W	16-bits PWM higher 8 bits [15:8] for Dot L4-CS15	00h
<b>pwm_bri176</b>	2B0h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L4-CS16	00h
<b>pwm_bri177</b>	2B1h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L4-CS16	00h
<b>pwm_bri178</b>	2B2h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L4-CS17	00h
<b>pwm_bri179</b>	2B3h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L4-CS17	00h
<b>pwm_bri180</b>	2B4h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L5-CS0	00h
<b>pwm_bri181</b>	2B5h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L5-CS0	00h
<b>pwm_bri182</b>	2B6h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L5-CS1	00h
<b>pwm_bri183</b>	2B7h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L5-CS1	00h
<b>pwm_bri184</b>	2B8h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L5-CS2	00h
<b>pwm_bri185</b>	2B9h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L5-CS2	00h
<b>pwm_bri186</b>	2BAh	R/W	16-bits PWM lower 8 bits [7:0] for Dot L5-CS3	00h
<b>pwm_bri187</b>	2BBh	R/W	16-bits PWM higher 8 bits [15:8] for Dot L5-CS3	00h
<b>pwm_bri188</b>	2BCh	R/W	16-bits PWM lower 8 bits [7:0] for Dot L5-CS4	00h
<b>pwm_bri189</b>	2BDh	R/W	16-bits PWM higher 8 bits [15:8] for Dot L5-CS4	00h
<b>pwm_bri190</b>	2BEh	R/W	16-bits PWM lower 8 bits [7:0] for Dot L5-CS5	00h
<b>pwm_bri191</b>	2BFh	R/W	16-bits PWM higher 8 bits [15:8] for Dot L5-CS5	00h
<b>pwm_bri192</b>	2C0h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L5-CS6	00h
<b>pwm_bri193</b>	2C1h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L5-CS6	00h
<b>pwm_bri194</b>	2C2h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L5-CS7	00h
<b>pwm_bri195</b>	2C3h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L5-CS7	00h
<b>pwm_bri196</b>	2C4h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L5-CS8	00h
<b>pwm_bri197</b>	2C5h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L5-CS8	00h
<b>pwm_bri198</b>	2C6h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L5-CS9	00h
<b>pwm_bri199</b>	2C7h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L5-CS9	00h
<b>pwm_bri200</b>	2C8h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L5-CS10	00h
<b>pwm_bri201</b>	2C9h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L5-CS10	00h
<b>pwm_bri202</b>	2CAh	R/W	16-bits PWM lower 8 bits [7:0] for Dot L5-CS11	00h
<b>pwm_bri203</b>	2CBh	R/W	16-bits PWM higher 8 bits [15:8] for Dot L5-CS11	00h
<b>pwm_bri204</b>	2CCh	R/W	16-bits PWM lower 8 bits [7:0] for Dot L5-CS12	00h
<b>pwm_bri205</b>	2CDh	R/W	16-bits PWM higher 8 bits [15:8] for Dot L5-CS12	00h
<b>pwm_bri206</b>	2CEh	R/W	16-bits PWM lower 8 bits [7:0] for Dot L5-CS13	00h

<b>pwm_bri207</b>	2CFh	R/W	16-bits PWM higher 8 bits [15:8] for Dot L5-CS13	00h
<b>pwm_bri208</b>	2D0h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L5-CS14	00h
<b>pwm_bri209</b>	2D1h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L5-CS14	00h
<b>pwm_bri210</b>	2D2h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L5-CS15	00h
<b>pwm_bri211</b>	2D3h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L5-CS15	00h
<b>pwm_bri212</b>	2D4h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L5-CS16	00h
<b>pwm_bri213</b>	2D5h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L5-CS16	00h
<b>pwm_bri214</b>	2D6h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L5-CS17	00h
<b>pwm_bri215</b>	2D7h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L5-CS17	00h

## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

The LP5866 integrates 18 constant current sinks with 6 switching FETs and one LP5866 can drive up to 108 LED dots or 36 RGB pixels and achieve great dimming effect. In smart home, gaming keyboards, and other human-machine interaction applications, the device can greatly improve user experience with a small amount of components.

### 8.2 Typical Application

#### 8.2.1 Application

Figure 8-1 shows an example of typical application, which uses one LP5866 to drive 36 common-anode RGB LEDs through I<sup>2</sup>C communication.

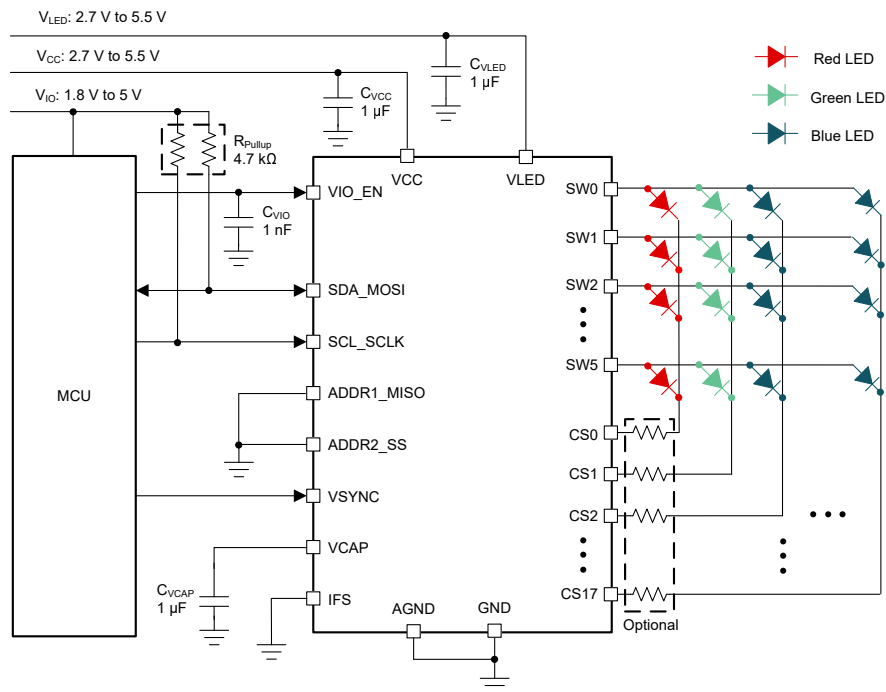


Figure 8-1. Typical Application – LP5866 Driving 36 RGB LEDs (108 LED Dots)



## 8.2.2 Design Requirements

**Table 8-1. Design Parameters**

PARAMETER	VALUE
VCC / VIO	3.3V
VLED	5V
RGB LED count	36
Scan number	6
Interface	I <sup>2</sup> C
LED maximum average current (red, green, blue)	4mA, 3mA, 2mA
LED maximum peak current (red, green, blue)	24mA, 18mA, 12mA

### 8.2.3 Detailed Design Procedure

LP5866 requires an external capacitor  $C_{V_{CAP}}$ , whose value is  $1\mu\text{F}$  connected from  $V_{CAP}$  to GND for proper operation of internal LDO. The capacitor must be placed as close to the device as possible.

TI recommends  $1\mu\text{F}$  capacitors be placed between VCC / VLED with GND, and a  $1\text{nF}$  capacitor placed between VIO with GND. Place the capacitors as close to the device as possible.

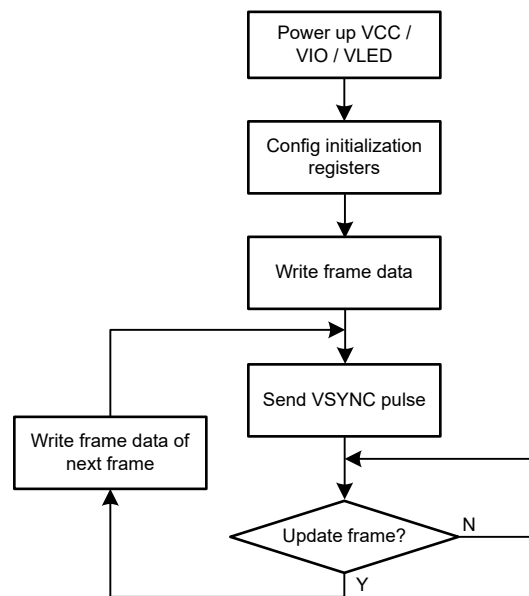
Pull-up resistors  $R_{\text{pull-up}}$  are a requirement for SCL and SDA when using I<sup>2</sup>C as communication method. In typical applications, TI recommends  $1.8\text{k}\Omega$  to  $4.7\text{k}\Omega$  resistors.

To decrease thermal dissipation from device to ambient, resistors  $R_{CS}$  can optionally be placed in serial with the LED. Voltage drop on these resistors must left enough margins for VSAT to ensure the device works normally.

#### 8.2.3.1 Program Procedure

When selecting data refresh Mode 1, outputs are refreshed instantly after data is received.

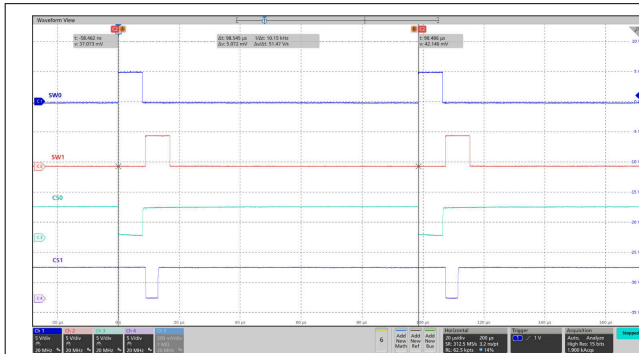
When selecting data refresh Mode 2/3, VSYNC signal is required for synchronized display. Programming flow is shown as [Figure 8-2](#). To display full pixel of last frame, VSYNC pulse must be sent to the device after the end of last PWM. Time between two pulses  $t_{\text{VSYNC}}$  must be larger than the whole PWM time of all Dots  $t_{\text{frame}}$ . Common selection like 60Hz, 90Hz, 120Hz or even higher refresh frequency can be supported. High pulse width longer than  $t_{\text{VSYNC\_H}}$  is required at the beginning of each VSYNC frame, and data must not be write to PWM registers during high pulse width.



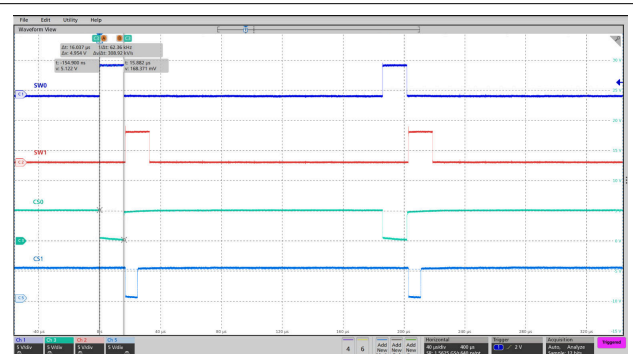
**Figure 8-2. Program Procedure**

### 8.2.4 Application Performance Plots

The following figures show the application performance plots.

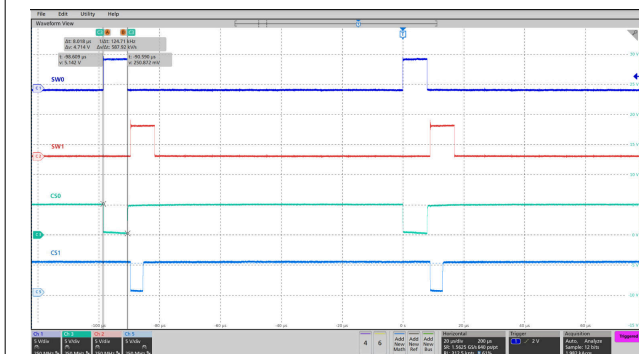


**Figure 8-3. Scan Lines and Current Sinks Waveforms of SW0, SW1, CS0, CS1**



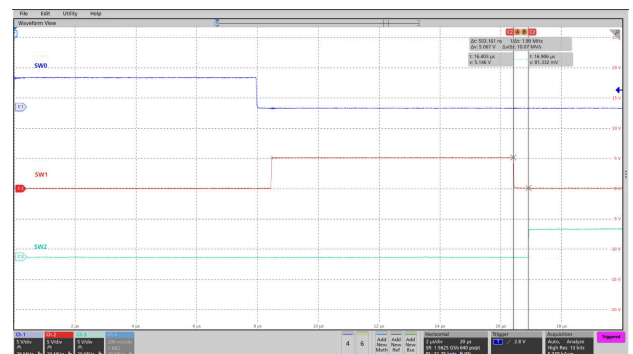
PWM frequency = 62.5kHz

**Figure 8-4. Scan Lines and Current Sinks Waveforms of SW0, SW1, CS0, CS1**



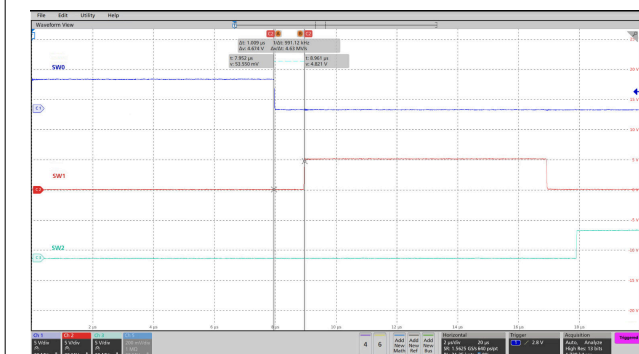
PWM frequency = 125kHz

**Figure 8-5. Scan Lines and Current Sinks Waveforms of SW0, SW1, CS0, CS1**



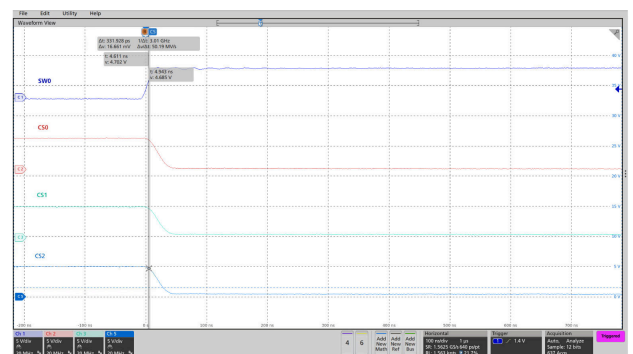
Switch blank time  $t_{SW\_BLK} = 0.5\mu s$

**Figure 8-6. Scan Lines Switching Waveforms of SW0, SW1, SW2**



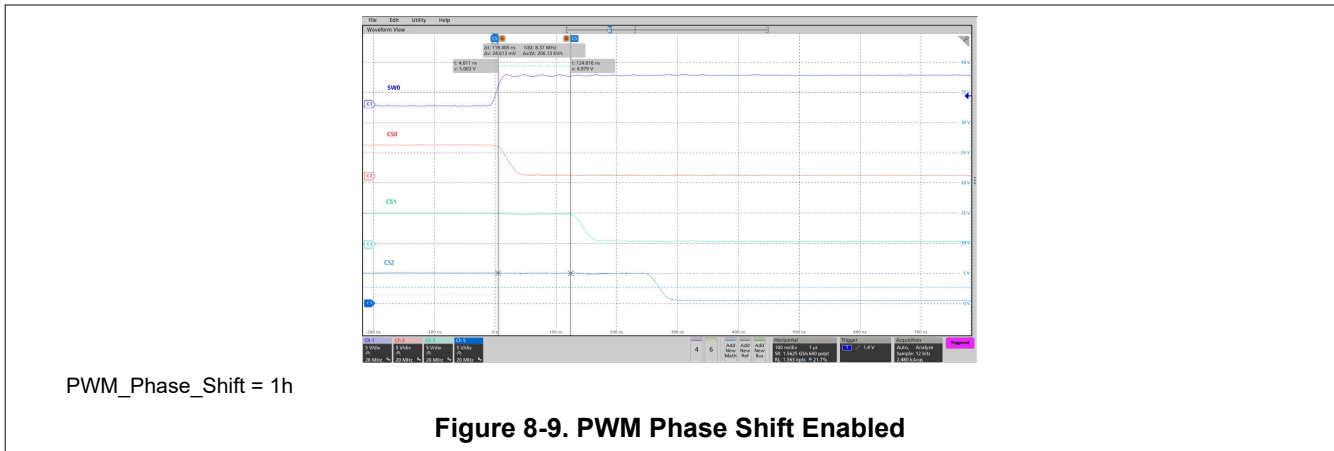
Switch blank time  $t_{SW\_BLK} = 1\mu s$

**Figure 8-7. Scan Lines Switching Waveforms of SW0, SW1, SW2**



PWM\_Phase\_Shift = 0h

**Figure 8-8. PWM Phase Shift Disabled**



## 8.3 Power Supply Recommendations

### 8.3.1 Power Supply Recommendations

#### VDD Input Supply Recommendations

LP5866 is designed to operate from a 2.7V to 5.5V VDD voltage supply. This input supply must be well regulated and can provide the peak current required by the LED matrix. The resistance of the VDD supply rail must be low enough such that the input current transient does not cause the LP5866 VDD supply voltage to drop below the maximum POR voltage.

### 8.3.2 Power Supply Recommendations

#### VIO Input Supply Recommendations

LP5866 is designed to operate with a 1.65V to 5.5V VIO\_EN voltage supply. The VIO\_EN supply must be well regulated and can provide the peak current required by the LED configuration without voltage drop under load transients like start-up or rapid brightness change.

### 8.3.3 Power Supply Recommendations

#### VLED Input Supply Recommendations

LP5866 is designed to operate with a 2.7V to 5.5V VLED voltage supply. The VLED supply must be well regulated and can provide the peak current required by the LED configuration without voltage drop, under load transients like start-up or rapid brightness change. The resistance of the input supply rail must be low enough so that the input current transient does not cause the VLED supply voltage to drop below LED  $V_f + V_{SAT}$  voltage.

## 8.4 Layout

### 8.4.1 Layout Guidelines

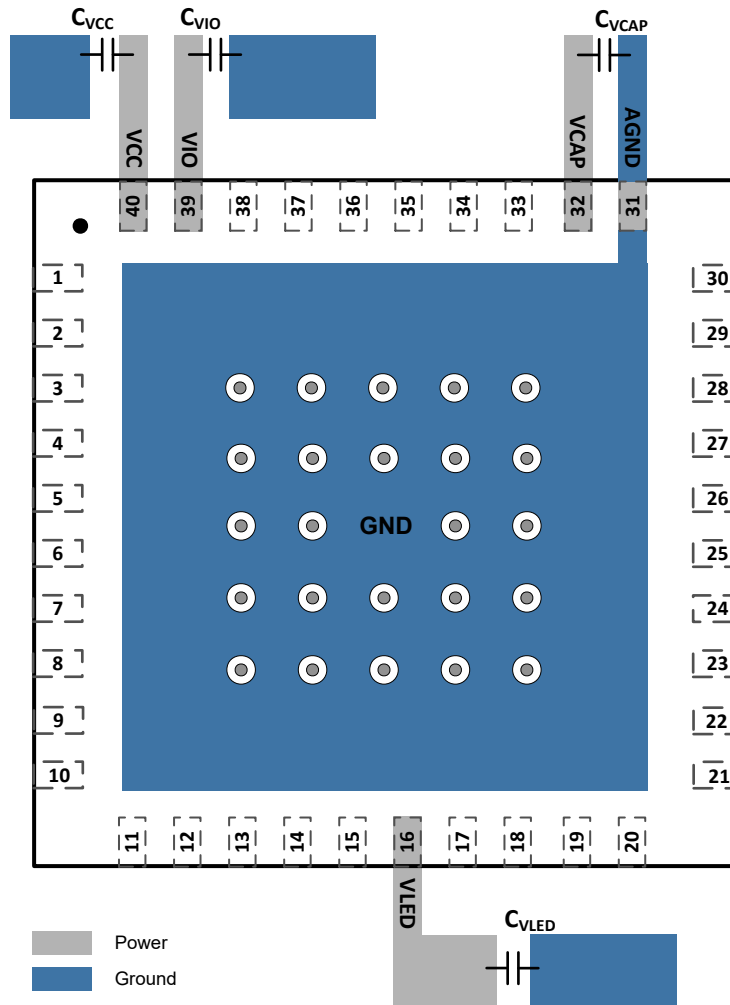
the below guidelines for layout design can help to get a better on-board performance.

- The decoupling capacitors  $C_{VCC}$  and  $C_{VLED}$  for power supply must be close to the chip to have minimized the impact of high-frequency noise and ripple from power.  $C_{V_{CAP}}$  for internal LDO must be put as close to chip as possible. GND plane connections to  $C_{VLED}$  and GND pins must be on TOP layer copper with multiple vias connecting to system ground plane.  $C_{VIO}$  for internal enable block also must be put as close to chip as possible.
- The exposed thermal pad must be well soldered to the board, which can have better mechanical reliability. The action can optimize heat transfer so that increasing thermal performance. AGND pin must be connected to thermal pad and system ground.
- The major heat flow path from the package to the ambient is through copper on the PCB. Several methods can help thermal performance. Below exposed thermal pad of IC, putting much vias through the PCB to other

ground layer can dissipate more heat. Maximizing the copper coverage on the PCB can increase the thermal conductivity of the board.

- Low inductive and resistive path of switch load loop can help to provide a high slew rate. Therefore, path of VLED – SWx must be short and wide and avoid parallel wiring and narrow trace. Transient current in SWx pins is much larger than CSy pins, so that trace for SWx must be wider than CSy.

**8.4.2 Layout Example**



**Figure 8-10. LP5866 Layout Example**

## 9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.2 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 9.3 Trademarks

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### 9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2021) to Revision A (September 2024)	Page
• Updated DBT package information.....	4
• Updated thermal information of DBT package.....	7
• Updated I <sup>2</sup> C Timing Requirements.....	7
• Added I <sup>2</sup> C Standard Mode Timing Requirements.....	7
• Added timing parameters diagrams.....	11
• Updated application design parameters.....	41

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">LP5866DBTR</a>	Active	Production	TSSOP (DBT)   38	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LP5866DBT
LP5866DBTR.A	Active	Production	TSSOP (DBT)   38	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LP5866DBT
<a href="#">LP5866MDBTR</a>	Active	Production	TSSOP (DBT)   38	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	5866MDBT
LP5866MDBTR.A	Active	Production	TSSOP (DBT)   38	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	5866MDBT
<a href="#">LP5866RKPR</a>	Active	Production	VQFN (RKP)   40	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LP5866
LP5866RKPR.A	Active	Production	VQFN (RKP)   40	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LP5866

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP5866RKPR	VQFN	RKP	40	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

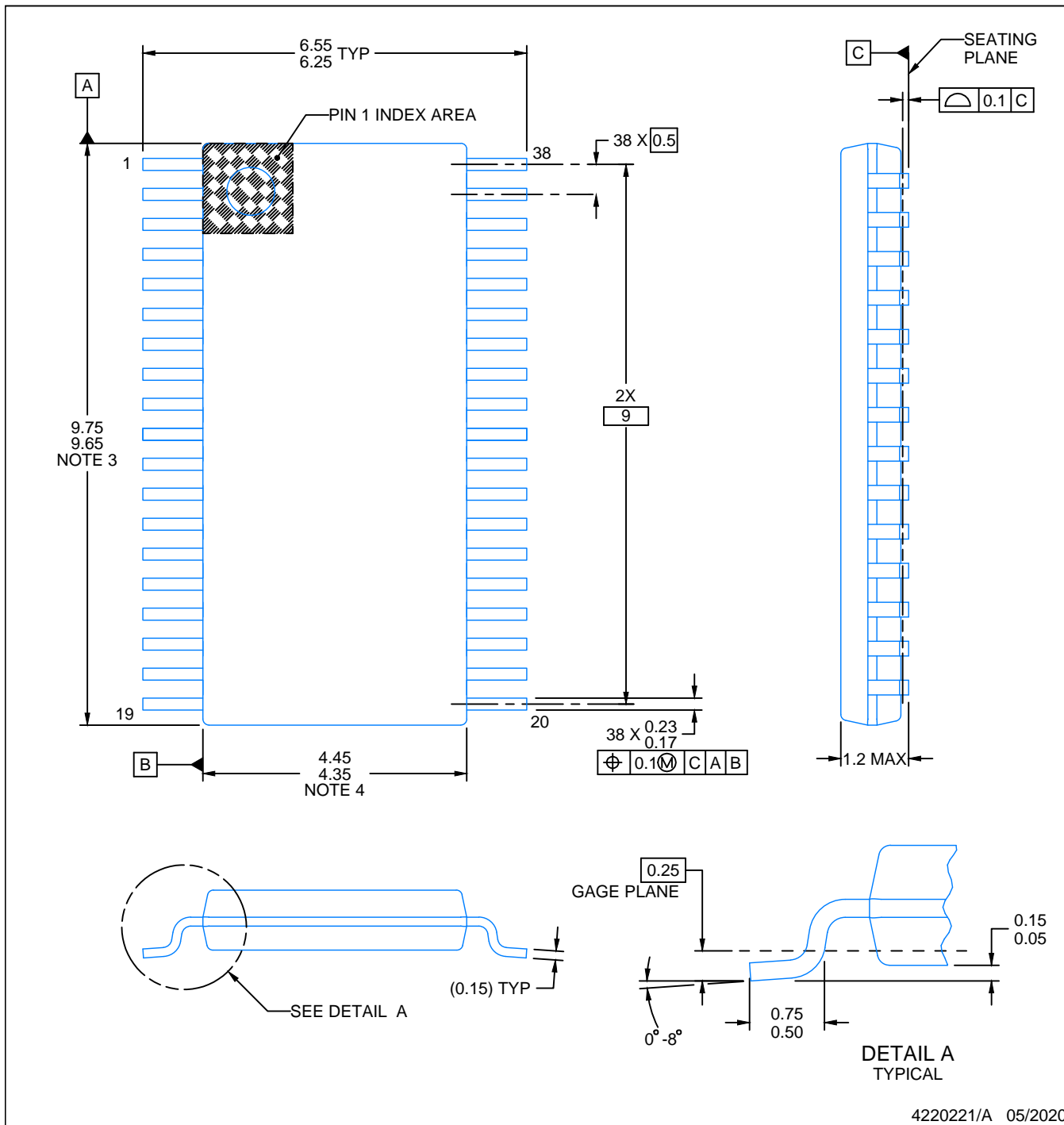
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP5866RKPR	VQFN	RKP	40	3000	367.0	367.0	35.0

# PACKAGE OUTLINE

DBT0038A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

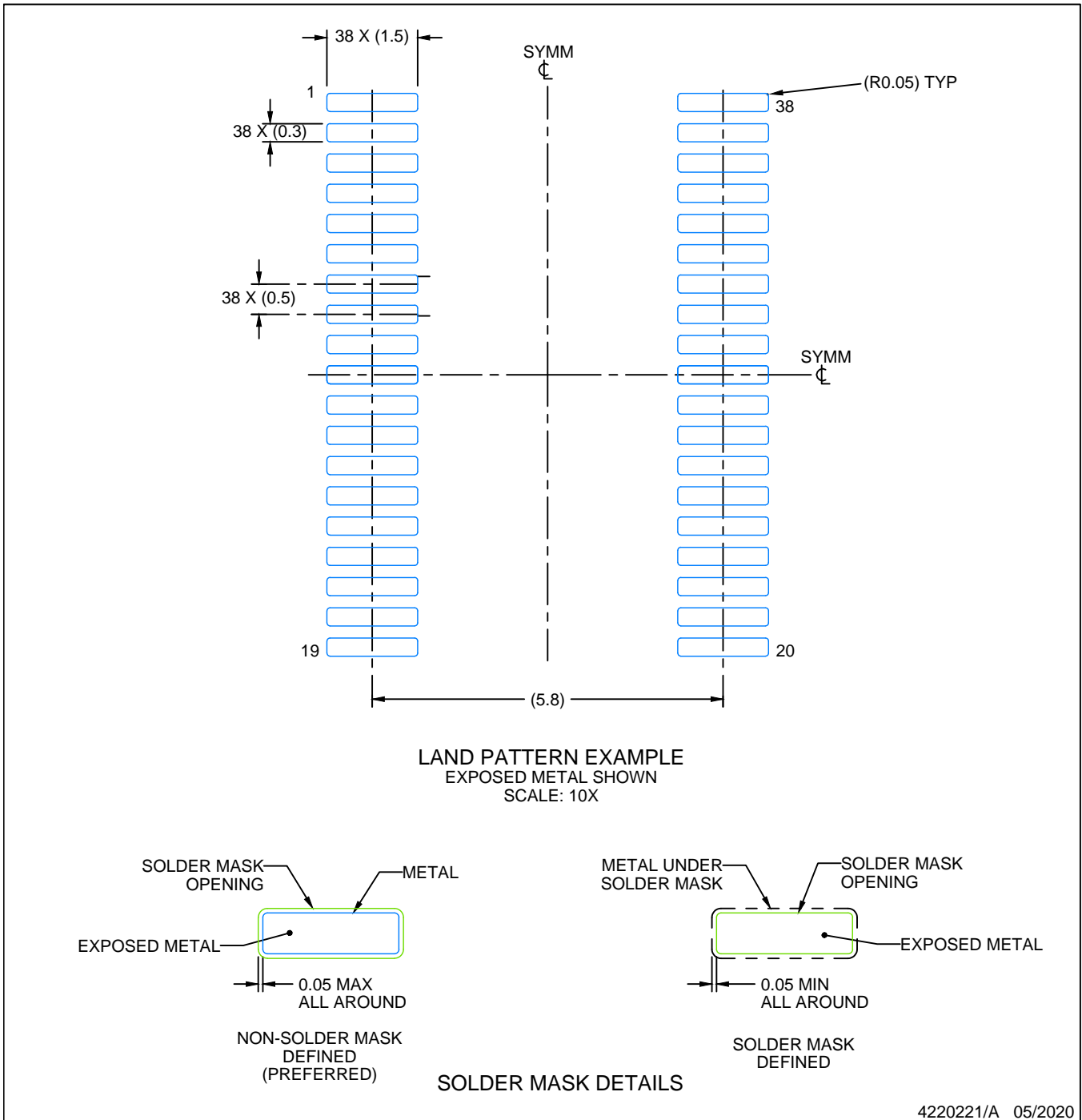
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

DBT0038A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

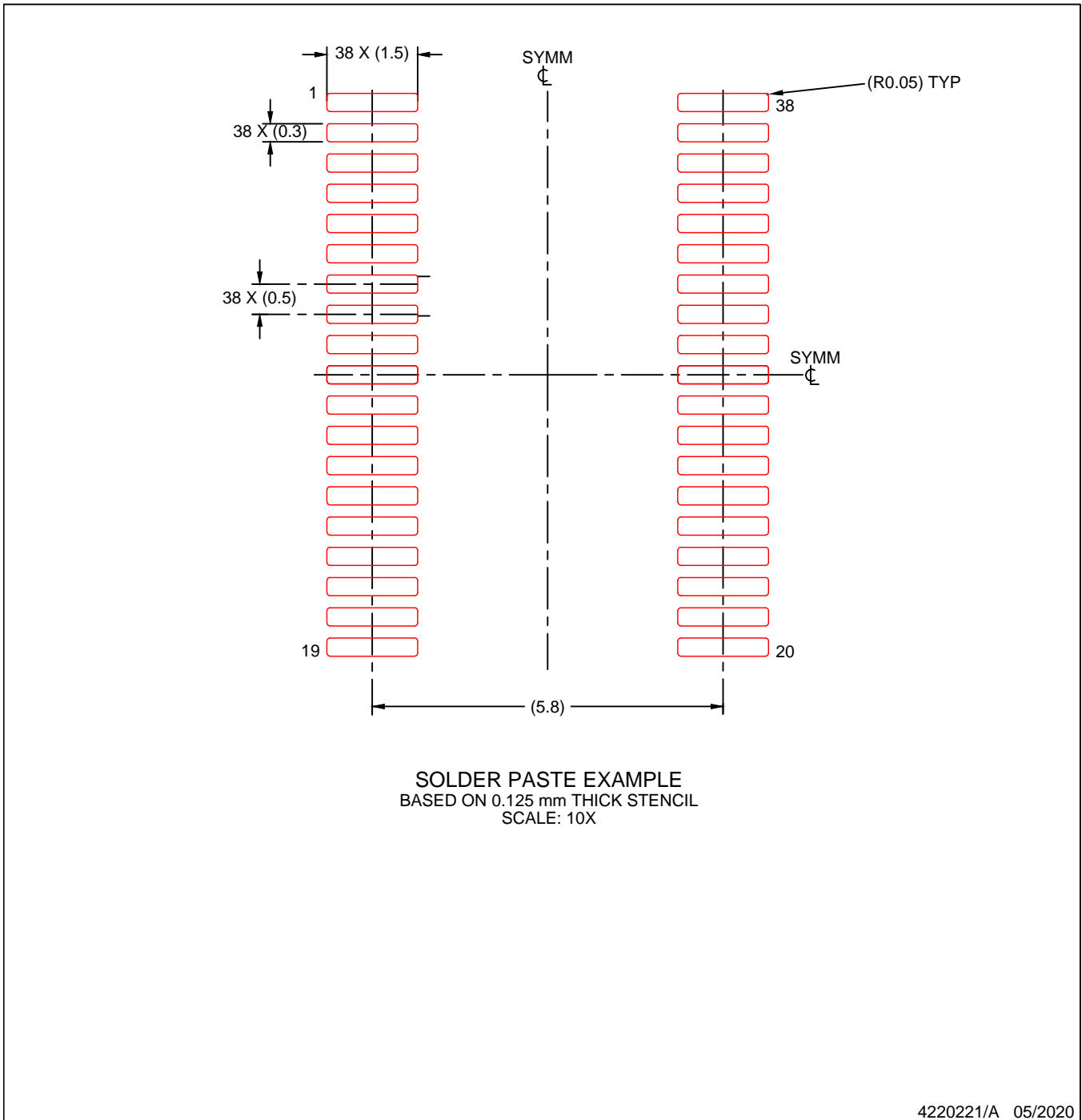
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBT0038A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

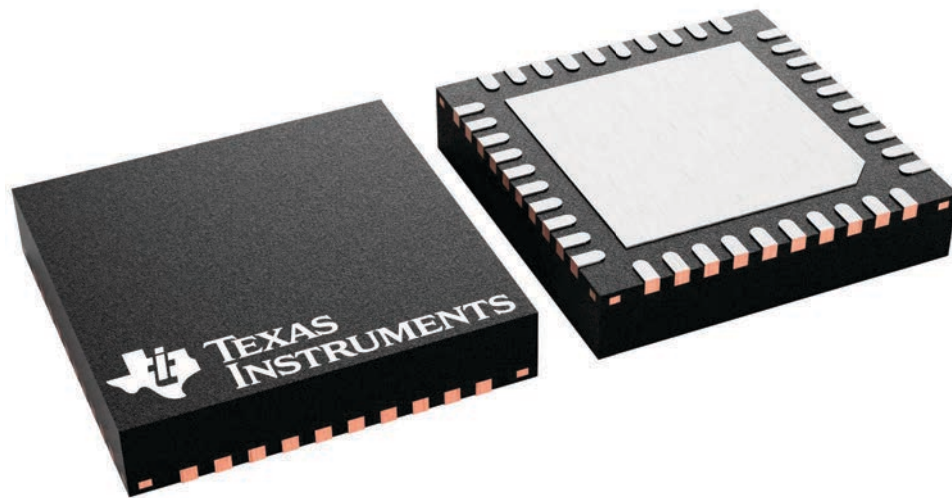
**RKP 40**

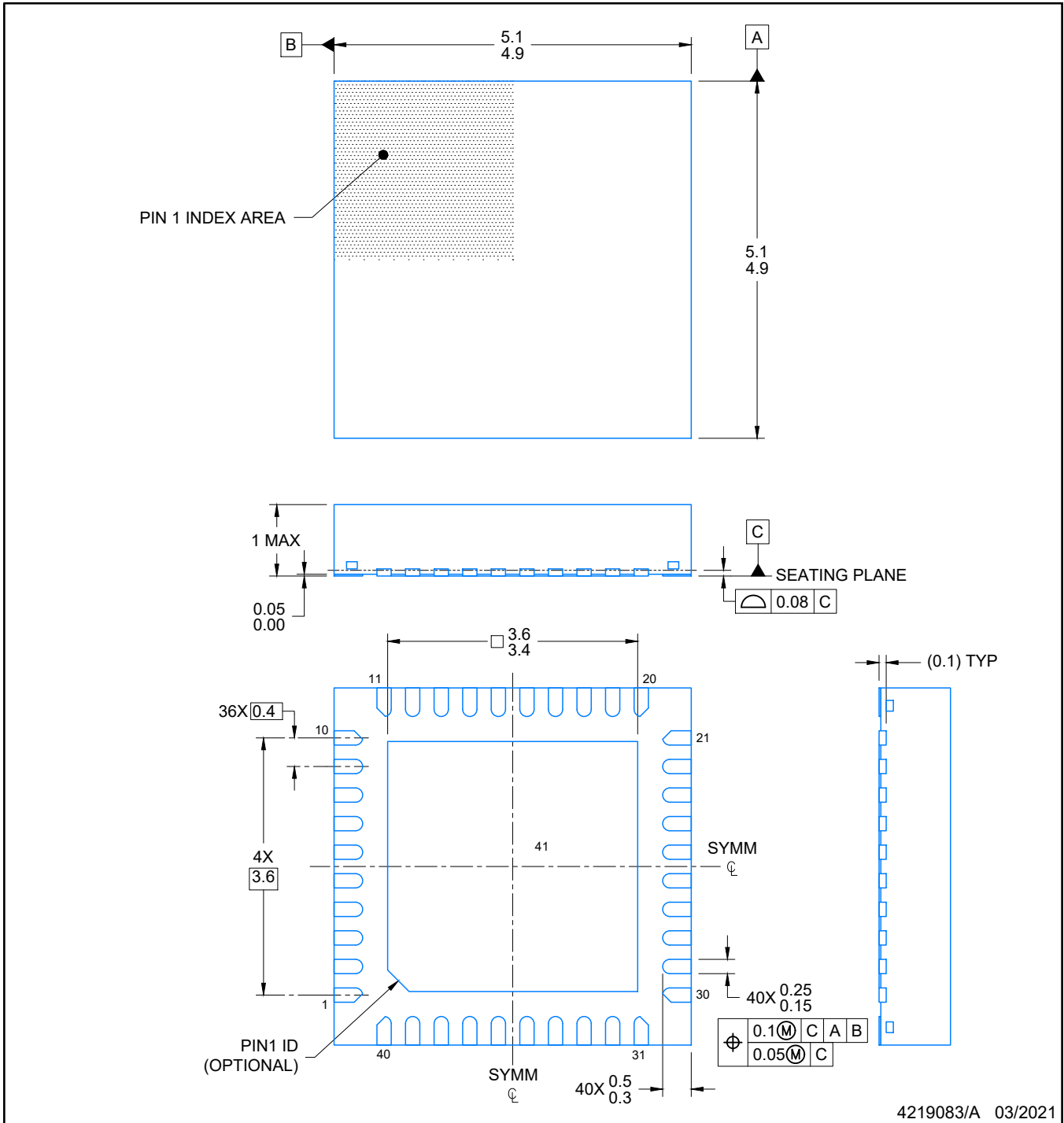
**VQFN - 1 mm max height**

5 x 5, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.





NOTES:

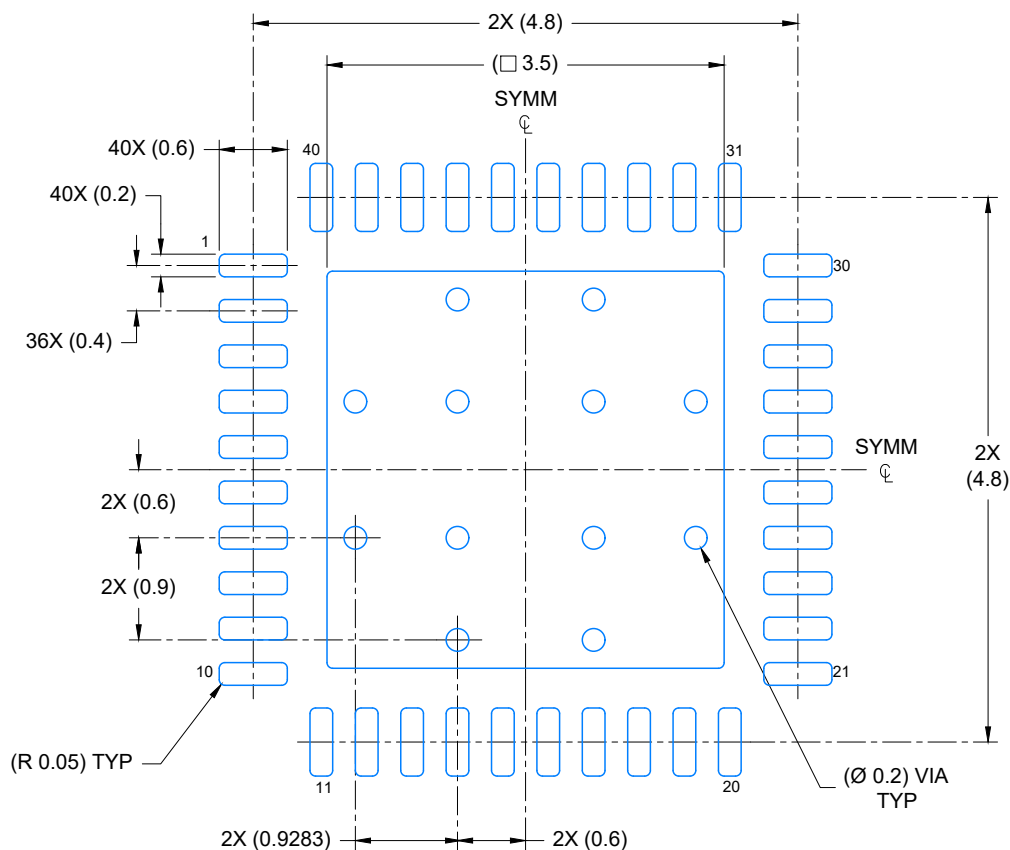
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

RKP0040B

VQFN - 1 mm max height

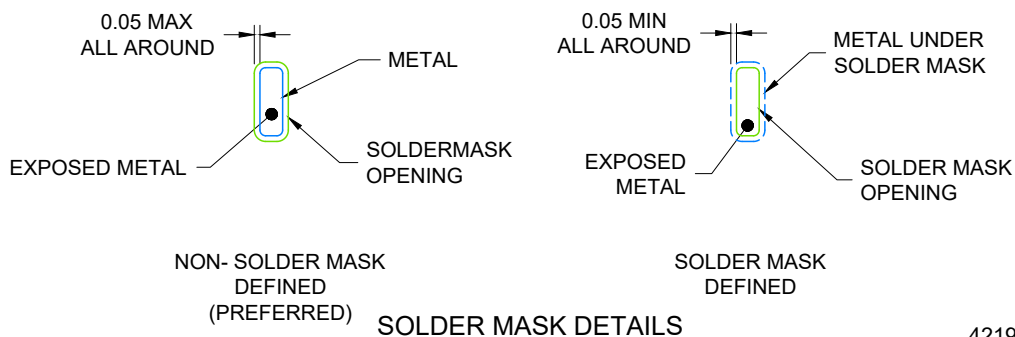
PLASTIC QUAD FLATPACK- NO LEAD



## LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

SCALE: 15X



4219083/A 03/2021

NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

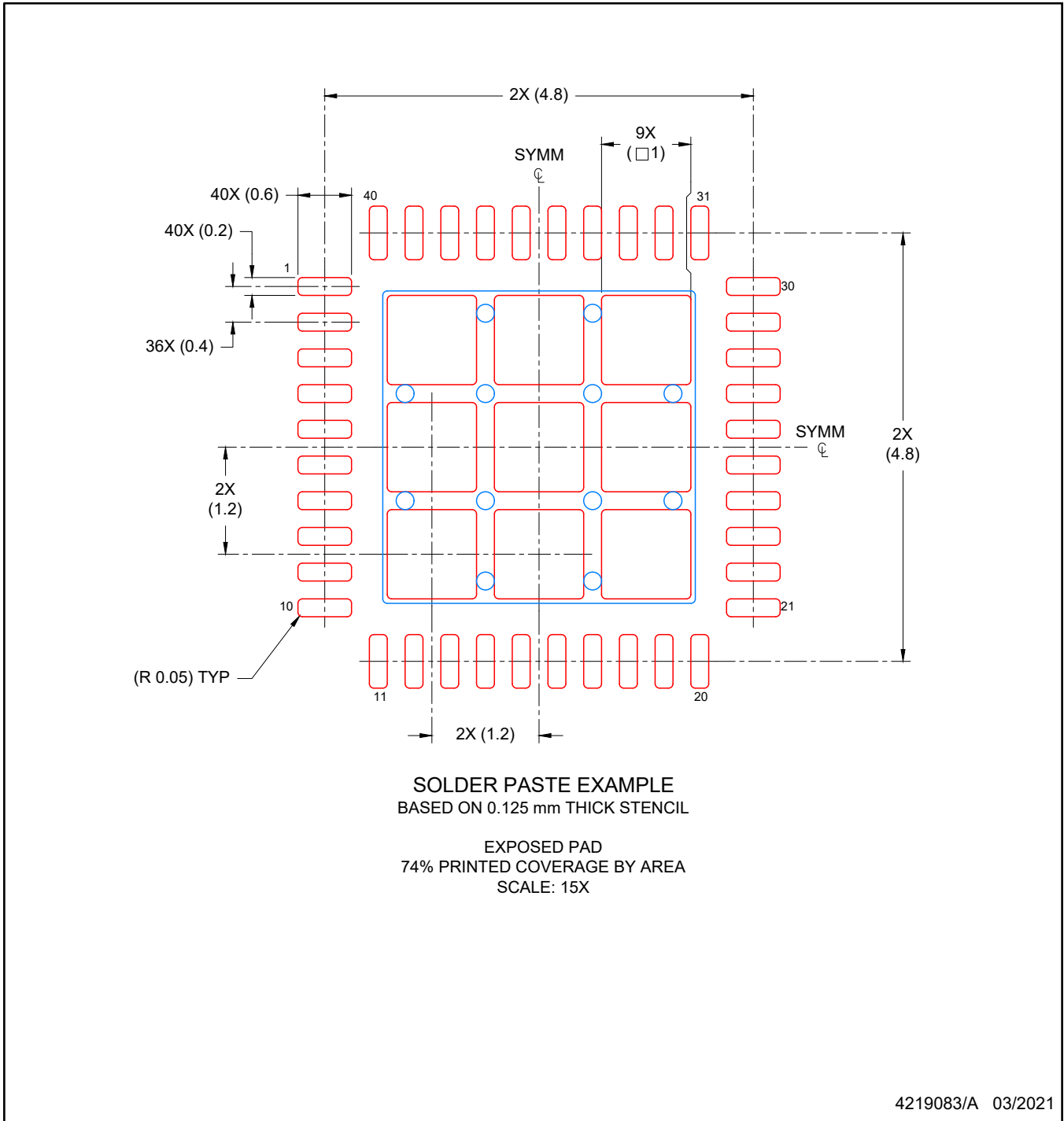


# EXAMPLE STENCIL DESIGN

VQFN - 1 mm max height

RKP0040B

PLASTIC QUAD FLATPACK- NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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