

OPAx192-Q1 36-V Precision, Rail-to-Rail Input/Output, Low-Offset Voltage, Low-Input Bias Current Op Amp With e-trim™

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
 - Device Temperature Grade 1: -40°C to $+125^{\circ}\text{C}$ Ambient Operating Temperature
 - Device HBM ESD Classification Level 3A
 - Device CDM ESD Classification Level 4A
- Low Offset Voltage: $\pm 5\ \mu\text{V}$
- Low Offset Voltage Drift: $\pm 0.2\ \mu\text{V}/^{\circ}\text{C}$
- Low Noise: $5.5\ \text{nV}/\sqrt{\text{Hz}}$ at 1 kHz
- High Common-Mode Rejection: 140 dB
- Low Bias Current: $\pm 5\ \text{pA}$
- Rail-to-Rail Input and Output
- Wide Bandwidth: 10 MHz GBW
- High Slew Rate: 20 V/ μs
- Low Quiescent Current: 1 mA per Amplifier
- Wide Supply: $\pm 2.25\ \text{V}$ to $\pm 18\ \text{V}$, 4.5 V to 36 V
- EMI/RFI Filtered Inputs
- Differential Input Voltage Range to Supply Rail
- High Capacitive-Load-Drive Capability: 1 nF
- Industry-Standard Package:
 - Single and Dual Channel in VSSOP-8

2 Applications

- Motor Control for Automotive
- Traction Inverter
- On-Board Charger
- Precision Current Sensing

3 Description

The OPAx192-Q1 family (OPA192-Q1 and OPA2192-Q1) is a new generation of 36-V, e-trim operational amplifiers. The OPAx192-Q1 family of operational amplifiers use e-trim™, a method of package-level trim for offset and offset temperature drift implemented during the final steps of manufacturing after the plastic molding process. This method minimizes the influence of inherent input transistor mismatch, as well as errors induced during package molding.

These devices offer outstanding dc precision and ac performance, including rail-to-rail input/output, low offset ($\pm 5\ \mu\text{V}$, typical), low offset drift ($\pm 0.2\ \mu\text{V}/^{\circ}\text{C}$, typical), and 10-MHz bandwidth.

Unique features such as differential input-voltage range to the supply rail, high output current ($\pm 65\ \text{mA}$), high capacitive-load drive of up to 1 nF, and high slew rate (20 V/ μs) make the OPAx192-Q1 a robust, high-performance operational amplifier for high-voltage industrial applications.

The OPAx192-Q1 family of op amps is available in an 8-pin VSSOP package and is specified from -40°C to $+125^{\circ}\text{C}$.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA192-Q1	VSSOP (8)	3.00 mm x 3.00 mm
OPA2192-Q1		

(1) For all available packages, see the package option addendum at the end of the data sheet.

OPAx192-Q1 Maintains Ultra-Low Input Offset Voltage Over Temperature

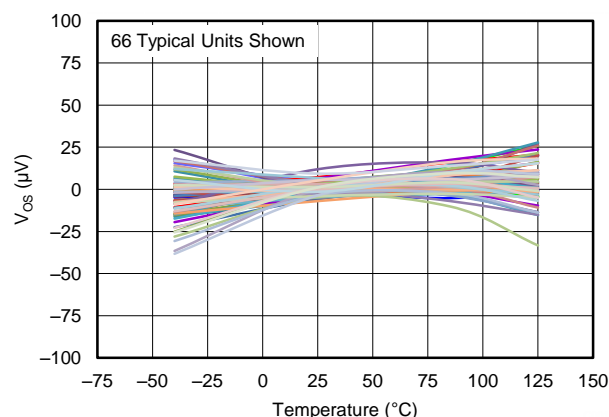


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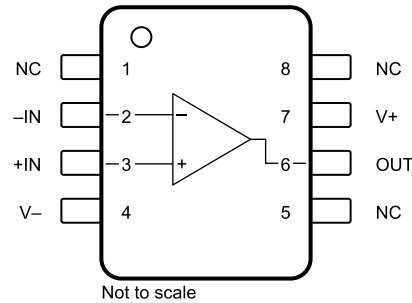
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4 Revision History

DATE	REVISION	NOTES
December 2017	*	Initial release

5 Pin Configuration and Functions

**OPA192-Q1 DGK Package
8-Pin VSSOP
Top View**

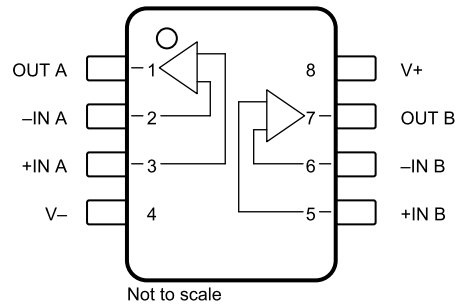


NC – No internal connection.

Pin Functions: OPA192-Q1

PIN		I/O	DESCRIPTION
NAME	OPA192-Q1 DGK (VSSOP)		
+IN	3	I	Noninverting input
-IN	2	I	Inverting input
NC	1, 5, 8	—	No internal connection (can be left floating)
OUT	6	O	Output
V+	7	—	Positive (highest) power supply
V-	4	—	Negative (lowest) power supply

**OPA2192-Q1 DGK Package
8-Pin VSSOP
Top View**



Pin Functions: OPA2192-Q1

PIN		I/O	DESCRIPTION
NAME	OPA2192-Q1 DGK (VSSOP)		
+IN A	3	I	Noninverting input, channel A
+IN B	5	I	Noninverting input, channel B
+IN C	—	I	Noninverting input, channel C
+IN D	—	I	Noninverting input, channel D
-IN A	2	I	Inverting input, channel A
-IN B	6	I	Inverting input, channel B
-IN C	—	I	Inverting input, channel C
-IN D	—	I	Inverting input, channel D
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
OUT C	—	O	Output, channel C
OUT D	—	O	Output, channel D
V+	8	—	Positive (highest) power supply
V-	4	—	Negative (lowest) power supply

6 Specifications

6.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
Supply voltage, $V_S = (V+) - (V-)$				± 20 (40, single-supply)	V
Signal input pins	Voltage	Common-mode	$(V-) - 0.5$	$(V+) + 0.5$	V
		Differential		$(V+) - (V-) + 0.2$	
Current				± 10	mA
Output short circuit ⁽²⁾			Continuous		
Latch-up per JESD78D			Class 1		
Temperature	Operating range		-55	150	°C
	Junction			150	
	Storage, T_{stg}		-65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
OPA192-Q1				
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 ⁽¹⁾	± 4000	V
		Charged device model (CDM), per AEC Q100-011	± 500	
OPA2192-Q1				
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 ⁽¹⁾	± 4000	V
		Charged device model (CDM), per AEC Q100-011	± 500	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage, $V_S = (V+) - (V-)$	4.5 (± 2.25)		36 (± 18)	V
Specified temperature	-40		+125	°C

6.4 Thermal Information: OPA192-Q1

THERMAL METRIC ⁽¹⁾		OPA192-Q1	
		DGK (VSSOP)	
		8 PINS	
			UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	180.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	102.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	10.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	100.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Thermal Information: OPA2192-Q1

THERMAL METRIC ⁽¹⁾		OPA2192-Q1	
		DGK (VSSOP)	
		8 PINS	
			UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	158	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	78.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	3.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	77.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.6 Electrical Characteristics: $V_S = \pm 4\text{ V to } \pm 18\text{ V}$ ($V_S = 8\text{ V to } 36\text{ V}$)

at $T_A = 25^\circ\text{C}$, $V_{CM} = V_{OUT} = V_S / 2$, and $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage			± 5	± 25	μV
		$T_A = 0^\circ\text{C to } 85^\circ\text{C}$		± 8	± 50	
		$T_A = -40^\circ\text{C to } 125^\circ\text{C}$		± 10	± 75	
	$V_{CM} = (V+) - 1.5\text{ V}$			± 10	± 40	
		$T_A = 0^\circ\text{C to } 85^\circ\text{C}$		± 25	± 150	
		$T_A = -40^\circ\text{C to } 125^\circ\text{C}$		± 50	± 250	
dV_{OS}/dT	Input offset voltage drift			± 0.1	± 0.8	$\mu\text{V}/^\circ\text{C}$
				± 0.2	± 1.0	
PSRR	Power-supply rejection ratio	$T_A = -40^\circ\text{C to } 125^\circ\text{C}$		± 0.3	± 1.0	$\mu\text{V/V}$
INPUT BIAS CURRENT						
I_B	Input bias current			± 5	± 20	pA
		$T_A = -40^\circ\text{C to } 125^\circ\text{C}$			± 5	nA
I_{OS}	Input offset current			± 2	± 20	pA
		$T_A = -40^\circ\text{C to } 125^\circ\text{C}$			± 2	nA
NOISE						
E_n	Input voltage noise	$(V-) - 0.1\text{ V} < V_{CM} < (V+) - 3\text{ V}$	$f = 0.1\text{ Hz to } 10\text{ Hz}$	1.30		μV_{PP}
		$(V+) - 1.5\text{ V} < V_{CM} < (V+) + 0.1\text{ V}$	$f = 0.1\text{ Hz to } 10\text{ Hz}$	4		
e_n	Input voltage noise density	$(V-) - 0.1\text{ V} < V_{CM} < (V+) - 3\text{ V}$	$f = 100\text{ Hz}$	10.5		$\text{nV}/\sqrt{\text{Hz}}$
			$f = 1\text{ kHz}$	5.5		
		$(V+) - 1.5\text{ V} < V_{CM} < (V+) + 0.1\text{ V}$	$f = 100\text{ Hz}$	32		
			$f = 1\text{ kHz}$	12.5		
NOISE (continued)						
i_n	Input current noise density	$f = 1\text{ kHz}$		1.5		$\text{fA}/\sqrt{\text{Hz}}$
INPUT VOLTAGE						
V_{CM}	Common-mode voltage range			$(V-) - 0.1$	$(V+) + 0.1$	V
CMRR	Common-mode rejection ratio	$(V-) - 0.1\text{ V} < V_{CM} < (V+) - 3\text{ V}$		120	140	dB
			$T_A = -40^\circ\text{C to } 125^\circ\text{C}$	114	126	
		$(V+) - 1.5\text{ V} < V_{CM} < (V+)$		100	120	
			$T_A = -40^\circ\text{C to } 125^\circ\text{C}$	86	100	
		$(V+) - 3\text{ V} < V_{CM} < (V+) - 1.5\text{ V}$		See Typical Characteristics		
INPUT IMPEDANCE						
Z_{ID}	Differential			$100 \parallel 1.6$		$\text{M}\Omega \parallel \text{pF}$
Z_{IC}	Common-mode			$1 \parallel 6.4$		$10^{13}\Omega \parallel \text{pF}$
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	$(V-) + 0.6\text{ V} < V_O < (V+) - 0.6\text{ V}$, $R_{LOAD} = 2\text{ k}\Omega$		120	134	dB
			$T_A = -40^\circ\text{C to } 125^\circ\text{C}$	114	126	
		$(V-) + 0.3\text{ V} < V_O < (V+) - 0.3\text{ V}$, $R_{LOAD} = 10\text{ k}\Omega$		126	140	
			$T_A = -40^\circ\text{C to } 125^\circ\text{C}$	120	134	

Electrical Characteristics: $V_S = \pm 4\text{ V}$ to $\pm 18\text{ V}$ ($V_S = 8\text{ V}$ to 36 V) (continued)

 at $T_A = 25^\circ\text{C}$, $V_{CM} = V_{OUT} = V_S / 2$, and $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
GBW	Unity gain bandwidth				10		MHz
SR	Slew rate	G = 1, 10-V step			20		V/ μs
t_s	Settling time	To 0.01%	$V_S = \pm 18\text{ V}$, G = 1, 10-V step		1.4		μs
			$V_S = \pm 18\text{ V}$, G = 1, 5-V step		0.9		
		To 0.001%	$V_S = \pm 18\text{ V}$, G = 1, 10-V step		2.1		
			$V_S = \pm 18\text{ V}$, G = 1, 5-V step		1.8		
t_{OR}	Overload recovery time	$V_{IN} \times G = V_S$			200		ns
THD+N	Total harmonic distortion + noise	G = 1, f = 1 kHz, $V_O = 3.5 V_{RMS}$			0.00008%		
	Crosstalk	OPA2192-Q1 at dc			150		dB
		OPA2192-Q1 at f = 100 kHz			130		
OUTPUT							
V_O	Voltage output swing from rail	Positive rail	No load		5	15	mV
			$R_{LOAD} = 10\text{ k}\Omega$		95	110	
			$R_{LOAD} = 2\text{ k}\Omega$		430	500	
		Negative rail	No load		5	15	
			$R_{LOAD} = 10\text{ k}\Omega$		95	110	
			$R_{LOAD} = 2\text{ k}\Omega$		430	500	
I_{SC}	Short-circuit current				± 65		mA
C_{LOAD}	Capacitive load drive				See Typical Characteristics		
Z_O	Open-loop output impedance	f = 1 MHz, $I_O = 0\text{ A}$; see Figure 29			375		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	$I_O = 0\text{ A}$			1	1.2	mA
		$T_A = -40^\circ\text{C}$ to 125°C , $I_O = 0\text{ A}$				1.5	
TEMPERATURE							
	Thermal protection ⁽¹⁾				140		$^\circ\text{C}$

 (1) For a detailed description of thermal protection, see [Thermal Protection](#).

6.7 Electrical Characteristics: $V_S = \pm 2.25\text{ V}$ to $\pm 4\text{ V}$ ($V_S = 4.5\text{ V}$ to 8 V)

at $T_A = 25^\circ\text{C}$, $V_{CM} = V_{OUT} = V_S / 2$, and $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
OFFSET VOLTAGE								
V_{OS}	Input offset voltage	$V_{CM} = (V+) - 3\text{ V}$	$T_A = 0^\circ\text{C}$ to 85°C		± 5	± 25	μV	
			$T_A = -40^\circ\text{C}$ to 125°C		± 8	± 50		
		$(V+) - 3.5\text{ V} < V_{CM} < (V+) - 1.5\text{ V}$				± 10	± 75	
						See Common-Mode Voltage Range		
V_{OS}	Input offset voltage	$V_{CM} = (V+) - 1.5\text{ V}$	$T_A = 0^\circ\text{C}$ to 85°C		± 10	± 40	μV	
			$T_A = -40^\circ\text{C}$ to 125°C		± 25	± 150		
					± 50	± 250		
dV_{OS}/dT	Input offset voltage drift	$V_{CM} = (V+) - 3\text{ V}$	$T_A = 0^\circ\text{C}$ to 85°C		± 0.1	± 0.8	$\mu\text{V}/^\circ\text{C}$	
			$T_A = -40^\circ\text{C}$ to 125°C		± 0.2	± 1.1		
		$V_{CM} = (V+) - 1.5\text{ V}$, $T_A = -40^\circ\text{C}$ to 125°C		± 0.5	± 3			
PSRR	Power-supply rejection ratio	$T_A = -40^\circ\text{C}$ to 125°C , $V_{CM} = V_S / 2 - 0.75\text{ V}$			± 1		$\mu\text{V}/\text{V}$	
INPUT BIAS CURRENT								
I_B	Input bias current				± 5	± 20	pA	
		$T_A = -40^\circ\text{C}$ to 125°C					± 5	nA
I_{OS}	Input offset current				± 2	± 20	pA	
		$T_A = -40^\circ\text{C}$ to 125°C					± 2	nA
NOISE								
E_n	Input voltage noise	$(V-) - 0.1\text{ V} < V_{CM} < (V+) - 3\text{ V}$, $f = 0.1\text{ Hz}$ to 10 Hz			1.30		μV_{PP}	
		$(V+) - 1.5\text{ V} < V_{CM} < (V+) + 0.1\text{ V}$, $f = 0.1\text{ Hz}$ to 10 Hz			4			
e_n	Input voltage noise density	$(V-) - 0.1\text{ V} < V_{CM} < (V+) - 3\text{ V}$	$f = 100\text{ Hz}$		10.5		$\text{nV}/\sqrt{\text{Hz}}$	
			$f = 1\text{ kHz}$		5.5			
		$(V+) - 1.5\text{ V} < V_{CM} < (V+) + 0.1\text{ V}$	$f = 100\text{ Hz}$		32			
			$f = 1\text{ kHz}$		12.5			
i_n	Input current noise density		$f = 1\text{ kHz}$		1.5		$\text{fA}/\sqrt{\text{Hz}}$	
INPUT VOLTAGE								
V_{CM}	Common-mode voltage range			$(V-) - 0.1$		$(V+) + 0.1$	V	
CMRR	Common-mode rejection ratio	$(V-) - 0.1\text{ V} < V_{CM} < (V+) - 3\text{ V}$	$T_A = -40^\circ\text{C}$ to 125°C	94	110		dB	
				90	104			
		$(V+) - 1.5\text{ V} < V_{CM} < (V+)$	$T_A = -40^\circ\text{C}$ to 125°C	100	120			
				84	100			
	$(V+) - 3\text{ V} < V_{CM} < (V+) - 1.5\text{ V}$			See Typical Characteristics				
INPUT IMPEDANCE								
Z_{ID}	Differential				$100 \parallel 1.6$		$\text{M}\Omega \parallel \text{pF}$	
Z_{IC}	Common-mode				$1 \parallel 6.4$		$10^{13}\Omega \parallel \text{pF}$	
OPEN-LOOP GAIN								
A_{OL}	Open-loop voltage gain	$(V-) + 0.6\text{ V} < V_O < (V+) - 0.6\text{ V}$, $R_{LOAD} = 2\text{ k}\Omega$	$T_A = -40^\circ\text{C}$ to 125°C	110	120		dB	
				100	114			
		$(V-) + 0.3\text{ V} < V_O < (V+) - 0.3\text{ V}$, $R_{LOAD} = 10\text{ k}\Omega$	$T_A = -40^\circ\text{C}$ to 125°C	110	126			
				110	120			

Electrical Characteristics: $V_S = \pm 2.25\text{ V}$ to $\pm 4\text{ V}$ ($V_S = 4.5\text{ V}$ to 8 V) (continued)

 at $T_A = 25^\circ\text{C}$, $V_{CM} = V_{OUT} = V_S / 2$, and $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
GBW	Unity gain bandwidth				10		MHz
SR	Slew rate	G = 1, 10-V step			20		V/ μs
t_s	Settling time	To 0.01%	$V_S = \pm 3\text{ V}$, G = 1, 5-V step		1		μs
t_{OR}	Overload recovery time	$V_{IN} \times G = V_S$			200		ns
	Crosstalk	OPA2192-Q1 at dc			150		dB
		OPA2192-Q1 f = 100 kHz			130		
OUTPUT							
V_O	Voltage output swing from rail	Positive rail	No load		5	15	mV
			$R_{LOAD} = 10\text{ k}\Omega$		95	110	
			$R_{LOAD} = 2\text{ k}\Omega$		430	500	
		Negative rail	No load		5	15	
			$R_{LOAD} = 10\text{ k}\Omega$		95	110	
			$R_{LOAD} = 2\text{ k}\Omega$		430	500	
I_{SC}	Short-circuit current				± 65		mA
C_{LOAD}	Capacitive load drive				See Typical Characteristics		
Z_O	Open-loop output impedance	f = 1 MHz, $I_O = 0\text{ A}$; see Figure 29			375		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	$I_O = 0\text{ A}$			1	1.2	mA
				$T_A = -40^\circ\text{C}$ to 125°C		1.5	
TEMPERATURE							
	Thermal protection ⁽¹⁾				140		$^\circ\text{C}$

 (1) For a detailed description of thermal protection, see [Thermal Protection](#).

6.8 Typical Characteristics

Table 1. Table of Graphs

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	Figure 1 to Figure 6
Offset Voltage Drift Distribution	Figure 7 to Figure 8
Offset Voltage vs Temperature	Figure 9
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Offset Voltage vs Power Supply	Figure 13
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Input Bias Current vs Common-Mode Voltage	Figure 16
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Crosstalk vs Frequency	Figure 46

6.9 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_S = \pm 18\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$, and $C_L = 100\text{ pF}$, (unless otherwise noted)

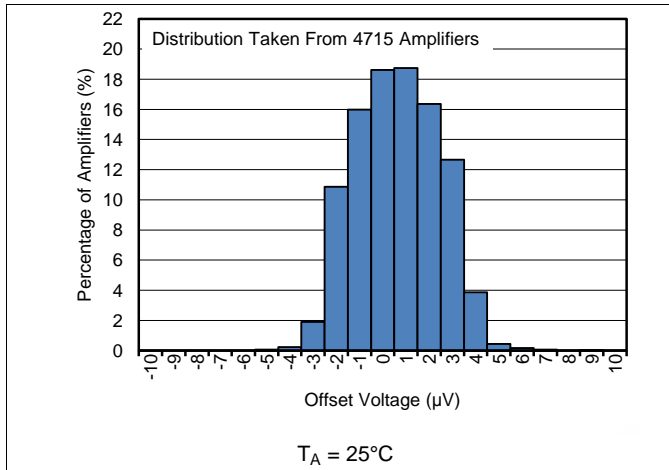


Figure 1. Offset Voltage Production Distribution at 25°C

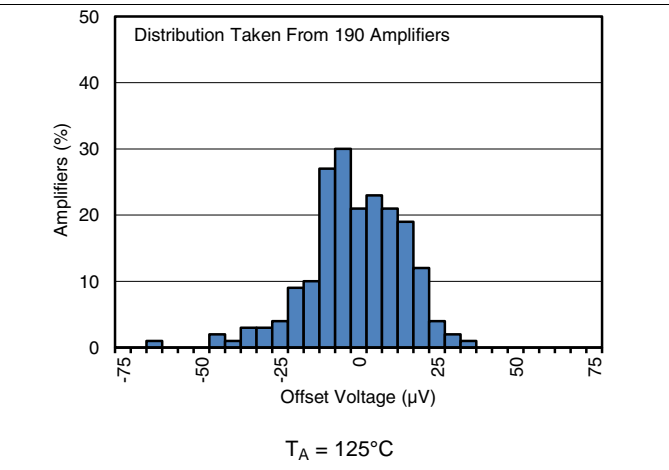


Figure 2. Offset Voltage Production Distribution at 125°C

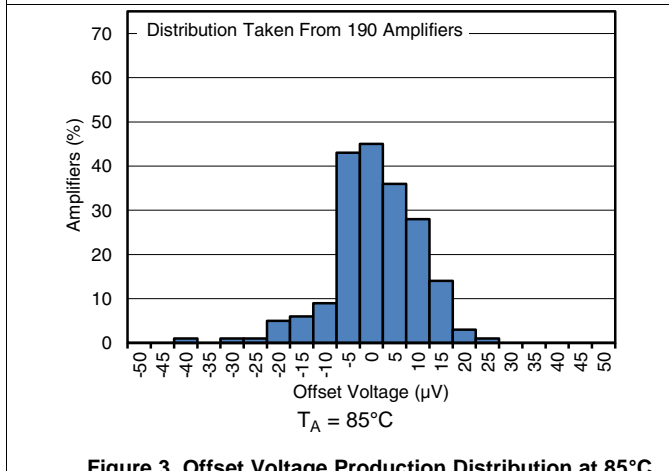


Figure 3. Offset Voltage Production Distribution at 85°C

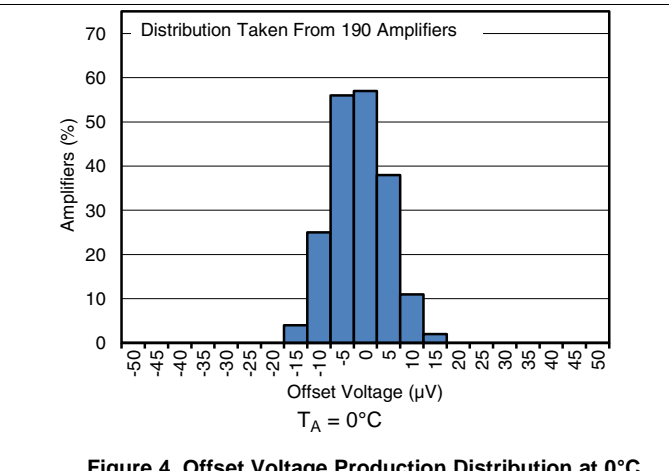


Figure 4. Offset Voltage Production Distribution at 0°C

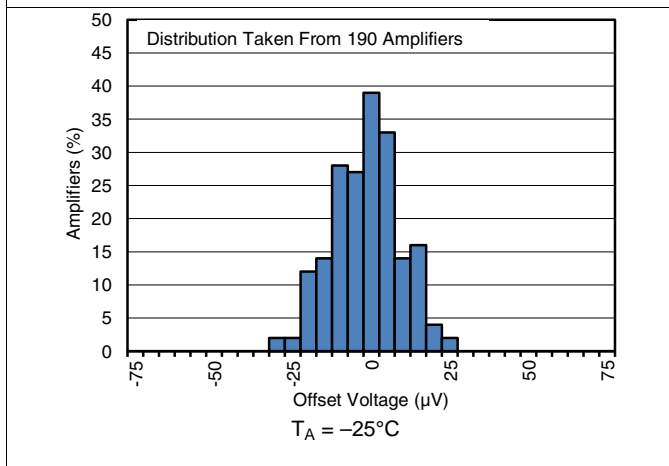


Figure 5. Offset Voltage Production Distribution at -25°C

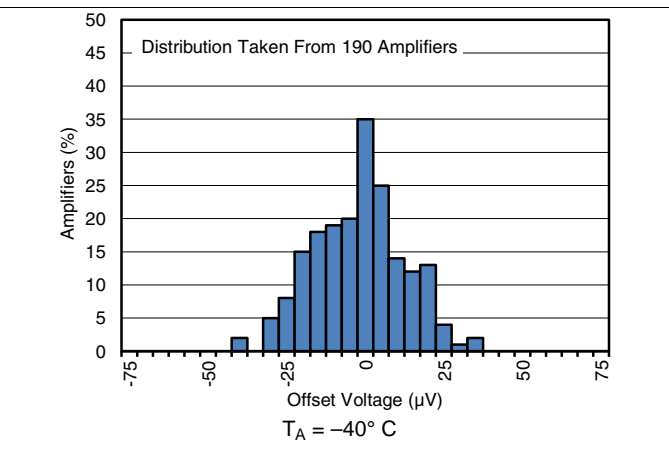


Figure 6. Offset Voltage Production Distribution at -40°C

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 18\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$, and $C_L = 100\text{ pF}$, (unless otherwise noted)

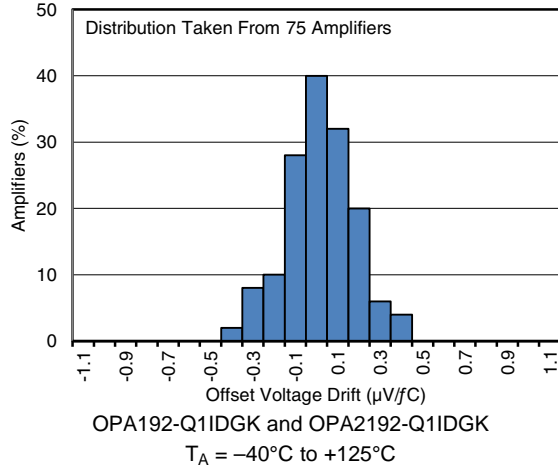


Figure 7. Offset Voltage Drift Distribution

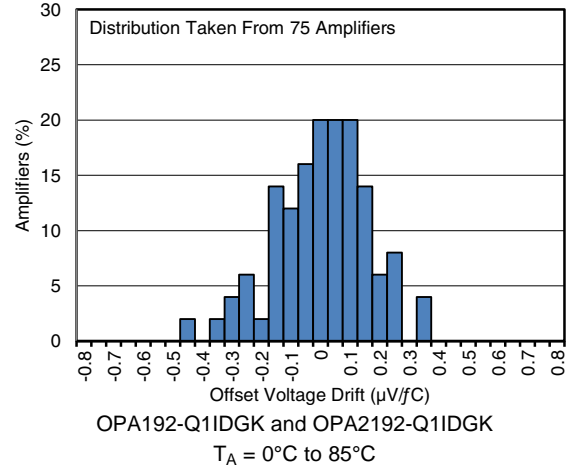


Figure 8. Offset Voltage Drift Distribution

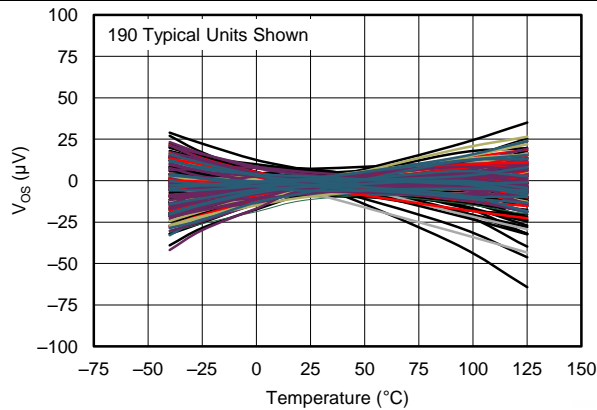


Figure 9. Offset Voltage vs Temperature

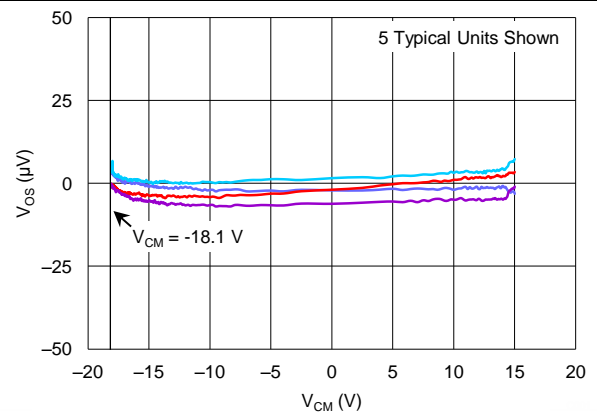


Figure 10. Offset Voltage vs Common-Mode Voltage

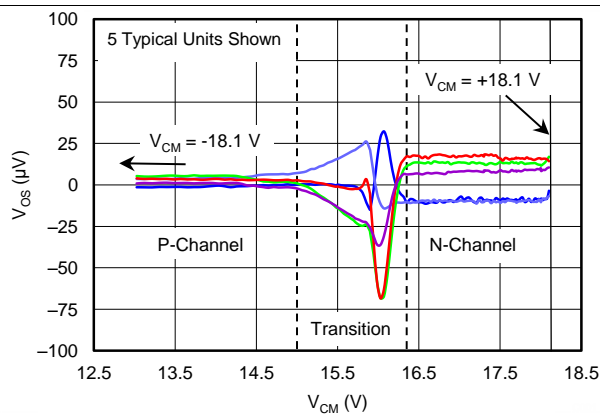


Figure 11. Offset Voltage vs Common-Mode Voltage

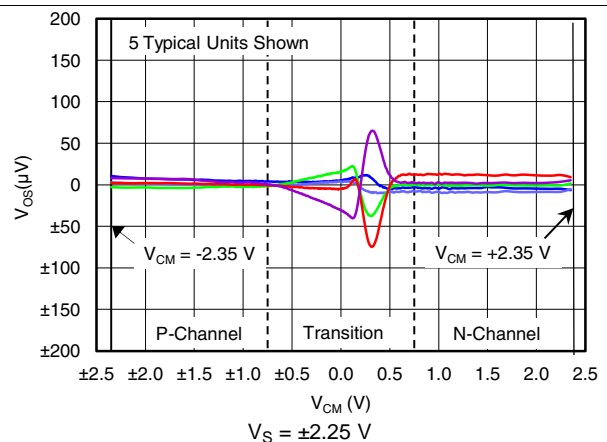


Figure 12. Offset Voltage vs Common-Mode Voltage

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 18\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$, and $C_L = 100\text{ pF}$, (unless otherwise noted)

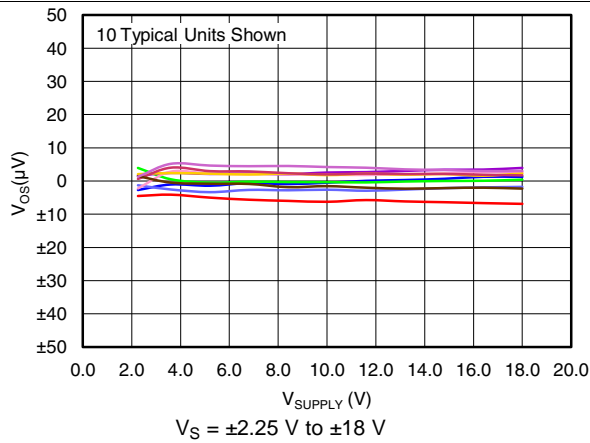


Figure 13. Offset Voltage vs Power Supply

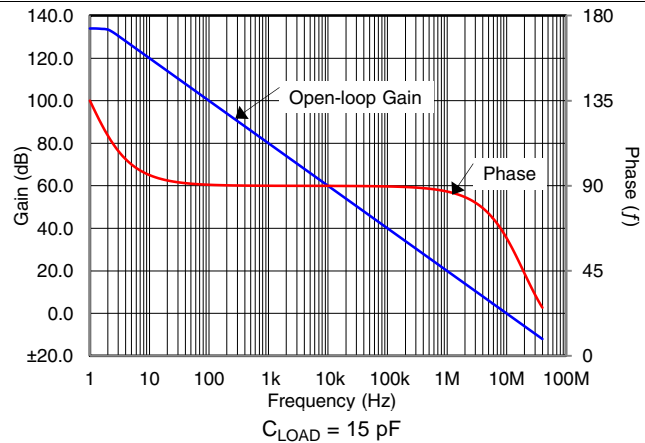


Figure 14. Open-Loop Gain and Phase vs Frequency

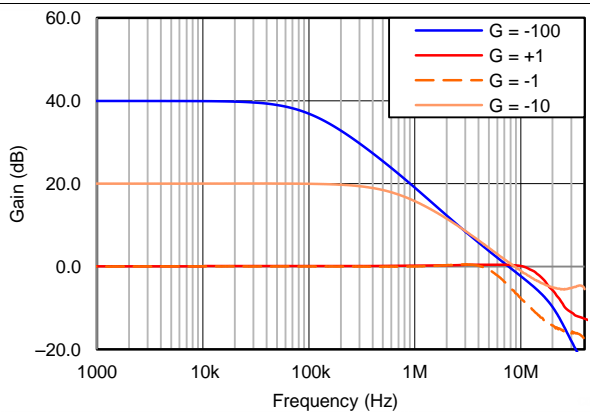


Figure 15. Closed-Loop Gain and Phase vs Frequency

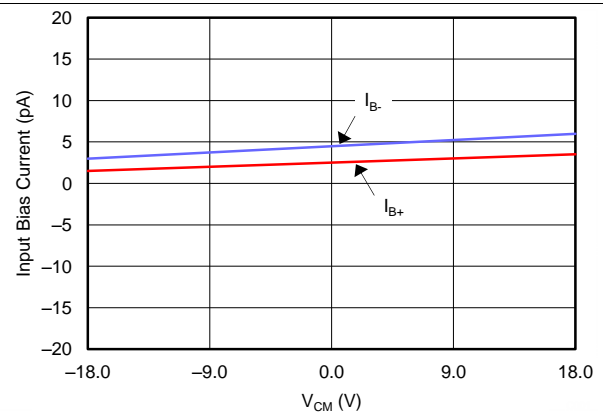


Figure 16. Input Bias Current vs Common-Mode Voltage

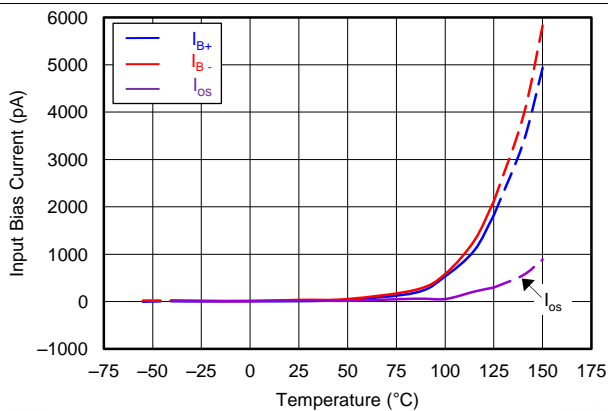


Figure 17. Input Bias Current vs Temperature

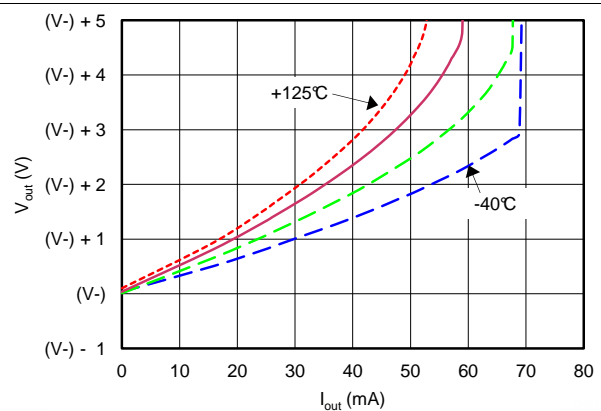


Figure 18. Output Voltage Swing vs Output Current (Maximum Supply)

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 18\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$, and $C_L = 100\text{ pF}$, (unless otherwise noted)

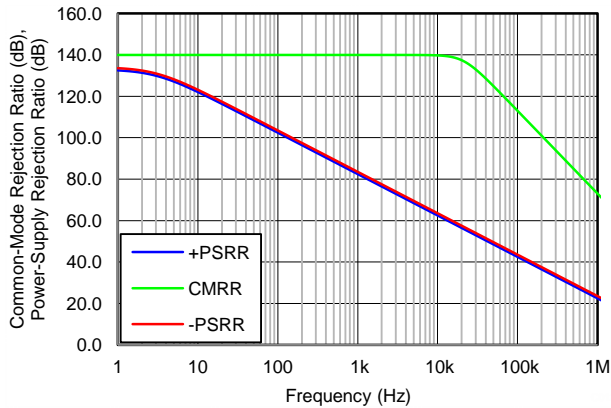


Figure 19. CMRR and PSRR vs Frequency

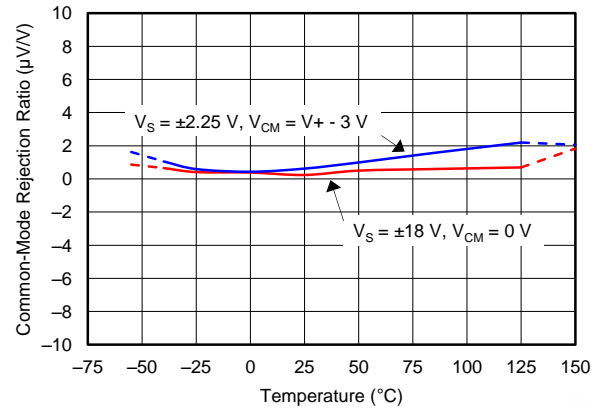


Figure 20. CMRR vs Temperature

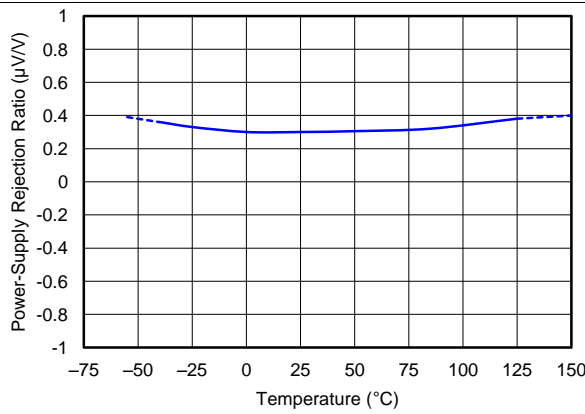


Figure 21. PSRR vs Temperature

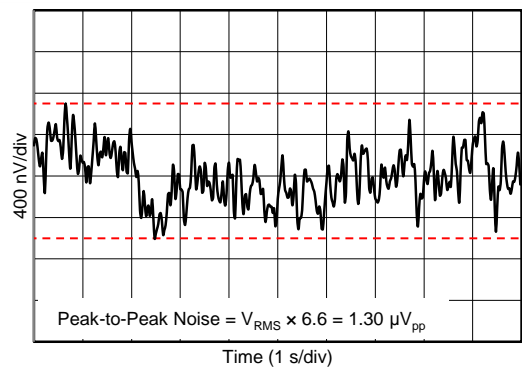


Figure 22. 0.1-Hz to 10-Hz Noise

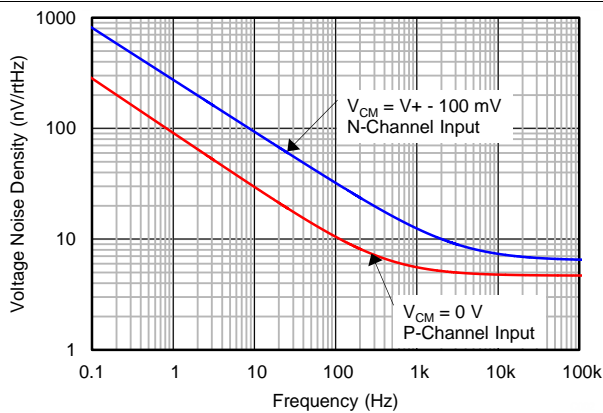


Figure 23. Input Voltage Noise Spectral Density vs Frequency

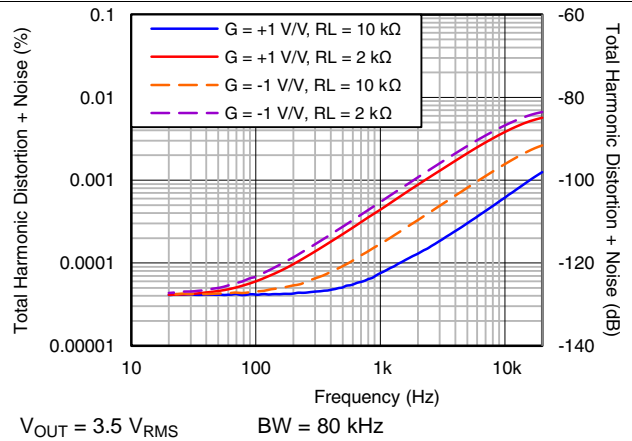


Figure 24. THD+N Ratio vs Frequency

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 18\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$, and $C_L = 100\text{ pF}$, (unless otherwise noted)

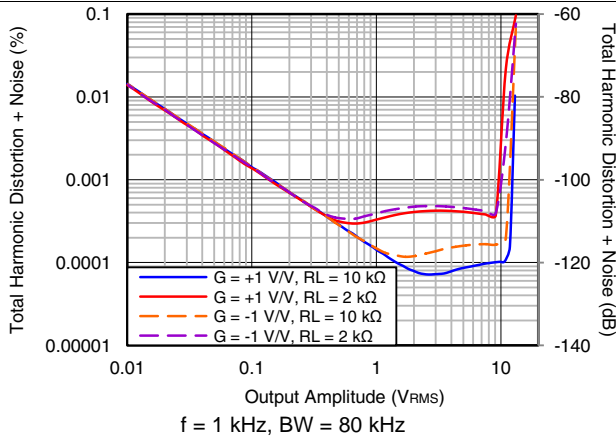


Figure 25. THD+N vs Output Amplitude

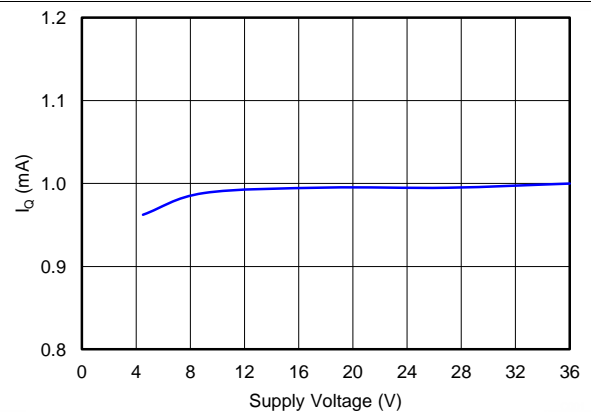


Figure 26. Quiescent Current vs Supply Voltage

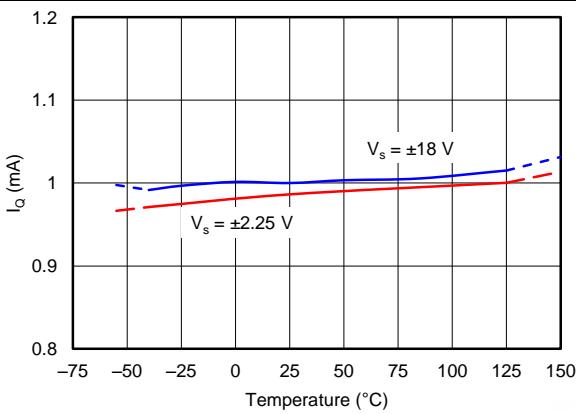


Figure 27. Quiescent Current vs Temperature

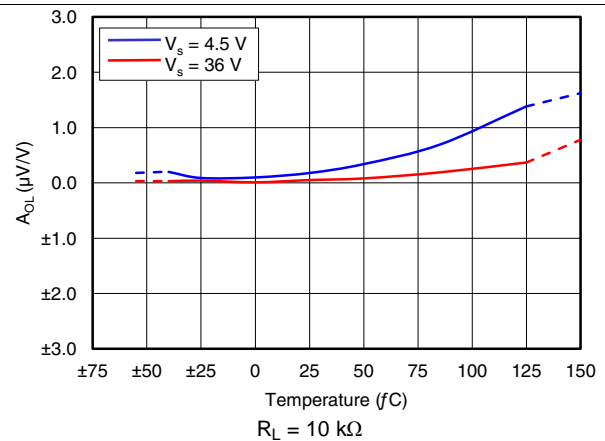


Figure 28. Open-Loop Gain vs Temperature

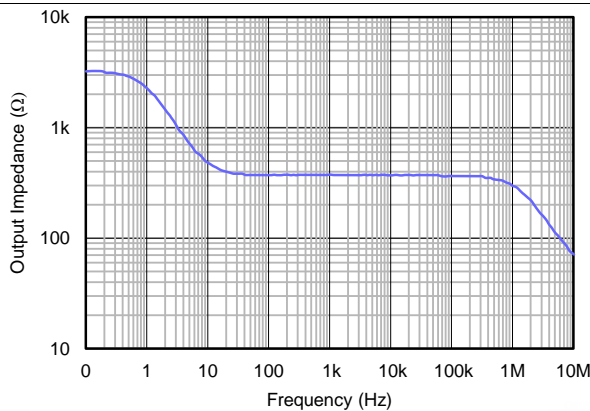


Figure 29. Open-Loop Output Impedance vs Frequency

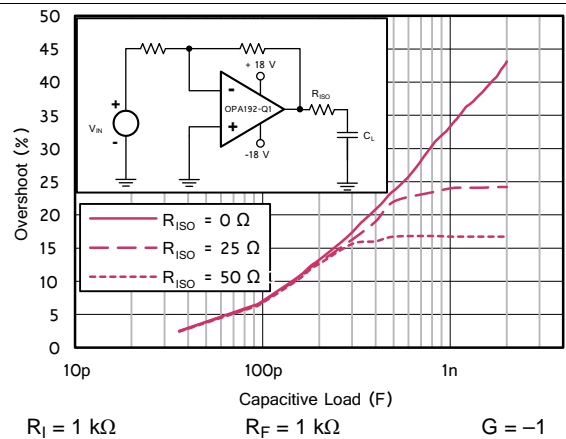


Figure 30. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 18\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$, and $C_L = 100\text{ pF}$, (unless otherwise noted)

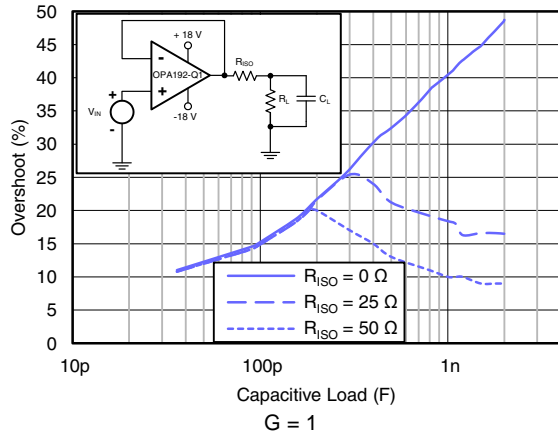


Figure 31. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

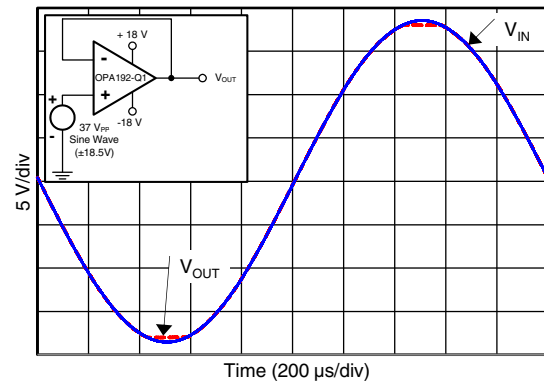


Figure 32. No Phase Reversal

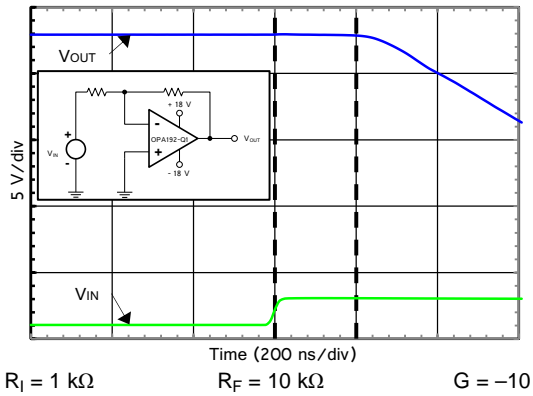


Figure 33. Positive Overload Recovery

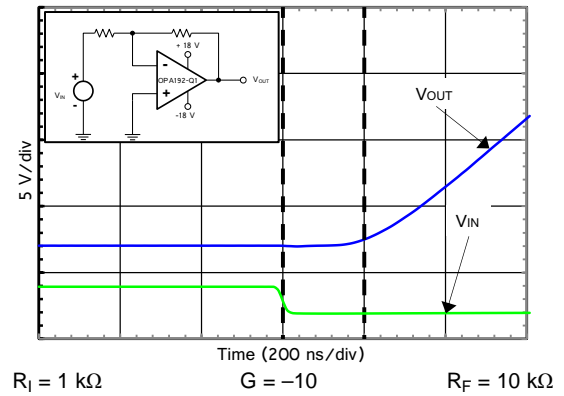


Figure 34. Negative Overload Recovery

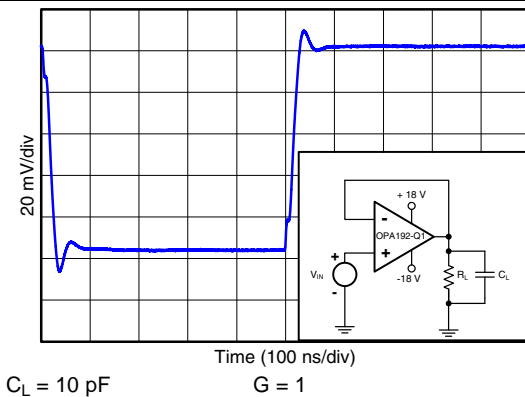


Figure 35. Small-Signal Step Response (100 mV)

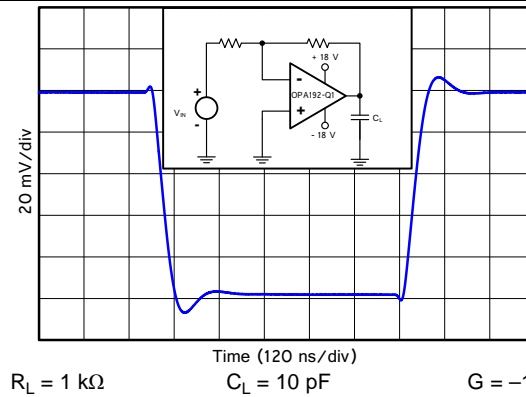


Figure 36. Small-Signal Step Response (100 mV)

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 18\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$, and $C_L = 100\text{ pF}$, (unless otherwise noted)

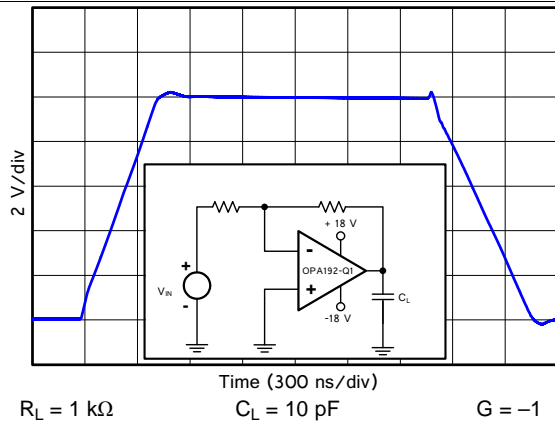


Figure 37. Large-Signal Step Response

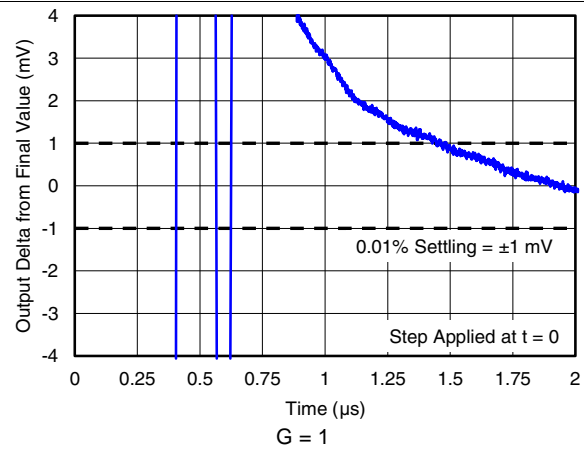


Figure 38. Settling Time (10-V Positive Step)

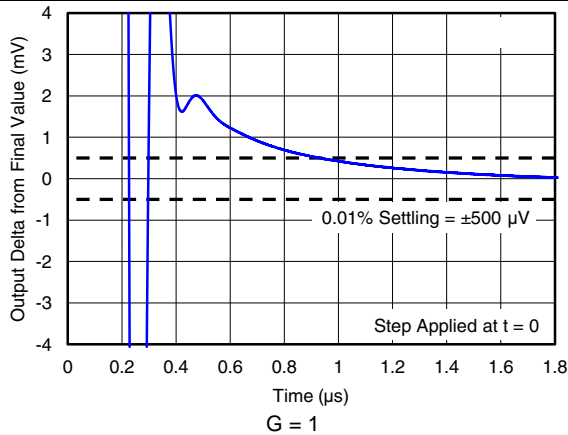


Figure 39. Settling Time (5-V Positive Step)

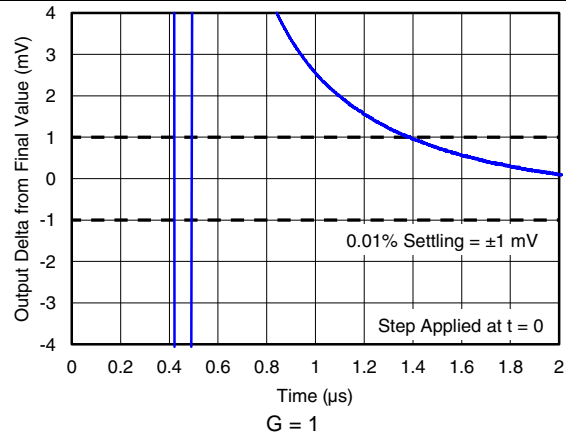


Figure 40. Settling Time (10-V Negative Step)

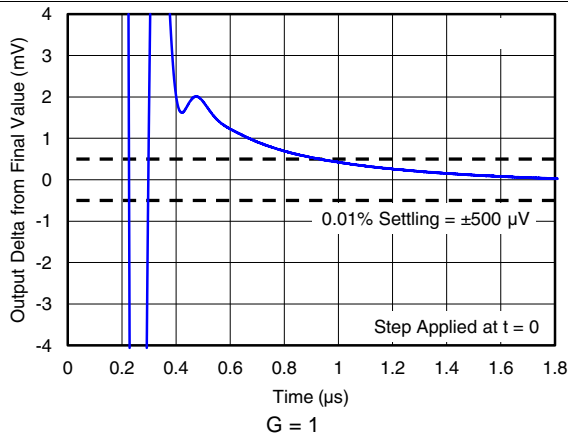


Figure 41. Settling Time (5-V Negative Step)

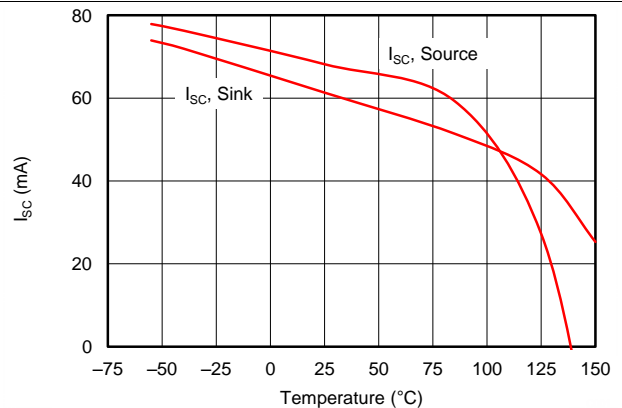


Figure 42. Short-Circuit Current vs Temperature

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 18\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$, and $C_L = 100\text{ pF}$, (unless otherwise noted)

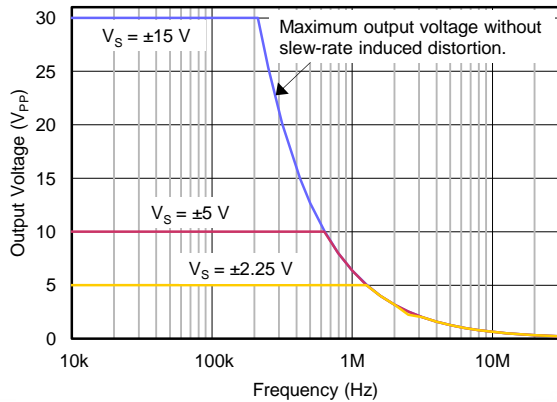


Figure 43. Maximum Output Voltage vs Frequency

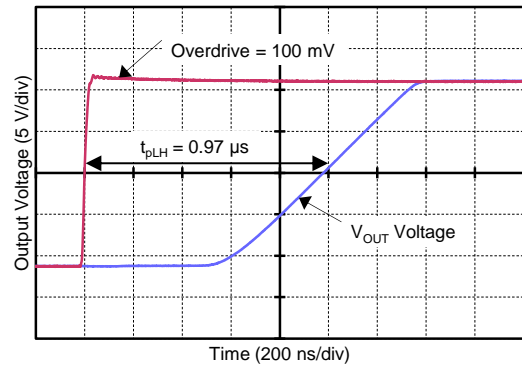


Figure 44. Propagation Delay Rising Edge

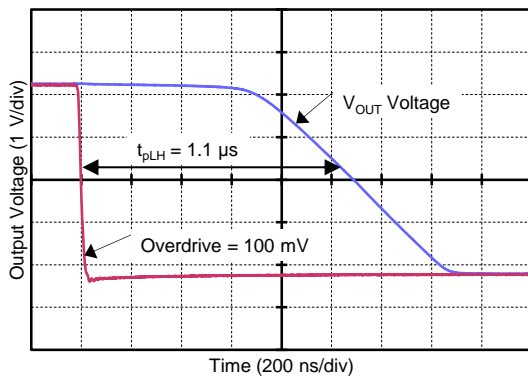


Figure 45. Propagation Delay Falling Edge

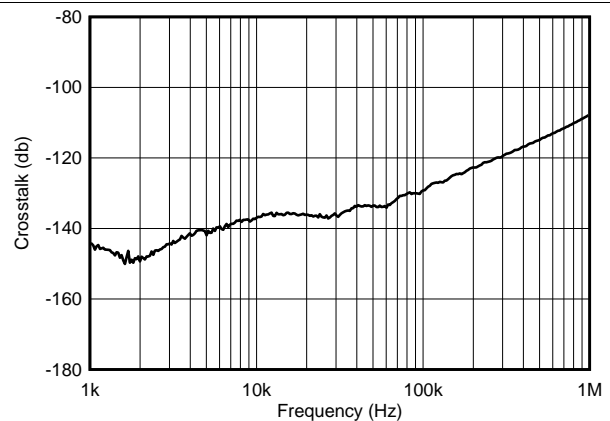


Figure 46. Crosstalk vs Frequency

7 Parameter Measurement Information

7.1 Input Offset Voltage Drift

The OPAx192-Q1 family of operational amplifiers is manufactured using TI's e-trim technology. Each amplifier input offset voltage and input offset voltage drift is trimmed in production, thereby minimizing errors associated with input offset voltage and input offset voltage drift. The e-trim technology is a TI proprietary method of trimming internal device parameters during either wafer probing or final testing. When trimming input offset voltage drift the systematic or linear drift error on each device is trimmed to zero. This results in the remaining errors associated with input offset drift are minimal and are the result from only nonlinear error sources. [Figure 47](#) illustrates this concept.

Input Offset Voltage Drift (continued)

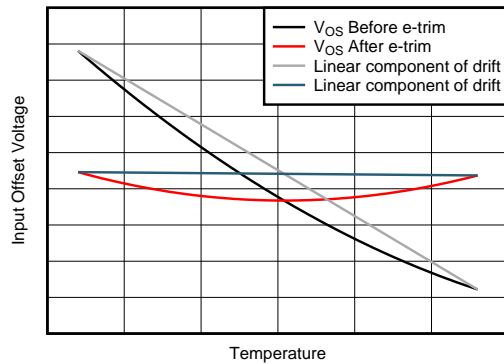


Figure 47. Input Offset Before and After Drift Trim

Figure 48 shows six typical units.

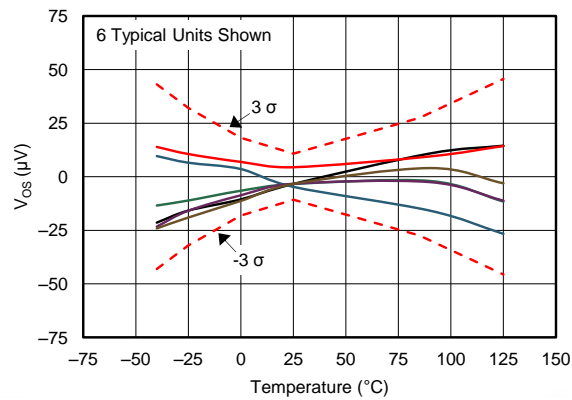


Figure 48. Input Offset Voltage Drift vs Temperature for Six Typical Units

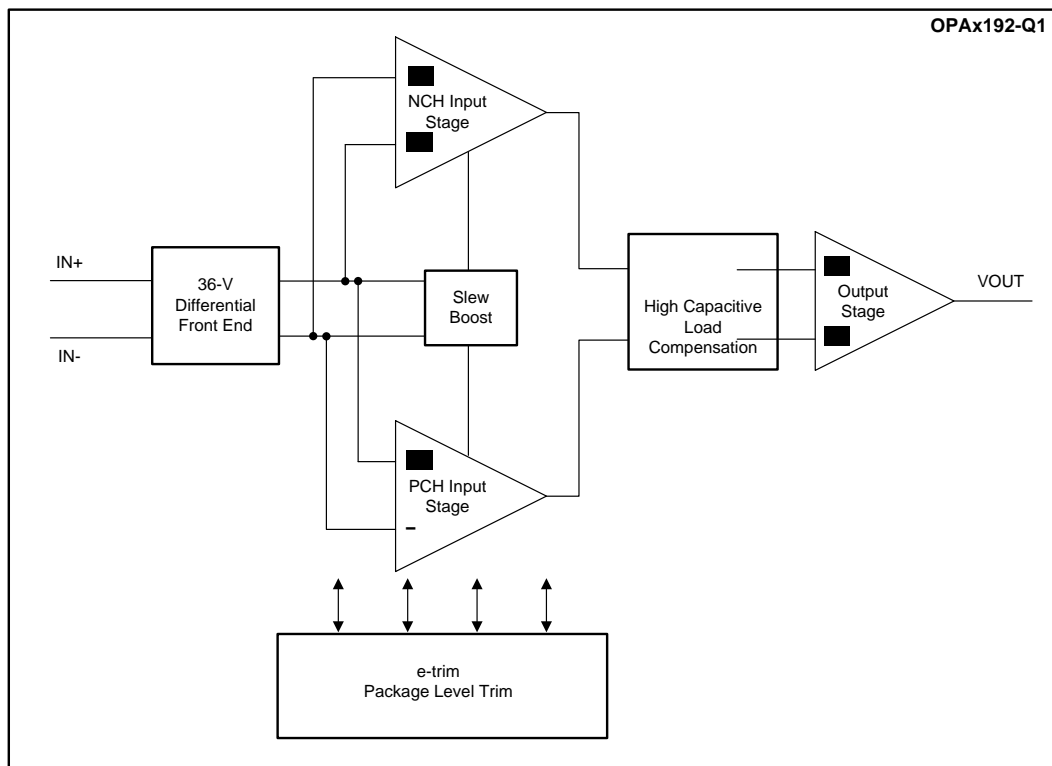
8 Detailed Description

8.1 Overview

The OPAx192-Q1 family of operational amplifiers use *e-trim*, a method of package-level trim for offset and offset temperature drift implemented during the final steps of manufacturing after the plastic molding process. This method minimizes the influence of inherent input transistor mismatch, as well as errors induced during package molding. The trim communication occurs on the output pin of the standard pinout, and after the trim points are set, further communication to the trim structure is permanently disabled. The [Functional Block Diagram](#) shows the simplified diagram of the OPAx192-Q1 with e-trim.

Unlike previous e-trim op amps, the OPAx192-Q1 uses a patented two-temperature trim architecture to achieve a very low offset voltage of 25 μV (maximum) and low voltage offset drift of 0.5 $\mu\text{V}/^\circ\text{C}$ (maximum) over the full specified temperature range. This level of precision performance at wide supply voltages makes these amplifiers useful for high-impedance industrial sensors, filters, and high-voltage data acquisition.

8.2 Functional Block Diagram

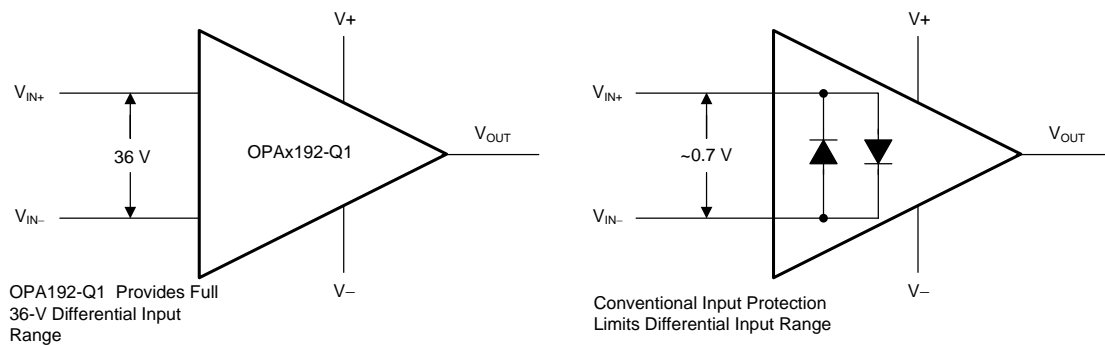


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8.3 Feature Description

8.3.1 Input Protection Circuitry

The OPAx192-Q1 uses a unique input architecture to eliminate the need for input protection diodes but still provides robust input protection under transient conditions. Conventional input diode protection schemes shown in Figure 49 can be activated by fast transient step responses and can introduce signal distortion and settling time delays because of alternate current paths, as shown in Figure 50. For low-gain circuits, these fast-ramping input signals forward-bias back-to-back diodes, causing an increase in input current, and resulting in extended settling time, as shown in Figure 51.



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Figure 49. OPAx192-Q1 Input Protection Does Not Limit Differential Input Capability

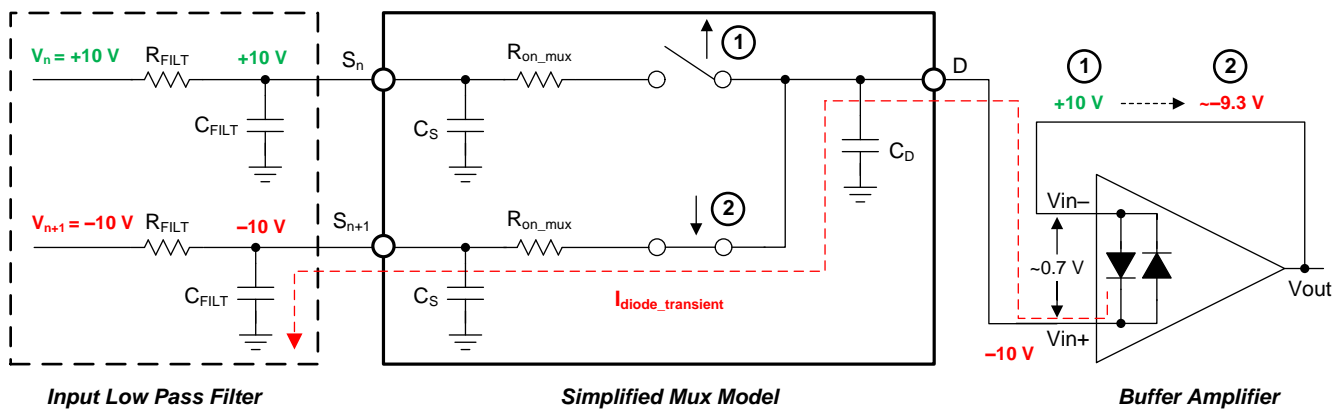


Figure 50. Back-to-Back Diodes Create Settling Issues

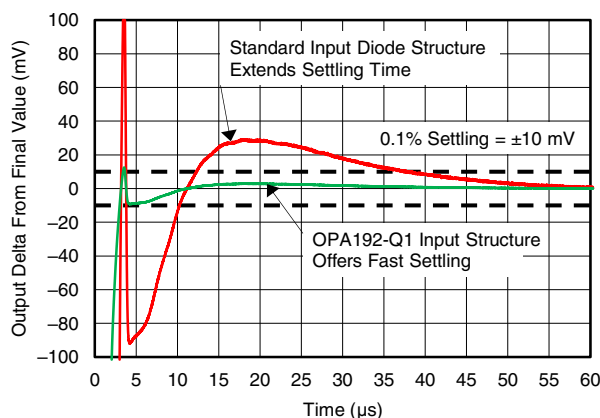


Figure 51. OPAx192-Q1 Protection Circuit Maintains Fast-Settling Transient Response

Feature Description (continued)

The OPAx192-Q1 family of operational amplifiers provides a true high-impedance differential input capability for high-voltage applications. This patented input protection architecture does not introduce additional signal distortion or delayed settling time, making the device an optimal op amp for multichannel, high-switched, input applications. The OPAx192-Q1 can tolerate a maximum differential swing (voltage between inverting and noninverting pins of the op amp) of up to 36 V, making the device suitable for use as a comparator or in applications with fast-ramping input signals such as multiplexed data-acquisition systems; see [Figure 61](#).

8.3.2 EMI Rejection

The OPAx192-Q1 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPAx192-Q1 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. [Figure 52](#) shows the results of this testing on the OPAx192-Q1. [Table 2](#) shows the EMIRR IN+ values for the OPAx192-Q1 at particular frequencies commonly encountered in real-world applications. Applications listed in [Table 2](#) may be centered on or operated near the particular frequency shown. Detailed information can also be found in the application report [EMI Rejection Ratio of Operational Amplifiers](#) available for download from [www.ti.com](#).

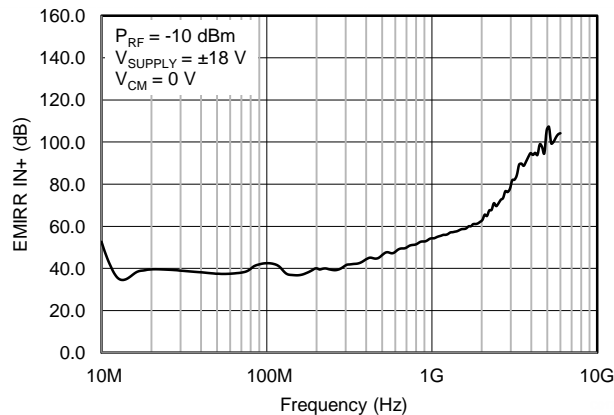


Figure 52. EMIRR Testing

Table 2. OPAx192-Q1 EMIRR IN+ For Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	44.1 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	52.8 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	61.0 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	69.5 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	88.7 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	105.5 dB

8.3.3 Phase Reversal Protection

The OPAx192-Q1 family has internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The OPAx192-Q1 is a rail-to-rail input op amp; therefore, the common-mode range can extend up to the rails. Input signals beyond the rails do not cause phase reversal; instead, the output limits into the appropriate rail. This performance is shown in Figure 53.

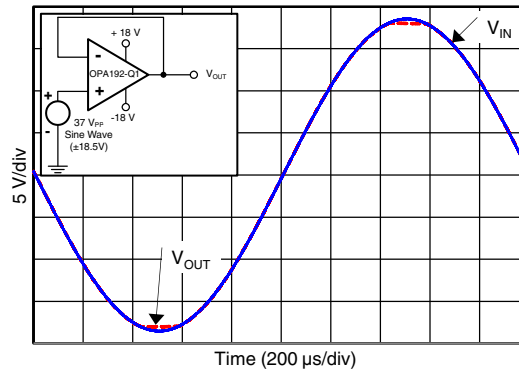
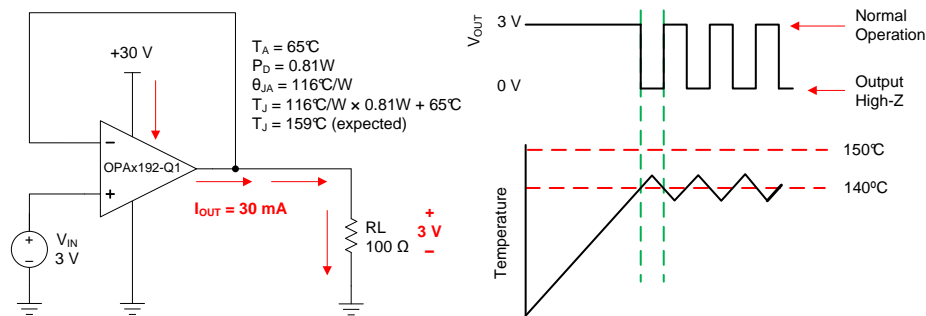


Figure 53. No Phase Reversal

8.3.4 Thermal Protection

The internal power dissipation of any amplifier causes its internal (junction) temperature to rise. This phenomenon is called *self heating*. The absolute maximum junction temperature of the OPAx192-Q1 is 150°C. Exceeding this temperature causes damage to the device. The OPAx192-Q1 has a thermal protection feature that prevents damage from self heating. The protection works by monitoring the temperature of the device and turning off the op amp output drive for temperatures above 140°C. Figure 54 shows an application example for the OPAx192-Q1 that has significant self heating (159°C) because of the power dissipation (0.81 W). Thermal calculations indicate that for an ambient temperature of 65°C the device junction temperature must reach 187°C. The actual device, however, turns off the output drive to maintain a safe junction temperature. Figure 54 shows how the circuit behaves during thermal protection. During normal operation, the device acts as a buffer so the output is 3 V. When self heating causes the device junction temperature to increase above 140°C, the thermal protection forces the output to a high-impedance state and the output is pulled to ground through resistor RL.



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Figure 54. Thermal Protection

8.3.5 Capacitive Load and Stability

The OPAx192-Q1 features a patented output stage capable of driving large capacitive loads, and in a unity-gain configuration, directly drives up to 1 nF of pure capacitive load. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads; see Figure 55 and Figure 56. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier is stable in operation.

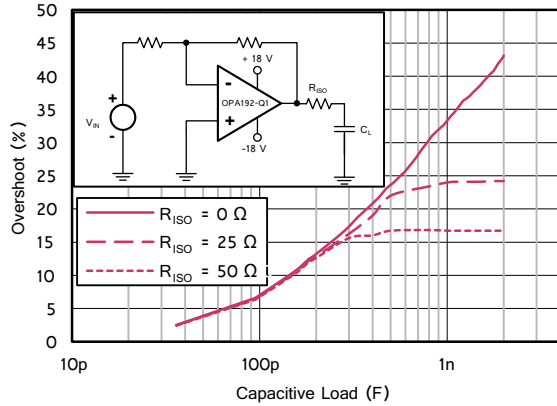


Figure 55. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

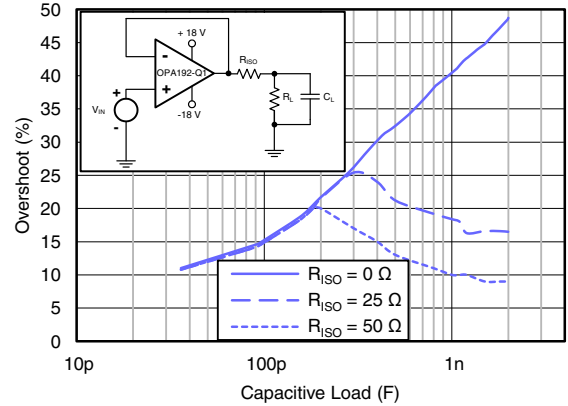


Figure 56. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

For additional drive capability in unity-gain configurations, improve capacitive load drive by inserting a small (10 Ω to 20 Ω) resistor, R_{ISO} , in series with the output, as shown in Figure 57. This resistor significantly reduces ringing and maintains dc performance for purely capacitive loads. However, if a resistive load is in parallel with the capacitive load, then a voltage divider is created, thus introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_{ISO} / R_L , and is generally negligible at low output levels. A high capacitive-load drive makes the OPAx192-Q1 work well with applications such as reference buffers, MOSFET gate drives, and cable-shield drives. The circuit shown in Figure 57 uses an isolation resistor, R_{ISO} , to stabilize the output of an op amp. R_{ISO} modifies the open-loop gain of the system for increased phase margin, and results using the OPAx192-Q1 are summarized in Table 3. For additional information on techniques to optimize and design using this circuit, TI Precision Design [Capacitive Load Drive Solution using an Isolation Resistor](#) details complete design goals, simulation, and test results.

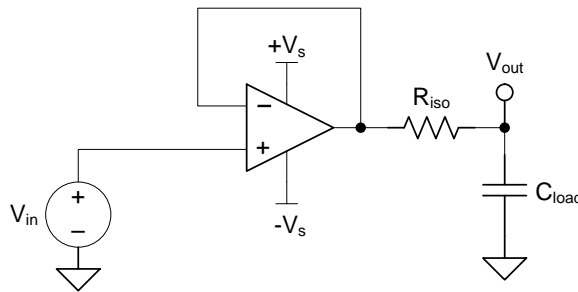


Figure 57. Extending Capacitive Load Drive with the OPAx192-Q1

Table 3. OPAx192-Q1 Capacitive Load Drive Solution Using Isolation Resistor Comparison of Calculated and Measured Results

PARAMETER	VALUE										
	100 pF		1000 pF		0.01 μF		0.1 μF		1 μF		
Capacitive Load	100 pF		1000 pF		0.01 μF		0.1 μF		1 μF		
Phase Margin	45°	60°	45°	60°	45°	60°	45°	60°	45°	60°	
R_{ISO} (Ω)	47	360	24	100	20	51	6.2	15.8	2	4.7	
Measured Overshoot (%)	23.2	8.6	10.4	22.5	9.0	22.1	8.7	23.1	8.6	21	8.6
Calculated PM	45.1°	58.1°	45.8°	59.7°	46.1°	60.1°	45.2°	60.2°	47.2°	60.2°	



For step-by-step design procedure, circuit schematics, bill of materials, printed circuit board (PCB) files, simulation results, and test results, refer to TI Precision Design TIDU032, [Capacitive Load Drive Solution using an Isolation Resistor](#).

8.3.6 Common-Mode Voltage Range

The OPAx192-Q1 is a 36-V, true rail-to-rail input operational amplifier with an input common-mode range that extends 100 mV beyond either supply rail. This wide range is achieved with paralleled complementary N-channel and P-channel differential input pairs, as shown in Figure 58. The N-channel pair is active for input voltages close to the positive rail, typically $(V+) - 3\text{ V}$ to 100 mV above the positive supply. The P-channel pair is active for inputs from 100 mV below the negative supply to approximately $(V+) - 1.5\text{ V}$. There is a small transition region, typically $(V+) - 3\text{ V}$ to $(V+) - 1.5\text{ V}$ in which both input pairs are on. This transition region can vary modestly with process variation, and within this region PSRR, CMRR, offset voltage, offset drift, noise and THD performance may be degraded compared to operation outside this region.

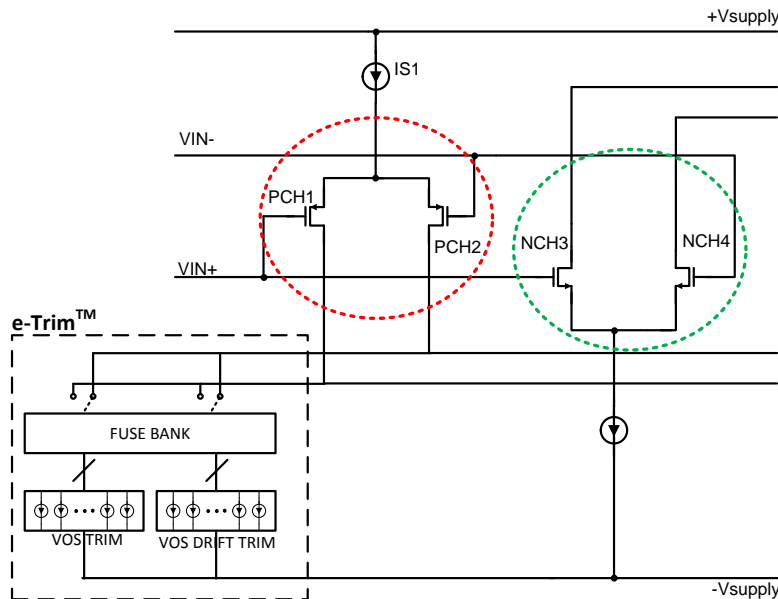


Figure 58. Rail-to-Rail Input Stage

To achieve the best performance for two-stage rail-to-rail input amplifiers, avoid the transition region when possible. The OPAx192-Q1 uses a precision trim for both the N-channel and P-channel regions. This technique enables significantly lower levels of offset than previous-generation devices, causing variance in the transition region of the input stages to appear exaggerated relative to offset over the full common-mode range, as shown in Figure 59.

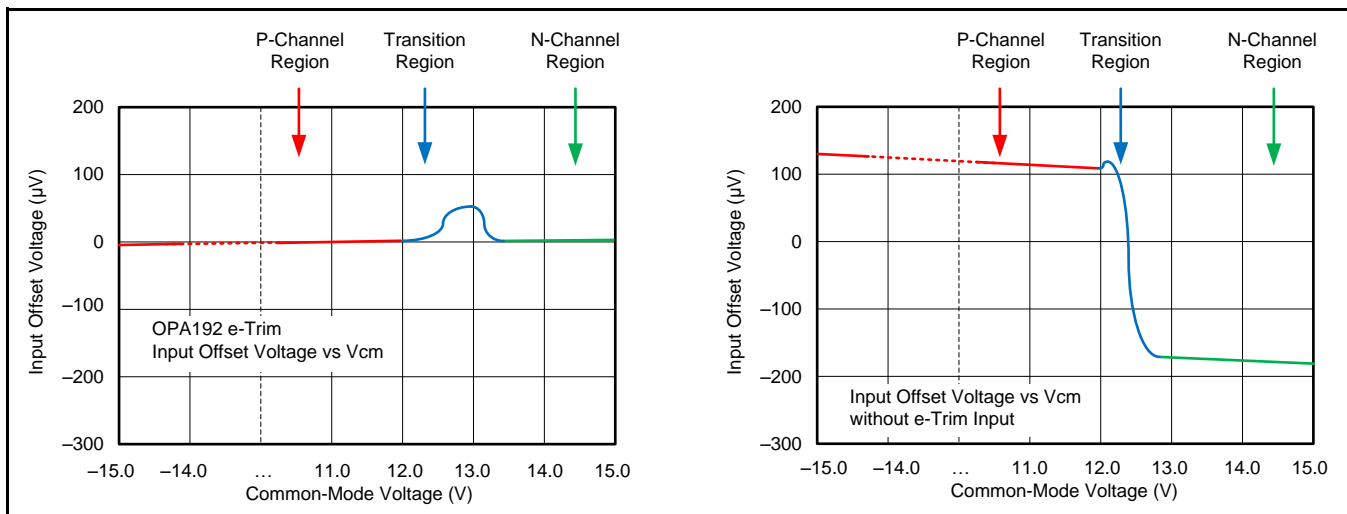
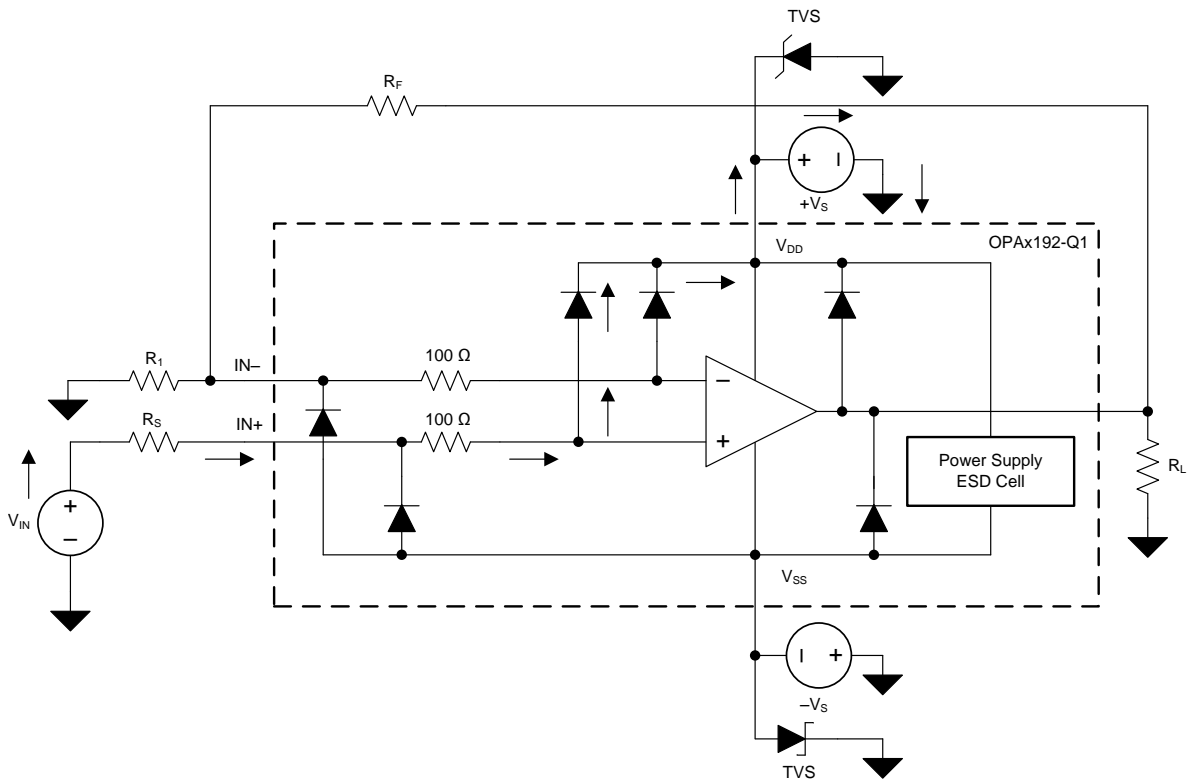


Figure 59. Common-Mode Transition vs Standard Rail-to-Rail Amplifiers

8.3.7 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress (EOS). These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. Figure 60 shows an illustration of the ESD circuits contained in the OPAX192-Q1 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device or the power-supply ESD cell, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.



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Figure 60. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event is very short in duration and very high voltage (for example, 1 kV, 100 ns), whereas an EOS event is long duration and lower voltage (for example, 50 V, 100 ms). The ESD diodes are designed for out-of-circuit ESD protection (that is, during assembly, test, and storage of the device before being soldered to the PCB). During an ESD event, the ESD signal is passed through the ESD steering diodes to an absorption circuit (labeled ESD power-supply circuit). The ESD absorption circuit clamps the supplies to a safe level.

Although this behavior is necessary for out-of-circuit protection, excessive current and damage is caused if activated in-circuit. A transient voltage suppressors (TVS) can be used to prevent against damage caused by turning on the ESD absorption circuit during an in-circuit ESD event. Using the appropriate current limiting resistors and TVS diodes allows for the use of device ESD diodes to protect against EOS events.

8.3.8 Overload Recovery

Overload recovery is defined as the time required for the op amp output to recover from a saturated state to a linear state. The output devices of the op amp enter a saturation region when the output voltage exceeds the rated operating voltage, either due to the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the OPAx192-Q1 is approximately 200 ns.

8.4 Device Functional Modes

The OPAx192-Q1 has a single functional mode and is operational when the power-supply voltage is greater than 4.5 V (± 2.25 V). The maximum power supply voltage for the OPAx192-Q1 is 36 V (± 18 V).

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

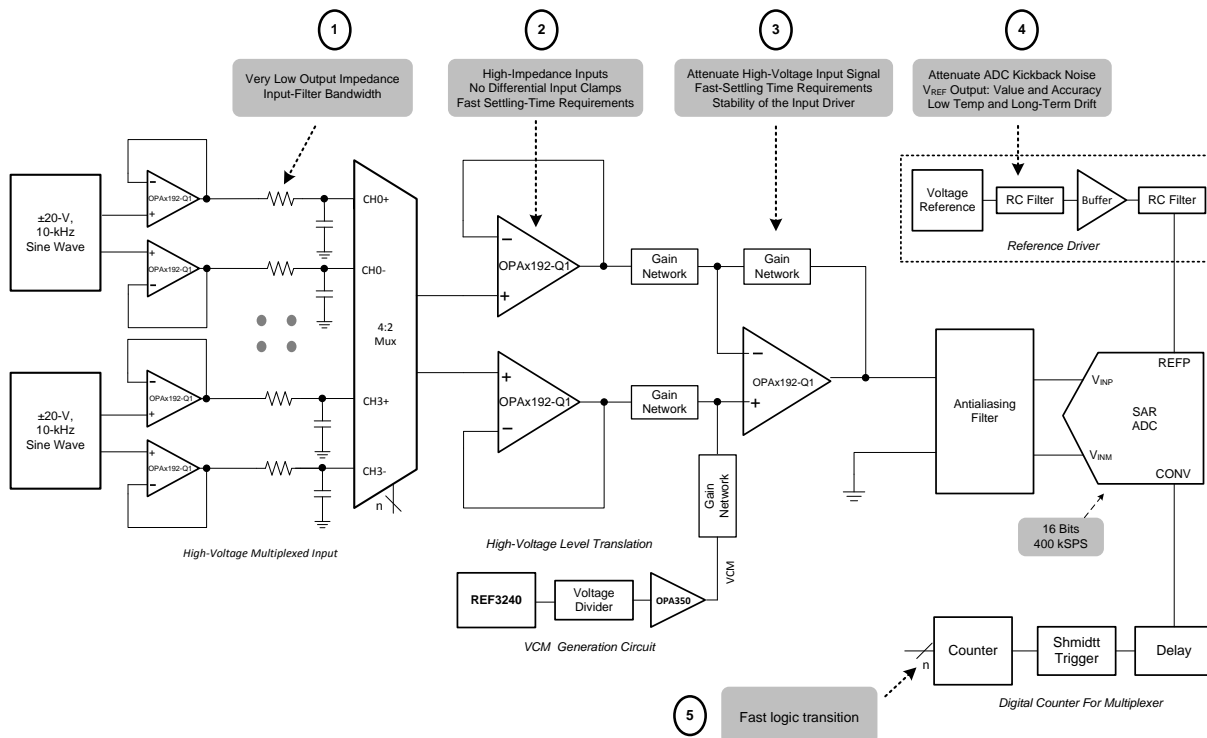
9.1 Application Information

The OPAx192-Q1 family offers outstanding dc precision and ac performance. These devices operate up to 36-V supply rails and offer true rail-to-rail input and output, ultra-low offset voltage and offset voltage drift, as well as 10-MHz bandwidth and high capacitive load drive. These features make the OPAx192-Q1 a robust, high-performance operational amplifier for high-voltage industrial applications.

9.2 Typical Applications

9.2.1 16-Bit Precision Multiplexed Data-Acquisition System

Figure 61 shows a 16-bit, differential, 4-channel, multiplexed data-acquisition system. This example is typical in industrial applications that require low distortion and a high-voltage differential input. The circuit uses the ADS8864, a 16-bit, 400-kSPS successive-approximation-resistor (SAR) analog-to-digital converter (ADC), along with a precision, high-voltage, signal-conditioning front end, and a 4-channel differential multiplexer (mux). This TI Precision Design details the process for optimizing the precision, high-voltage, front-end drive circuit using the OPAx192-Q1 and OPA140 to achieve excellent dynamic performance and linearity with the ADS8864.



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Figure 61. OP Ax192-Q1 in 16-Bit, 400-kSPS, 4-Channel, Multiplexed Data Acquisition System for High-Voltage Inputs With Lowest Distortion

Typical Applications (continued)

9.2.1.1 Design Requirements

The primary objective is to design a ± 20 V, differential 4-channel multiplexed data acquisition system with lowest distortion using the 16-bit ADS8864 at a throughput of 400 kSPS for a 10 kHz full-scale pure sine-wave input. The design requirements for this block design are:

- System Supply Voltage: ± 15 V
- ADC Supply Voltage: 3.3 V
- ADC Sampling Rate: 400 kSPS
- ADC Reference Voltage (REFP): 4.096 V
- System Input Signal: A high-voltage differential input signal with a peak amplitude of 10 V and frequency (f_{IN}) of 10 kHz are applied to each differential input of the mux.

9.2.1.2 Detailed Design Procedure

The purpose of this precision design is to design an optimal high voltage multiplexed data acquisition system for highest system linearity and fast settling. The overall system block diagram is illustrated in [Figure 61](#). The circuit is a multichannel data acquisition signal chain consisting of an input low-pass filter, multiplexer (mux), mux output buffer, attenuating SAR ADC driver, digital counter for mux and the reference driver. The architecture allows fast sampling of multiple channels using a single ADC, providing a low-cost solution. The two primary design considerations to maximize the performance of a precision multiplexed data acquisition system are the mux input analog front-end and the high-voltage level translation SAR ADC driver design. However, carefully design each analog circuit block based on the ADC performance specifications in order to achieve the fastest settling at 16-bit resolution and lowest distortion system. The diagram includes the most important specifications for each individual analog block.

This design systematically approaches each analog circuit block to achieve a 16-bit settling for a full-scale input stage voltage and linearity for a 10-kHz sinusoidal input signal at each input channel. The first step in the design is to understand the requirement for extremely low impedance input-filter design for the mux. This understanding helps in the decision of an appropriate input filter and selection of a mux to meet the system settling requirements. The next important step is the design of the attenuating analog front-end (AFE) used to level translate the high-voltage input signal to a low-voltage ADC input when maintaining amplifier stability. The next step is to design a digital interface to switch the mux input channels with minimum delay. The final design challenge is to design a high-precision, reference-driver circuit that provides the required REFP reference voltage with low offset, drift, and noise contributions.

9.2.1.3 Application Curve

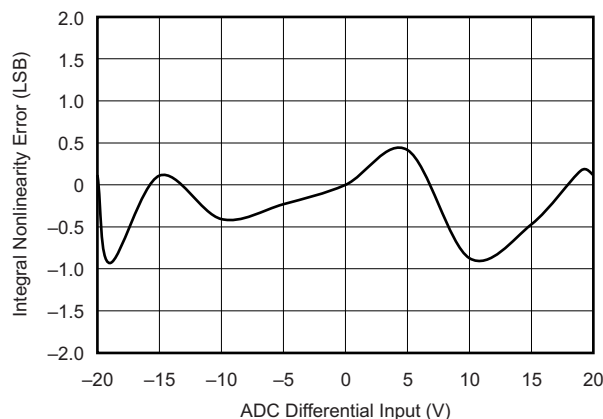


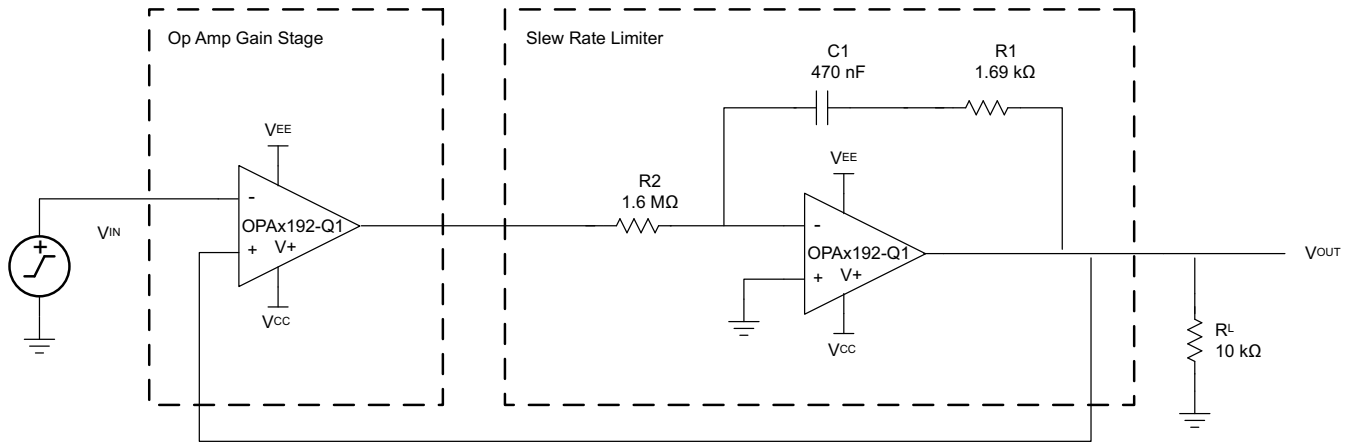
Figure 62. ADC 16-Bit Linearity Error for the Multiplexed Data Acquisition Block



For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, refer to [TI Precision Design TIDU181, 16-bit, 400-kSPS, 4-Channel, Multiplexed Data Acquisition System for High Voltage Inputs with Lowest Distortion](#).

9.2.2 Slew Rate Limit for Input Protection

In control systems for valves or motors, abrupt changes in voltages or currents can cause mechanical damages. By controlling the slew rate of the command voltages into the drive circuits, the load voltages ramps up and down at a safe rate. For symmetrical slew-rate applications (positive slew rate equals negative slew rate), one additional op amp provides slew-rate control for a given analog gain stage. The unique input protection and high output current and slew rate of the OPAx192-Q1 make the device an optimal amplifier to achieve slew rate control for both dual- and single-supply systems. [Figure 63](#) shows the OPAx192-Q1 in a slew-rate limit design.



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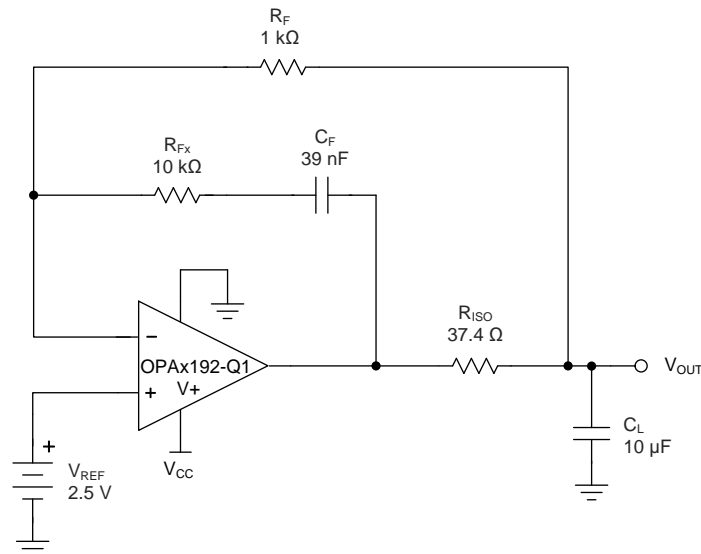
Figure 63. Slew Rate Limiter Uses One Op Amp



For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, see [TI Precision Design TIDU026, Slew Rate Limiter Uses One Op Amp](#).

9.2.3 Precision Reference Buffer

The OPAx192-Q1 features high output current drive capability and low input offset voltage, making the device an excellent reference buffer to provide an accurate buffered output with ample drive current for transients. For the 10- μ F ceramic capacitor shown in [Figure 64](#), R_{ISO} , a 37.4- Ω isolation resistor, provides separation of two feedback paths for optimal stability. Feedback path number one is through R_F and is directly at the output (V_{OUT}). Feedback path number two is through R_{FX} and C_F and is connected at the output of the op amp. The optimized stability components shown for the 10- μ F load give a closed-loop signal bandwidth at V_{OUT} of 4 kHz and still provides a loop gain phase margin of 89°. Any other load capacitances require recalculation of the stability components: R_F , R_{FX} , C_F , and R_{ISO} .



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Figure 64. Precision Reference Buffer

10 Power-Supply Recommendations

The OPAx192-Q1 is specified for operation from 4.5 V to 36 V (± 2.25 V to ± 18 V); many specifications apply from -40°C to $+125^{\circ}\text{C}$. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in [Typical Characteristics](#).

CAUTION

Supply voltages larger than 40 V can permanently damage the device; see [Absolute Maximum Ratings](#).

Place 0.1- μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see [Layout](#).

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
 - Connect low-ESR, 0.1- μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. .
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in [Figure 66](#), keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, TI recommends baking the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

11.2 Layout Example

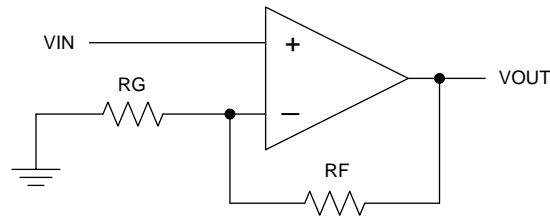
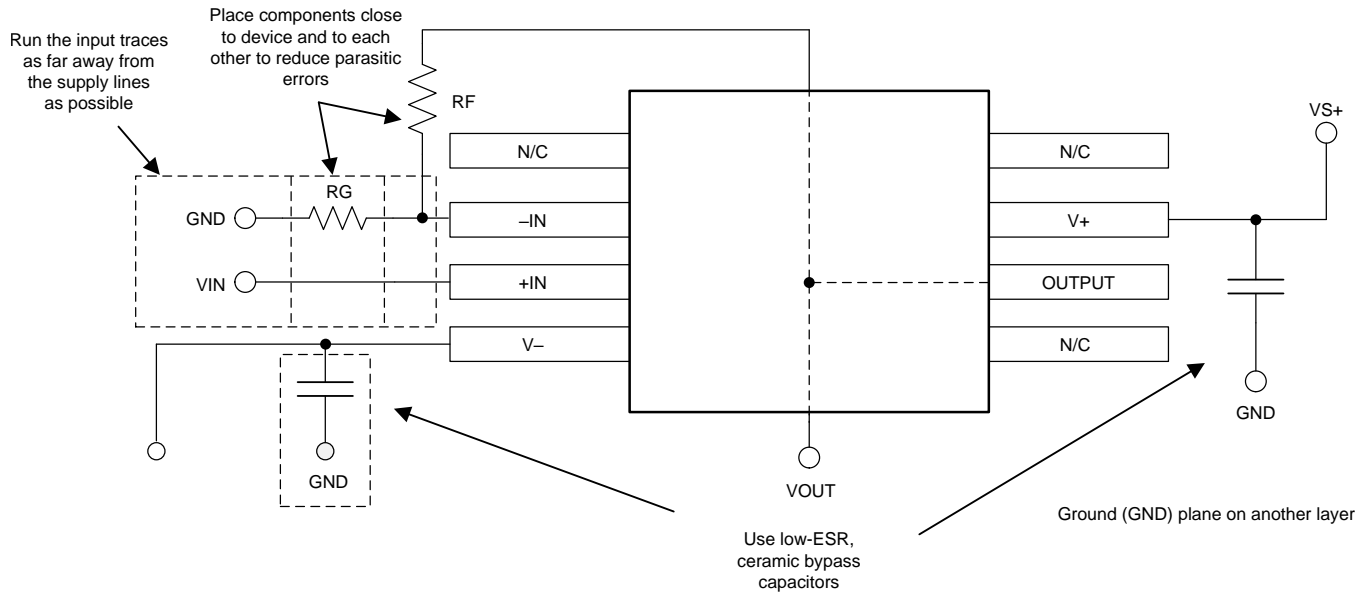


Figure 65. Schematic Representation



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Figure 66. Operational Amplifier Board Layout for Noninverting Configuration

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a [free download](#) from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the [TINA-TI folder](#).

12.1.1.2 TI Precision Designs

The OPA192 is featured in several Texas Instruments (TI) Precision Designs, available online at <http://www.ti.com/ww/en/analog/precision-designs/>. TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits.

12.2 Related Links

[Table 4](#) lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
OPA192-Q1	Click here	Click here	Click here	Click here	Click here
OPA2192-Q1	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

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Bluetooth is a registered trademark of Bluetooth SIG, Inc.

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12.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA192QDGKRQ1	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	192
OPA192QDGKRQ1.B	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	192
OPA2192QDGKRQ1	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2192
OPA2192QDGKRQ1.B	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2192

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF OPA192-Q1, OPA2192-Q1 :

- Catalog : [OPA192](#), [OPA2192](#)

NOTE: Qualified Version Definitions:

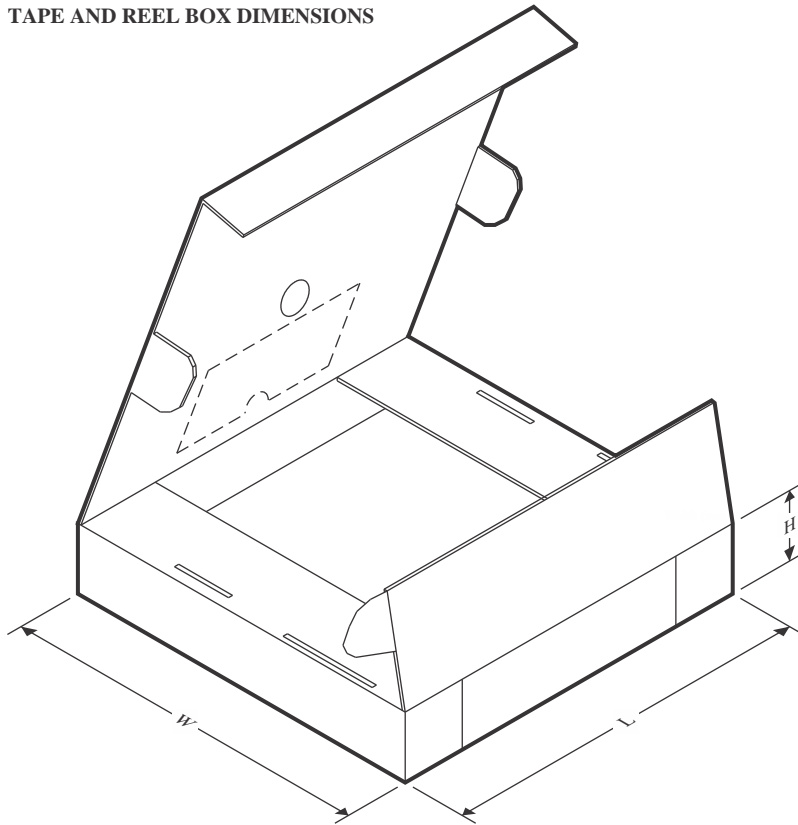
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA192QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2192QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA192QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2192QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0

DGK0008A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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