



Burr-Brown Products  
from Texas Instruments



OPA734, OPA2734  
OPA735, OPA2735

SBOS282B – DECEMBER 2003 – REVISED FEBRUARY 2005

# 0.05 $\mu$ V/°C max, SINGLE-SUPPLY CMOS OPERATIONAL AMPLIFIERS Zero-Drift Series

## FEATURES

- LOW OFFSET VOLTAGE: 5 $\mu$ V (max)
- ZERO DRIFT: 0.05 $\mu$ V/°C max
- QUIESCENT CURRENT: 750 $\mu$ A (max)
- SINGLE-SUPPLY OPERATION
- LOW BIAS CURRENT: 200pA (max)
- SHUTDOWN
- MicroSIZE PACKAGES
- WIDE SUPPLY RANGE: 2.7V to 12V

## APPLICATIONS

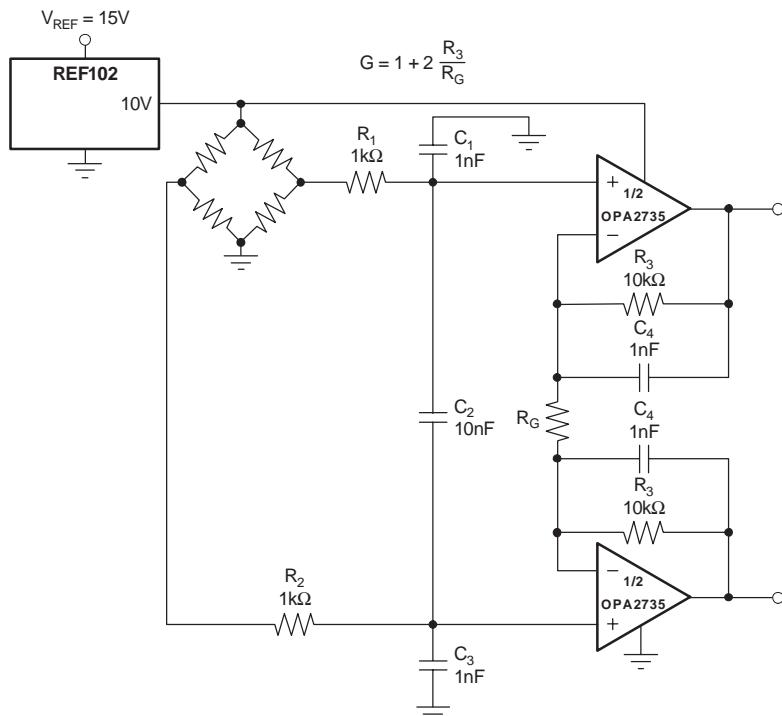
- TRANSDUCER APPLICATIONS
- TEMPERATURE MEASUREMENTS
- ELECTRONIC SCALES
- MEDICAL INSTRUMENTATION
- BATTERY-POWERED INSTRUMENTS
- HANDHELD TEST EQUIPMENT

## DESCRIPTION

The OPA734 and OPA735 series of CMOS operational amplifiers use auto-zeroing techniques to simultaneously provide low offset voltage (5 $\mu$ V max) and near-zero drift over time and temperature. These miniature, high-precision, low quiescent current amplifiers offer high input impedance and rail-to-rail output swing within 50mV of the rails. Either single or bipolar supplies can be used in the range of +2.7V to +12V ( $\pm$ 1.35V to  $\pm$ 6V). They are optimized for low-voltage, single-supply operation.

The OPA734 family includes a shutdown mode. Under logic control, the amplifiers can be switched from normal operation to a standby current that is 9 $\mu$ A (max) and the output placed in a high-impedance state.

The single version is available in the MicroSIZE SOT23-5 (SOT23-6 for shutdown version) and the SO-8 packages. The dual version is available in the MSOP-8 and SO-8 packages (MSOP-10 only for the shutdown version). All versions are specified for operation from -40°C to +85°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

## ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage	.....	+13.2V
Signal Input Terminals, Voltage <sup>(2)</sup>	..... (V-) – 0.5V to (V+) + 0.5V	
Current <sup>(2)</sup>	.....	±10mA
Output Short Circuit <sup>(3)</sup>	.....	Continuous
Operating Temperature	.....	–40°C to +150°C
Storage Temperature	.....	–65°C to +150°C
Junction Temperature	.....	+150°C
Lead Temperature (soldering, 10s)	.....	+300°C
ESD Rating (Human Body Model), OPA734	.....	1000V
ESD Rating (Human Body Model), OPA735, OPA2734, OPA2735	.....	2000V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less.

(3) Short-circuit to ground, one amplifier per package.

## PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
<b>Shutdown Version</b>						
OPA734	SOT23-6	DBV	–40°C to +85°C	NSB	OPA734AIDBV	Tape and Reel, 250
"	"	"	"	"	OPA734AIDBV	Tape and Reel, 3000
OPA734	SO-8	D	–40°C to +85°C	OPA734A	OPA734AID	Rails, 100
"	"	"	"	"	OPA734AIDR	Tape and Reel, 2500
OPA2734	MSOP-10	DGS	–40°C to +85°C	BGO	OPA2734AIDGST	Tape and Reel, 250
"	"	"	"	"	OPA2734AIDGSR	Tape and Reel, 2500
<b>Non-Shutdown Version</b>						
OPA735	SOT23-5	DBV	–40°C to +85°C	NSC	OPA735AIDBV	Tape and Reel, 250
"	"	"	"	"	OPA735AIDBV	Tape and Reel, 3000
OPA735	SO-8	D	–40°C to +85°C	OPA735A	OPA735AID	Rails, 100
"	"	"	"	"	OPA735AIDR	Tape and Reel, 2500
OPA2735	SO-8	D	–40°C to +85°C	OPA2735A	OPA2735AID	Rails, 100
"	"	"	"	"	OPA2735AIDR	Tape and Reel, 2500
OPA2735	MSOP-8	DGK	–40°C to +85°C	BGN	OPA2735AIDGKT	Tape and Reel, 250
"	"	"	"	"	OPA2735AIDGKR	Tape and Reel, 2500

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

**ELECTRICAL CHARACTERISTICS:  $V_S = \pm 5V$  ( $V_S = +10V$ )**
**Boldface** limits apply over the specified temperature range,  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

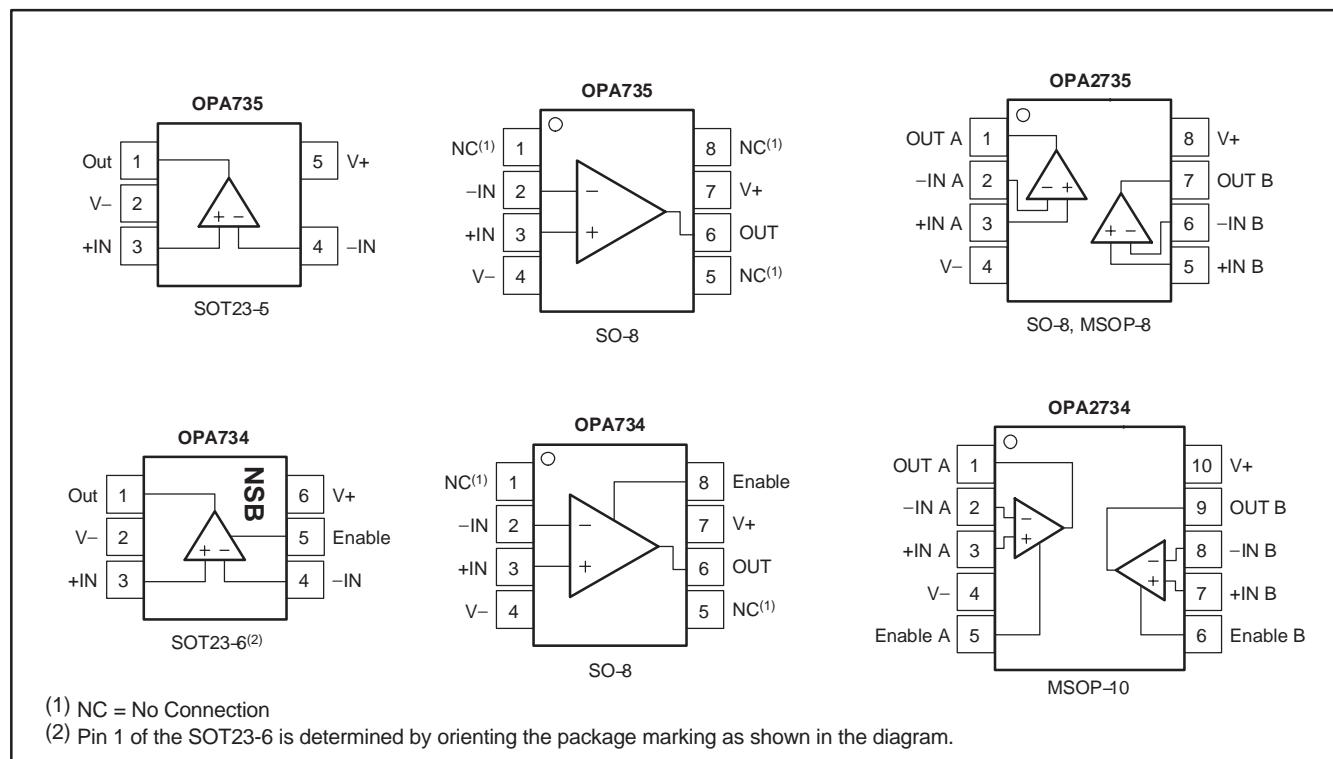
 At  $T_A = +25^{\circ}\text{C}$ ,  $R_L = 10\text{k}\Omega$  connected to  $V_S/2$ , and  $V_{\text{OUT}} = V_S/2$ , unless otherwise noted.

PARAMETER	CONDITIONS	OPA734, OPA2734, OPA735, OPA2735			UNIT
		MIN	TYP	MAX	
<b>OFFSET VOLTAGE</b>					
Input Offset Voltage <b>vs Temperature</b>	$V_{\text{OS}}$ $dV_{\text{OS}}/dT$		1 0.01 0.2 Note (1) 0.1	5 0.05 1.8	$\mu\text{V}$ $\mu\text{V}^{\circ}\text{C}$ $\mu\text{V}/\text{V}$ $\mu\text{V}/\text{V}$
vs Power Supply	$\text{PSRR}$	$V_S = 2.7V$ to $12V$ , $V_{\text{CM}} = 0V$			
Long-Term Stability					
Channel Separation, dc					
<b>INPUT BIAS CURRENT</b>					
Input Bias Current <b>over Temperature</b>	$I_B$	$V_{\text{CM}} = V_S/2$		$\pm 100$	$\text{pA}$
Input Offset Current	$I_{\text{OS}}$	$V_{\text{CM}} = V_S/2$		$\pm 200$ <b>See Typical Characteristics</b> $\pm 200$	$\text{pA}$ $\text{pA}$
<b>NOISE</b>					
Input Voltage Noise, $f = 0.01\text{Hz}$ to $1\text{Hz}$	$e_n$			0.8	$\mu\text{V}_{\text{PP}}$
Input Voltage Noise, $f = 0.1\text{Hz}$ to $10\text{Hz}$	$e_n$			2.5	$\mu\text{V}_{\text{PP}}$
Input Voltage Noise Density, $f = 1\text{kHz}$	$e_n$			135	$\text{nV}/\sqrt{\text{Hz}}$
Input Current Noise Density, $f = 1\text{kHz}$	$i_n$			40	$\text{fA}/\sqrt{\text{Hz}}$
<b>INPUT VOLTAGE RANGE</b>					
Common-Mode Voltage Range	$V_{\text{CM}}$		$(V-) - 0.1V < V_{\text{CM}} < (V+) - 1.5V$	$(V-) - 0.1$ 115	$(V+) - 1.5$
Common-Mode Rejection Ratio	$\text{CMRR}$			130	$\text{V}$ $\text{dB}$
<b>INPUT CAPACITANCE</b>					
Differential				2	$\text{pF}$
Common-Mode				10	$\text{pF}$
<b>OPEN-LOOP GAIN</b>					
Open-Loop Voltage Gain	$A_{\text{OL}}$	$(V-) + 100\text{mV} < V_O < (V+) - 100\text{mV}$		115	$\text{dB}$
<b>FREQUENCY RESPONSE</b>					
Gain-Bandwidth Product	$\text{GBW}$			1.6	$\text{MHz}$
Slew Rate	$\text{SR}$	$G = +1$		1.5	$\text{V}/\mu\text{s}$
<b>OUTPUT</b>					
Voltage Output Swing from Rail		$R_L = 10\text{k}\Omega$		20	$\text{mV}$
Short-Circuit Current	$I_{\text{SC}}$			$\pm 20$	$\text{mA}$
Open-Loop Output Impedance		$f = 1\text{MHz}$ , $I_O = 0$		125	$\Omega$
Capacitive Load Drive	$C_{\text{LOAD}}$			See Typical Characteristics	
<b>ENABLE/SHUTDOWN</b>					
$t_{\text{OFF}}$				1.5	$\mu\text{s}$
$t_{\text{ON}}^{(2)}$				150	$\mu\text{s}$
$V_L$ (amplifier is shutdown)			$V-$	$(V-) + 0.8$	$\text{V}$
$V_H$ (amplifier is active)			$(V-) + 2$	$V+$	$\text{V}$
$I_{\text{QSD}}$ (per amplifier)			4	9	$\mu\text{A}$
Input Bias Current of Enable Pin			3		$\mu\text{A}$
<b>POWER SUPPLY</b>					
Operating Voltage Range	$V_S$			2.7 to 12 ( $\pm 1.35$ to $\pm 6$ )	$\text{V}$
Quiescent Current (per amplifier)	$I_Q$	$I_O = 0$		0.6	$\text{mA}$
<b>TEMPERATURE RANGE</b>					
Specified Range			-40		$^{\circ}\text{C}$
Operating Range			-40	+85	$^{\circ}\text{C}$
Storage Range			-65	+150	$^{\circ}\text{C}$
Thermal Resistance	$\theta_{\text{JA}}$			+150	$^{\circ}\text{C}/\text{W}$
SOT23-5, SOT23-6			200		$^{\circ}\text{C}/\text{W}$
MSOP-8, MSOP-10, SO-8			150		$^{\circ}\text{C}/\text{W}$

 (1) 300-hour life test at  $150^{\circ}\text{C}$  demonstrated randomly distributed variation in the range of measurement limits—approximately  $1\mu\text{V}$ .

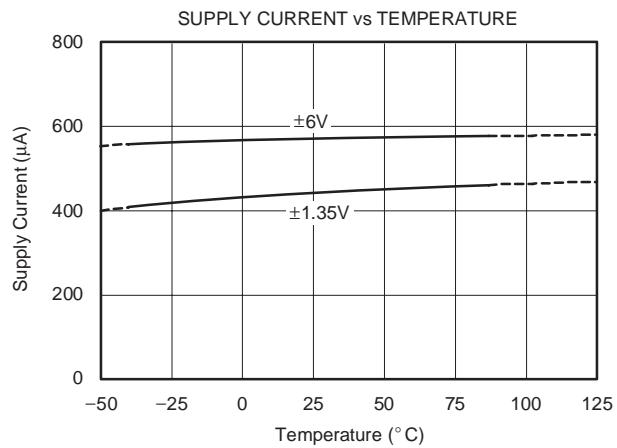
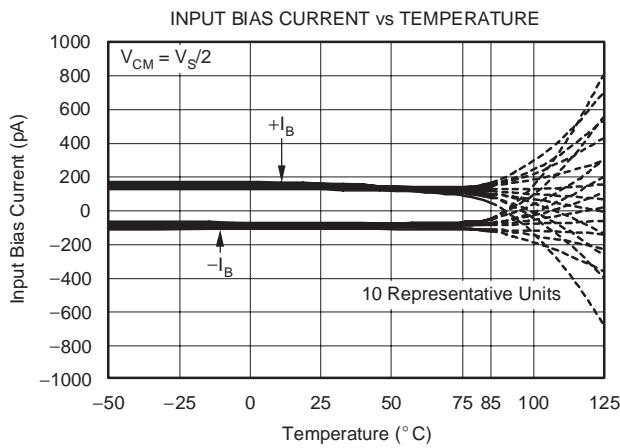
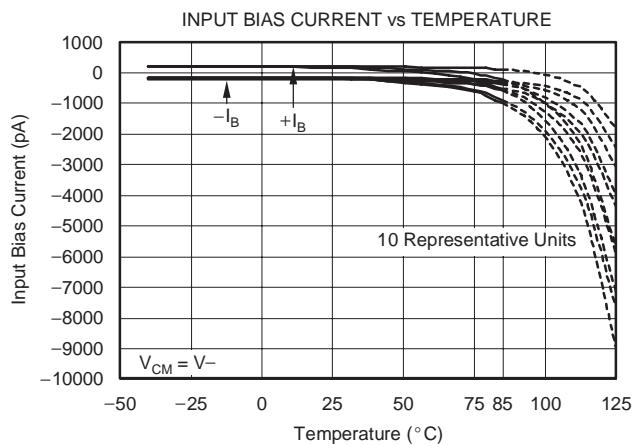
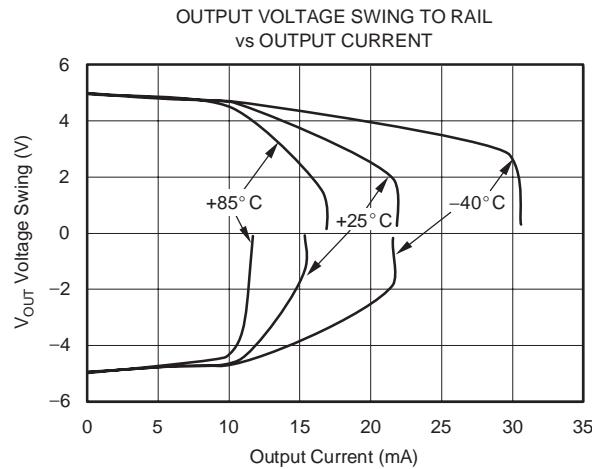
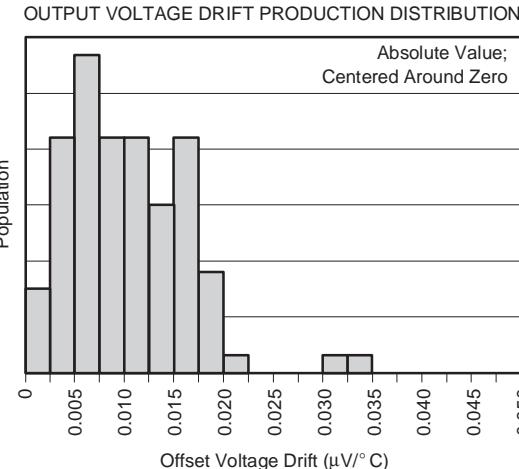
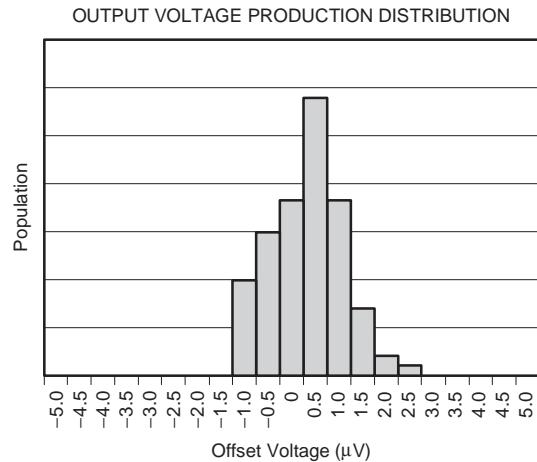
 (2) Device requires one complete auto-zero cycle to return to  $V_{\text{OS}}$  accuracy.

## PIN CONFIGURATIONS



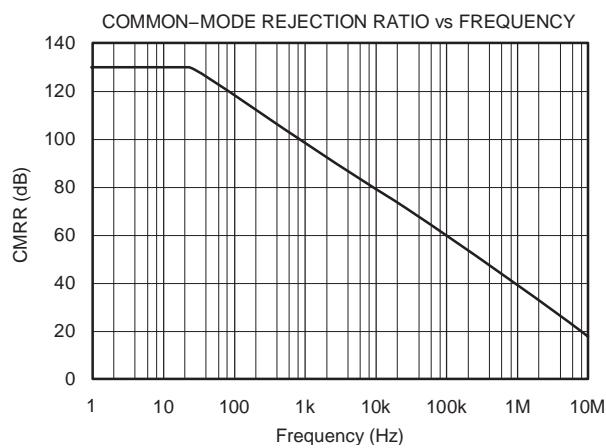
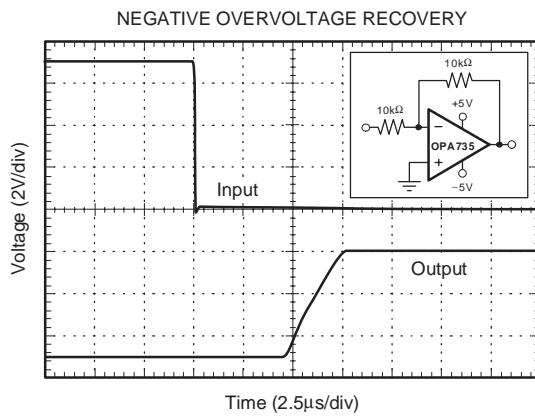
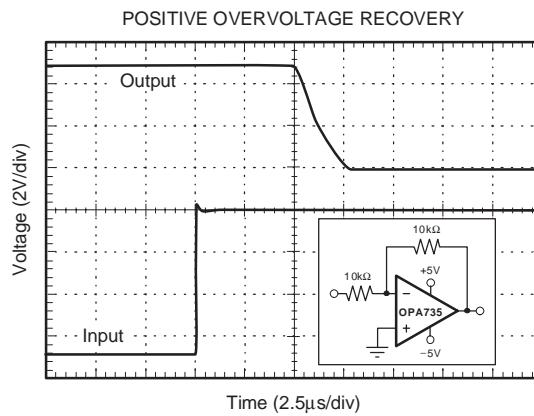
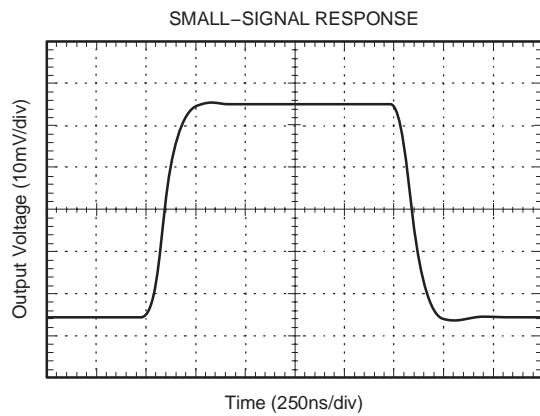
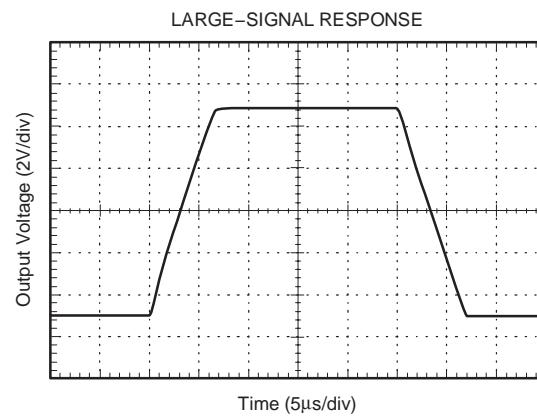
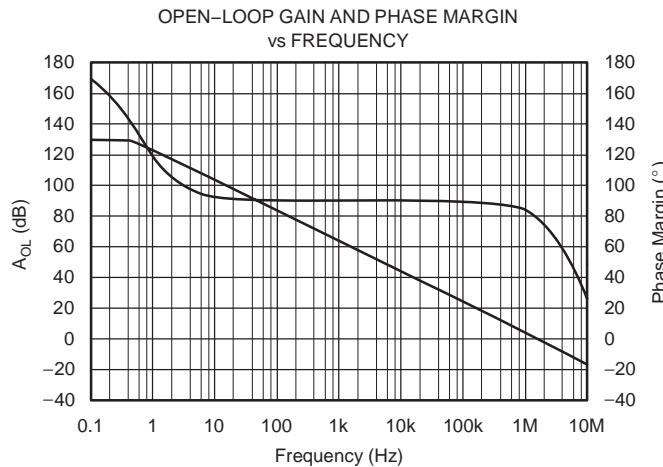
## TYPICAL CHARACTERISTICS

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 5\text{V}$  (same as  $+10\text{V}$ ).



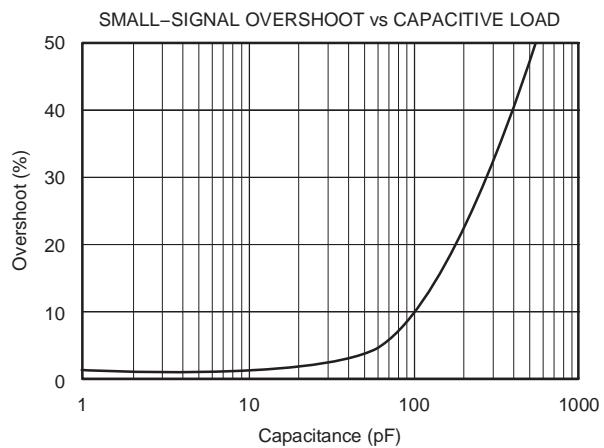
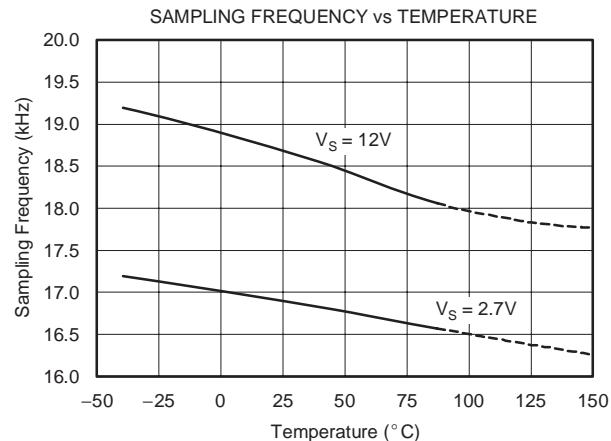
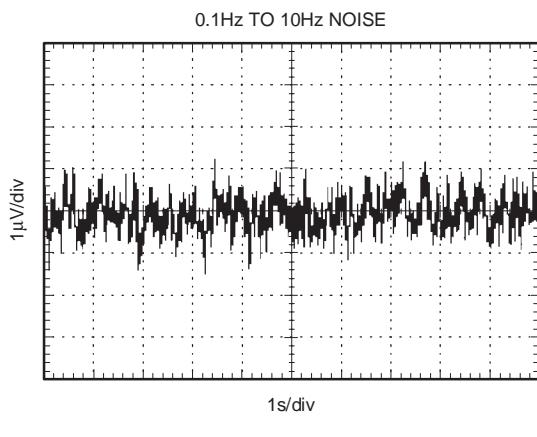
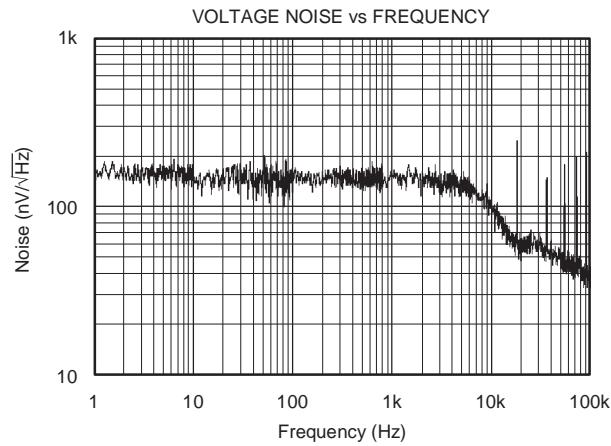
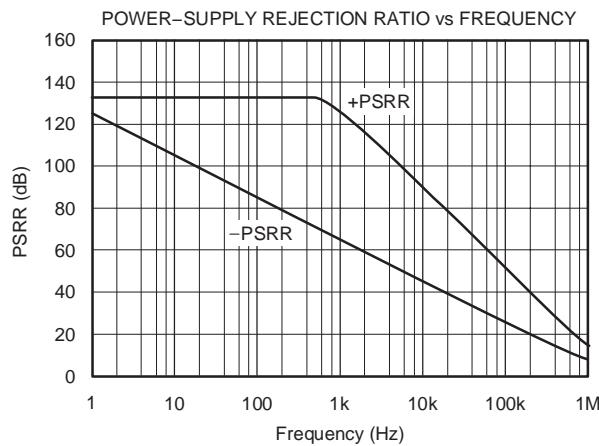
## TYPICAL CHARACTERISTICS (continued)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 5\text{V}$  (same as  $+10\text{V}$ ).



## TYPICAL CHARACTERISTICS (continued)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 5\text{V}$  (same as  $+10\text{V}$ ).



## APPLICATIONS INFORMATION

The OPA734 and OPA735 series of op amps are unity-gain stable and free from unexpected output phase reversal. They use auto-zeroing techniques to provide low offset voltage and demonstrate very low drift over time and temperature.

Good layout practice mandates the use of a  $0.1\mu\text{F}$  capacitor placed closely across the supply pins.

For lowest offset voltage and precision performance, circuit layout and mechanical conditions should be optimized. Avoid temperature gradients that create thermoelectric (Seebeck) effects in thermocouple junctions formed from connecting dissimilar conductors. These thermally-generated potentials can be made to cancel by assuring that they are equal on both input terminals:

1. Use low thermoelectric-coefficient connections (avoid dissimilar metals).
2. Thermally isolate components from power supplies or other heat sources.
3. Shield op amp and input circuitry from air currents such as cooling fans.

Following these guidelines will reduce the likelihood of junctions being at different temperatures, which can cause thermoelectric voltages of  $0.1\mu\text{V}/^\circ\text{C}$  or higher, depending on the materials used.

## OPERATING VOLTAGE

The OPA734 and OPA735 op amp family operates with a power-supply range of  $+2.7\text{V}$  to  $+12\text{V}$  ( $\pm 1.35\text{V}$  to  $\pm 6\text{V}$ ). Supply voltages higher than  $+13.2\text{V}$  (absolute maximum) can permanently damage the amplifier. Parameters that vary over supply voltage or temperature are shown in the Typical Characteristics section of this data sheet.

## OPA734 ENABLE FUNCTION

The enable/shutdown digital input is referenced to the  $V_-$  supply voltage of the op amp. A logic HIGH enables the op amp. A valid logic HIGH is defined as  $> (V_-) + 2\text{V}$ . The valid logic HIGH signal can be up to the positive supply, independent of the negative power supply voltage. A valid logic LOW is defined as  $< 0.8\text{V}$  above the  $V_-$  supply pin. If dual or split power supplies are used, be sure that logic input signals are properly referred to the negative supply voltage. The Enable pin is connected to internal pull-up circuitry and will enable the device if this pin is left open circuit.

The logic input is a CMOS input. Separate logic inputs are provided for each op amp on the dual version. For battery-operated applications, this feature can be used to greatly reduce the average current and extend battery life.

The enable time is  $150\mu\text{s}$ , which includes one full auto-zero cycle required by the amplifier to return to  $V_{OS}$  accuracy. Prior to returning to full accuracy, the amplifier may function properly, but with unspecified offset voltage.

Disable time is  $1.5\mu\text{s}$ . When disabled, the output assumes a high-impedance state. The disable state allows the OPA734 to be operated as a gated amplifier, or to have the output multiplexed onto a common analog output bus.

## INPUT VOLTAGE

The input common-mode range extends from  $(V_-) - 0.1\text{V}$  to  $(V_+) - 1.5\text{V}$ . For normal operation, the inputs must be limited to this range. The common-mode rejection ratio is only valid within the specified input common-mode range. A lower supply voltage results in lower input common-mode range; therefore, attention to these values must be given when selecting the input bias voltage. For example, when operating on a single  $3\text{V}$  power supply, common-mode range is from  $0.1\text{V}$  below ground to half the power-supply voltage.

Normally, input bias current is approximately  $100\text{pA}$ ; however, input voltages exceeding the power supplies can cause excessive current to flow in or out of the input pins. Momentary voltages greater than the power supply can be tolerated if the input current is limited to  $10\text{mA}$ . This is easily accomplished with an input resistor, as shown in Figure 1.

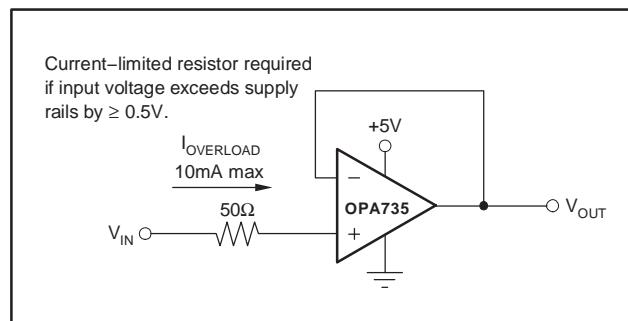


Figure 1. Input Current Protection

## INTERNAL OFFSET CORRECTION

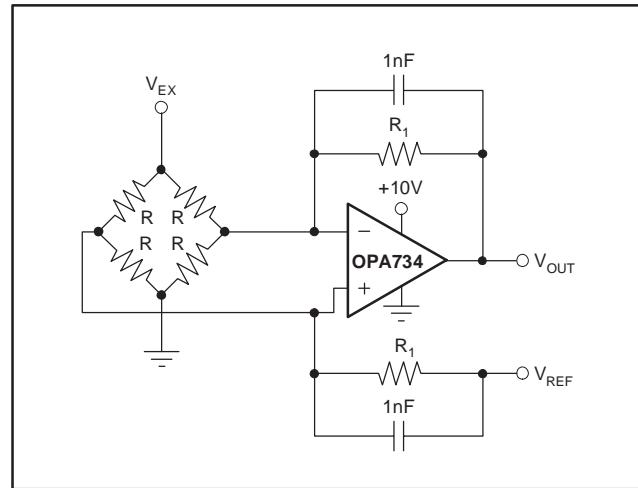
The OPA734 and OPA735 series of op amps use an auto-zero topology with a time-continuous  $1.6\text{MHz}$  op amp in the signal path. This amplifier is zero-corrected every  $100\mu\text{s}$  using a proprietary technique. Upon power-up, the amplifier requires one full auto-zero cycle of approximately  $100\mu\text{s}$  in addition to the start-up time for the bias circuitry to achieve specified  $V_{OS}$  accuracy. Prior to this time, the amplifier may function properly but with unspecified offset voltage.

Low-gain ( $< 20$ ) operation demands that the auto-zero circuitry correct for common-mode rejection errors of the main amplifier. Because these errors can be larger than 0.1% of a full-scale input step change, one calibration cycle (100 $\mu$ s) can be required to achieve full accuracy.

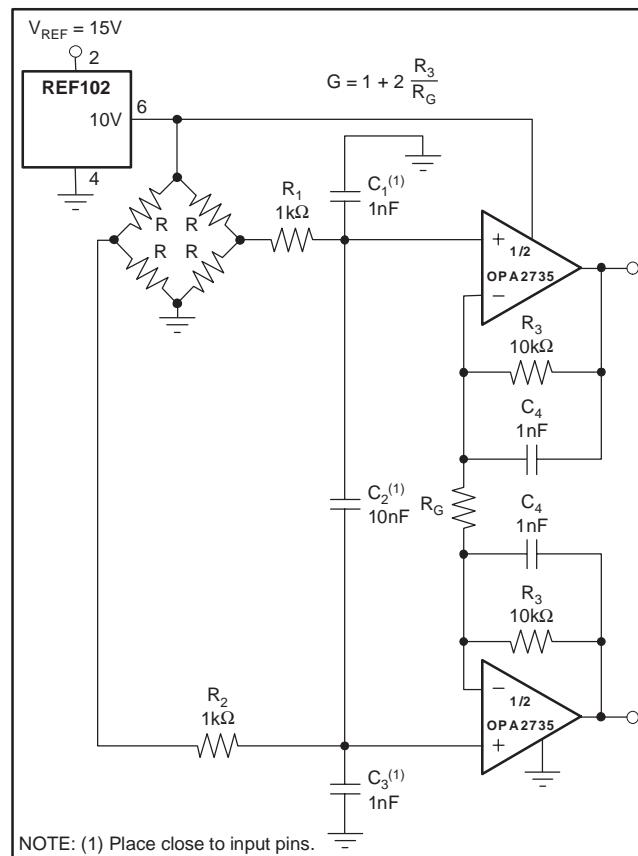
The term *clock feedthrough* describes the presence of the clock frequency in the output spectrum. In auto-zeroed op amps, clock feedthrough may result from the settling of the internal sampling capacitor, or from the small amount of charge injection that occurs during the sample-and-hold of the op amp offset voltage. Feedthrough can be minimized by keeping the source impedance relatively low ( $< 1\text{k}\Omega$ ) and matching the source impedance on both input terminals. If the source resistance is high ( $> 1\text{k}\Omega$ ) feedthrough can generally be reduced with a capacitor of  $1\text{nF}$  or greater in parallel with the source or feedback resistors. See the circuit application examples.

## LAYOUT GUIDELINES

Attention to good layout practices is always recommended. Keep traces short. When possible, use a PCB ground plane with surface-mount components placed as close to the device pins as possible. Place a  $0.1\mu\text{F}$  capacitor closely across the supply pins. These guidelines should be applied throughout the analog circuit to improve performance and provide benefits such as reducing the electromagnetic-interference (EMI) susceptibility.



**Figure 2. Single Op Amp Bridge Amplifier Circuit**



**Figure 3. Differential Output Bridge Amplifier**

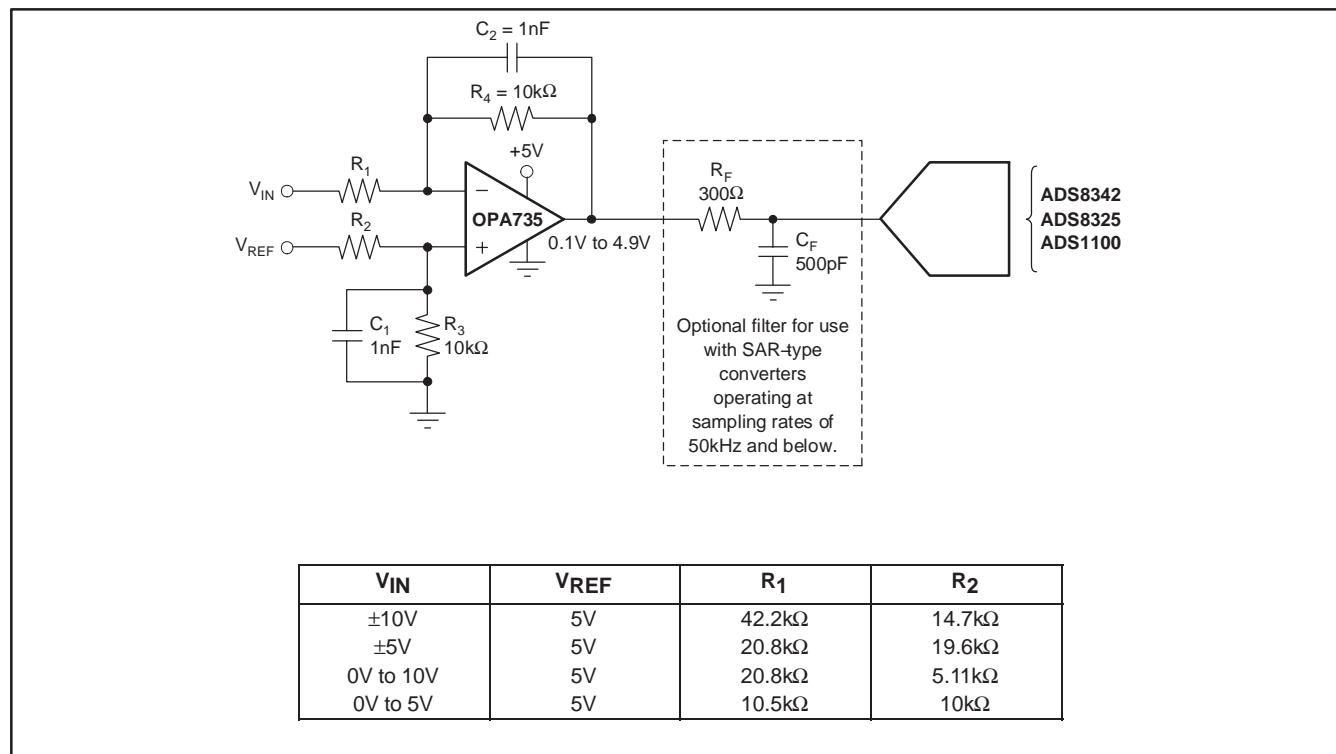


Figure 4. Driving ADC

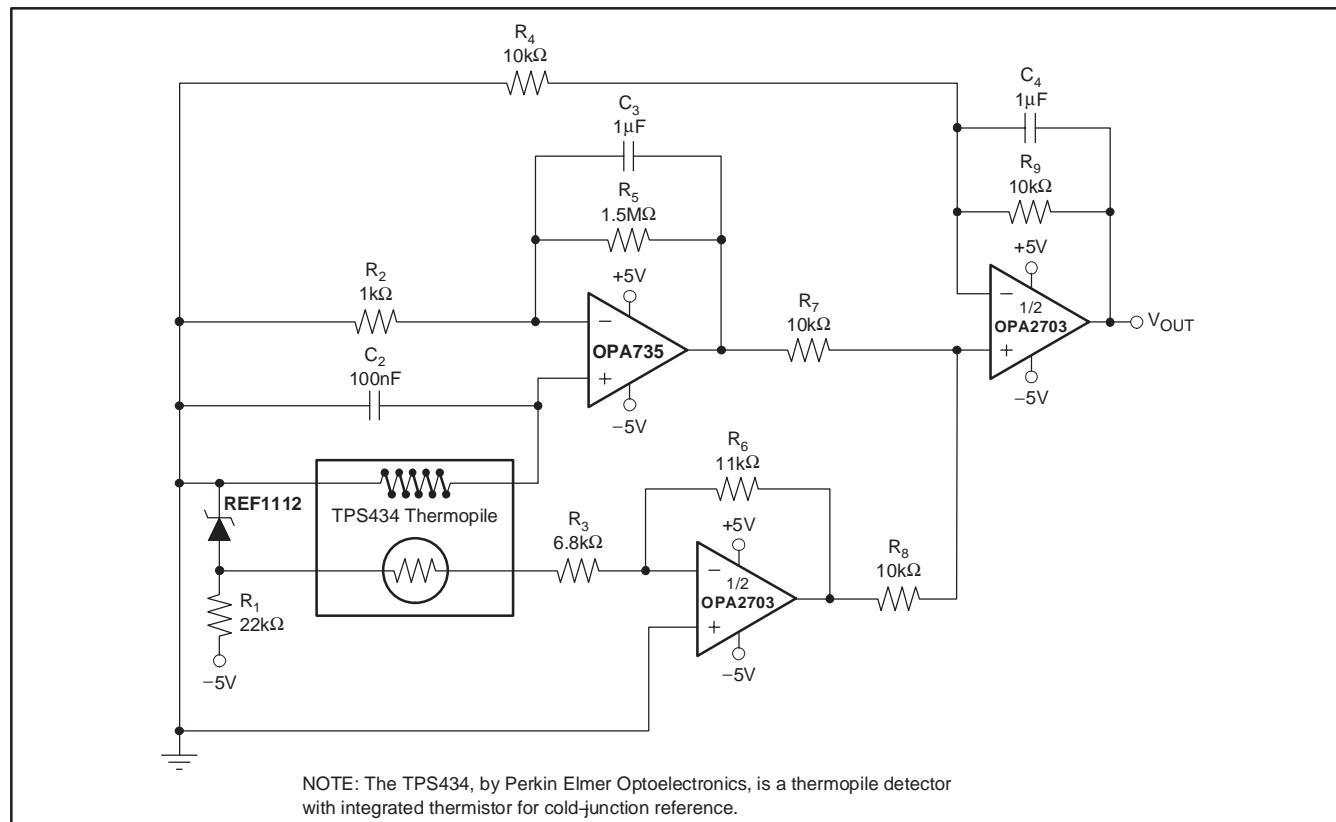
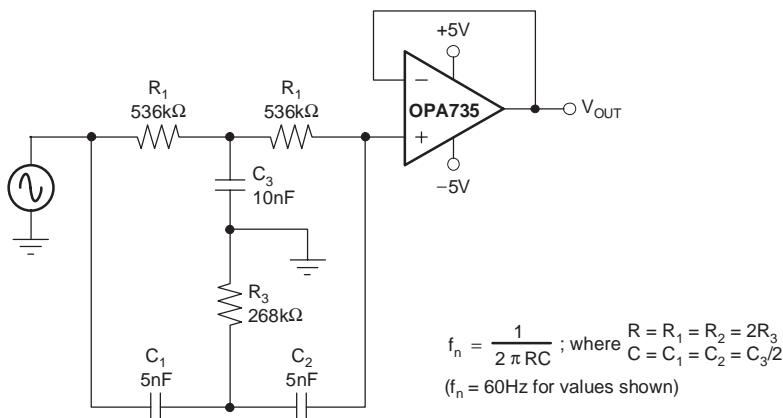
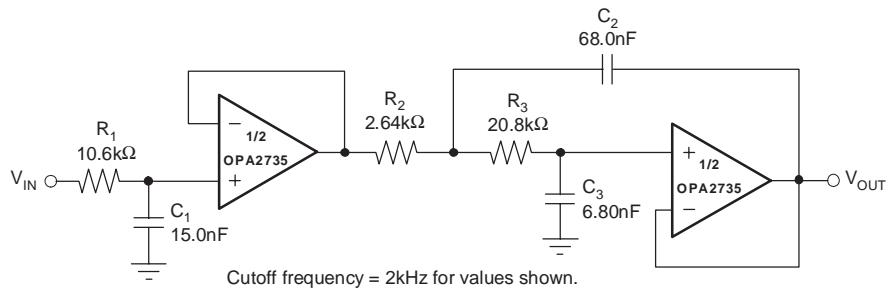


Figure 5. Thermopile Non-Contact Surface Temperature Measurement

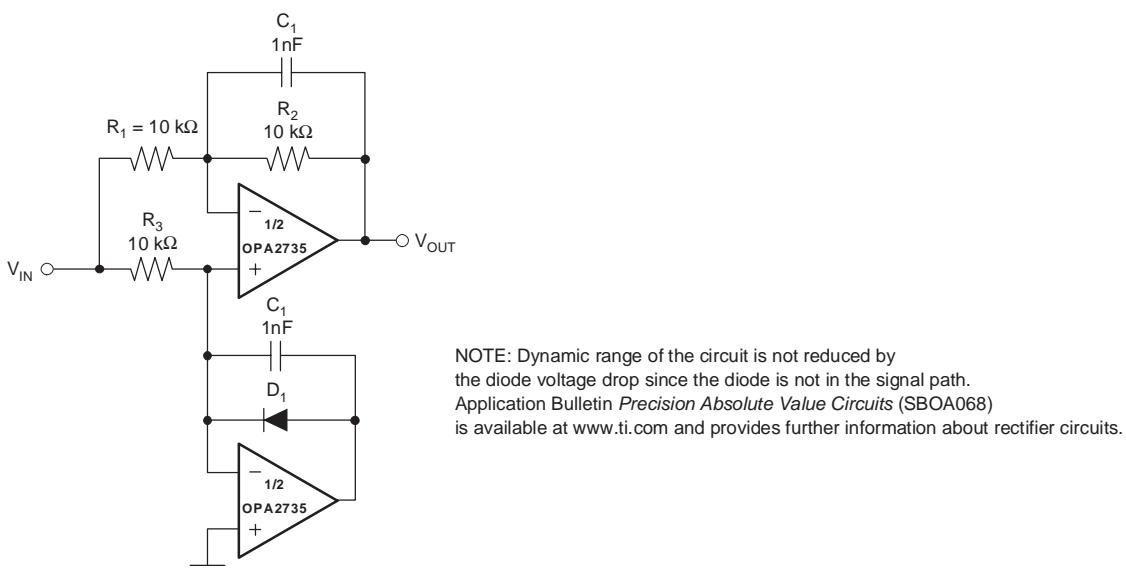


**Figure 6. Twin-T Notch Filter**

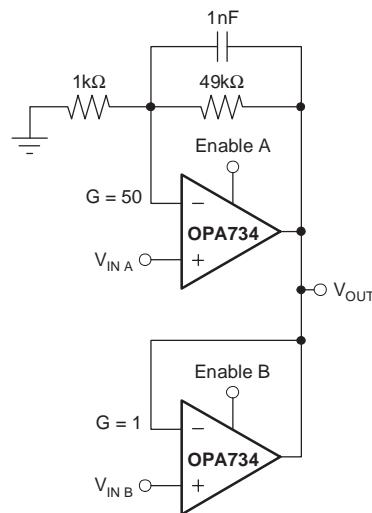


NOTE: FilterPro is a low-pass filter design program available for download at no cost from TI's web site (www.ti.com). The program can be used to easily determine component values for other cutoff frequencies or filter types.

**Figure 7. High DC Accuracy, 3-Pole Low-Pass Filter**



**Figure 8. Precision Full-Wave Rectifier with Full Dynamic Range**



Enable inputs are CMOS logic compatible.

Figure 9. High-Precision 2-Input MUX for Programmable Gain

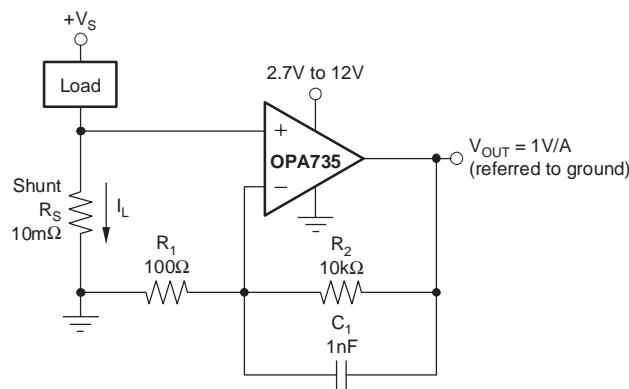


Figure 10. Low-Side Power-Supply Current Sensing

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">OPA2734AIDGSR</a>	Active	Production	VSSOP (DGS)   10	2500   LARGE T&R	Yes	Call TI   Nipdaug	Level-2-260C-1 YEAR	-40 to 85	BGO
OPA2734AIDGSR.B	Active	Production	VSSOP (DGS)   10	2500   LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 85	BGO
<a href="#">OPA2734AIDGST</a>	Active	Production	VSSOP (DGS)   10	250   SMALL T&R	Yes	Call TI   Nipdaug	Level-2-260C-1 YEAR	-40 to 85	BGO
OPA2734AIDGST.B	Active	Production	VSSOP (DGS)   10	250   SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 85	BGO
<a href="#">OPA2735AID</a>	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2735A
OPA2735AID.B	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2735A
OPA2735AIDG4	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2735A
<a href="#">OPA2735AIDGKR</a>	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	Call TI   Sn   Nipdaug   Nipdau	Level-2-260C-1 YEAR	-40 to 85	BGN
OPA2735AIDGKR.B	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 85	BGN
<a href="#">OPA2735AIDGKT</a>	Active	Production	VSSOP (DGK)   8	250   SMALL T&R	Yes	Call TI   Sn   Nipdaug   Nipdau	Level-2-260C-1 YEAR	-40 to 85	BGN
OPA2735AIDGKT.B	Active	Production	VSSOP (DGK)   8	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BGN
<a href="#">OPA2735AIDR</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2735A
OPA2735AIDR.B	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2735A
OPA2735AIDRG4	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2735A
OPA2735AIDRG4.B	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2735A
<a href="#">OPA734AID</a>	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 734A
OPA734AID.B	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 734A
<a href="#">OPA734AIDBVR</a>	Active	Production	SOT-23 (DBV)   6	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NSB
OPA734AIDBVR.B	Active	Production	SOT-23 (DBV)   6	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NSB
<a href="#">OPA734AIDBVT</a>	Active	Production	SOT-23 (DBV)   6	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NSB
OPA734AIDBVT.B	Active	Production	SOT-23 (DBV)   6	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NSB

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA734AIDBVTG4	Active	Production	SOT-23 (DBV)   6	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NSB
OPA734AIDBVTG4.B	Active	Production	SOT-23 (DBV)   6	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NSB
<b>OPA735AID</b>	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 735A
OPA735AID.B	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 735A
<b>OPA735AIDBVR</b>	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NSC
OPA735AIDBVR.B	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NSC
OPA735AIDBVRG4	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NSC
<b>OPA735AIDBVT</b>	Active	Production	SOT-23 (DBV)   5	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NSC
OPA735AIDBVT.B	Active	Production	SOT-23 (DBV)   5	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NSC
OPA735AIDBVTG4	Active	Production	SOT-23 (DBV)   5	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NSC
OPA735AIDG4	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 735A
OPA735AIDG4.B	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 735A
<b>OPA735AIDR</b>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 735A
OPA735AIDR.B	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 735A

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

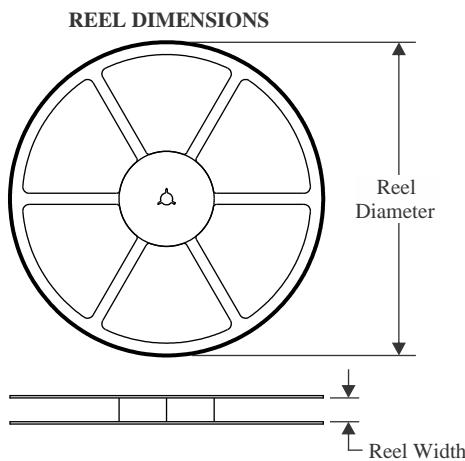
<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

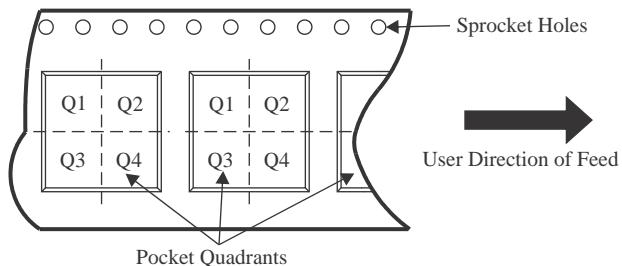
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

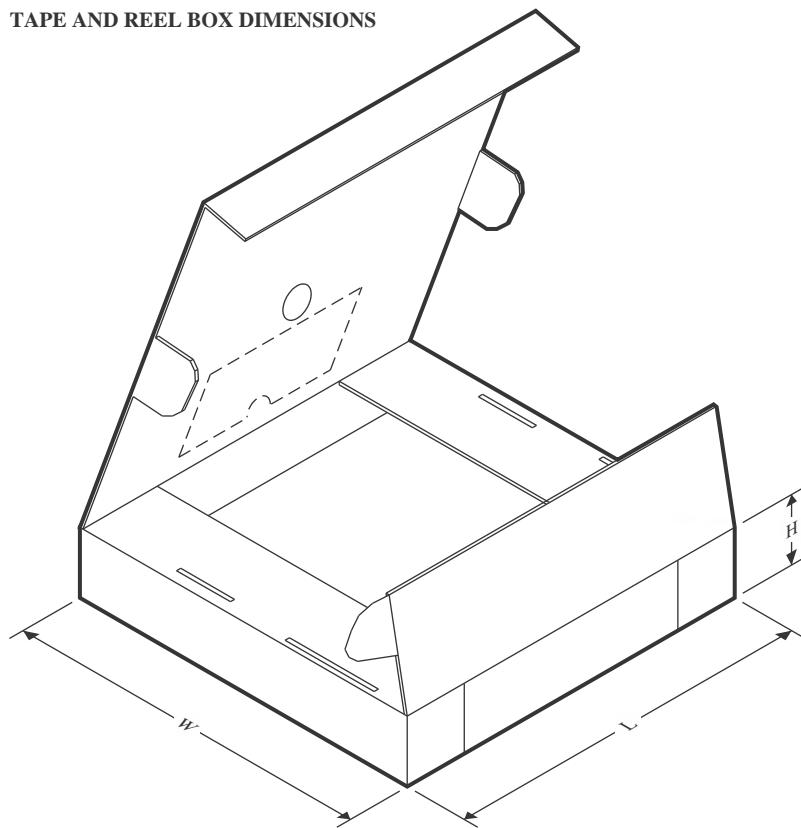
**TAPE AND REEL INFORMATION**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2735AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2735AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2735AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2735AIDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA734AIDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
OPA734AIDBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
OPA734AIDBVTG4	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
OPA735AIDBVR	SOT-23	DBV	5	3000	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA735AIDBVT	SOT-23	DBV	5	250	178.0	8.4	3.3	3.2	1.4	4.0	8.0	Q3
OPA735AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2735AIDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA2735AIDGKT	VSSOP	DGK	8	250	213.0	191.0	35.0
OPA2735AIDR	SOIC	D	8	2500	353.0	353.0	32.0
OPA2735AIDRG4	SOIC	D	8	2500	353.0	353.0	32.0
OPA734AIDBVR	SOT-23	DBV	6	3000	445.0	220.0	345.0
OPA734AIDBVT	SOT-23	DBV	6	250	445.0	220.0	345.0
OPA734AIDBVTG4	SOT-23	DBV	6	250	445.0	220.0	345.0
OPA735AIDBVR	SOT-23	DBV	5	3000	565.0	140.0	75.0
OPA735AIDBVT	SOT-23	DBV	5	250	565.0	140.0	75.0
OPA735AIDR	SOIC	D	8	2500	353.0	353.0	32.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T ( $\mu$ m)	B (mm)
OPA2735AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA2735AID.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA2735AIDG4	D	SOIC	8	75	506.6	8	3940	4.32
OPA734AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA734AID.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA735AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA735AID.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA735AIDG4	D	SOIC	8	75	506.6	8	3940	4.32
OPA735AIDG4.B	D	SOIC	8	75	506.6	8	3940	4.32

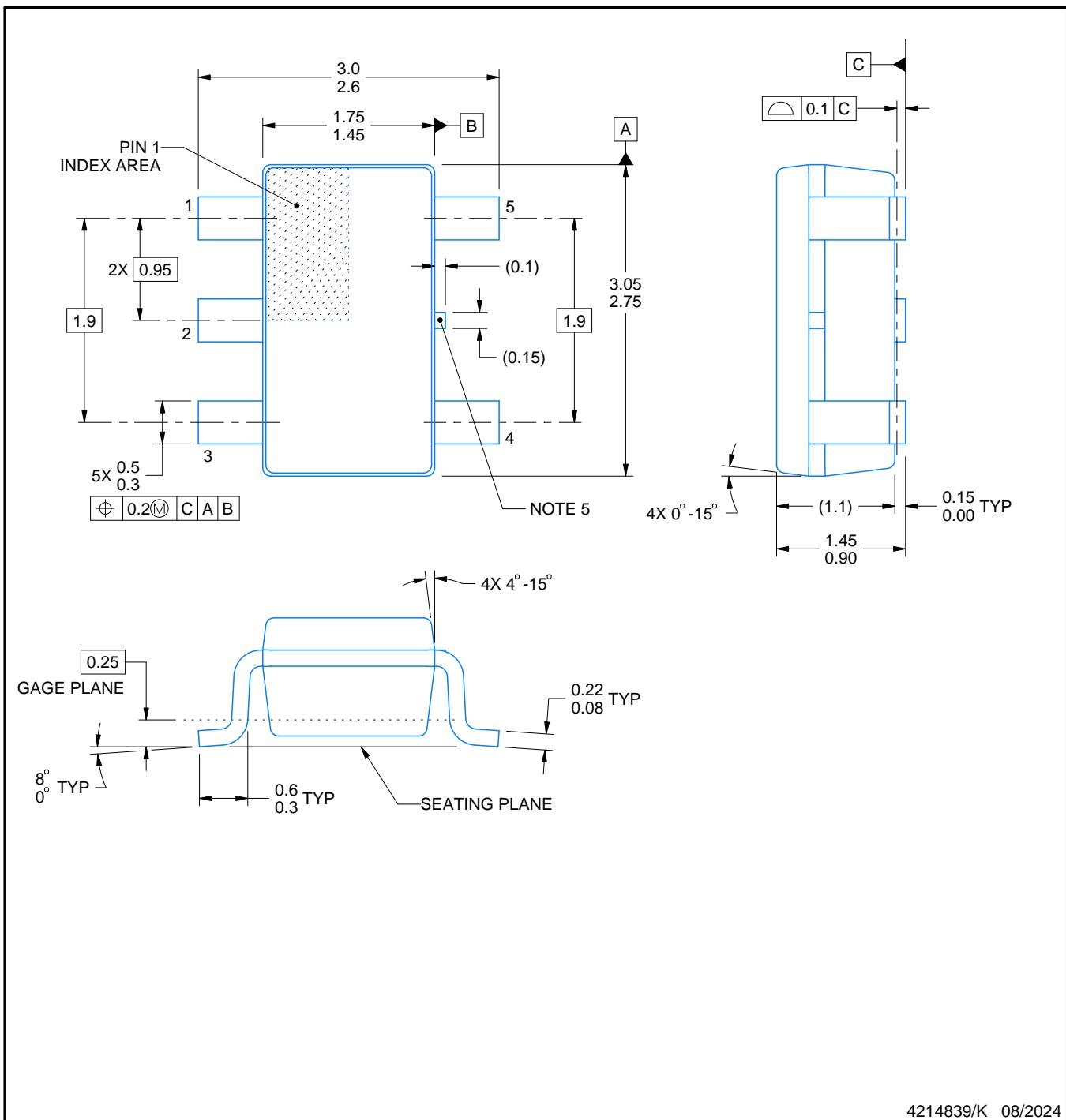
# PACKAGE OUTLINE

DBV0005A



SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/K 08/2024

## NOTES:

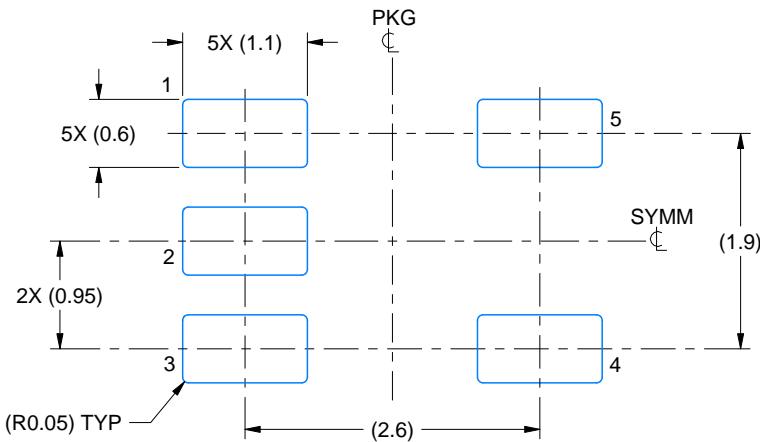
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

# EXAMPLE BOARD LAYOUT

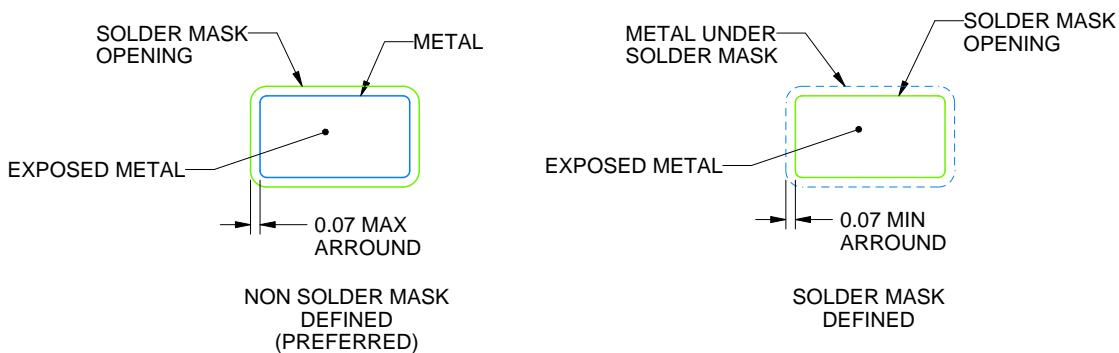
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

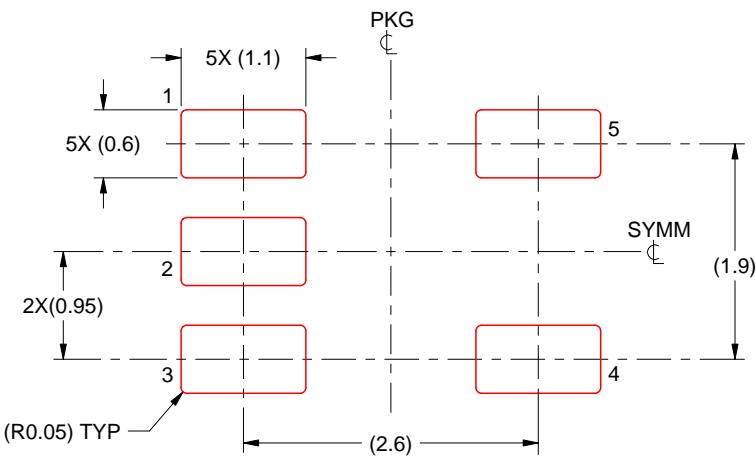
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

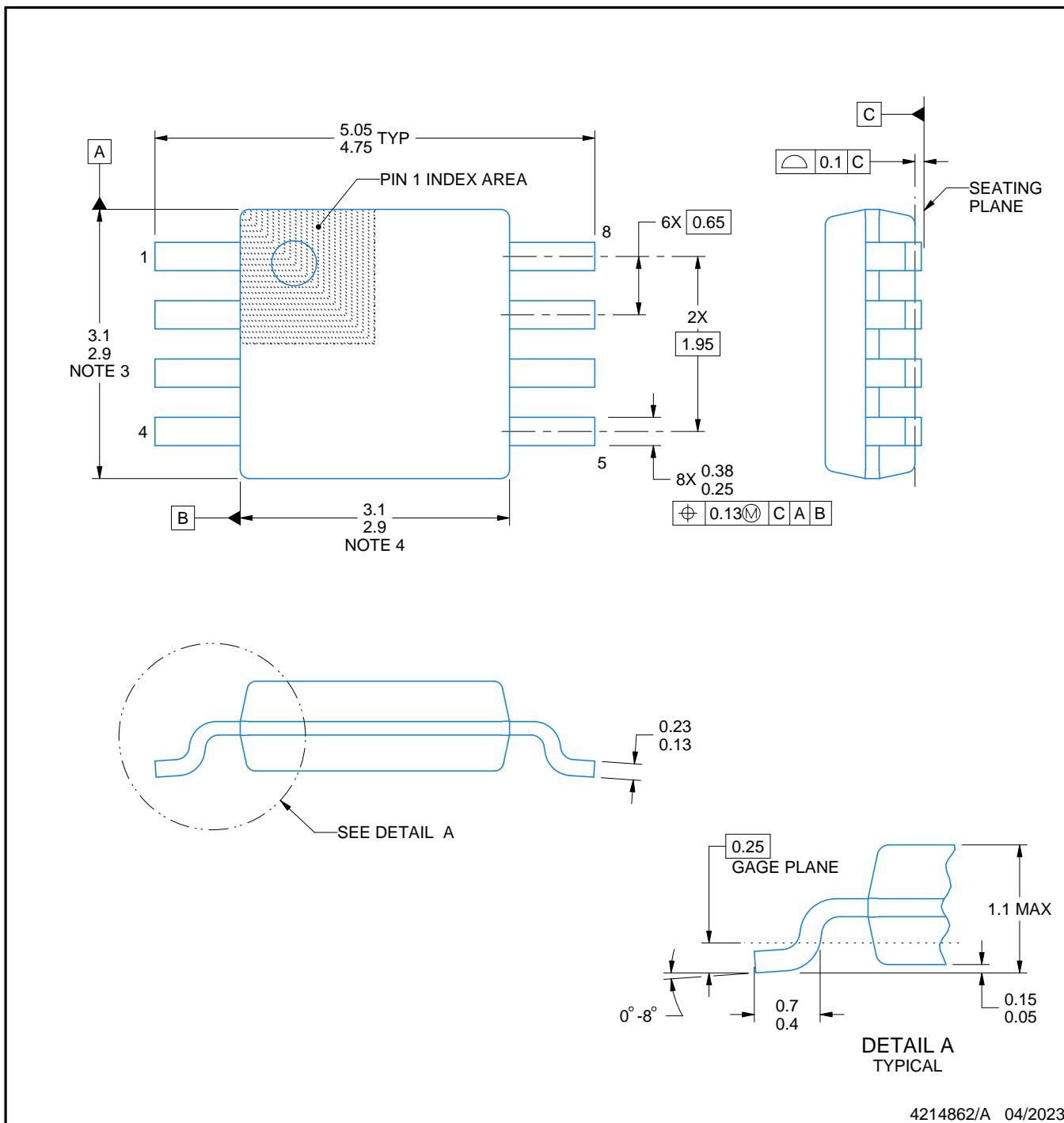
# PACKAGE OUTLINE

DGK0008A



VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES:

PowerPAD is a trademark of Texas Instruments.

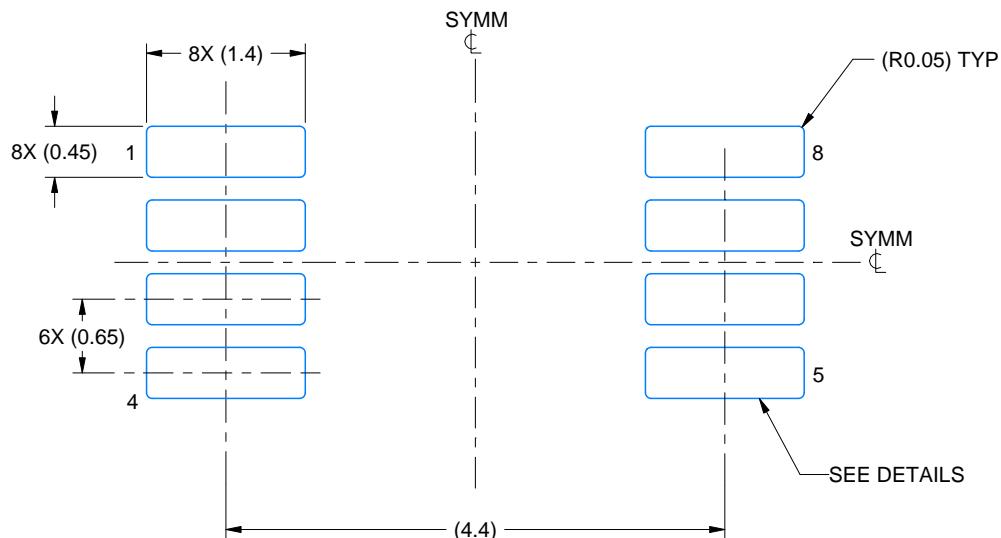
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

# EXAMPLE BOARD LAYOUT

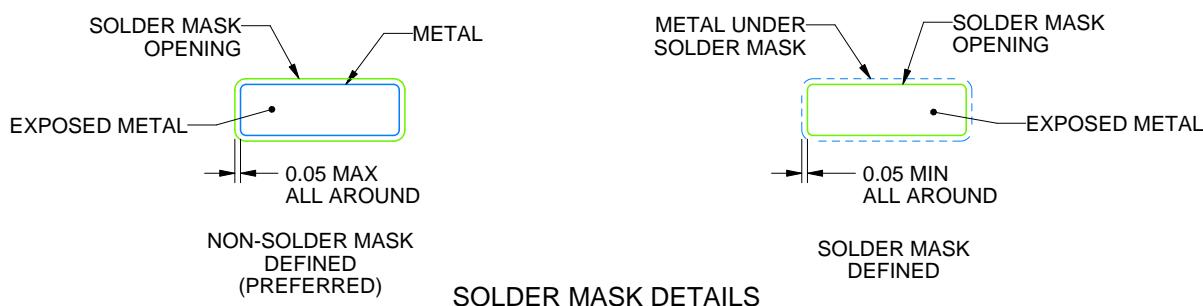
DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

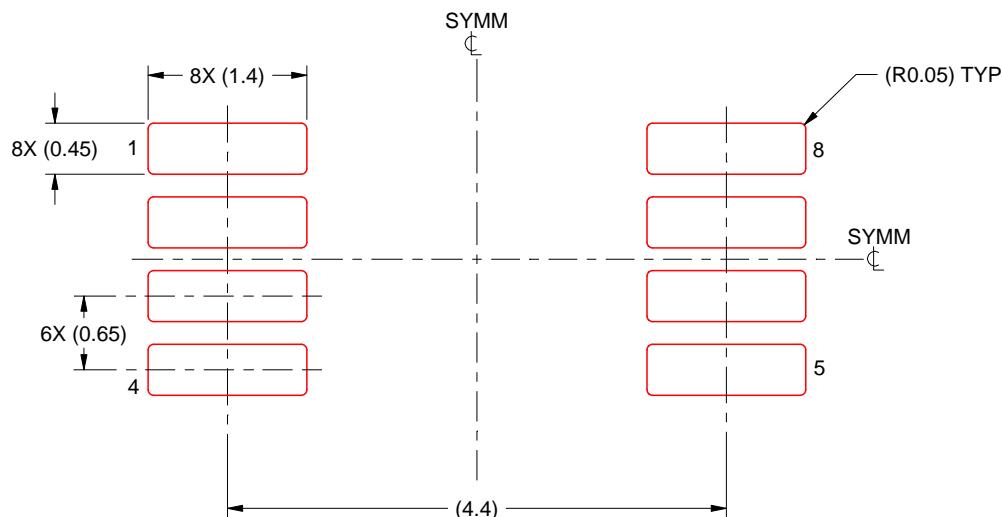
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

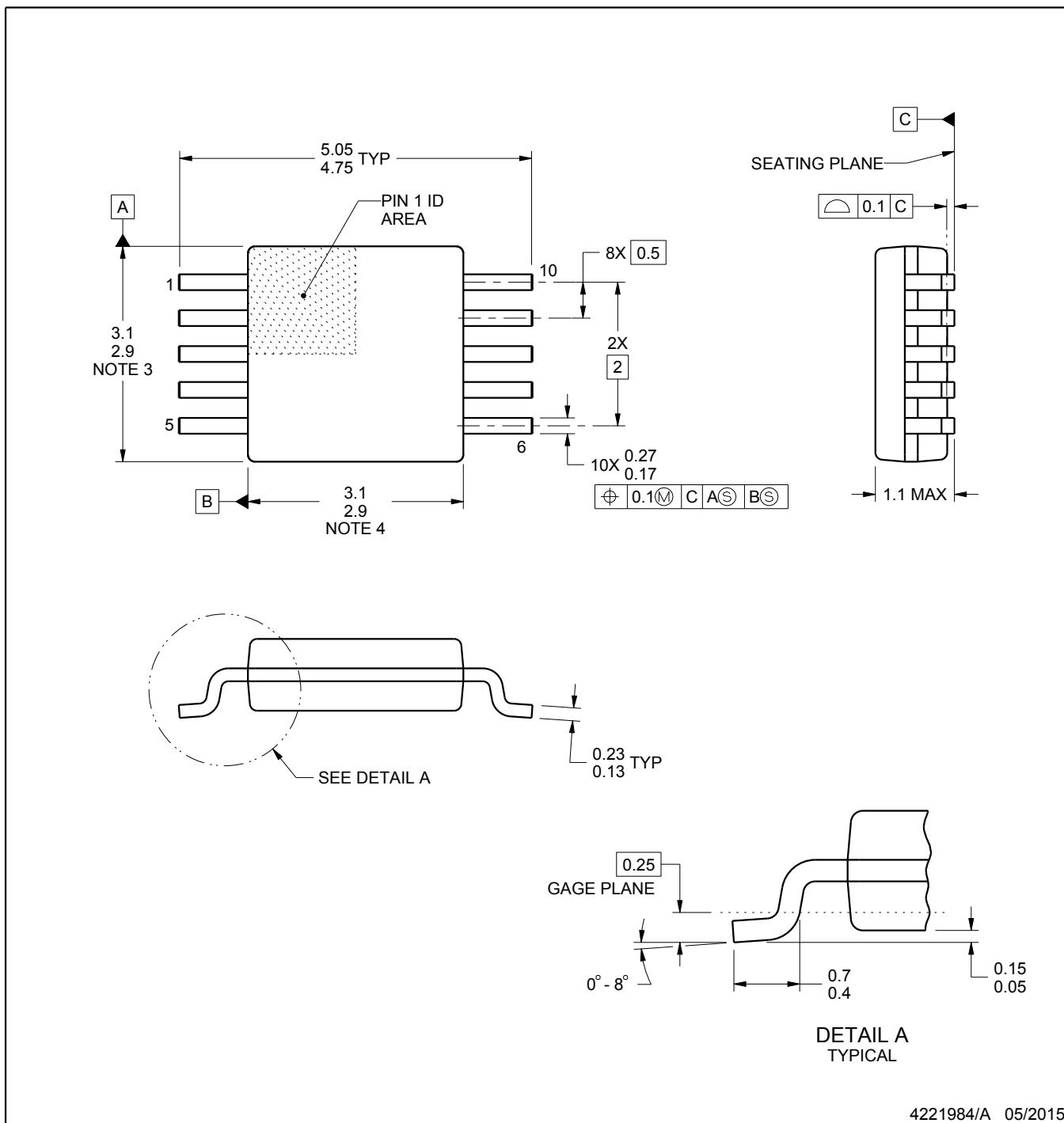
# PACKAGE OUTLINE

DGS0010A



VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4221984/A 05/2015

NOTES:

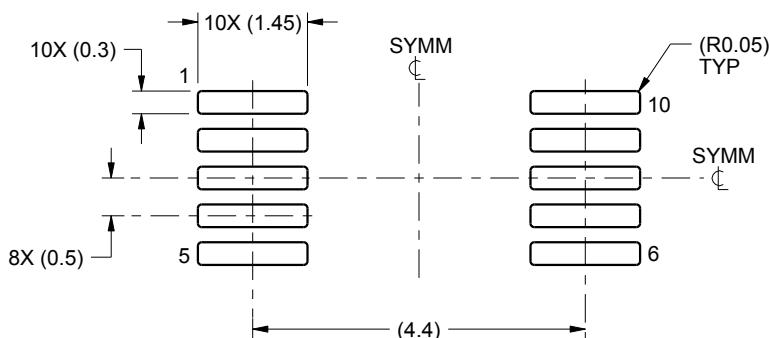
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.

# EXAMPLE BOARD LAYOUT

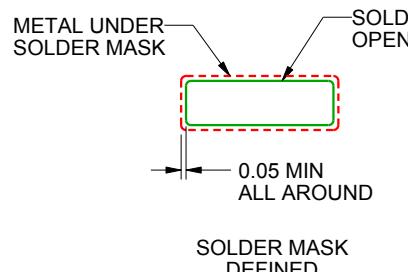
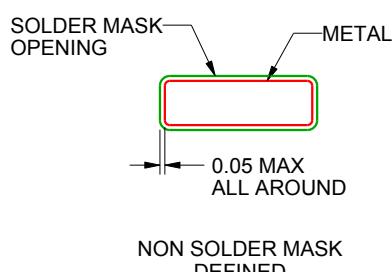
DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

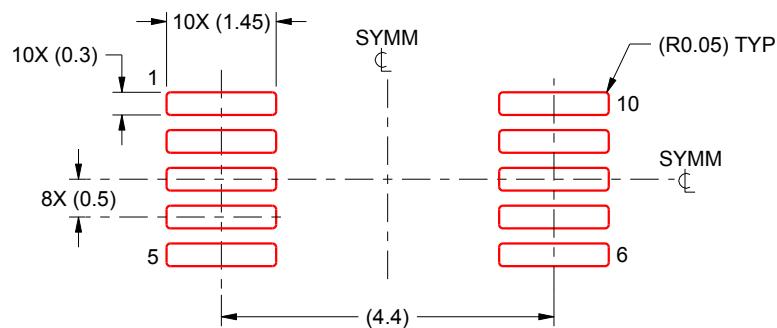
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

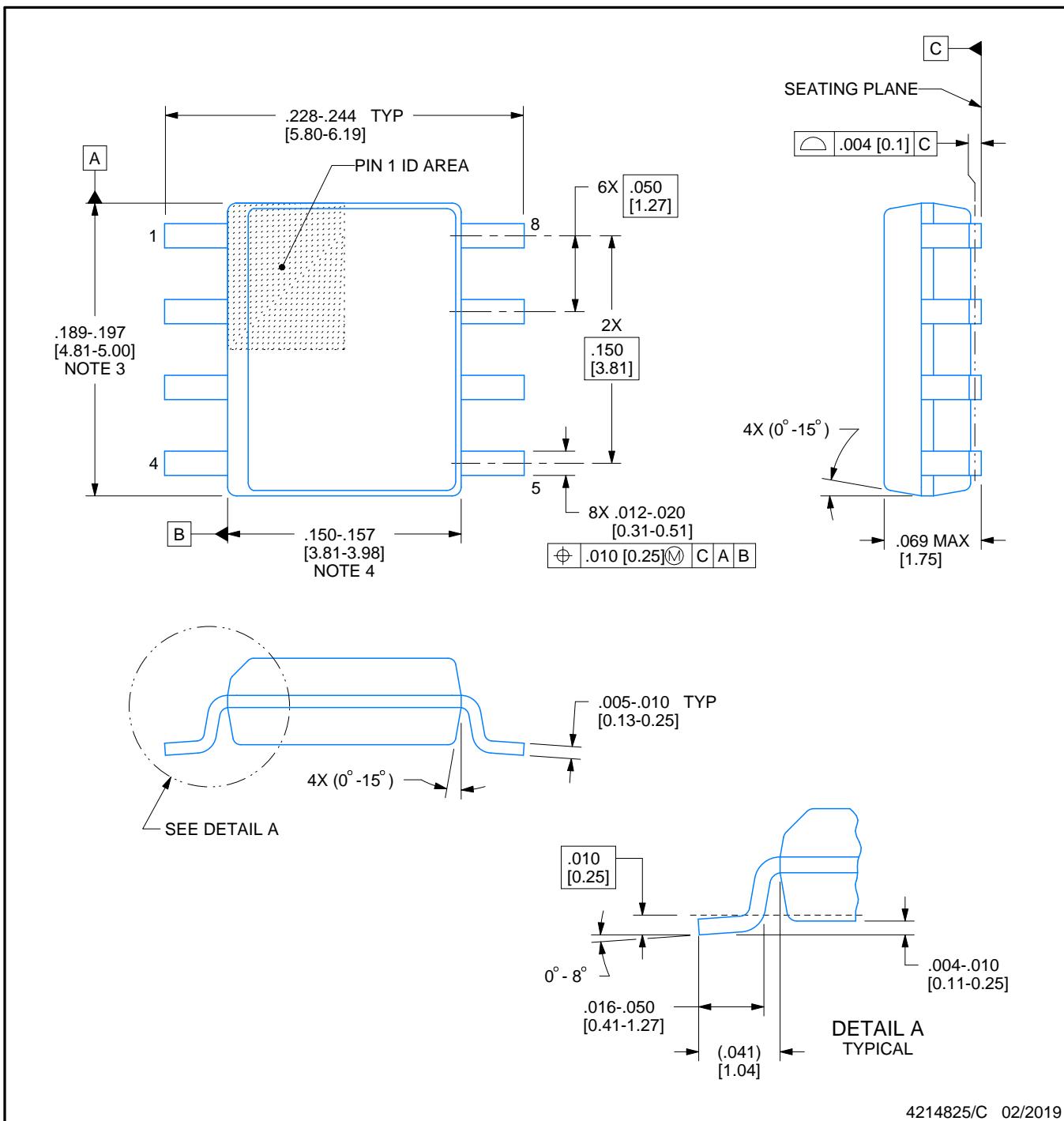
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



# PACKAGE OUTLINE

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



### NOTES:

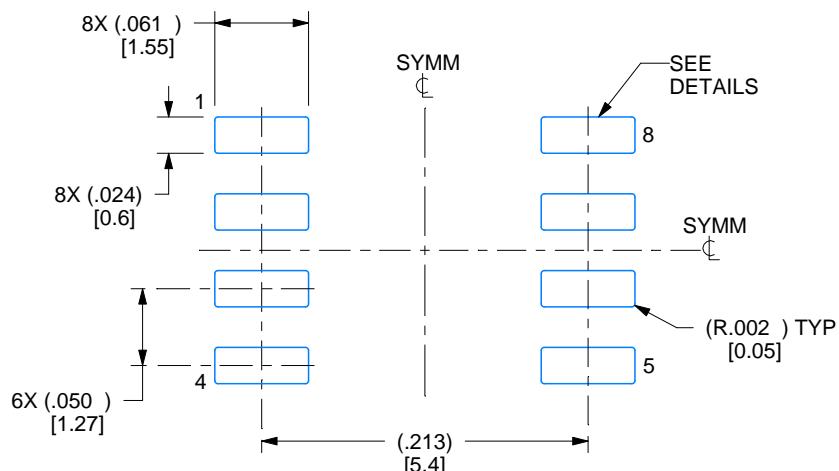
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

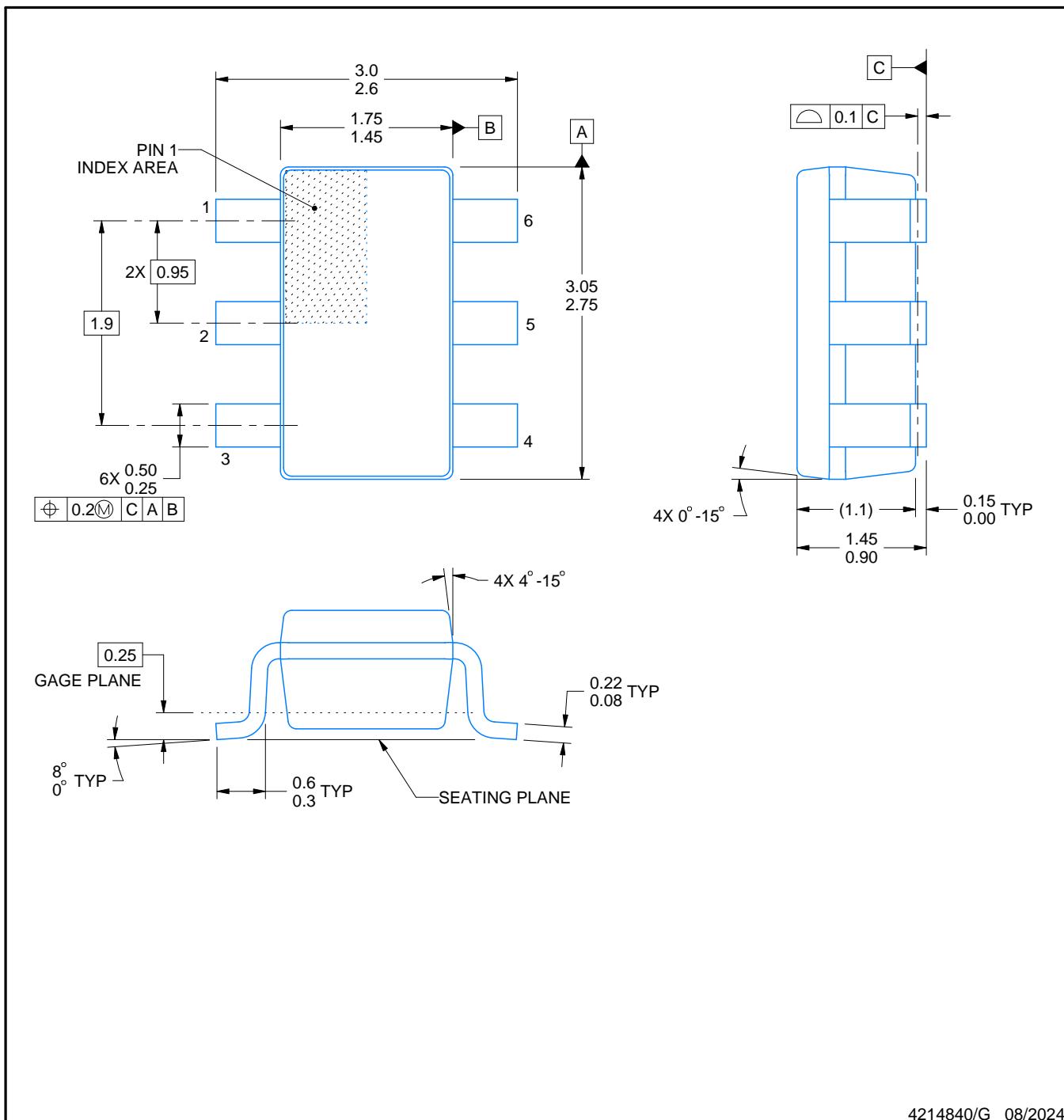
# PACKAGE OUTLINE

DBV0006A



SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



## NOTES:

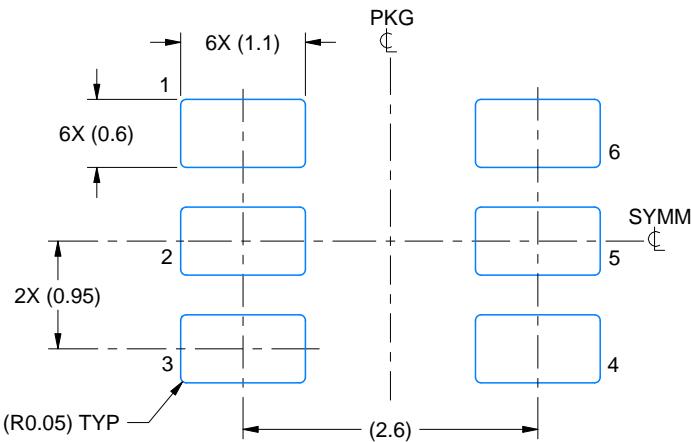
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

# EXAMPLE BOARD LAYOUT

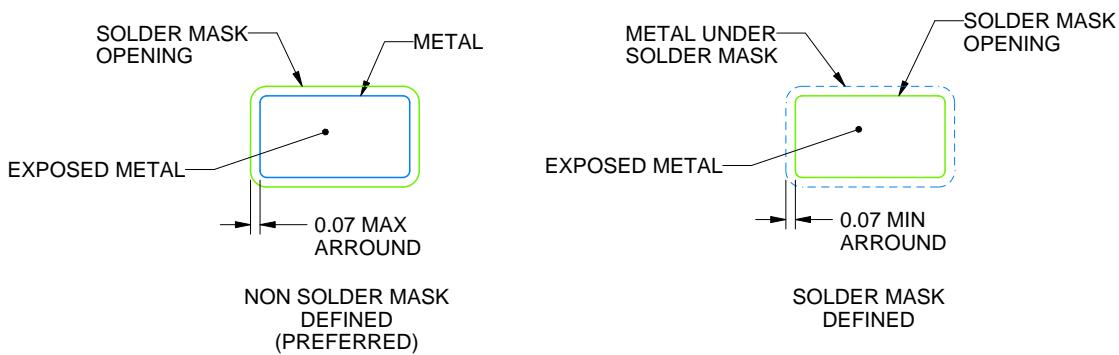
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

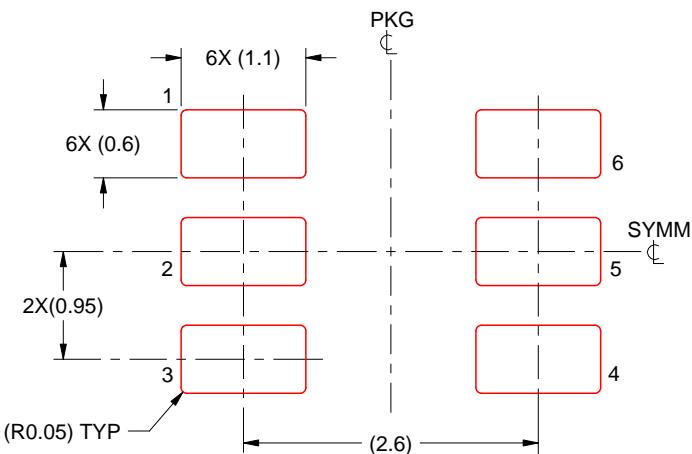
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025