

SCAN921821 Dual 18-Bit Serializer with Pre-emphasis, IEEE 1149.1 (JTAG), and At-Speed BIST

Check for Samples: [SCAN921821](#)

FEATURES

- **15-66 MHz Dual 18:1 Serializer with 2.376 Gbps Total Throughput**
- **8-level Selectable Pre-emphasis on Each Channel Drives Lossy Cables and Backplanes**
- **>15kV HBM ESD Protection on Bus LVDS I/O Pins**
- **Robust BLVDS Serial Data Transmission with Embedded Clock for Exceptional Noise Immunity and Low EMI**
- **Power Saving Control Pin for Each Channel**
- **IEEE 1149.1 "JTAG" Compliant**
- **At-Speed BIST - PRBS Generation**
- **No External Coding Required**
- **Internal PLL, No External PLL Components Required**
- **Single +3.3V Power Supply**
- **Low Power: 260 mW (typ) Per Channel at 66 MHz with PRBS-15 Pattern**
- **Single 3.3 V Supply**
- **Fabricated with Advanced CMOS Process Technology**
- **Industrial –40 to +85°C Temperature Range**
- **Compact 100-ball NFBGA Package**

DESCRIPTION

The SCAN921821 is a dual channel 18-bit serializer featuring signal conditioning, boundary SCAN, and at-speed BIST. Each serializer block transforms an 18-bit parallel LVCMOS/LVTTL data bus into a single Bus LVDS data stream with embedded clock. This single serial data stream with embedded clock simplifies PCB design and reduces PCB cost by narrowing data paths that in turn reduce PCB size and layers. The single serial data stream also reduces cable size, the number of connectors, and eliminates clock-to-data and data-to-data skew.

Each channel also has an 8-level selectable pre-emphasis feature that significantly extends performance over lossy interconnect. Each channel also has its own powerdown pin that saves power by reducing supply current when the channel is not being used.

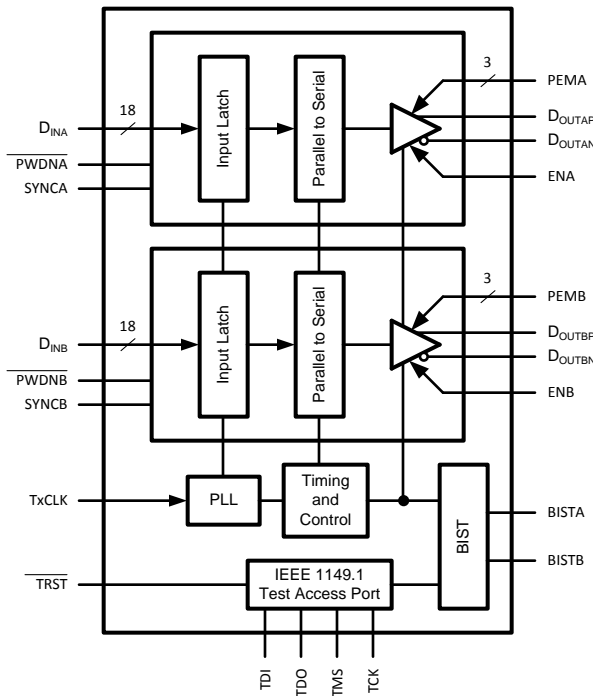
The SCAN921821 also incorporates advanced testability features including IEEE 1149.1 and at-speed BIST PRBS pattern generation to facilitate verification of board and link integrity



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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Block Diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

| | | | |
|---|------------------------------|------------------------------|---------|
| Supply Voltage (V_{DD}) | | -0.3V to +4V | |
| Supply Voltage (V_{DD}) Ramp Rate | | < 30 V/ms | |
| LVC MOS/LVTTL Input Voltage | | -0.3V to ($V_{DD} + 0.3V$) | |
| LVC MOS/LVTTL Output Voltage | | -0.3V to ($V_{DD} + 0.3V$) | |
| Bus LVDS Driver Output Voltage | | -0.3V to +3.9V | |
| Bus LVDS Output Short Circuit Duration | | 10ms | |
| Junction Temperature | | +150°C | |
| Storage Temperature | | -65°C to +150°C | |
| Lead Temperature (Soldering, 4 seconds) | | +220°C | |
| Maximum Package Power Dissipation at 25°C | NFBGA-100 | 3.57 W | |
| | Derating Above 25°C | 28.57 mW/°C | |
| Thermal resistance | θ_{JA} | 35°C/W | |
| | θ_{JC} | 11.1°C/W | |
| ESD Rating | HBM, 1.5 K Ω , 100 pF | All pins | >8 kV |
| | | Bus LVDS pins | >15 kV |
| | MM, 0 Ω , 200 pF | | >1200 V |
| | CDM | | >2 kV |

- (1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be specified. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.

Recommended Operating Conditions

| | Min | Nom | Max | Units |
|--|------|-----|------|--------|
| Supply Voltage (V_{DD}) | 3.15 | 3.3 | 3.45 | V |
| Operating Free Air Temperature (T_A) | -40 | +25 | +85 | °C |
| Clock Rate | 15 | | 66 | MHz |
| Supply Noise | | | 100 | mV p-p |

DC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. ⁽¹⁾⁽²⁾

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|--|---|--|------|------|----------|-------|
| LVC MOS/LVTTL Input DC Specifications | | | | | | |
| V_{IH} | High Level Input Voltage | | 2.0 | | V_{DD} | V |
| V_{IL} | Low Level Input Voltage | | GND | | 0.8 | V |
| V_{CL} | Input Clamp Voltage | $I_{CL} = -18$ mA | -1.5 | -0.7 | | V |
| I_{INH} | High Level Input Current | $V_{IN} = V_{DD} = V_{DDMAX}$ | -20 | ±2 | +20 | µA |
| I_{INL} | Low Level Output Current | $V_{IN} = V_{SS}, V_{DD} = V_{DDMAX}$ | -10 | ±2 | +10 | µA |
| 1149.1 (JTAG) DC Specifications | | | | | | |
| V_{IH} | High Level Input Voltage | | 2.0 | | V_{DD} | V |
| V_{IL} | Low Level Input Voltage | | GND | | 0.8 | V |
| V_{CL} | Input Clamp Voltage | $I_{CL} = -18$ mA | -1.5 | -0.7 | | V |
| I_{INH} | High Level Input Current | $V_{IN} = V_{DD} = V_{DDMAX}$ | -20 | | +20 | µA |
| I_{INL} | Low Level Output Current | $V_{IN} = V_{SS}, V_{DD} = V_{DDMAX}$ | -200 | | +200 | µA |
| V_{OH} | High Level Output Voltage | $I_{OH} = -9$ mA | 2.3 | | V_{DD} | mV |
| V_{OL} | Low Level Output Voltage | $I_{OL} = 9$ mA | GND | | 0.5 | mV |
| I_{OS} | Output Short Circuit Current | $V_{OUT} = 0$ V | -100 | -80 | -50 | mA |
| I_{OZ} | Output Tri-state Current | \overline{PWDN} or EN = 0.8V, $V_{OUT} = 0$ V | -10 | | +10 | µA |
| | | \overline{PWDN} or EN = 0.8V, $V_{OUT} = V_{DD}$ | -30 | | +30 | µA |
| Bus LVDS Output DC Specifications | | | | | | |
| V_{OD} | Output Differential Voltage (DO+) - (DO-) | See Figure 10 , $R_L = 100\Omega$ | 450 | 500 | 550 | mV |
| ΔV_{OD} | Output Differential Voltage Unbalance | | | 2 | 15 | mV |
| V_{OS} | Offset Voltage | | 1.05 | 1.2 | 1.25 | V |
| ΔV_{OS} | Offset Voltage Unbalance | | | 2.7 | 15 | mV |

(1) Typical values are given for $V_{CC} = 3.3$ V and $T_A = +25$ °C.

(2) Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground except V_{OD} , ΔV_{OD} , V_{TH} and V_{TL} which are differential voltages.

DC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.⁽¹⁾⁽²⁾

| Symbol | Parameter | Conditions | Min | Typ | Max | Units | |
|--|---|--|--|------|------|-------|----|
| Q _{POV} | Pre-Emphasis Output Voltage Ratio V _{ODPRE} / V _{OD} | Pre-Emphasis Level = 1 | 1.10 | 1.24 | 1.35 | | |
| | | Pre-Emphasis Level = 2 | 1.35 | 1.47 | 1.55 | | |
| | | Pre-Emphasis Level = 3 | 1.55 | 1.70 | 1.80 | | |
| | | Pre-Emphasis Level = 4 | 1.80 | 1.91 | 1.95 | | |
| | | Pre-Emphasis Level = 5 | 1.95 | 2.08 | 2.20 | | |
| | | Pre-Emphasis Level = 6 | 2.10 | 2.21 | 2.35 | | |
| | | Pre-Emphasis Level = 7 | 2.15 | 2.30 | 2.50 | | |
| I _{OS} | Output Short Circuit Current | DO = 0V, Din = H, $\overline{\text{PWDN}}$ and EN = 2.4V | -10 | -25 | -75 | mA | |
| I _{OZ} | TRI-STATE Output Current | $\overline{\text{PWDN}}$ or EN = 0.8V, DO = 0V ⁽³⁾ | -10 | ± 1 | +10 | µA | |
| | | $\overline{\text{PWDN}}$ or EN = 0.8V, DO = VDD ⁽³⁾ | -55 | ± 6 | +55 | µA | |
| Power Supply Current (DVDD, PVDD and AVDD Pins) | | | | | | | |
| I _{DD} | Total Supply Current (includes load current) | C _L = 15pF, R _L = 100 Ω | f = 66 MHz, PRBS-15 Pattern | | 160 | 225 | mA |
| | | | f = 66 MHz, Worst Case Pattern (Checker-Board Pattern) | | 180 | | mA |
| I _{DDP} | Total Supply Current with Pre-Emphasis (includes load current) | C _L = 15pF, R _L = 100 Ω | f = 66 MHz, PRBS-15 Pattern | | 240 | | mA |
| | | | f = 66 MHz, Worst Case Pattern (Checker-Board Pattern) | | 280 | 325 | mA |
| I _{DDX} | Supply Current Powerdown | $\overline{\text{PWDN}}$ = 0.8V, EN = 0.8V | | 1.0 | 3.0 | mA | |

(3) I_{OZ} is measured at each pin. The DOUT pin not under test is floated to isolate the TRI-STATE current flow.

Timing Requirements for TCLK

Over recommended operating supply and temperature ranges unless otherwise specified.⁽¹⁾⁽²⁾

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|-------------------|----------------------------|--------------------|------|------|------|----------|
| t _{TCP} | Transmit Clock Period | | 15.2 | T | 66.7 | ns |
| t _{TCH} | Transmit Clock High Time | | 0.4T | 0.5T | 0.6T | ns |
| t _{TCL} | Transmit Clock Low Time | | 0.4T | 0.5T | 0.6T | ns |
| t _{CLKT} | TCLK Input Transition Time | | | 3 | 6 | ns |
| t _{JIT} | TCLK Input Jitter | See ⁽³⁾ | | | 80 | ps (RMS) |

(1) Typical values are given for V_{CC} = 3.3V and T_A = +25°C.

(2) Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground except V_{OD}, ΔV_{OD}, V_{TH} and V_{TL} which are differential voltages.

(3) Specified by design using statistical analysis.

AC Electrical Characteristics

 Over recommended operating supply and temperature ranges unless otherwise specified. ⁽¹⁾⁽²⁾

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|--|---|--|---------------------|-----------------|----------------------|-------------|
| Serializer AC Specifications | | | | | | |
| t_{LLHT} | Bus LVDS Low-to-High Transition Time | See Figure 2 , ⁽³⁾ $R_L = 100\Omega$, $C_L = 10\text{pF}$ to GND | | 0.3 | 0.4 | ns |
| t_{LHLT} | Bus LVDS High-to-Low Transition Time | | | 0.3 | 0.4 | ns |
| t_{DIS} | DIN (0-17) Setup to TCLK | See Figure 4 , ⁽³⁾ $R_L = 100\Omega$, $C_L = 10\text{pF}$ to GND | 1.9 | | | ns |
| t_{DIH} | DIN (0-17) Hold from TCLK | | 0.6 | | | ns |
| t_{HZD} | DO \pm HIGH to TRI-STATE Delay | See Figure 5 $R_L = 100\Omega$, $C_L = 10\text{pF}$ to GND | | 3.9 | 10 | ns |
| t_{LZD} | DO \pm LOW to TRI-STATE Delay | | | 3.5 | 10 | ns |
| t_{ZHD} | DO \pm TRI-STATE to HIGH Delay | | | 3.2 | 10 | ns |
| t_{ZLD} | DO \pm TRI-STATE to LOW Delay | | | 2.4 | 10 | ns |
| t_{SPW} | SYNC Pulse Width | See Figure 7 , $R_L = 100\Omega$ | $5 \cdot t_{TCP}$ | | $6 \cdot t_{TCP}$ | ns |
| t_{PLD} | Serializer PLL Lock Time | See Figure 6 , $R_L = 100\Omega$ | $510 \cdot t_{TCP}$ | | $1024 \cdot t_{TCP}$ | ns |
| t_{SD} | Serializer Delay | See Figure 8 , $R_L = 100\Omega$ | $t_{TCP} + 2.5$ | $t_{TCP} + 4.5$ | $t_{TCP} + 6.5$ | ns |
| t_{SKCC} | Channel to Channel Skew | | | 70 | | ps |
| t_{RJIT} | Random Jitter | Room Temperature, $V_{DD} = 3.3\text{V}$, 66 MHz | | 6.1 | | ps (RMS) |
| t_{DJIT} | Deterministic Jitter Figure 9 , ⁽³⁾ | 15 MHz | -390 | | 320 | ps |
| | | 66 MHz | -60 | | 30 | ps |
| 1149.1 (JTAG) AC Specifications | | | | | | |
| f_{MAX} | Maximum TCK Clock Frequency | $C_L = 15\text{pF}$, $R_L = 500\Omega$ | 25 | | | MHz |
| t_S | TDI or TMS Setup to TCK, H or L | | 2.4 | | | ns |
| t_H | TDI or TMS Hold from TCK, H or L | | 2.8 | | | ns |
| t_{W1} | TCK Pulse Width, H or L | | 10 | | | ns |
| t_{W2} | $\overline{\text{TRST}}$ Pulse Width, L | | 10 | | | ns |
| t_{REC} | Recovery Time, $\overline{\text{TRST}}$ to TCK | | 2 | | | ns |

 (1) Typical values are given for $V_{CC} = 3.3\text{V}$ and $T_A = +25^\circ\text{C}$.

 (2) Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground except VOD, ΔVOD , VTH and VTL which are differential voltages.

(3) Specified by design using statistical analysis.

AC Timing Diagrams and Test Circuits

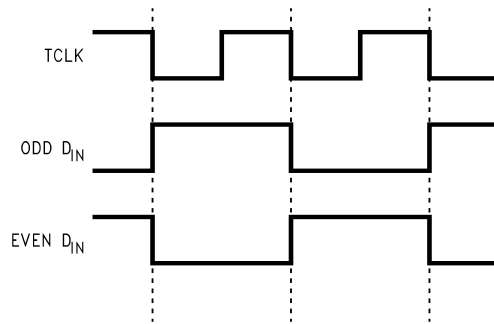


Figure 1. "Worst Case" Serializer IDD Test Pattern

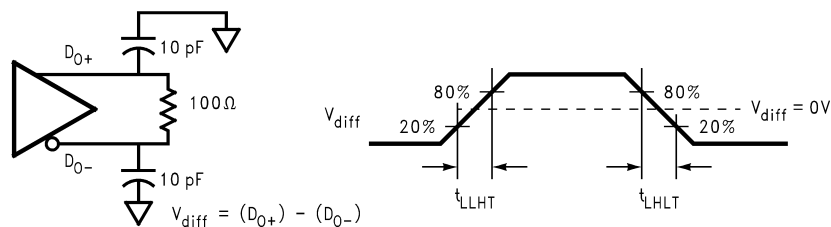


Figure 2. Serializer Bus LVDS Distributed Output Load and Transition Times

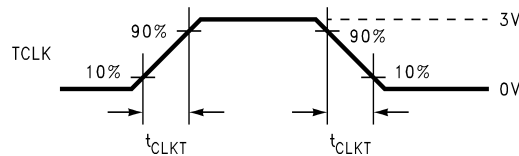


Figure 3. Serializer Input Clock Transition Time

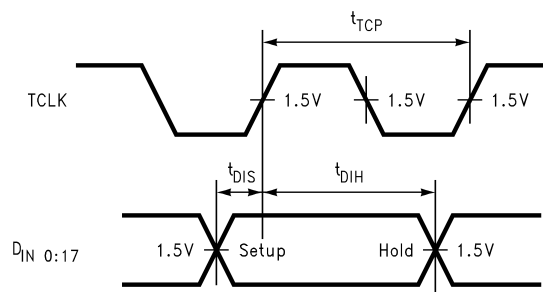


Figure 4. Serializer Setup/Hold Times

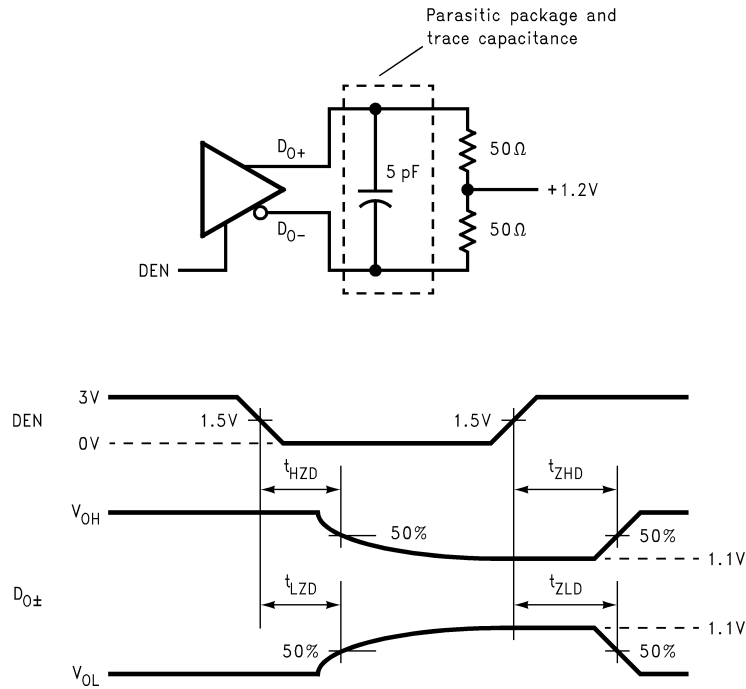


Figure 5. Serializer TRI-STATE Test Circuit and Timing

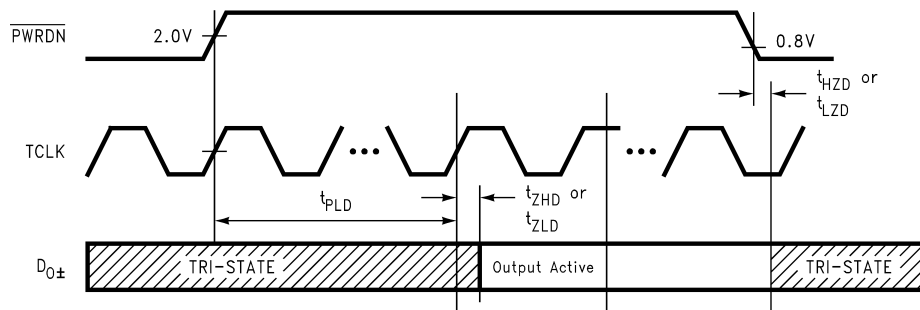


Figure 6. Serializer PLL Lock Time, and $\overline{\text{PWRDN}}$ TRI-STATE Delays

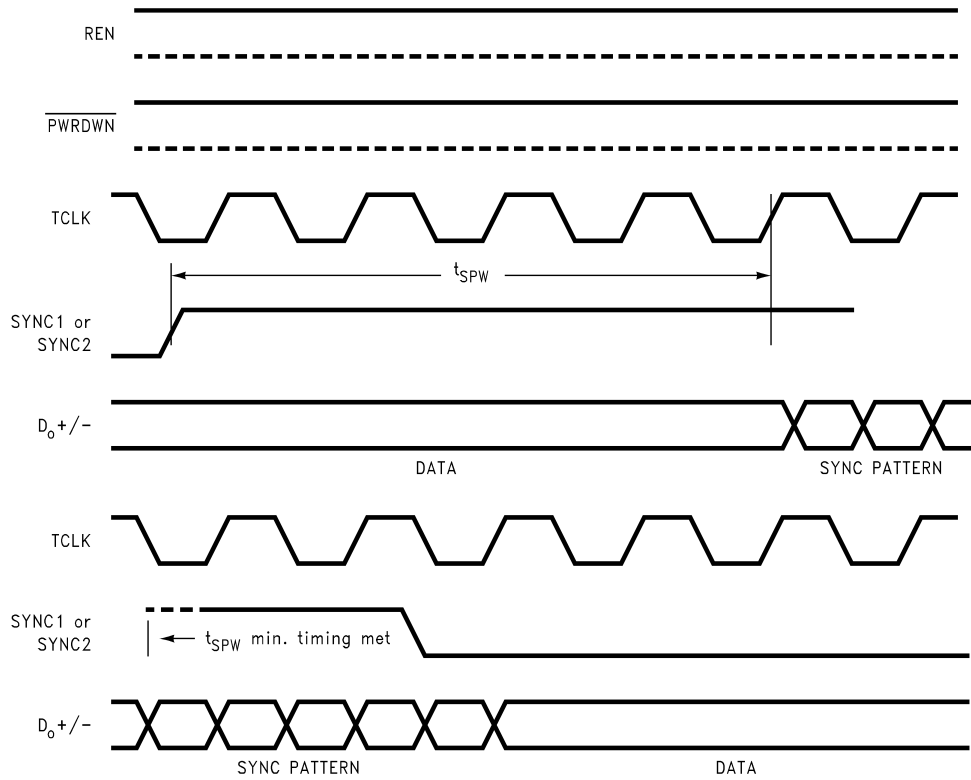


Figure 7. SYNC Timing Delay

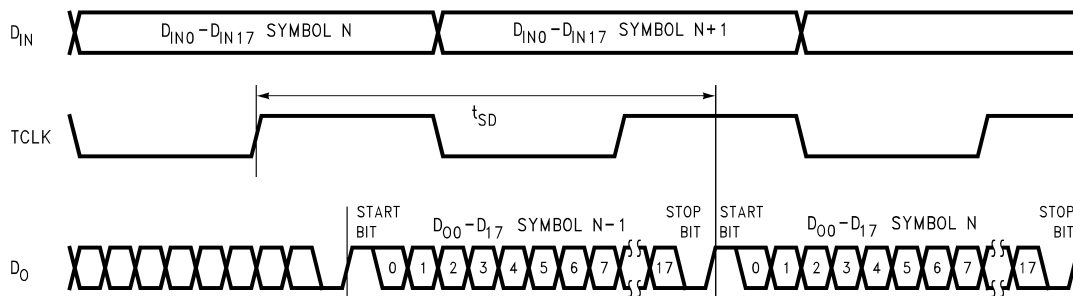


Figure 8. Serializer Delay

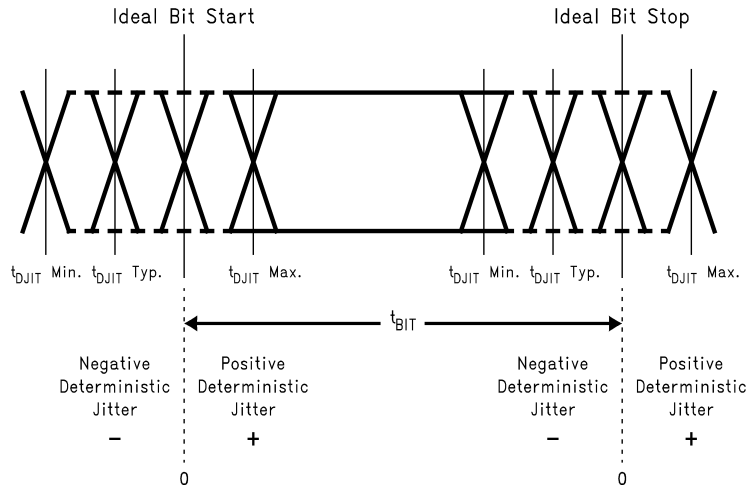
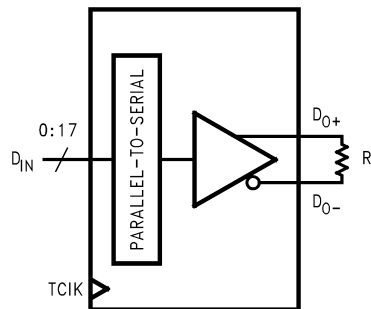


Figure 9. Deterministic Jitter and Ideal Bit Position



$$V_{OD} = (D_{O+}) - (D_{O-})$$

Differential output signal is shown as $(D_{O+}) - (D_{O-})$, device in Data Transfer mode.

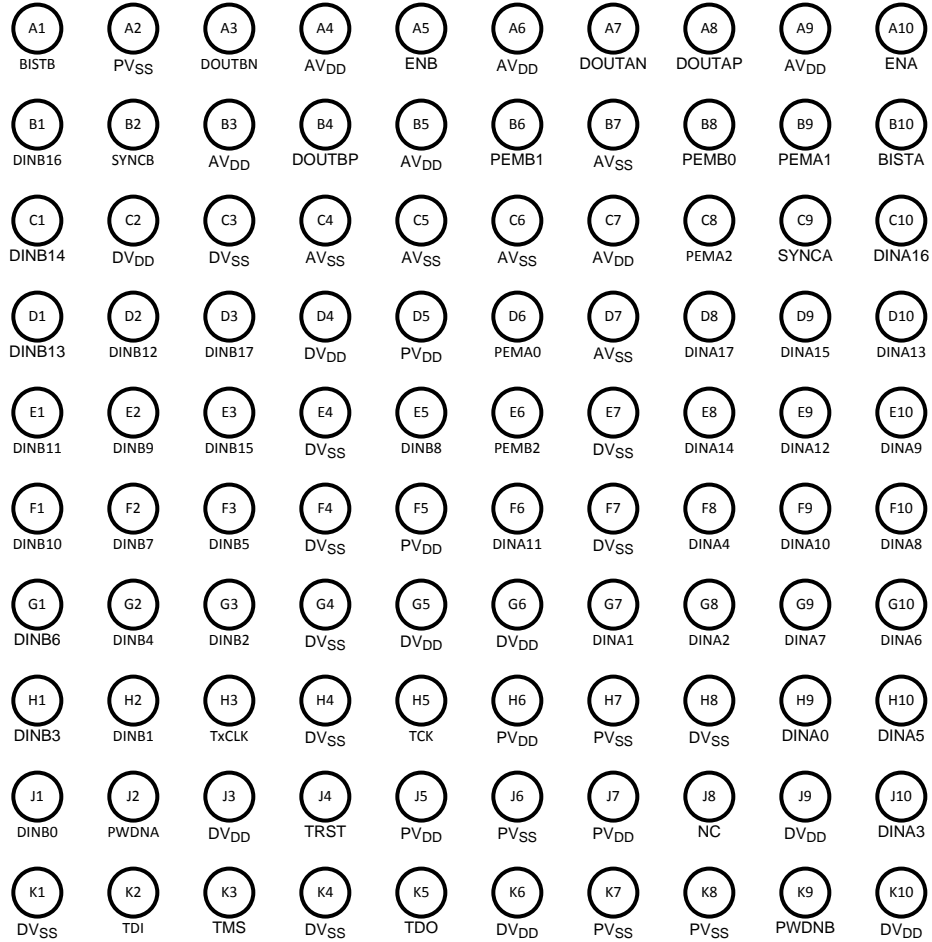
Figure 10. V_{OD} Diagram

Pre-emphasis Truth Table

| PEM LEVEL | PEM2 | PEM1 | PEM0 |
|-----------|------|------|------|
| 0 | L | L | L |
| 1 | L | L | H |
| 2 | L | H | L |
| 3 | L | H | H |
| 4 | H | L | L |
| 5 | H | L | H |
| 6 | H | H | L |
| 7 | H | H | H |

Pin Diagram

Figure 11. SCAN921821TVV
Top View



Pin Descriptions

| Pin Name | Pin Count | I/O, Type | Description |
|--------------------------------|-----------|-----------|---|
| DATA PINS | | | |
| DINA0-17 | 18 | I, LVCMOS | Transmitter <u>inputs</u> . There is a pull-down circuitry on each of these pins which are active if respective <u>PWDNA</u> or <u>PWDNB</u> pin is pulled high. |
| DINB0-17 | 18 | | |
| DOUTAP | 1 | O,BLVDS | Inverting and non-inverting differential transmitter outputs. |
| DOUTAN | 1 | | |
| DOUTBP | 1 | | |
| DOUTAN | 1 | | |
| TIMING AND CONTROL PINS | | | |
| TxCLK | 1 | I, LVCMOS | Transmitter reference clock. Used to strobe data at the inputs and to drive the transmitter PLL. There is a pull-up circuitry on this pin which is always active. |
| ENA | 1 | I, LVCMOS | Transmitter outputs <u>enable pins</u> . There is a pull-down circuitry on each of these pins that are active if corresponding <u>PWDNA</u> or <u>PWDNB</u> pin is pulled high. When these pins are set to LOW, the transmitter outputs will be disabled. The PLL will remain locked. |
| ENB | 1 | | |
| <u>PWDNA</u> | 1 | I, LVCMOS | Stand-by mode pins. There is a pull-down circuitry on each of these pins that are always active. When these pins are set to LOW, the transmitter will be put in low power mode and the PLL will lose lock. |
| <u>PWDNB</u> | 1 | | |
| SYNCA | 1 | I, LVCMOS | Transmitter synchronization pins. There is a pull-down circuitry on each of these pins that are active if corresponding <u>PWDNA</u> or <u>PWDNB</u> pin is pulled high. When these pins are set to HIGH, the transmitter will ignore incoming data and send SYNC patterns to provide a locking reference to receiver(s). |
| SYNCB | 1 | | |
| PRE-EMPHASIS PINS | | | |
| PEMA0-2 | 3 | I, LVCMOS | 8-level pre-emphasis selection pins. There is a pull-down circuitry on each of these pins which are active if corresponding <u>PWDNA</u> or <u>PWDNB</u> pin is pulled high. |
| PEMB0-2 | 3 | | |
| JTAG PINS | | | |
| TDI | 1 | I, LVCMOS | Test Data Input to support IEEE 1149.1. There is a pull-up circuitry on this pin which is always active. |
| TDO | 1 | O, LVCMOS | Test Data Output to support IEEE 1149.1. |
| TMS | 1 | I, LVCMOS | Test Mode Select Input to support IEEE 1149.1. There is a pull-up circuitry on this pin which is always active. |
| TCK | 1 | I, LVCMOS | Test Clock Input to support IEEE 1149.1. There is no failsafe circuitry on this pin. |
| <u>TRST</u> | 1 | I, LVCMOS | Test Reset Input to support IEEE 1149.1. There is a pull-up circuitry on this pin which is always active. |
| BIST PINS | | | |
| BISTA | 1 | I, LVCMOS | BIST selection pins. These pins select which transmitter will generate a PRBS like data. There is a pull-down circuitry on these pins which are active if corresponding <u>PWDNA</u> or <u>PWDNB</u> pin is pulled high. |
| BISTB | 1 | | |
| POWER PINS | | | |
| AVDD | 6 | I, POWER | Power Supply for the LVDS circuitry. |
| DVDD | 8 | I, POWER | Power Supply for the digital circuitry. |
| PVDD | 5 | I, POWER | Power Supply for the PLL and BG circuitry. |
| AVSS | 5 | I, POWER | Ground reference for the LVDS circuitry. |
| DVSS | 10 | I, POWER | Ground reference for the digital circuitry. |
| PVSS | 5 | I, POWER | Ground reference for the PLL and BG circuitry. |
| OTHER PINS | | | |
| NC | 1 | N/A | Not connected. |

REVISION HISTORY

| Changes from Revision B (April 2013) to Revision C | Page |
|--|------|
| • Changed layout of National Data Sheet to TI format | 11 |

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|------------------------------------|---------------|----------------------|-------------------|-------------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| SCAN921821TSM/NOPB | Active | Production | NFBGA (NZD) 100 | 240 JEDEC TRAY (10+1) | Yes | SNAGCU | Level-4-260C-72 HR | -40 to 85 | SCAN921821 TSM |
| SCAN921821TSM/NOPB.A | Active | Production | NFBGA (NZD) 100 | 240 JEDEC TRAY (10+1) | Yes | SNAGCU | Level-4-260C-72 HR | -40 to 85 | SCAN921821 TSM |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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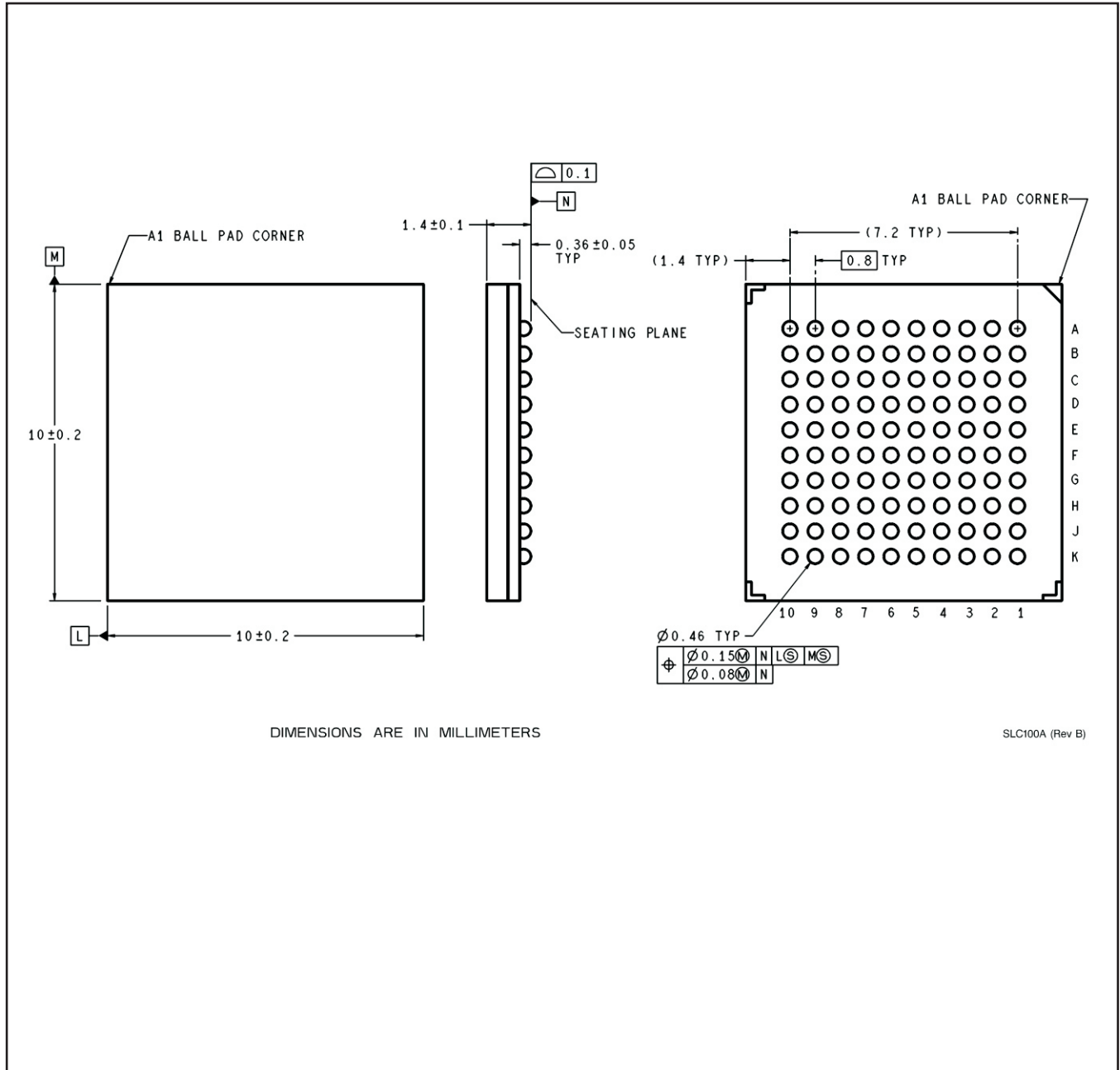
TRAY


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|--------------------------|--------------|--------------|------|-----|-------------------|----------------------|--------|--------|---------|---------|---------|---------|
| SCAN921821TSM/ NOPB | NZD | NFBGA | 100 | 240 | 10 X 24 | 150 | 322.6 | 135.9 | 7620 | 12.4 | 14.9 | 12.15 |
| SCAN921821TSM/ NOPB.A | NZD | NFBGA | 100 | 240 | 10 X 24 | 150 | 322.6 | 135.9 | 7620 | 12.4 | 14.9 | 12.15 |

NZD0100A



DIMENSIONS ARE IN MILLIMETERS

SLC100A (Rev B)

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