

## SNx4AHCT08 Quadruple 2-Input Positive-AND Gates

### 1 Features

- Inputs are TTL-voltage compatible
- Latch-up performance exceeds 250 mA per JESD 17
- ESD protection exceeds JESD 22:
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- On products compliant to MIL-PRF-38535, All parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

### 2 Applications

- [Servers](#)
- [Network switches](#)
- [PCs and notebooks](#)
- [Electronic points-of-sale](#)

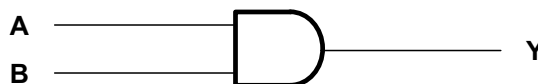
### 3 Description

The SNx4AHCT08 devices are quadruple 2-input positive-AND gates. These devices perform the Boolean function  $Y = A \times B$  or  $Y = \overline{\overline{A} + \overline{B}}$  in positive logic.

#### Package Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SNx4AHCT08	D (SOIC, 14)	8.65 mm × 3.91 mm
	DB (SSOP, 14)	6.20 mm × 5.30 mm
	NS (SOP, 14)	12.60 mm × 5.30 mm
	PW (TSSOP, 14)	5.00 mm × 4.40 mm
	RGY (VQFN, 14)	3.50 mm × 3.50 mm
	J (CDIP, 14)	19.56 mm × 6.67 mm
	W (CFP, 14)	9.21 mm × 5.97 mm
	DGV (TVSOP, 14)	3.60 mm × 4.40 mm
	N (PDIP, 14)	19.30 mm × 6.35 mm
	FK (LCCC, 20)	8.89 mm × 8.89 mm
BQA (WQFN, 14)	3.00 mm × 2.50 mm	

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic



## Table of Contents

<b>1 Features</b> .....	1	8.1 Overview.....	9
<b>2 Applications</b> .....	1	8.2 Functional Block Diagram.....	9
<b>3 Description</b> .....	1	8.3 Feature Description.....	9
<b>4 Revision History</b> .....	2	8.4 Device Functional Modes.....	9
<b>5 Pin Configuration and Functions</b> .....	3	<b>9 Application and Implementation</b> .....	10
<b>6 Specifications</b> .....	5	9.1 Application Information.....	10
6.1 Absolute Maximum Ratings.....	5	9.2 Typical Application.....	10
6.2 ESD Ratings.....	5	9.3 Power Supply Recommendations.....	11
6.3 Recommended Operating Conditions.....	5	9.4 Layout.....	11
6.4 Thermal Information.....	6	<b>10 Device and Documentation Support</b> .....	12
6.5 Electrical Characteristics.....	6	10.1 Receiving Notification of Documentation Updates..	12
6.6 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ .....	6	10.2 Support Resources.....	12
6.7 Noise Characteristics.....	7	10.3 Trademarks.....	12
6.8 Operating Characteristics.....	7	10.4 Electrostatic Discharge Caution.....	12
6.9 Typical Characteristics.....	7	10.5 Glossary.....	12
<b>7 Parameter Measurement Information</b> .....	8	<b>11 Mechanical, Packaging, and Orderable Information</b> .....	12
<b>8 Detailed Description</b> .....	9		

## 4 Revision History

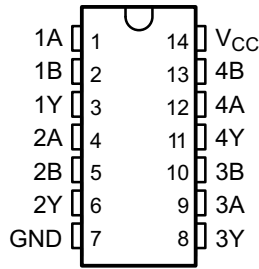
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision O (May 2023) to Revision P (October 2023)</b>	<b>Page</b>
<ul style="list-style-type: none"> <li>Updated R<math>\theta</math>JA values: D = 97.5 to 124.5; Updated D package for R<math>\theta</math>JC(top), R<math>\theta</math>JB, <math>\Psi</math>JT, <math>\Psi</math>JB, and R<math>\theta</math>JC(bot), all values in °C/W .....</li> </ul>	6

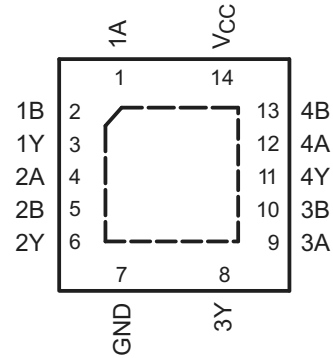
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<b>Changes from Revision N (September 2015) to Revision O (May 2023)</b>	<b>Page</b>
<ul style="list-style-type: none"> <li>Updated the numbering format for tables, figures, and cross-references throughout the document.....</li> <li>Updated the <i>package information</i> table to include BQA (WQFN).....</li> <li>Added BQA (WQFN) information to the <i>Thermal Information</i> table.....</li> </ul>	1 1 6

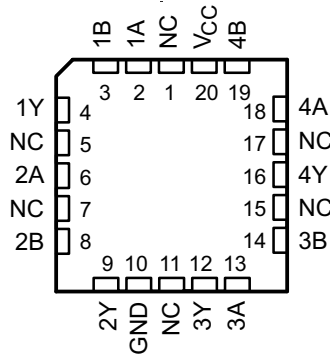
## 5 Pin Configuration and Functions



**Figure 5-1. SN54AHCT08 J or W Package, 14-Pin CDIP or CFP  
SN74AHCT08 D, DB, DGV, N, NS, or PW Package, 14-Pin SOIC, SSOP, TVSOP, PDIP, SO, or TSSOP (Top View)**



**Figure 5-2. SN74AHCT08 RGY or BQA Package, 14-Pin VQFN or WQFN (Top View)**



NC – No internal connection

**Figure 5-3. SN54HACT08 FK Package, 20-Pin LCCC (Top View)**

**Table 5-1. Pin Functions**

NAME	PIN				TYPE (1)	DESCRIPTION
	SN74AHCT08		SN54AHCT08			
	D, DB, DGV, N, NS, PW	RGY, BQA	J, W	FK		
1A	1	1	1	2	I	1A Input
1B	2	2	2	3	I	1B Input
1Y	3	3	3	4	O	1Y Output
2A	4	4	4	6	I	2A Input
2B	5	5	5	8	I	2B Input
2Y	6	6	6	9	O	2Y Output
3Y	8	8	8	12	O	3Y Output
3A	9	9	9	13	I	3A Input
3B	10	10	10	14	I	3B Input
4Y	11	11	11	16	O	4Y Output
4A	12	12	12	18	I	4A Input
4B	13	13	13	19	I	4B Input
GND	7	7	7	10	—	Ground Pin

**Table 5-1. Pin Functions (continued)**

NAME	PIN				TYPE (1)	DESCRIPTION
	SN74AHCT08		SN54AHCT08			
	D, DB, DGV, N, NS, PW	RGY, BQA	J, W	FK		
NC	—	—	—	1	—	No Connection
				5		
				7		
				11		
				15		
				17		
V <sub>CC</sub>	14	14	14	20	—	Power Pin

(1) I = input, O = output

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	-0.5	7	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>	-0.5	7	V
V <sub>O</sub>	Output voltage range <sup>(2)</sup>	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0	-20	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub>	±20	mA
I <sub>O</sub>	Continuous output current	V <sub>O</sub> = 0 to V <sub>CC</sub>	±25	mA
Continuous current through V <sub>CC</sub> or GND			±50	mA
T <sub>stg</sub>	Storage temperature range	-65	150	°C
T <sub>J</sub>	Junction temperature		150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		SN54AHCT08		SN74AHCT08		UNIT
		MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	2		2		V
V <sub>IL</sub>	Low-level input voltage		0.8		0.8	V
V <sub>I</sub>	Input voltage	0	5.5	0	5.5	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current		-8		-8	mA
I <sub>OL</sub>	Low-level output current		8		8	mA
Δt/Δv	Input transition rise or fall rate		20		20	ns/V
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	125	°C

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI Application Report, *Implications of Slow or Floating CMOS Inputs*, (SCBA004).

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	SNx4AHCT08					UNIT	
	D (SOIC)	DB (SSOP)	DGV (TVSOP)	N (PDIP)	BQA (WQFN)		
	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	124.5	109.5	133.3	59.7	88.3	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	78.8	62.1	55.6	47.3	90.9	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	81	56.9	66.3	39.5	56.8	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	37	22.6	7.8	32.4	9.9	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	80.6	56.3	56.6	39.4	56.7	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, (SPRA953).

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54AHCT08		SN74AHCT08		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	4.5 V	4.4	4.5		4.4		4.4	V	
	I <sub>OH</sub> = -8 mA		3.94			3.8		3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	4.5 V			0.1			0.1	V	
	I <sub>OL</sub> = 8 mA				0.36		0.44	0.44		
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V			±0.1		±1 <sup>(1)</sup>	±1	μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			2		20	20	μA	
ΔI <sub>CC</sub> <sup>(2)</sup>	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5 V			1.35		1.5	1.5	mA	
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		4	10			10	pF	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V<sub>CC</sub> = 0 V.

(2) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.

## 6.6 Switching Characteristics, V<sub>CC</sub> = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			SN54AHCT08		SN74AHCT08		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 15 pF	5 <sup>(1)</sup>	6.9 <sup>(1)</sup>		1 <sup>(1)</sup>	8 <sup>(1)</sup>	1	8	ns
t <sub>PHL</sub>				5 <sup>(1)</sup>	6.9 <sup>(1)</sup>		1 <sup>(1)</sup>	8 <sup>(1)</sup>	1	8	
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 50 pF	5.5	7.9		1	9	1	9	ns
t <sub>PHL</sub>				5.5	7.9		1	9	1	9	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

### 6.7 Noise Characteristics

$V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$ <sup>(1)</sup>

PARAMETER		SN74AHCT08			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		0.4	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$		-0.4	-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$	4.4			V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

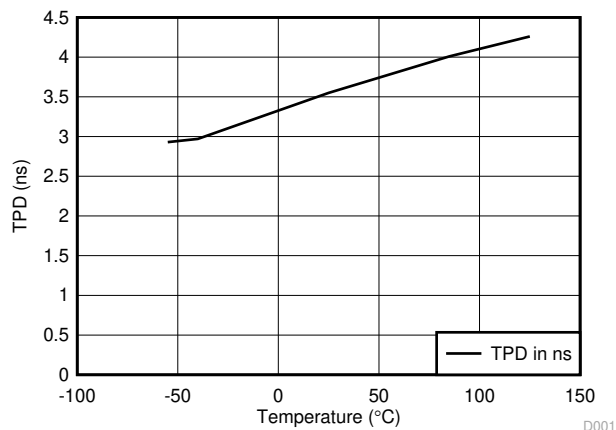
(1) Characteristics are for surface-mount packages only.

### 6.8 Operating Characteristics

$V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

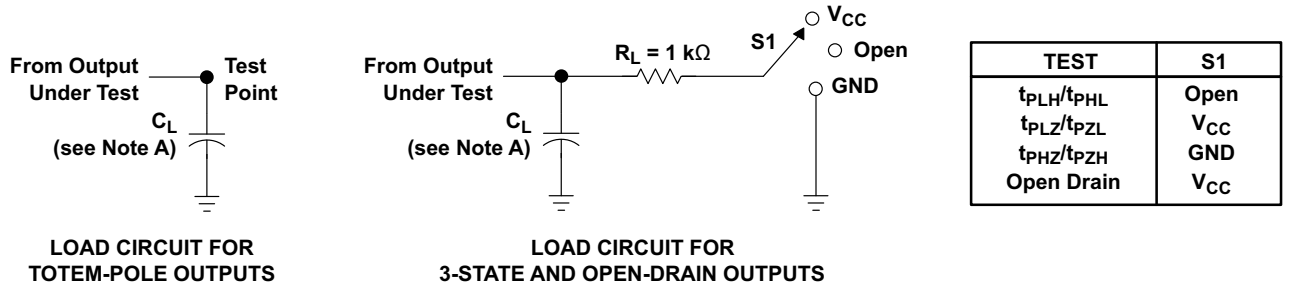
PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$	No load, $f = 1\text{ MHz}$	18	pF

### 6.9 Typical Characteristics



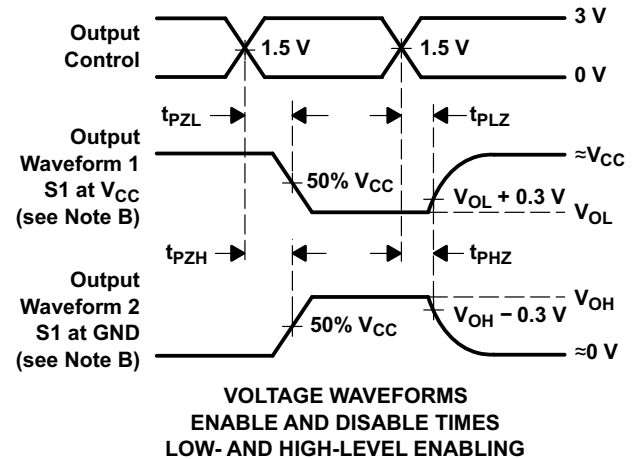
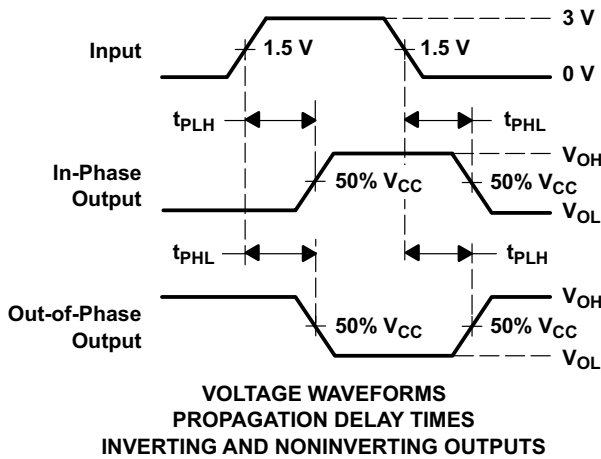
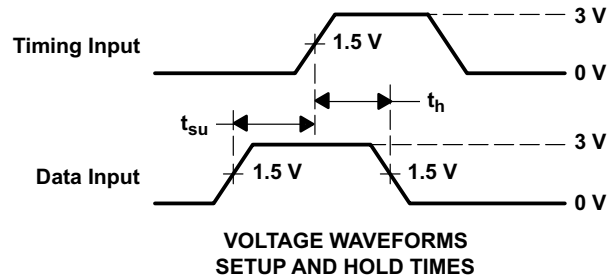
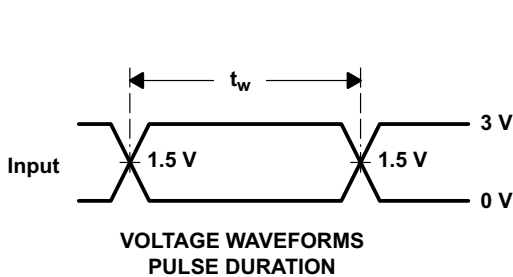
**Figure 6-1. TPD vs Temperature**

## 7 Parameter Measurement Information



LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 3$  ns,  $t_f \leq 3$  ns.  
 D. The outputs are measured one at a time with one input transition per measurement.  
 E. All parameters and waveforms are not applicable to all devices.

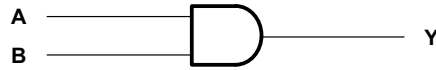
Figure 7-1. Load Circuit and Voltage Waveforms

## 8 Detailed Description

### 8.1 Overview

The SNx4AHCT08 devices are quadruple 2-input positive-AND gates with low drive that will produce slow rise and fall times. This slow transition reduces ringing on the output signal. The device has TTL inputs that allow up translation from 3.3 V to 5 V. The inputs are high impedance when  $V_{CC} = 0$  V.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

- Slow rise and fall time on outputs allow for low-noise outputs
- TTL inputs allow up translation from 3.3 V to 5 V

### 8.4 Device Functional Modes

Table 8-1 is the function table for the SNx4AHCT08.

**Table 8-1. Function Table  
(Each Gate)**

INPUTS		OUTPUT Y
A	B	
H	H	H
L	X	L
X	L	L

## 9 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

The SNx4AHCT08 devices are low-drive CMOS devices that can be used for a multitude of bus-interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The TTL inputs can accept voltages down to 3.3 V and translate up to 5 V.

### 9.2 Typical Application

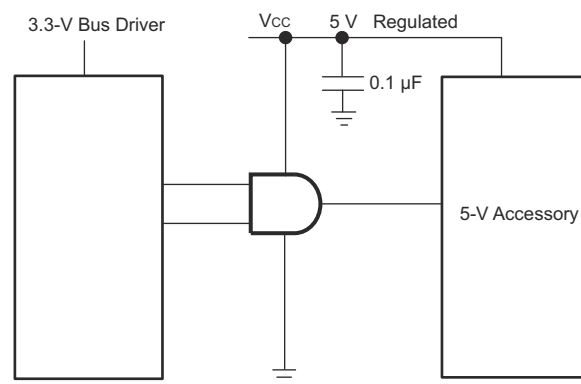


Figure 9-1. Typical Application Diagram

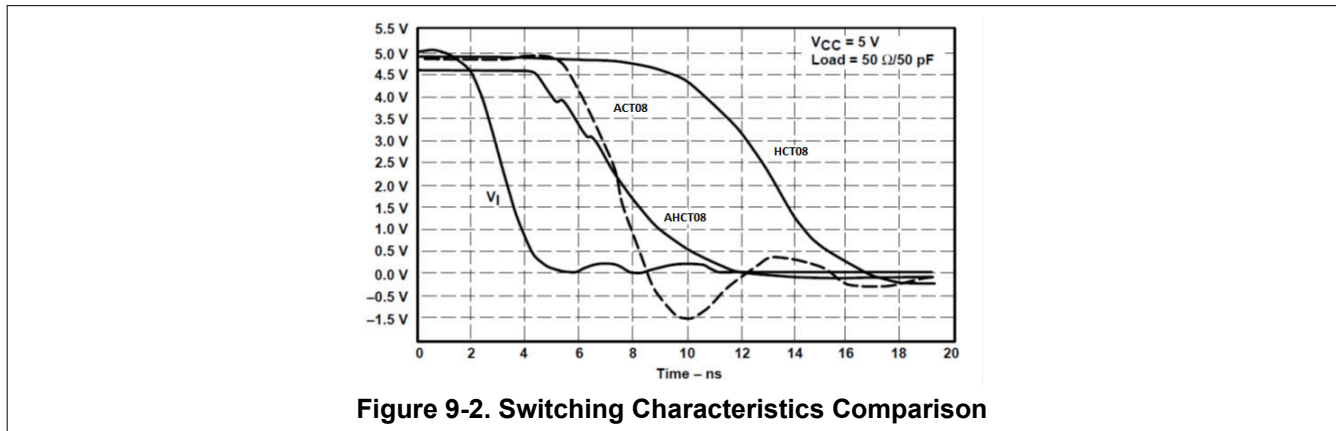
#### 9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

#### 9.2.2 Detailed Design Procedure

- Recommended input conditions
  - Rise time and fall time specs: See  $(\Delta t/\Delta V)$  in the [Recommended Operating Conditions](#) table.
  - Specified High and low levels: See  $(V_{IH}$  and  $V_{IL})$  in the [Recommended Operating Conditions](#) table.
  - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid  $V_{CC}$
- Recommend output conditions
  - Load currents should not exceed 25 mA per output and 50 mA total for the part
  - Outputs should not be pulled above  $V_{CC}$

### 9.2.3 Application Curves



### 9.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each  $V_{CC}$  pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1  $\mu\text{F}$  is recommended. If there are multiple  $V_{CC}$  pins, 0.01  $\mu\text{F}$  or 0.022  $\mu\text{F}$  is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1  $\mu\text{F}$  and 1  $\mu\text{F}$  are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

### 9.4 Layout

#### 9.4.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified in [Figure 9-3](#) are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$ ; whichever makes more sense or is more convenient. It is generally acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the IOs, so they cannot float when disabled.

## 9.4.2 Layout Example

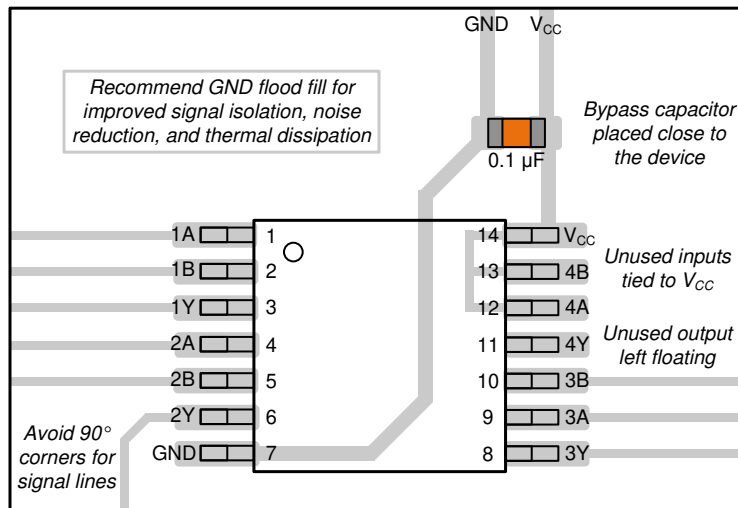


Figure 9-3. Example Layout for the SNx4AHCT08

## 10 Device and Documentation Support

### 10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 10.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 10.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9682101Q2A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9682101Q2A SNJ54AHCT 08FK
5962-9682101QCA	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9682101QC A SNJ54AHCT08J
5962-9682101QDA	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9682101QD A SNJ54AHCT08W
<a href="#">5962-9682101VDA</a>	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9682101VD A SNV54AHCT08W
5962-9682101VDA.A	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9682101VD A SNV54AHCT08W
<a href="#">SN74AHCT08BQAR</a>	Active	Production	WQFN (BQA)   14	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AHCT08
SN74AHCT08BQAR.A	Active	Production	WQFN (BQA)   14	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AHCT08
<a href="#">SN74AHCT08D</a>	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	-40 to 125	AHCT08
<a href="#">SN74AHCT08DBR</a>	Active	Production	SSOP (DB)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB08
SN74AHCT08DBR.A	Active	Production	SSOP (DB)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB08
<a href="#">SN74AHCT08DGV</a>	Active	Production	TVSOP (DGV)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB08
SN74AHCT08DGV.A	Active	Production	TVSOP (DGV)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB08
<a href="#">SN74AHCT08DR</a>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT08
SN74AHCT08DR.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT08
<a href="#">SN74AHCT08N</a>	NRND	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74AHCT08N
SN74AHCT08N.A	NRND	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74AHCT08N
<a href="#">SN74AHCT08NSR</a>	NRND	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT08
SN74AHCT08NSR.A	NRND	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT08
<a href="#">SN74AHCT08PW</a>	Obsolete	Production	TSSOP (PW)   14	-	-	Call TI	Call TI	-40 to 125	HB08
<a href="#">SN74AHCT08PWR</a>	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	HB08
SN74AHCT08PWR.A	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB08

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN74AHCT08PWRG4</a>	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB08
SN74AHCT08PWRG4.A	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB08
<a href="#">SN74AHCT08RGYR</a>	Active	Production	VQFN (RGY)   14	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HB08
SN74AHCT08RGYR.A	Active	Production	VQFN (RGY)   14	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HB08
<a href="#">SNJ54AHCT08FK</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9682101Q2A SNJ54AHCT08FK
SNJ54AHCT08FK.A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9682101Q2A SNJ54AHCT08FK
<a href="#">SNJ54AHCT08J</a>	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9682101QC A SNJ54AHCT08J
SNJ54AHCT08J.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9682101QC A SNJ54AHCT08J
<a href="#">SNJ54AHCT08W</a>	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9682101QD A SNJ54AHCT08W
SNJ54AHCT08W.A	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9682101QD A SNJ54AHCT08W

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54AHCT08, SN54AHCT08-SP, SN74AHCT08 :**

- Catalog : [SN74AHCT08](#), [SN54AHCT08](#)
- Enhanced Product : [SN74AHCT08-EP](#), [SN74AHCT08-EP](#)
- Military : [SN54AHCT08](#)
- Space : [SN54AHCT08-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHCT08BQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74AHCT08DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHCT08DGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AHCT08DR	SOIC	D	14	2500	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
SN74AHCT08DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHCT08NSR	SOP	NS	14	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
SN74AHCT08PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHCT08PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHCT08PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHCT08PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHCT08PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHCT08RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHCT08BQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74AHCT08DBR	SSOP	DB	14	2000	353.0	353.0	32.0
SN74AHCT08DGVR	TVSOP	DGV	14	2000	353.0	353.0	32.0
SN74AHCT08DR	SOIC	D	14	2500	340.5	336.1	32.0
SN74AHCT08DR	SOIC	D	14	2500	353.0	353.0	32.0
SN74AHCT08NSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74AHCT08PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74AHCT08PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AHCT08PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AHCT08PWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AHCT08PWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AHCT08RGYR	VQFN	RGY	14	3000	353.0	353.0	32.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9682101Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9682101QDA	W	CFP	14	25	506.98	26.16	6220	NA
5962-9682101VDA	W	CFP	14	25	506.98	26.16	6220	NA
5962-9682101VDA.A	W	CFP	14	25	506.98	26.16	6220	NA
SN74AHCT08N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHCT08N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHCT08N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHCT08N.A	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54AHCT08FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHCT08FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHCT08W	W	CFP	14	25	506.98	26.16	6220	NA
SNJ54AHCT08W.A	W	CFP	14	25	506.98	26.16	6220	NA

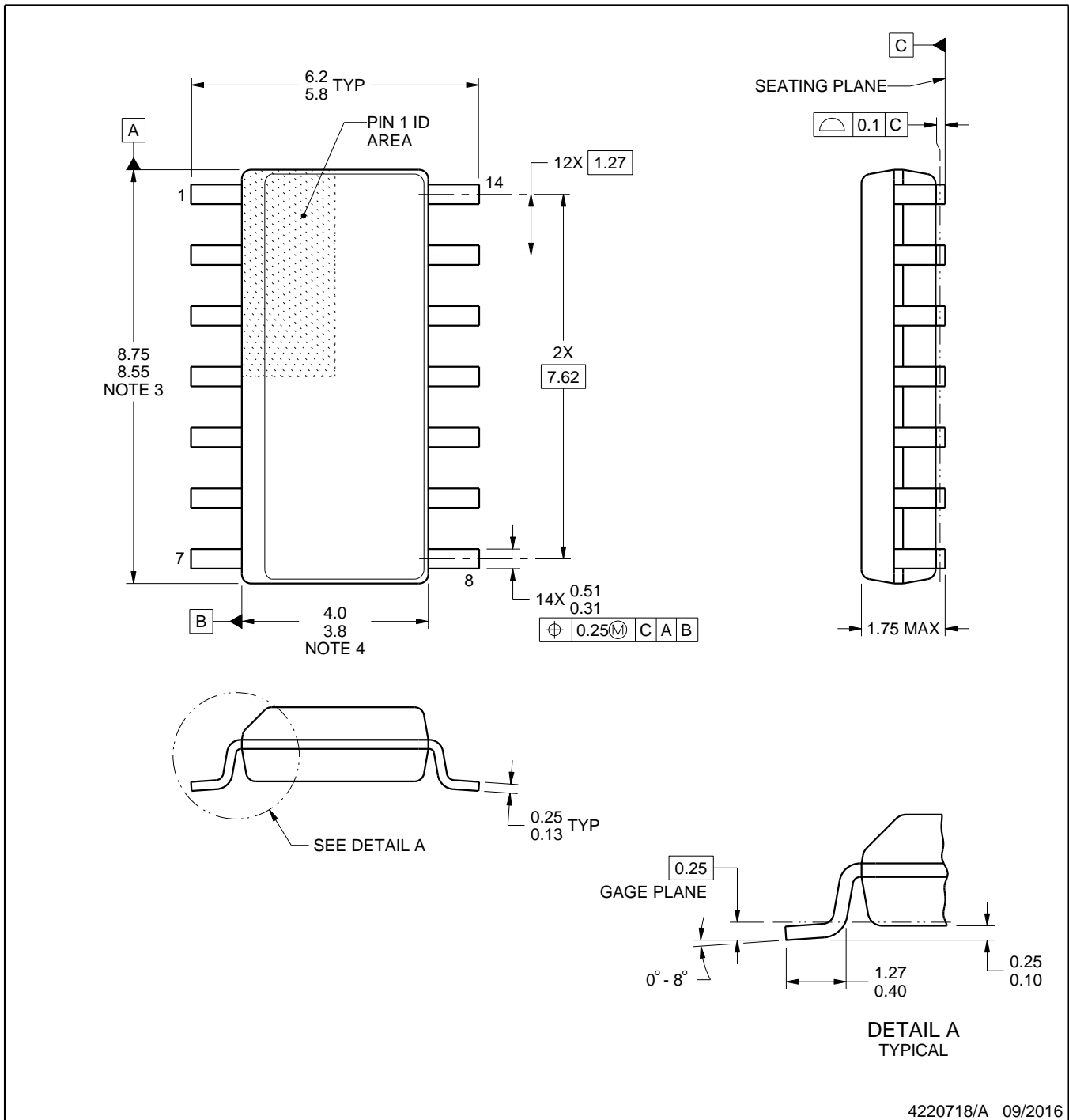
D0014A



# PACKAGE OUTLINE

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

- All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

**BQA 14**

**WQFN - 0.8 mm max height**

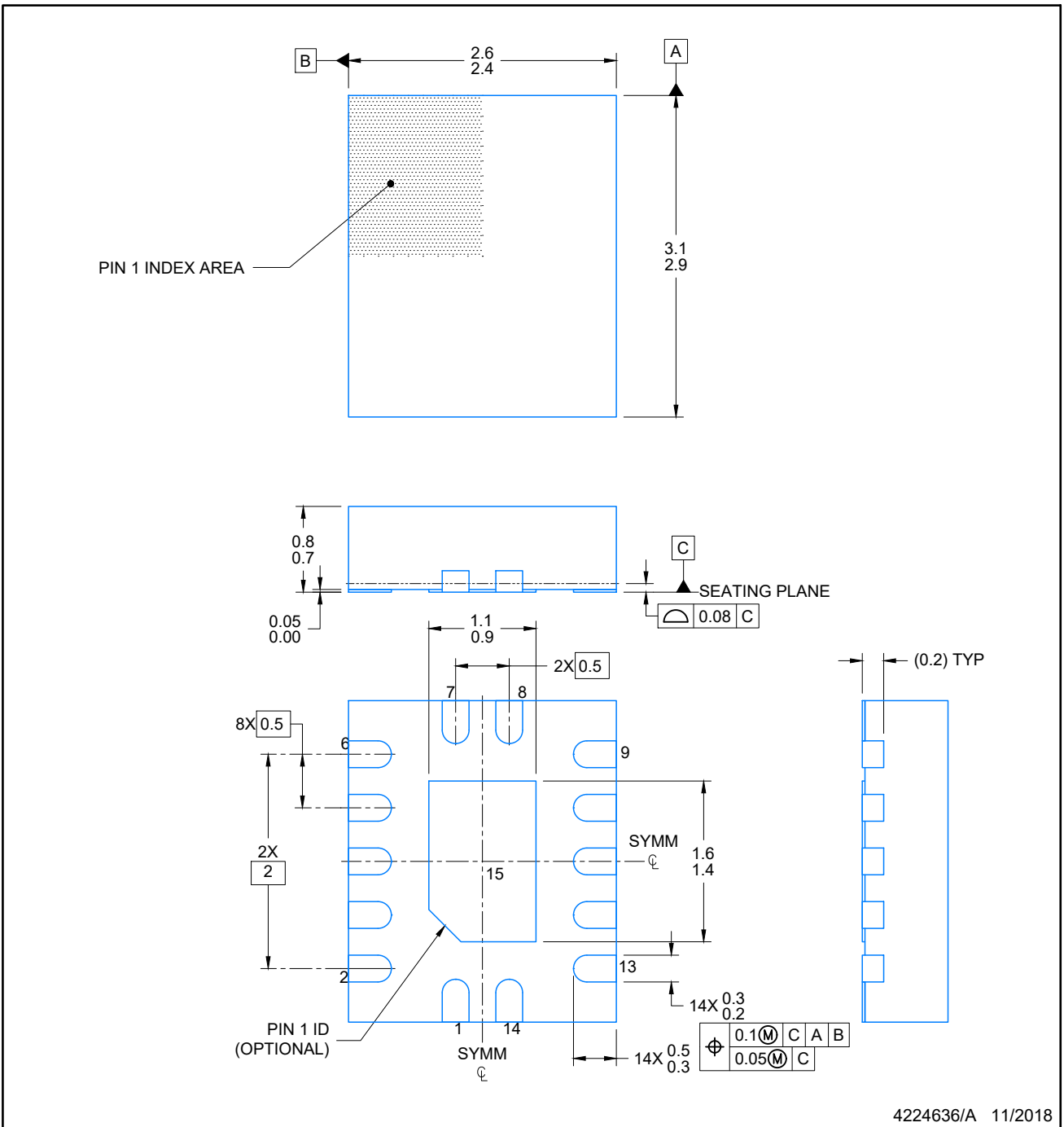
2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4227145/A



**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

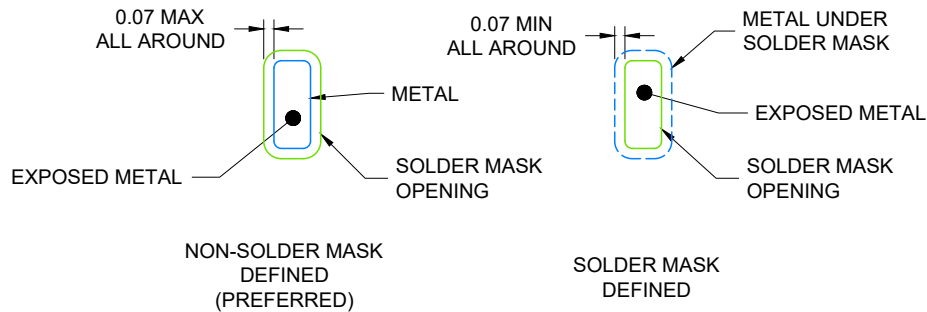
BQA0014A

WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X



4224636/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

BQA0014A

WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
88% PRINTED COVERAGE BY AREA  
SCALE: 20X

4224636/A 11/2018

NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F14

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

# DB0014A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4220762/A 05/2024

### NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220762/A 05/2024

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

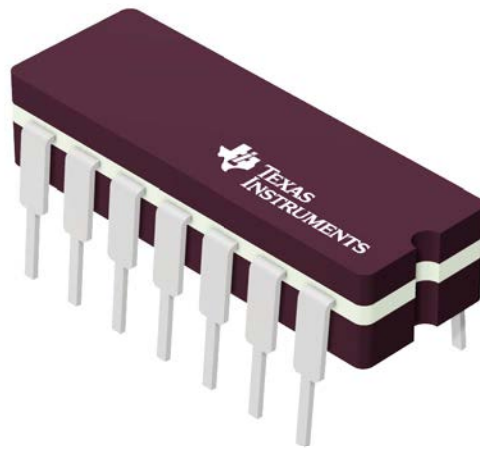
This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\

J 14

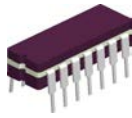
**GENERIC PACKAGE VIEW**  
**CDIP - 5.08 mm max height**  
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

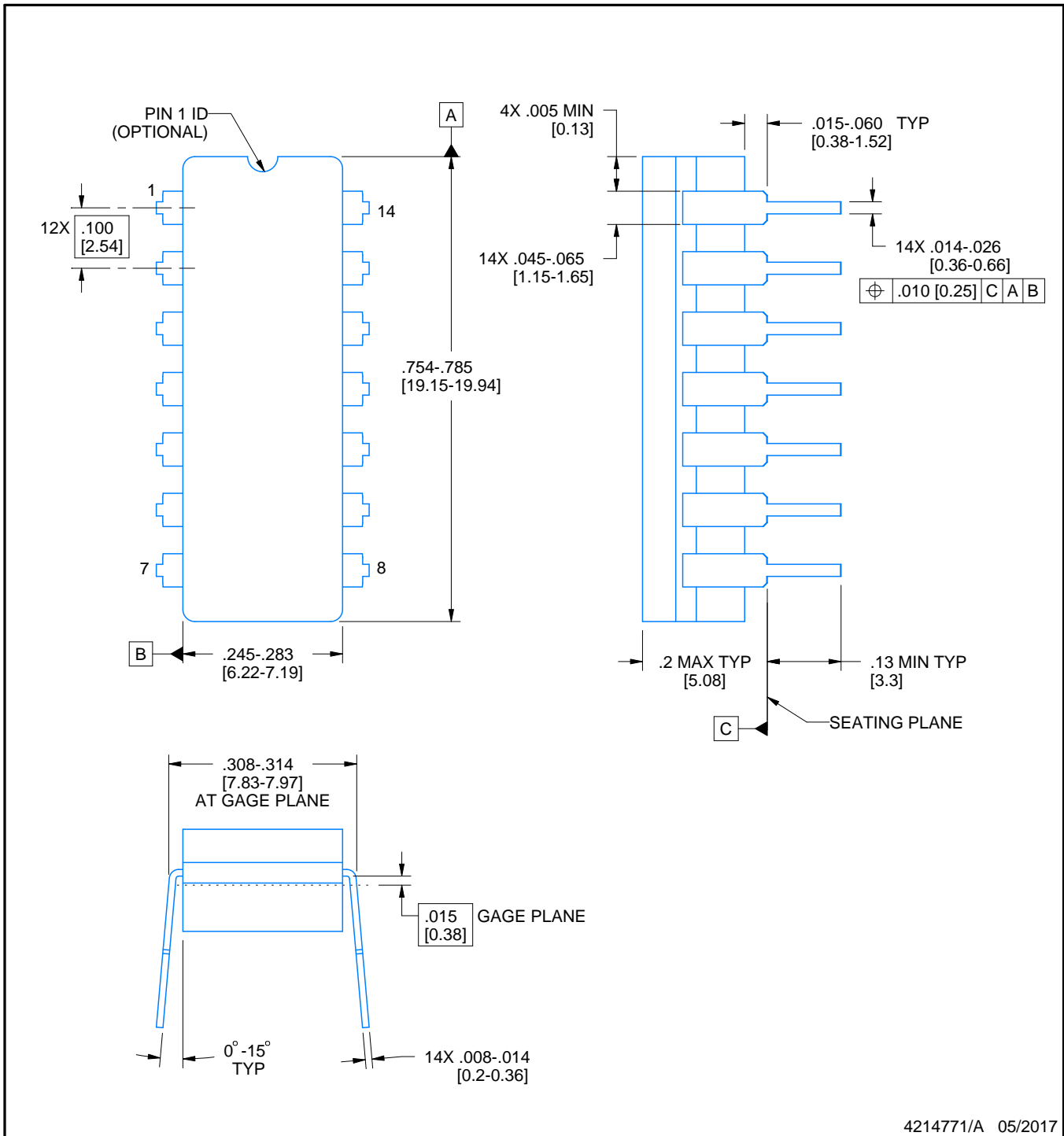
J0014A



# PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

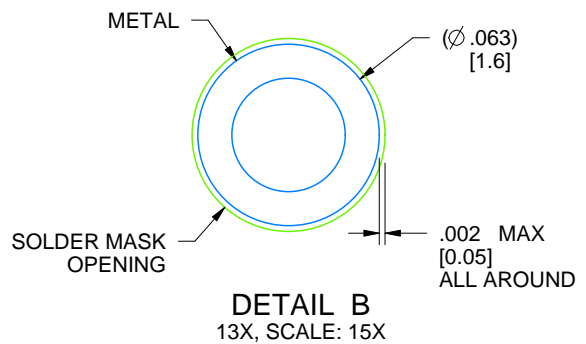
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

PW0014A



**PACKAGE OUTLINE**  
**TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

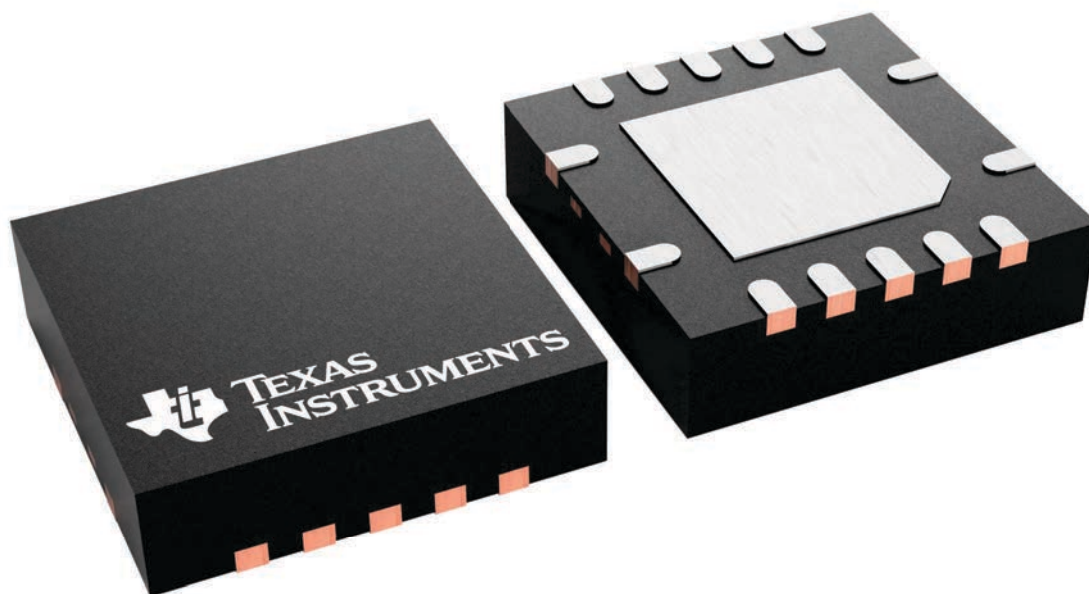
**RGY 14**

**VQFN - 1 mm max height**

3.5 x 3.5, 0.5 mm pitch

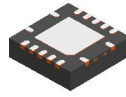
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4231541/A

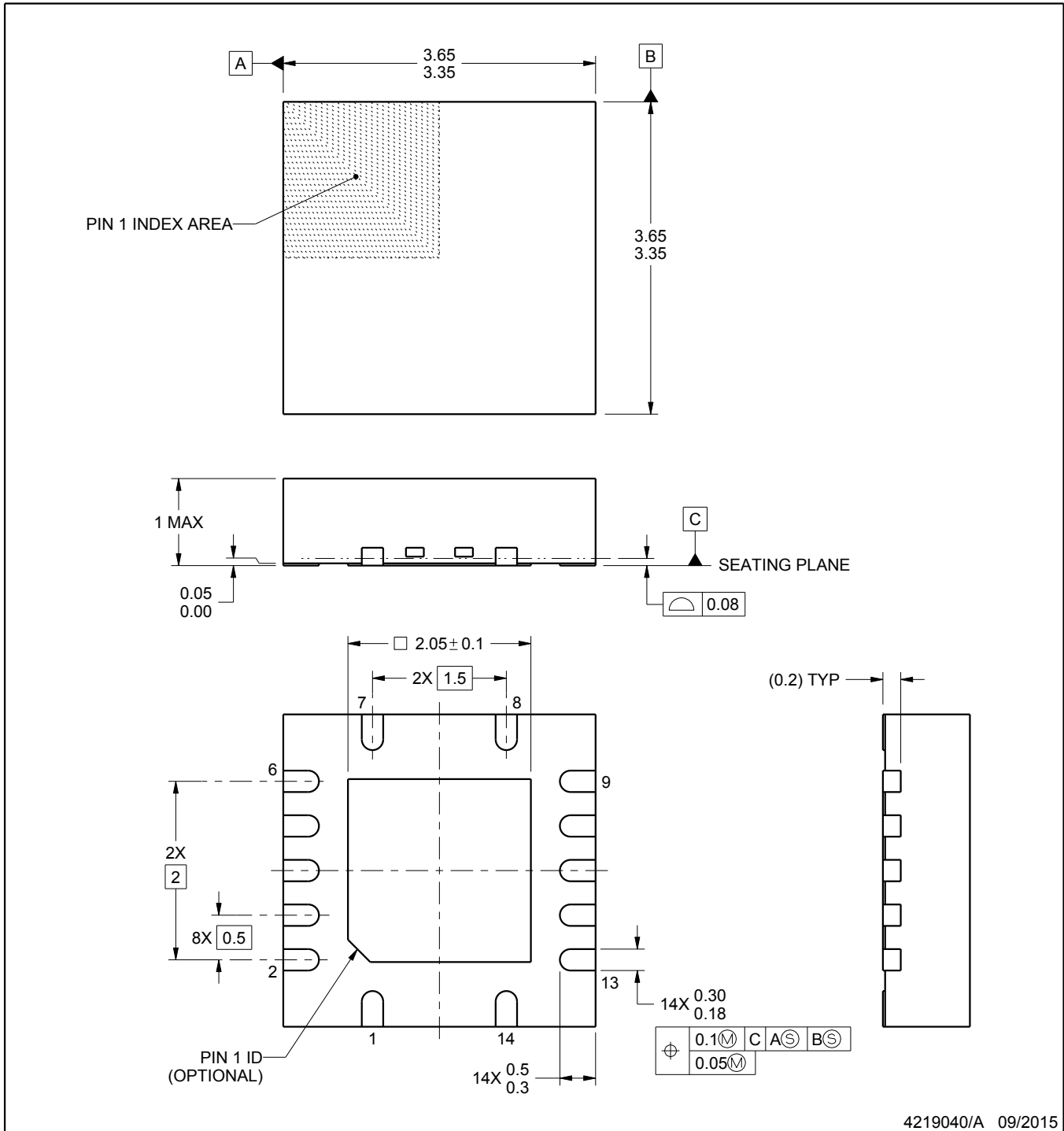
RGY0014A



PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4219040/A 09/2015

NOTES:

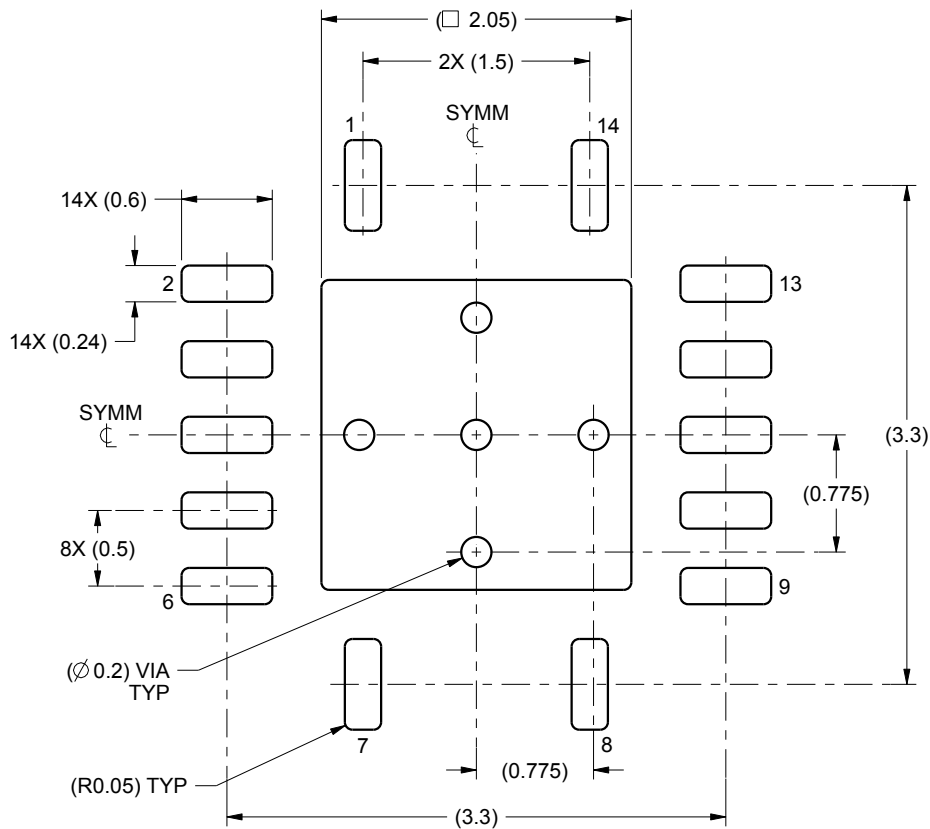
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

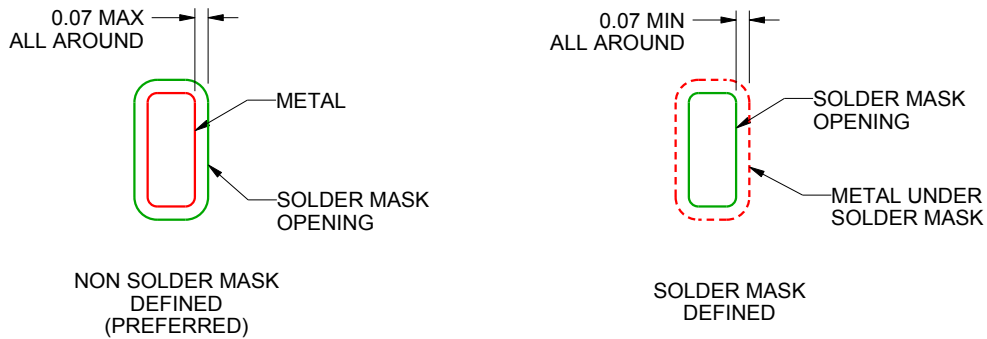
RGY0014A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:20X



SOLDER MASK DETAILS

4219040/A 09/2015

NOTES: (continued)

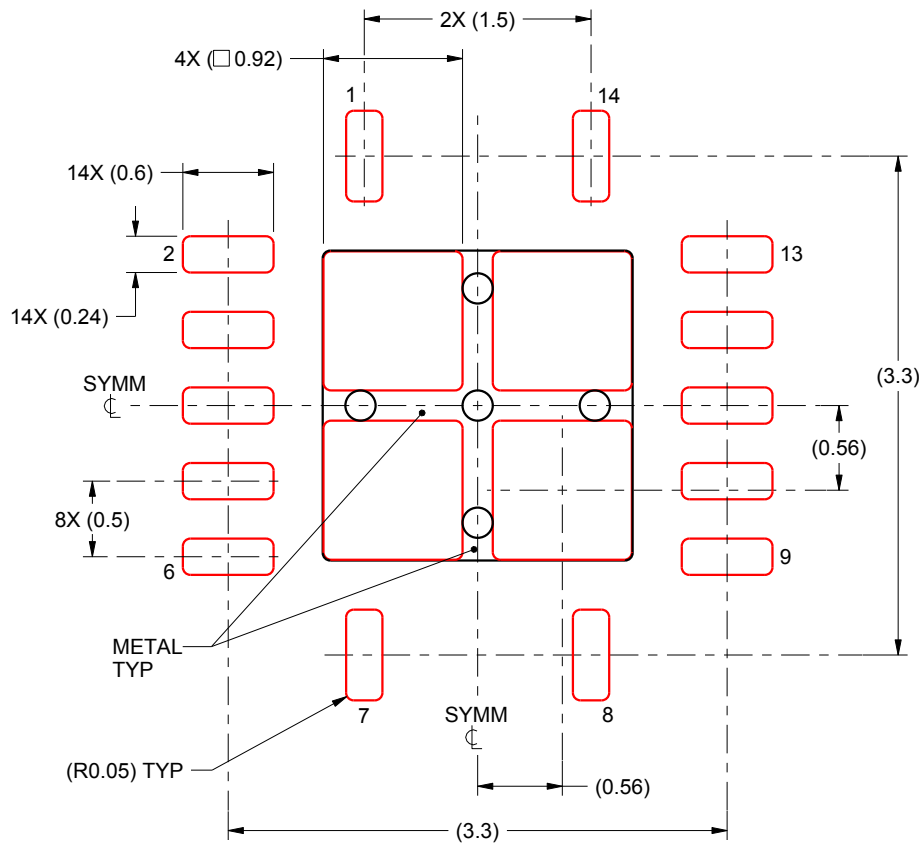
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slue271](http://www.ti.com/lit/slue271)).

# EXAMPLE STENCIL DESIGN

RGY0014A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
80% PRINTED SOLDER COVERAGE BY AREA  
SCALE:20X

4219040/A 09/2015

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Last updated 10/2025