

8-INPUT POSITIVE-NAND GATES

 Check for Samples: [SN54ALS30A](#), [SN54AS30](#), [SN74ALS30A](#), [SN74AS30](#)

FEATURES

- 8-Input Positive-NAND Gates
- Available in J, DW, N, and FK Packages

DESCRIPTION

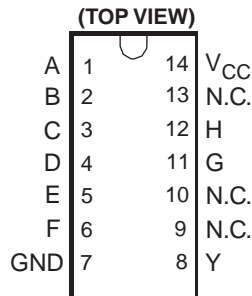
These devices contain an 8-input positive-NAND gate and perform the following Boolean functions in positive logic:

$$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H}$$

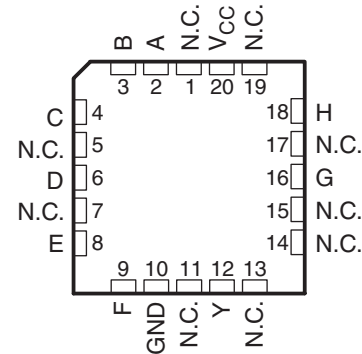
or

$$Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G}$$

SN54ALS30A, SN54AS30 . . . J PACKAGE
SN74ALS30A, SN74AS30 . . . DW OR N PACKAGE
SN74AS30 . . . DB PACKAGE



SN54ALS30A, SN54AS30 . . . FK PACKAGE
(TOP VIEW)



N.C. – No internal connection

ORDERING INFORMATION

| T _A | PACKAGE ^{(1) (2)} | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|----------------------------|---------------|-----------------------|------------------|
| 0°C to 70°C | PDIP – N | Tube | SN74ALS30AN | SN74ALS30AN |
| | | Tube | SN74AS30N | SN74AS30N |
| | SOIC – D | Tube | SN74AS30AD | ALS30A |
| | | Tape and reel | SN74ALS30ADR | |
| | | Tube | SN74AS30D | AS30 |
| | | Tape and reel | SN74AS30DR | |
| SSOP – DB | Tape and reel | SN74AS30DBR | AS30 | |
| –55°C to 125°C | CDIP – J | Tube | SNJ54ALS30AJ | SNJ54ALS30AJ |
| | | Tube | SNJ54AS30J | SNJ54AS30J |
| | LCCC –FK | Tube | SNJ54ALS30AFK | SNJ54ALS30AFK |
| | | Tube | SNJ54AS30FK | SNJ54AS30FK |

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

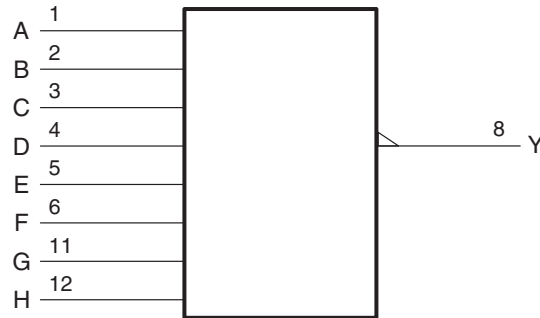


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Table 1. FUNCTION TABLE

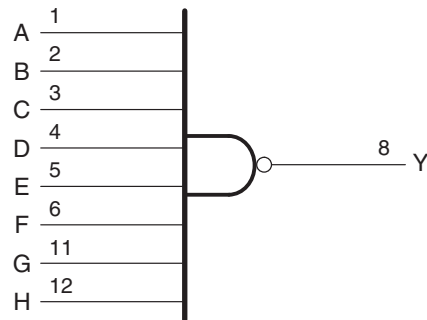
| INPUTS A–H | OUTPUT Y |
|----------------------|-------------|
| All inputs H | L |
| One or more inputs L | H |

LOGIC SYMBOL



A. This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin number shown are for the D, DB, J, and N packages.

LOGIC DIAGRAM (POSITIVE LOGIC)



Pin number shown are for the D, DB, J, and N packages.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---------------|--|------------|-----|------|
| V_{CC} | Supply voltage range | -0.5 | 7 | V |
| V_I | Input voltage range | -0.5 | 7 | V |
| θ_{JA} | Package thermal impedance ⁽²⁾ | D package | 86 | °C/W |
| | | DB package | 96 | |
| | | N package | 80 | |
| T_{stg} | Storage temperature range | -65 | 150 | °C |

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|----------|--------------------------------|----------------------|-----|--------------------|------|
| V_{CC} | Supply voltage | 4.5 | 5 | 5.5 | V |
| V_{IH} | High-level input voltage | 2 | | | V |
| V_{IL} | Low-level input voltage | | | 0.8 ⁽¹⁾ | V |
| | | | | 0.7 ⁽²⁾ | |
| I_{OH} | High-level output current | 'ALS30A | | -0.4 | mA |
| | | 'AS30 | | -2 | |
| I_{OL} | Low-level output current | SN54ALS30A | | 4 | mA |
| | | SN74ALS30A | | 8 | |
| | | 'AS30 | | 20 | |
| T_A | Operating free-air temperature | SN54ALS30A, SN54AS30 | -55 | 125 | °C |
| | | SN74ALS30A, SN74AS30 | 0 | 70 | |

- (1) Applies to the 'AS30 and SN74ALS30A across the full operating temperature range, and SN54ALS30A over the temperature range of -55°C to 7°C.
 (2) Applies to the SN54ALS30A over the temperature range of 70°C to 125°C.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|-------------|--|---------------------------|------------------|--------------------|--------------|------|
| V_{IK} | $V_{CC} = 4.5\text{ V}$, | $I_I = -18\text{ mA}$ | 'ALS30A 'AS30 | | -1.5 | V |
| V_{OH} | $V_{CC} = 4.5\text{ V to } 5.5\text{ V}$, | $I_{OH} = -0.4\text{ mA}$ | 'ALS30A | | $V_{CC} - 2$ | V |
| | | $I_{OH} = -2\text{ mA}$ | 'AS30 | | $V_{CC} - 2$ | |
| V_{OL} | $V_{CC} = 4.5\text{ V}$ | $I_{OL} = 4\text{ mA}$ | 'ALS30A | 0.25 | 0.4 | V |
| | | $I_{OL} = 8\text{ mA}$ | SN74ALS30A | 0.35 | 0.5 | |
| | | $I_{OL} = 20\text{ mA}$ | 'AS30 | 0.35 | 0.5 | |
| I_I | $V_{CC} = 5.5\text{ V}$, | $V_I = 7\text{ V}$ | | | 0.1 | mA |
| I_{IH} | $V_{CC} = 5.5\text{ V}$, | $V_I = 2.7\text{ V}$ | | | 20 | µA |
| I_{IL} | $V_{CC} = 5.5\text{ V}$, | $V_I = 0.4\text{ V}$ | 'ALS30A | | -0.1 | mA |
| | | | 'AS30 | | -0.5 | |
| $I_O^{(2)}$ | $V_{CC} = 5.5\text{ V}$, | $V_O = 2.25\text{ V}$ | SN54ALS30A | -20 | -112 | mA |
| | | | SN74ALS30A | -30 | -112 | |
| | | | 'AS30 | -30 | -112 | |
| I_{CCH} | $V_{CC} = 5.5\text{ V}$, | $V_I = 0\text{ V}$ | 'ALS30A | 0.22 | 0.36 | mA |
| | | | 'AS30 | 0.9 | 1.5 | |
| I_{CCL} | $V_{CC} = 5.5\text{ V}$, | $V_I = 4.5\text{ V}$ | 'ALS30A | 0.54 | 0.9 | mA |
| | | | 'AS30 | 3 | 4.9 | |

- (1) All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.
 (2) The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

SWITCHING CHARACTERISTICS

 over recommended operating conditions (unless otherwise noted (see [Figure 1](#)))

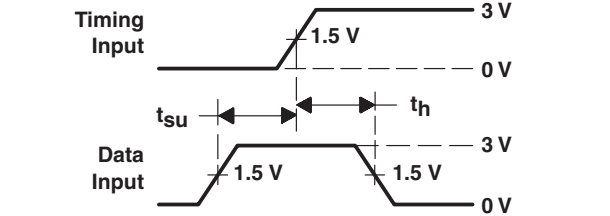
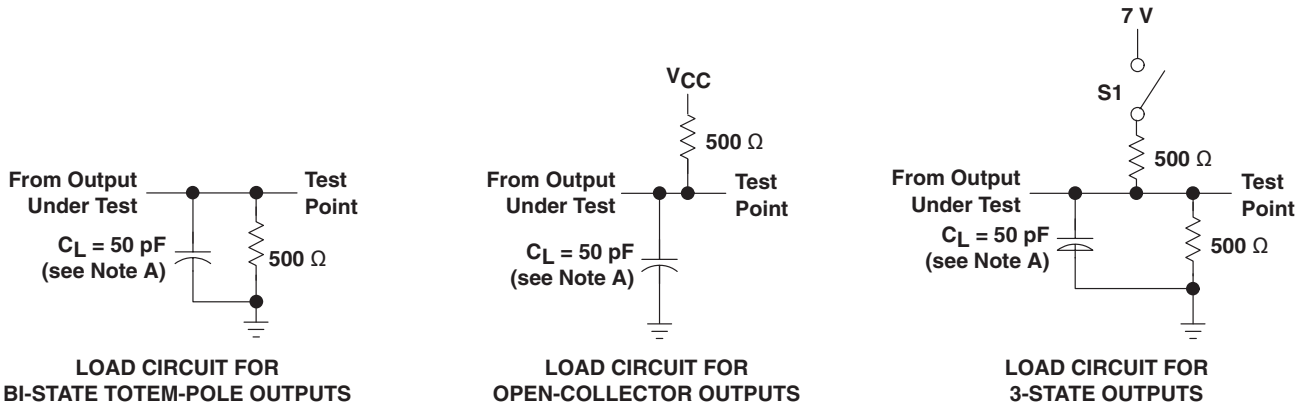
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | | MIN | MAX | UNIT |
|-----------|---------------------------|-------------|------------|-----|-----|------|
| t_{PLH} | A, B, C, D, E, F, G, or H | Y | SN54ALS30A | 3 | 15 | ns |
| | | | SN74ALS30A | 3 | 10 | |
| | | | SN54AS30 | 1 | 5.5 | |
| | | | SN74AS30 | 1 | 5 | |

SWITCHING CHARACTERISTICS (continued)

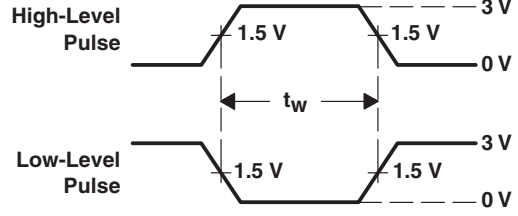
over recommended operating conditions (unless otherwise noted (see [Figure 1](#)))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | | MIN | MAX | UNIT |
|------------------|---------------------------|-------------|------------|-----|-----|------|
| t _{PHL} | A, B, C, D, E, F, G, or H | Y | SN54ALS30A | 3 | 15 | ns |
| | | | SN74ALS30A | 3 | 12 | |
| | | | SN54AS30 | 1 | 5 | |
| | | | SN74AS30 | 1 | 4.5 | |

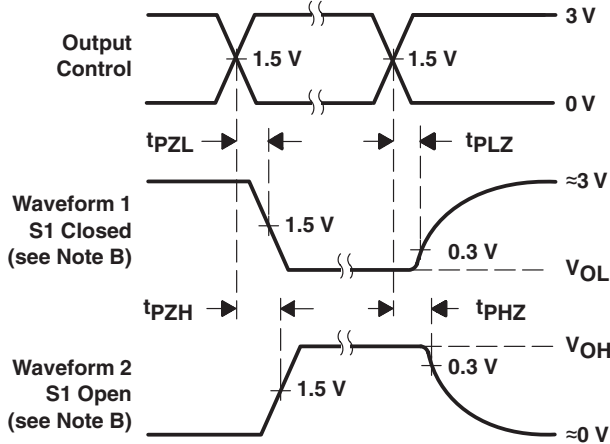
PARAMETER MEASUREMENT INFORMATION



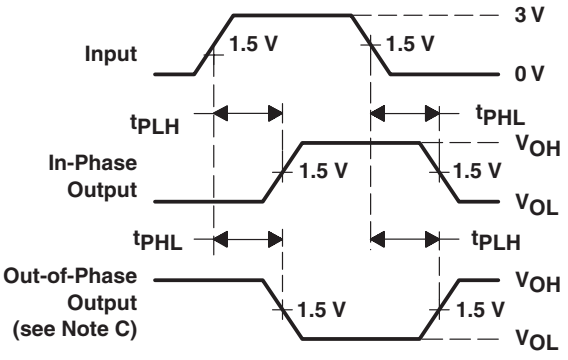
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES

- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
- D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
- E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

REVISION HISTORY

| Changes from Original (April 2009) to Revision E | Page |
|--|------|
| • Updated ORDERING INFORMATION table. | 1 |

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|----------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|------------------|---|
| 5962-86837012A | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962- 86837012A SNJ54ALS 30AFK |
| 5962-8683701DA | Active | Production | CFP (W) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8683701DA SNJ54ALS30AW |
| 5962-9755801QCA | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9755801QC A SNJ54AS30J |
| JM38510/37004B2A | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 37004B2A |
| JM38510/37004B2A.A | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 37004B2A |
| JM38510/37004BCA | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 37004BCA |
| JM38510/37004BCA.A | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 37004BCA |
| M38510/37004B2A | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 37004B2A |
| M38510/37004BCA | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 37004BCA |
| SN54ALS30AJ | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SN54ALS30AJ |
| SN54ALS30AJ.A | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SN54ALS30AJ |
| SN74ALS30AD | Obsolete | Production | SOIC (D) 14 | - | - | Call TI | Call TI | 0 to 70 | ALS30A |
| SN74ALS30ADB | Active | Production | SSOP (DB) 14 | 80 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | - | G30A |
| SN74ALS30ADB.A | Active | Production | SSOP (DB) 14 | 80 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | G30A |
| SN74ALS30ADBE4 | Active | Production | SSOP (DB) 14 | 80 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | See SN74ALS30ADB | G30A |
| SN74ALS30ADR | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS30A |
| SN74ALS30ADR.A | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS30A |
| SN74ALS30AN | Active | Production | PDIP (N) 14 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN74ALS30AN |
| SN74ALS30AN.A | Active | Production | PDIP (N) 14 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN74ALS30AN |
| SN74AS30DR | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | AS30 |

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---|
| SN74AS30DR.A | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | AS30 |
| SN74AS30N | Active | Production | PDIP (N) 14 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN74AS30N |
| SN74AS30N.A | Active | Production | PDIP (N) 14 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN74AS30N |
| SNJ54ALS30AFK | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962- 86837012A SNJ54ALS 30AFK |
| SNJ54ALS30AFK.A | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962- 86837012A SNJ54ALS 30AFK |
| SNJ54ALS30AJ | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SNJ54ALS30AJ |
| SNJ54ALS30AJ.A | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SNJ54ALS30AJ |
| SNJ54ALS30AW | Active | Production | CFP (W) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8683701DA SNJ54ALS30AW |
| SNJ54ALS30AW.A | Active | Production | CFP (W) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8683701DA SNJ54ALS30AW |
| SNJ54AS30J | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9755801QC A SNJ54AS30J |
| SNJ54AS30J.A | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9755801QC A SNJ54AS30J |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54ALS30A, SN54AS30, SN74ALS30A, SN74AS30 :

- Catalog : [SN74ALS30A](#), [SN74AS30](#)
- Military : [SN54ALS30A](#), [SN54AS30](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ALS30ADR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74AS30DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

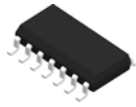
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ALS30ADR | SOIC | D | 14 | 2500 | 353.0 | 353.0 | 32.0 |
| SN74AS30DR | SOIC | D | 14 | 2500 | 353.0 | 353.0 | 32.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|--------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-86837012A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| 5962-8683701DA | W | CFP | 14 | 25 | 506.98 | 26.16 | 6220 | NA |
| JM38510/37004B2A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| JM38510/37004B2A.A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| M38510/37004B2A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SN74ALS30ADB | DB | SSOP | 14 | 80 | 530 | 10.5 | 4000 | 4.1 |
| SN74ALS30ADB.A | DB | SSOP | 14 | 80 | 530 | 10.5 | 4000 | 4.1 |
| SN74ALS30ADBE4 | DB | SSOP | 14 | 80 | 530 | 10.5 | 4000 | 4.1 |
| SN74ALS30AN | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74ALS30AN | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74ALS30AN.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74ALS30AN.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74AS30N | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74AS30N | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74AS30N.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74AS30N.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SNJ54ALS30AFK | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54ALS30AFK.A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54ALS30AW | W | CFP | 14 | 25 | 506.98 | 26.16 | 6220 | NA |
| SNJ54ALS30AW.A | W | CFP | 14 | 25 | 506.98 | 26.16 | 6220 | NA |

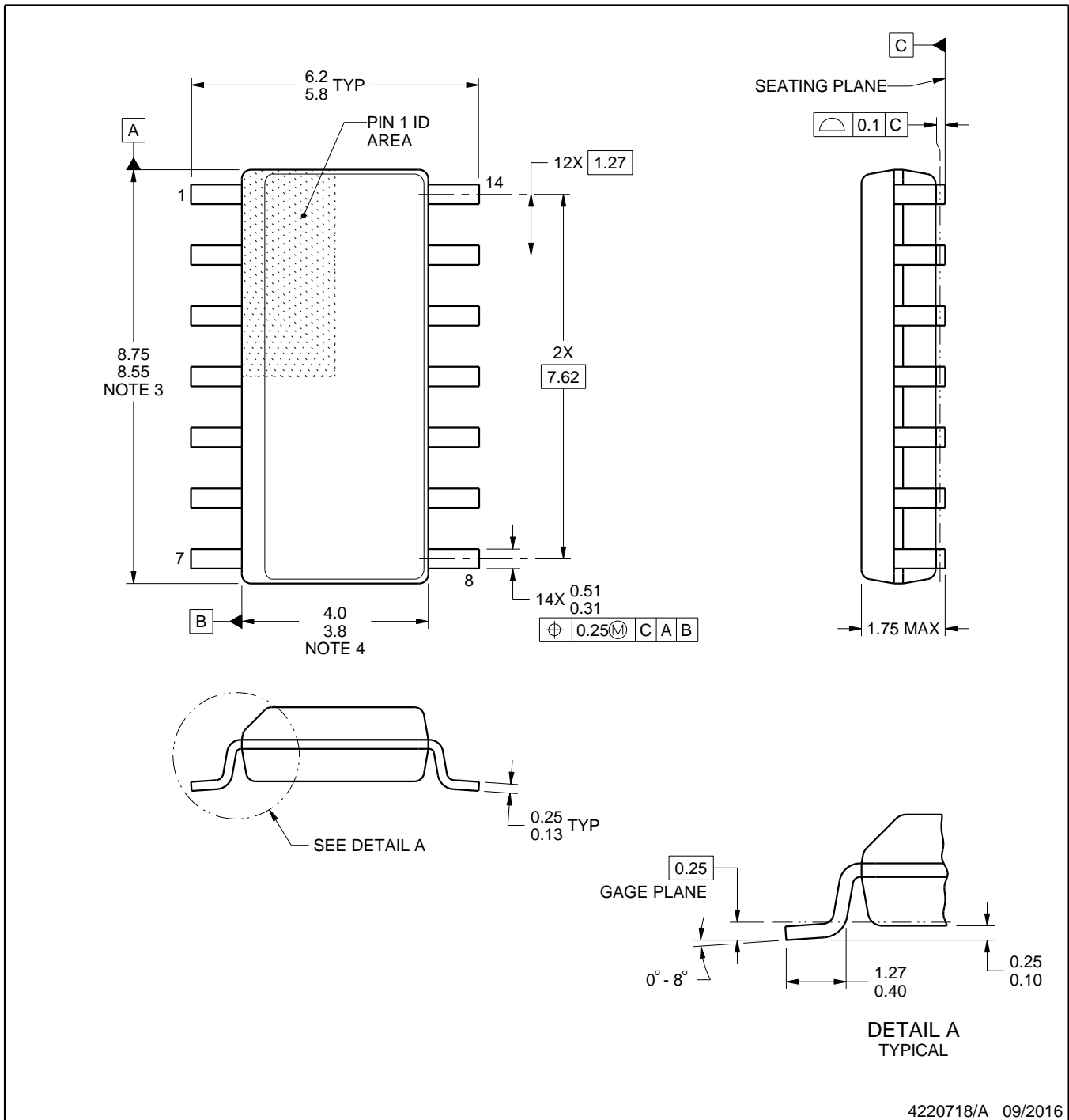
D0014A



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

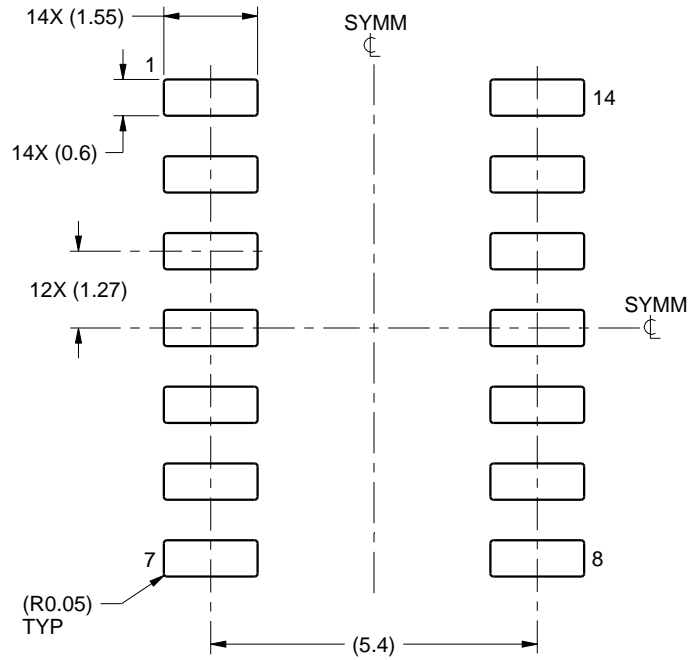
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

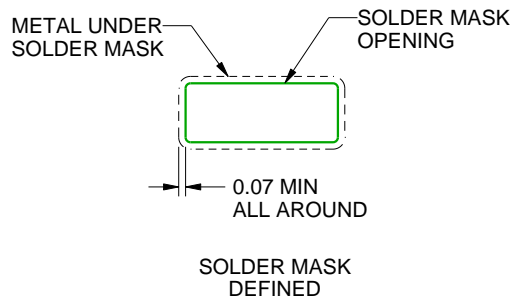
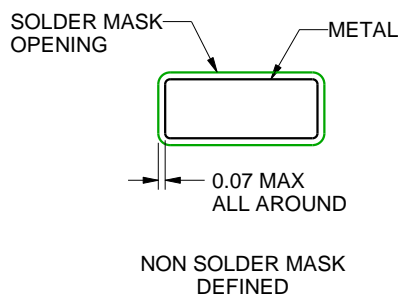
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

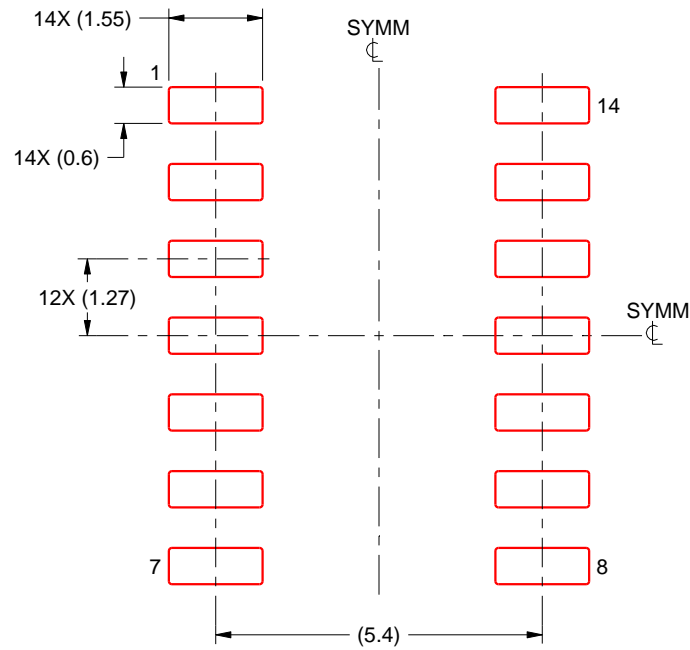
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

J 14

GENERIC PACKAGE VIEW
CDIP - 5.08 mm max height
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

J0014A



PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14

DB0014A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220762/A 05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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