SN55HVD75-EP 3.3-V Supply RS-485 With IEC ESD Protection

1 Features

- Bus I/O Protection
  - >±15-kV HBM Protection
  - >±12-kV IEC 61000-4-2 Contact Discharge
  - >±4-kV IEC 61000-4-4 Fast Transient Burst
- Extended Industrial Temperature Range –55°C to 125°C
- Large Receiver Hysteresis (80 mV) for Noise Rejection
- Low-Unit-Loading Allows Over 200 Connected Nodes
- Low-Power Consumption
  - Low-Standby Supply Current: < 2 µA
  - I_{CC} < 1-mA Quiescent During Operation
- 5-V Tolerant Logic Inputs Compatible With 3.3-V or 5-V Controllers
- Signaling Rate Options Optimized for: 250 kbps, 20 Mbps, 50 Mbps
- Available in a Small VSON Package
- **Supports Defense, Aerospace, and Medical Applications:**
  - Controlled Baseline
  - One Assembly/Test Site
  - One Fabrication Site
  - Available in Extended (–55°C to 125°C) Temperature Range
  - Extended Product Life Cycle
  - Extended Product-Change Notification
  - Product Traceability

2 Applications

- Factory Automation
- Telecommunications Infrastructure
- Motion Control

3 Description

These devices have robust 3.3-V drivers and receivers in a small package for demanding industrial applications. The bus pins are robust to ESD events with high levels of protection to human-body model and IEC contact discharge specifications.

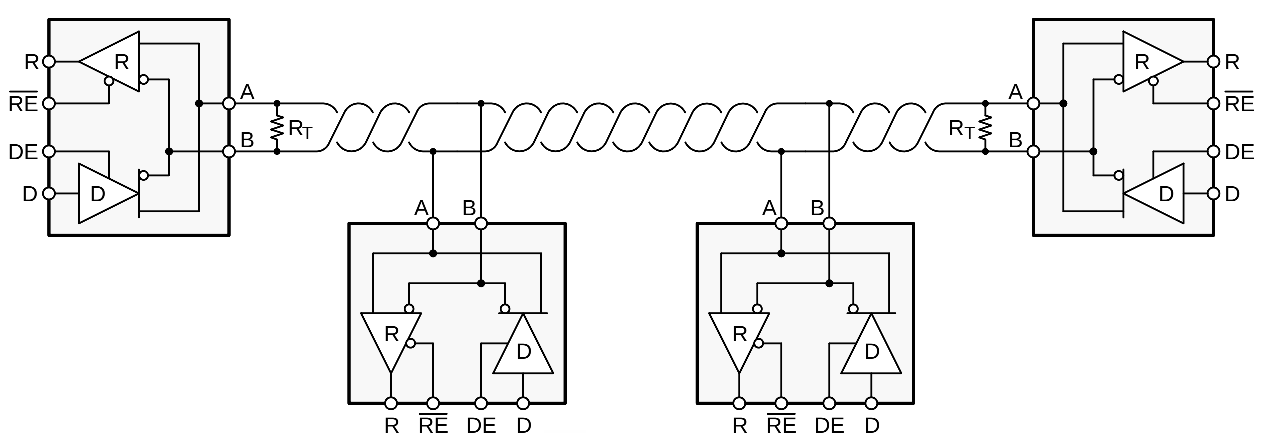
Each of these devices combines a differential driver and a differential receiver which operate from a single 3.3-V power supply. The driver differential outputs and the receiver differential inputs are connected internally to form a bus port suitable for half-duplex (two-wire bus) communication. These devices feature a wide common-mode voltage range making the devices suitable for multi-point applications over long cable runs. These devices are characterized from –55°C to 125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN55HVD75-EP	VSON (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Diagram



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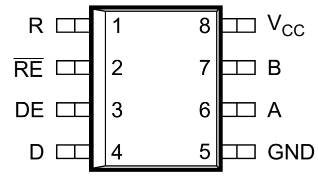
4 Revision History

Changes from Original (October 2015) to Revision A **Page**

- Deleted reference to RS-422 throughout the data sheet 1
- Deleted T_J and V_{CC} test conditions from $|V_{OD}|$, RL = 100 Ω 5
- Changed $|V_{OD}|$, RL = 100 Ω minimum from 2 V : to 1.8 V 5
- Added *Receiving Notification of Documentation Updates* section to *Device and Documentation Support* section 24

5 Pin Configuration and Functions

DRB Package
8-Pin VSON
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
A	6	Bus I/O	Driver output or receiver input (complementary to B).
B	7	Bus I/O	Driver output or receiver input (complementary to A).
D	4	Digital input	Driver data input.
DE	3	Digital input	Active-high driver enable.
GND	5	Reference potential	Local device ground.
R	1	Digital output	Receive data output .
$\overline{RE}$	2	Digital input	Active-low receiver enable.
V_{CC}	8	Supply	3-V to 3.6-V supply.

6 Specifications

6.1 Absolute Maximum Ratings

over recommended operating range (unless otherwise specified) [1]

	MIN	MAX	UNIT
Supply voltage, V_{CC}	–0.5	5.5	V
Voltage at A or B inputs	–13	16.5	V
Input voltage at any logic pin	–0.3	5.7	V
Voltage input, transient pulse, A and B, through 100 Ω	–100	100	V
Receiver output current	–24	24	mA
Junction temperature, T_J		170	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 [1]	All pins	±8000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 [2]	All pins	±1500	
		JEDEC standard 22, test method A115 (machine model)	All pins	±300	
		IEC 61000-4-2 ESD (air-gap discharge) [3]	Pins 5 to 7	±12000	
		IEC 61000-4-2 ESD (contact discharge)	Pins 5 to 7	±12000	
		IEC 61000-4-4 EFT (fast transient or burst)	Pins 5 to 7	±4000	
		IEC 60749-26 ESD HBM	Pins 5 to 7	±15000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) By inference from contact discharge results, see *Application and Implementation*.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_I	Input voltage at any bus terminal (separately or common mode)[1]	–7		12	V
V_{IH}	High-level input voltage (driver, driver enable, and receiver enable inputs)	2		V_{CC}	V
V_{IL}	Low-level input voltage (driver, driver enable, and receiver enable inputs)	0		0.8	V
V_{ID}	Differential input voltage	–12		12	V
I_O	Output current, driver	–60		60	mA
I_O	Output current, receiver	–8		8	mA
R_L	Differential load resistance	54	60		Ω
C_L	Differential load capacitance		50		pF
$1/t_{UI}$	Signaling rate			20	Mbps
T_A[2]	Operating free-air temperature (see *Thermal Information*)	–55		125	°C
T_J	Junction temperature	–55		150	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet.
(2) Operation is specified for internal (junction) temperatures up to 150°C. Self-heating due to internal power dissipation should be considered for each application. Maximum junction temperature is internally limited by the thermal shutdown (TSD) circuit which disables the driver outputs when the junction temperature reaches 170°C.

6.4 Thermal Information

THERMAL METRIC[1]		SN55HVD75-EP DRB (VSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	49.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	15.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over recommended operating range (unless otherwise specified)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\|V_{OD}\|$	Driver differential output voltage magnitude	R_L = 60 Ω, 375 Ω on each output to –7 V to 12 V	See Figure 6	1.5	2		V
		R_L = 54 Ω (RS-485)	See Figure 7	1.5	2		
		R_L = 100 Ω		1.8	2.5		
$\Delta\|V_{OD}\|$	Change in magnitude of driver differential output voltage	R_L = 54 Ω, C_L = 50 pF		–50	0	50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage	Center of two 27-Ω load resistors		1	$V_{CC}/2$	3	V
ΔV_{OC}	Change in differential driver output common-mode voltage			–50	0	50	mV
$V_{OC(PP)}$	Peak-to-peak driver common-mode output voltage				200		mV
C_{OD}	Differential output capacitance				15		pF
V_{IT+}	Positive-going receiver differential input voltage threshold			See (1)	–70	–20	mV
$V_{IT–}$	Negative-going receiver differential input voltage threshold			–200	–150	See (1)	mV
V_{HYS}	Receiver differential input voltage threshold hysteresis ($V_{IT+} – V_{IT–}$)			50	80		mV
V_{OH}	Receiver high-level output voltage	I_{OH} = –8 mA		2.4	V_{CC} – 0.3		V
V_{OL}	Receiver low-level output voltage	I_{OL} = 8 mA			0.2	0.4	V
I_I	Driver input, driver enable, and receiver enable input current			–2.75		2.75	µA
I_{OZ}	Receiver output high-impedance current	V_O = 0 V or V_{CC}, $\overline{RE}$ at V_{CC}		–1		1	µA
I_{OS}	Driver short-circuit output current			–165		165	mA
I_I	Bus input current (disabled driver)	V_{CC} = 3 V to 3.6 V or V_{CC} = 0 V DE at 0 V	V_I = 12 V		75	150	µA
			V_I = –7 V	–100	–40		
I_{CC}	Supply current (quiescent)	Driver and receiver enabled	DE = V_{CC}, $\overline{RE}$ = GND No load		750	950	µA
		Driver enabled, receiver disabled	DE = V_{CC}, $\overline{RE}$ = V_{CC} No load		300	500	
		Driver disabled, receiver enabled	DE = GND, $\overline{RE}$ = GND No load		600	800	
		Driver and receiver disabled	$\overline{DE}$ = GND, D = open $\overline{RE}$ = V_{CC}, No load		0.1	2	
	Supply current (dynamic)	See *Typical Characteristics*					

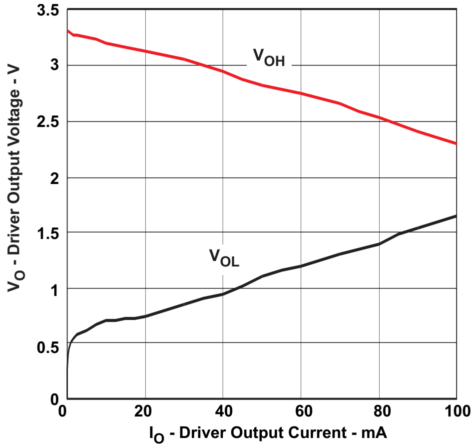
(1) Under any specific conditions, V_{IT+} is assured to be at least V_{HYS} higher than $V_{IT–}$.

6.6 Switching Characteristics: 20 Mbps Device, Bit Time ≥50 ns

over recommended operating conditions

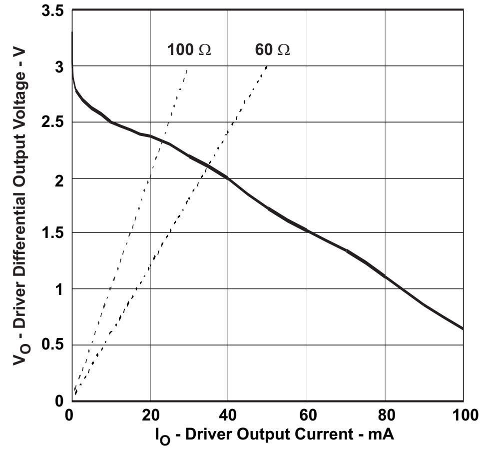
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DRIVER							
t_r, t_f	Driver differential output rise or fall time	R_L = 54 Ω C_L = 50 pF	See Figure 8	1	7	14	ns
t_{PHL}, t_{PLH}	Driver propagation delay			6	11	17	ns
$t_{SK(P)}$	Driver pulse skew, $\|t_{PHL} – t_{PLH}\|$				0	2	ns
t_{PHZ}, t_{PLZ}	Driver disable time		See Figure 9 and Figure 10		12	50	ns
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled			10	20	ns
		Receiver disabled			3	7	µs
RECEIVER							
t_r, t_f	Receiver output rise or fall time	C_L = 15 pF	See Figure 11		5	10	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time				60	70	ns
$t_{SK(P)}$	Receiver pulse skew, $\|t_{PHL} – t_{PLH}\|$				0	6	ns
t_{PLZ}, t_{PHZ}	Receiver disable time				15	30	ns
$t_{pZL(1)}$, $t_{PZH(1)}$, $t_{PZL(2)}$, $t_{PZH(2)}$	Receiver enable time	Driver enabled	See Figure 12		10	50	ns
		Driver disabled	See Figure 13		3	8	µs

6.7 Typical Characteristics



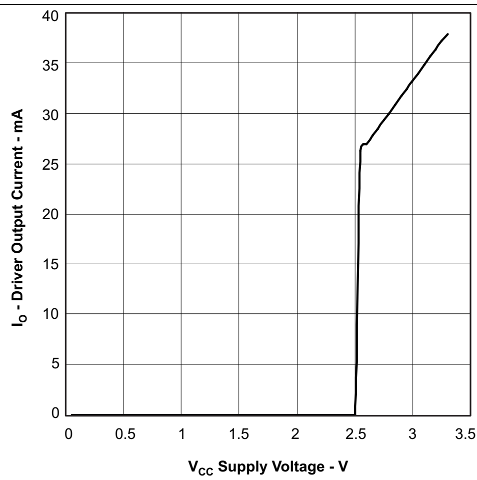
V_{CC} = 3.3 V DE = V_{CC} D = 0 V

Figure 1. Driver Output Voltage vs Driver Output Current



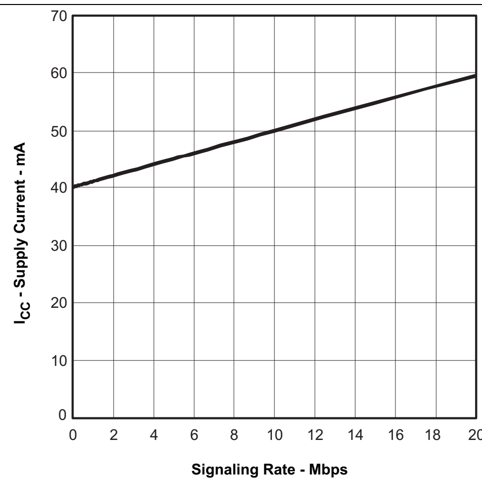
V_{CC} = 3.3 V DE = V_{CC} D = 0 V

Figure 2. Driver Differential Output Voltage vs Driver Output Current



T_A = 25°C R_L = 54 Ω D = V_{CC}
DE = V_{CC}

Figure 3. Driver Output Current vs Supply Voltage



R_L = 54 Ω

Figure 4. Supply Current vs Signal Rate

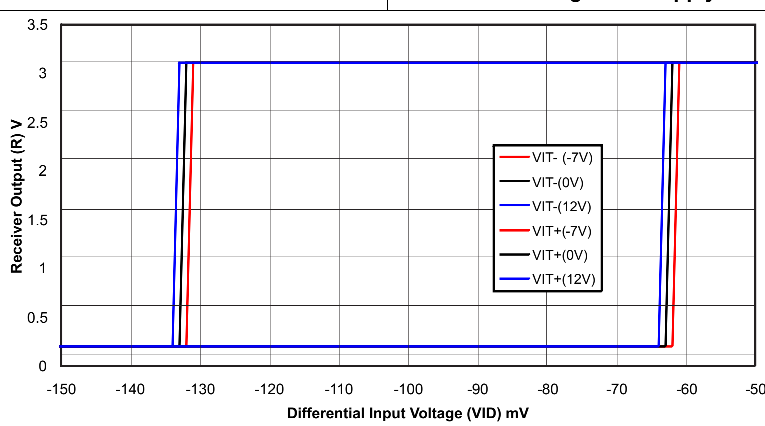


Figure 5. Receiver Output vs Input

7 Parameter Measurement Information

Input generator rate is 100 kbps, 50% duty cycle, rise or fall time is less than 6 ns, output impedance is 50 Ω.

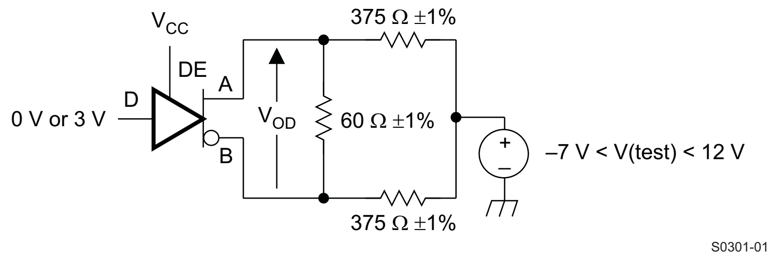


Figure 6. Measurement of Driver Differential Output Voltage With Common-Mode Load

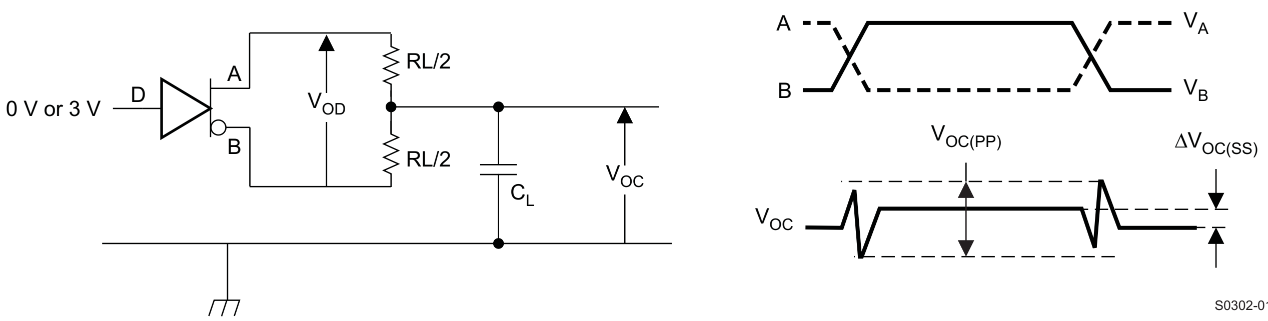


Figure 7. Measurement of Driver Differential and Common-Mode Output With RS-485 Load

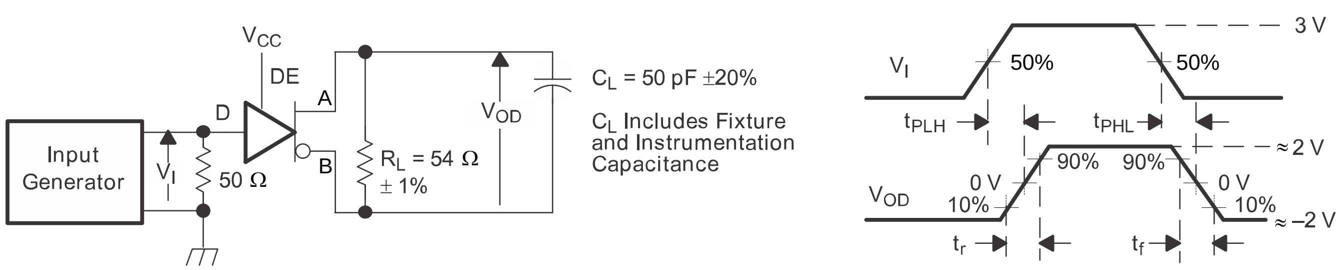


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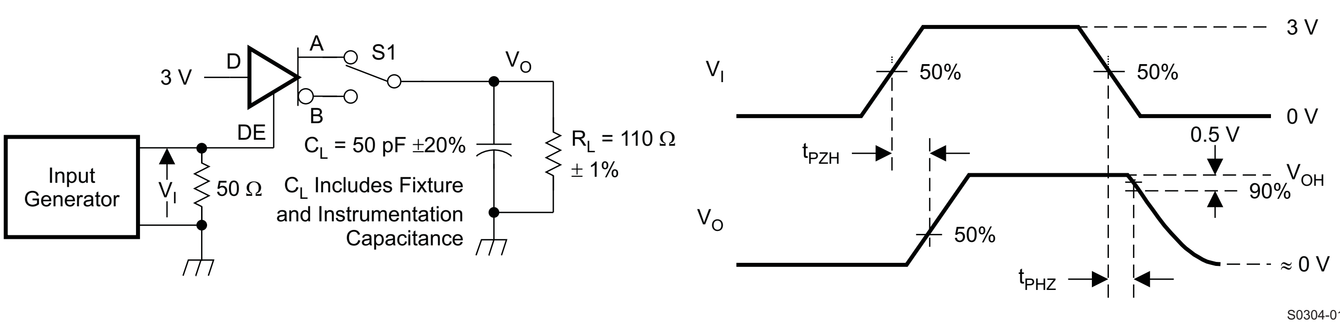
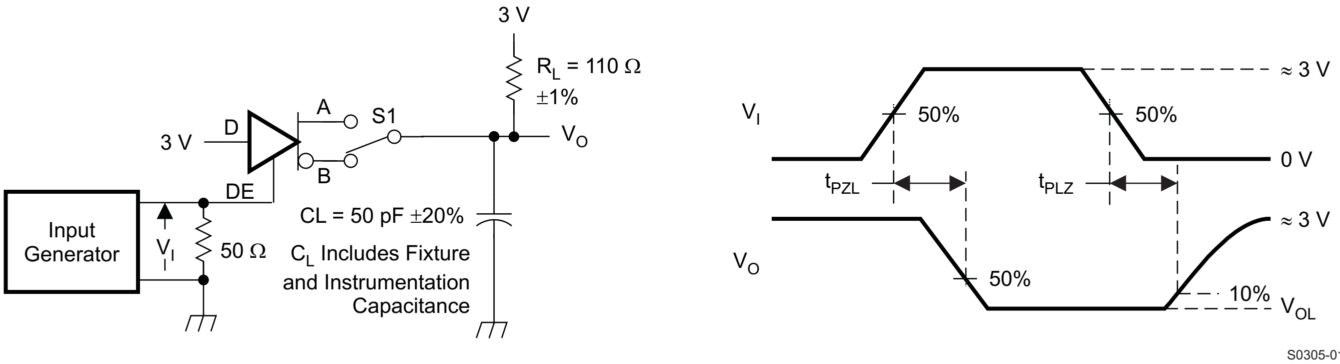
Figure 8. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays



D at 3 V to test non-inverting output, D at 0 V to test inverting output.

Figure 9. Measurement of Driver Enable and Disable Times With Active High Output and Pulldown Load

Parameter Measurement Information (continued)



D at 0 V to test non-inverting output, D at 3 V to test inverting output.

Figure 10. Measurement of Driver Enable and Disable Times With Active Low Output and Pullup Load

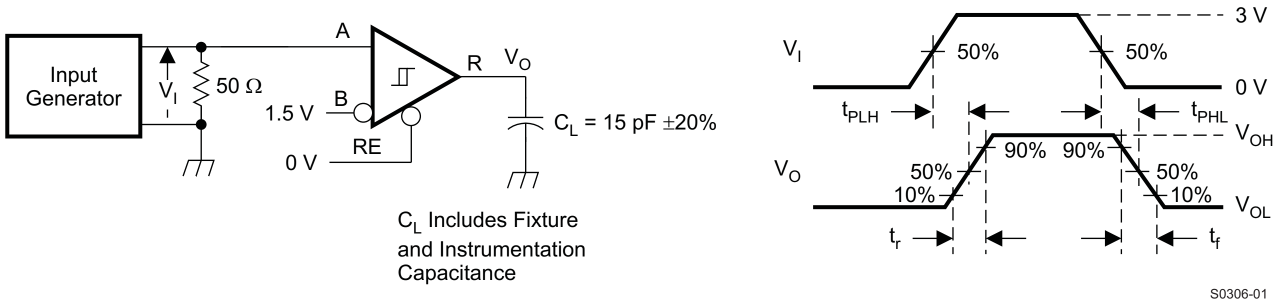


Figure 11. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

Parameter Measurement Information (continued)

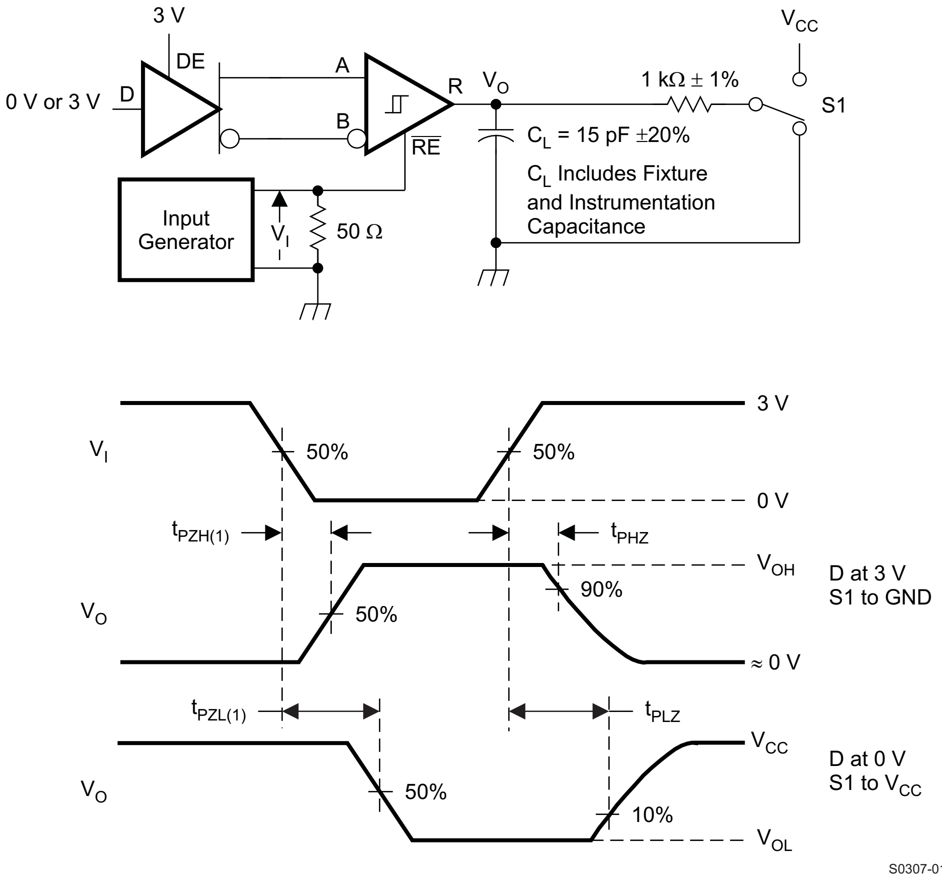


Figure 12. Measurement of Receiver Enable and Disable Times With Driver Enabled

Parameter Measurement Information (continued)

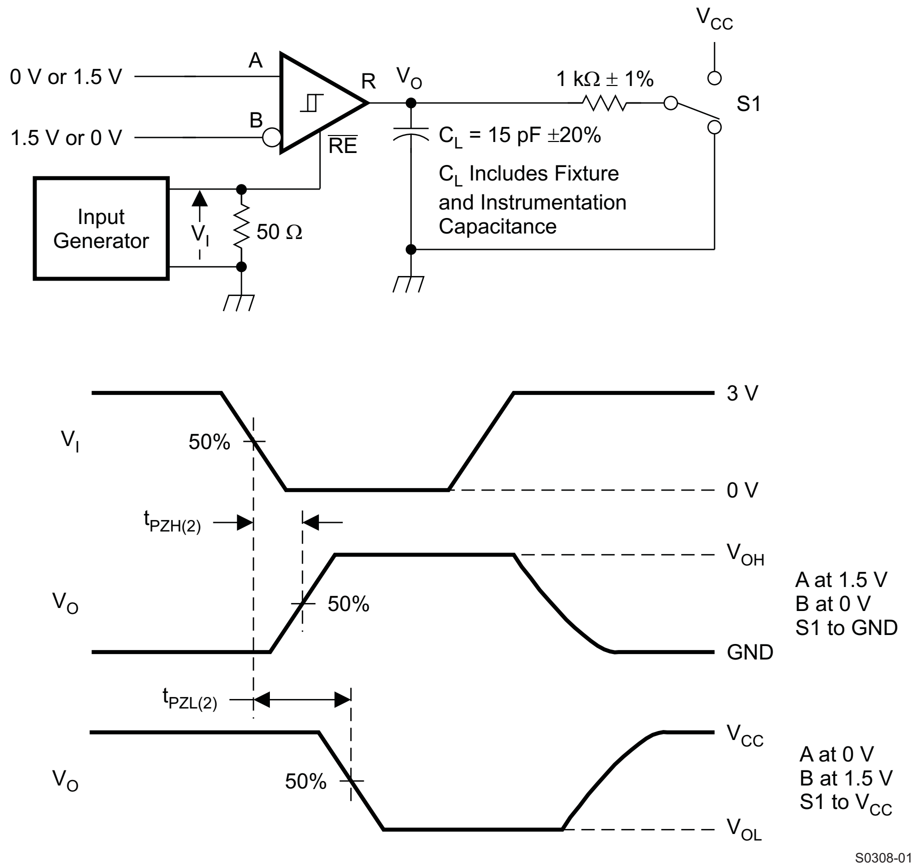


Figure 13. Measurement of Receiver Enable Times With Driver Disabled

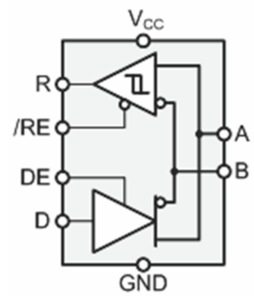
8 Detailed Description

8.1 Overview

The SN55HVD75-EP is a low-power, half-duplex RS-485 transceiver available in a speed grade suitable for data transmission up to 20 Mbps.

This device has active-high driver enables and active-low receiver enables. A standby current of less than 2 µA can be achieved by disabling both driver and receiver.

8.2 Functional Block Diagram



8.3 Feature Description

Internal ESD protection circuits protect the transceiver against electrostatic discharges (ESD) according to IEC 61000-4-2 of up to ±12 kV, and against electrical fast transients (EFT) according to IEC 61000-4-4 of up to ±4 kV.

The SN55HVD75-EP half-duplex family provides internal biasing of the receiver input thresholds in combination with large input threshold hysteresis. At a positive input threshold of V_{IT+} = –20 mV and an input hysteresis of V_{HYS} = 50 mV, the receiver output remains logic high under a bus-idle or bus-short condition even in the presence of 140-mV_{PP} differential noise without the need for external failsafe biasing resistors.

Device operation is specified over a wide ambient temperature range from –55°C to 125°C.

8.4 Device Functional Modes

When the driver enable pin, DE, is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case the differential output voltage defined as $V_{OD} = V_A – V_B$ is positive. When D is low, the output states reverse, B turns high, A becomes low, and V_{OD} is negative.

When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant. The DE pin has an internal pulldown resistor to ground; thus, when left open, the driver is disabled (high-impedance) by default. The D pin has an internal pullup resistor to V_{CC}; thus, when left open while the driver is enabled, output A turns high and B turns low.

Table 1. Driver Function Table

INPUT	ENABLE	OUTPUTS		DESCRIPTION
D	DE	A	B	
H	H	H	L	Actively drive bus high.
L	H	L	H	Actively drive bus low.
X	L	Z	Z	Driver disabled.
X	OPEN	Z	Z	Driver disabled by default.
OPEN	H	H	L	Actively drive bus high by default.

When the receiver enable pin, $\overline{RE}$, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A – V_B$ is positive and higher than the positive input threshold, V_{IT+}, the receiver output, R, turns high. When V_{ID} is negative and lower than the negative input threshold, $V_{IT–}$, the receiver output turns low. If V_{ID} is between V_{IT+} and $V_{IT–}$, the output is indeterminate.

When $\overline{RE}$ is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

Table 2. Receiver Function Table

DIFFERENTIAL INPUT $V_{ID} = V_A – V_B$	ENABLE $\overline{RE}$	OUTPUT R	DESCRIPTION
$V_{IT+} < V_{ID}$	L	H	Receive valid bus high.
$V_{IT–} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state.
$V_{ID} < V_{IT–}$	L	L	Receive valid bus low.
X	H	Z	Receiver disabled.
X	OPEN	Z	Receiver disabled by default.
Open-circuit bus	L	H	Failsafe high output.
Short-circuit bus	L	H	Failsafe high output.
Idle (terminated) bus	L	H	Failsafe high output.

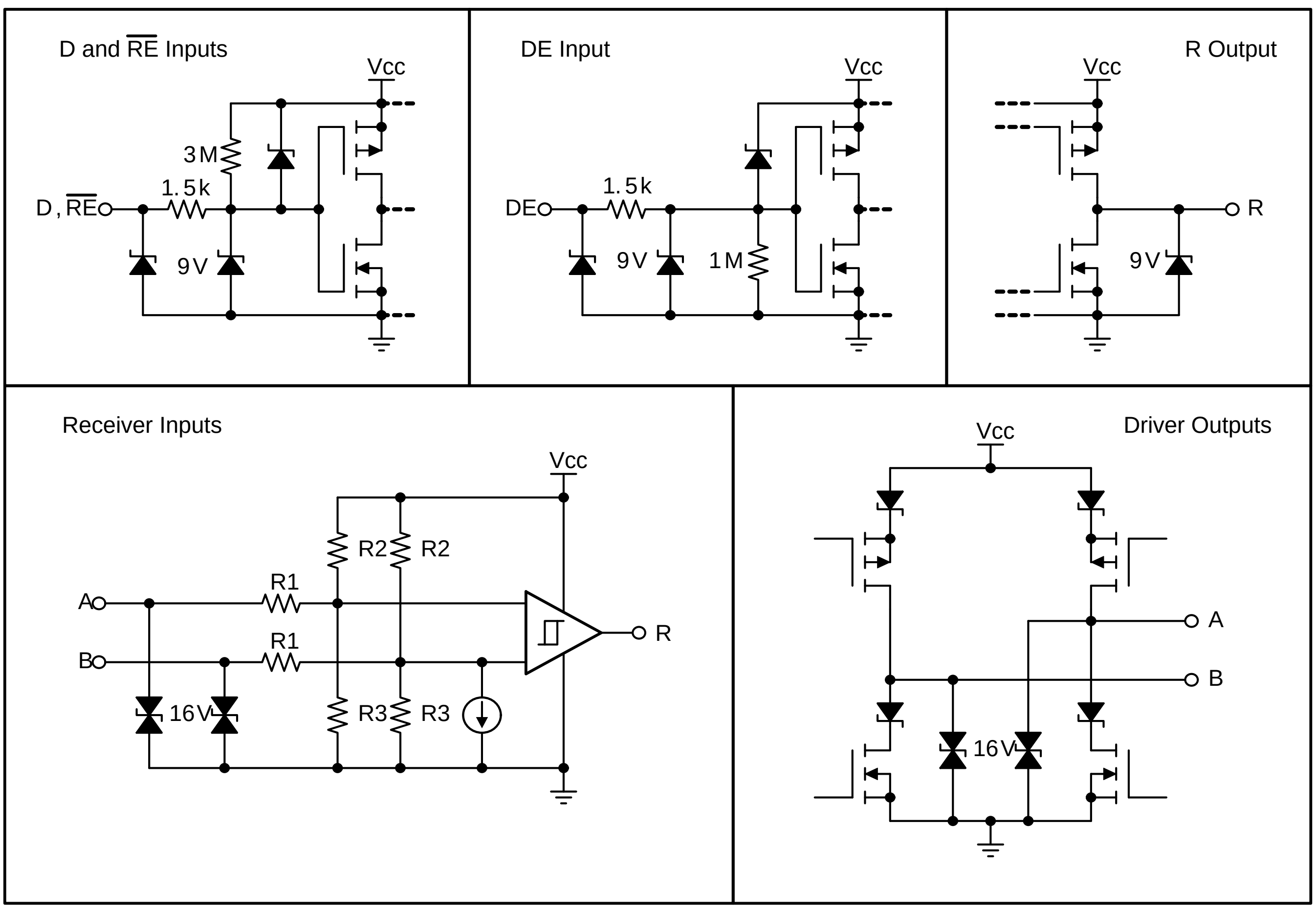


Figure 14. Equivalent Input and Output Circuit Diagrams

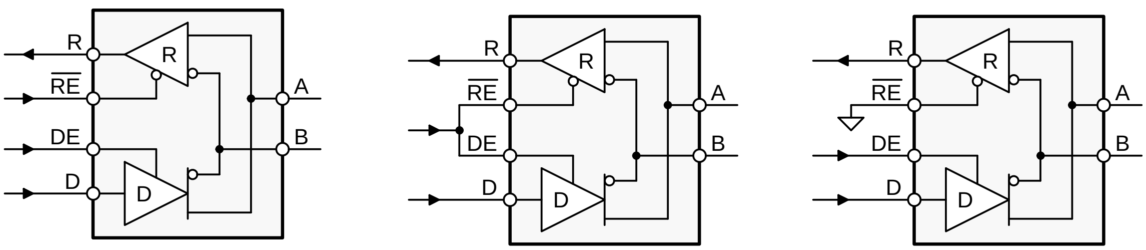
9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN55HVD75-EP is a half-duplex RS-485 transceiver commonly used for asynchronous data transmission. The driver and receiver enable pins allow for the configuration of different operating modes.



a) Independent driver and receiver enable signals

b) Combined enable signals for use as directional control pin

c) Receiver always on

Figure 15. Transceiver Configurations

Using independent enable lines provides the most flexible control as it allows for the driver and the receiver to be turned on and off individually. While this configuration requires two control lines, it allows for selective listening into the bus traffic, whether the driver is transmitting data or not.

Combining the enable signals simplifies the interface to the controller by forming a single direction-control signal. In this configuration, the transceiver operates as a driver when the direction-control line is high, and as a receiver when the direction-control line is low.

Additionally, only one line is required when connecting the receiver-enable input to ground and controlling only the driver-enable input. In this configuration, a node not only receives the data from the bus, but also the data it sends and can verify that the correct data have been transmitted.

9.2 Typical Application

An RS-485 bus consists of multiple transceivers connected in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T, whose value matches the characteristic impedance, Z_0, of the cable. This method, known as parallel termination, allows for relatively high data rates over long cable lengths.

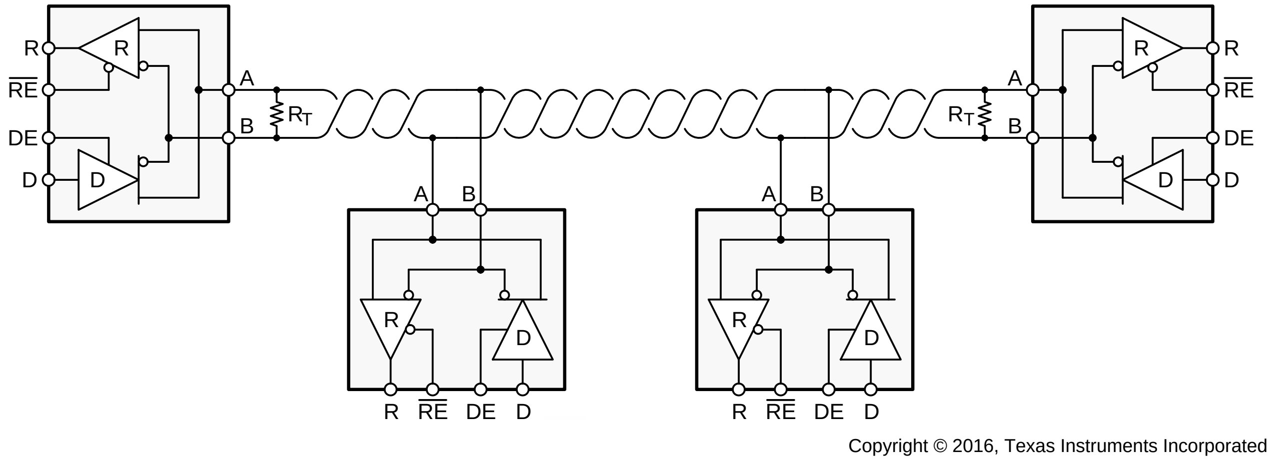


Figure 16. Typical RS-485 Network With SN55HVD75-EP Transceivers

Common cables used are unshielded twisted pair (UTP), such as low-cost CAT-5 cable with Z_0 = 100 Ω, and RS-485 cable with Z_0 = 120 Ω. Typical cable sizes are AWG 22 and AWG 24.

The maximum bus length is typically given as 4000 ft or 1200 m, and represents the length of an AWG 24 cable whose cable resistance approaches the value of the termination resistance, thus reducing the bus signal by half or 6 dB. Actual maximum usable cable length depends on the signaling rate, cable characteristics, and environmental conditions.

9.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

9.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and bus length, meaning the higher the data rate, the shorter the cable length; and conversely, the lower the data rate, the longer the cable may be without introducing data errors. While most RS-485 systems use data rates between 10 kbps and 100 kbps, some applications require data rates up to 250 kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

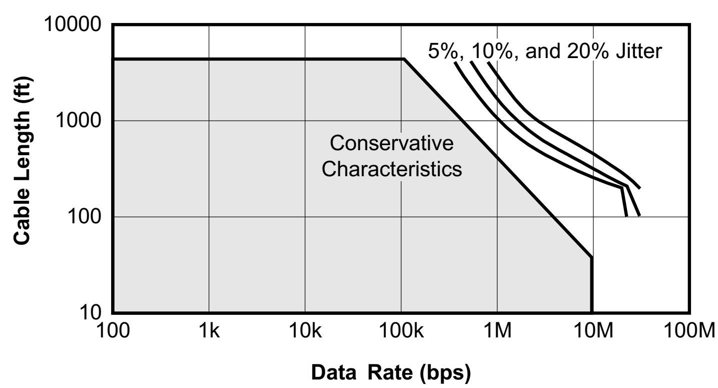


Figure 17. Cable Length vs Data Rate Characteristic

Typical Application (continued)

9.2.1.2 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a non-terminated piece of bus line which can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in Equation 1.

$$L_{stub} \le 0.1 \times t_r \times v \times c$$

where:

- t_r is the 10/90 rise time of the driver
- c is the speed of light (3×10^8 m/s)
- v is the signal velocity of the cable or trace as a factor of c (1)

Per Equation 1, Table 3 shows the maximum cable-stub lengths for the minimum driver output rise times of the SN55HVD75-EP half-duplex transceiver for a signal velocity of 78%.

Table 3. Maximum Stub Length

DEVICE	MINIMUM DRIVER OUTPUT RISE TIME (ns)	MAXIMUM STUB LENGTH (m)	MAXIMUM STUB LENGTH (ft)
SN55HVD75-EP	2	0.05	0.16

9.2.1.3 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to drive 32 unit loads (UL), where 1 unit load represents a receiver input current of 1 mA at 12 V, or a load impedance of approximately 12 kΩ. Because the SN55HVD75-EP has a receiver input current of 150 µA at 12 V, they are 3/20 UL transceivers, and no more than 213 transceivers should be connected to the bus.

9.2.1.4 Receiver Failsafe

The differential receiver is failsafe to invalid bus states caused by:

- Open bus conditions such as a disconnected connector
- Shorted bus conditions such as cable damage shorting the twisted-pair together, or
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver will output a failsafe logic high so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds such that the input-indeterminate range does not include 0-V differential. To comply with RS-485 standards, the receiver output must output a high when the differential input V_{ID} is more positive than 200 mV, and must output a low when V_{ID} is more negative than –200 mV. The receiver parameters which determine the failsafe performance are V_{IT+}, $V_{IT–}$, and V_{HYS} (the separation between V_{IT+} and $V_{IT–}$). As shown in *Electrical Characteristics*, differential signals more negative than –200 mV will always cause a low receiver output, and differential signals more positive than 200 mV will always cause a high receiver output.

When the differential input signal is close to zero, it is still above the maximum V_{IT+} threshold of –20 mV, and the receiver output will be high. Only when the differential input is more than V_{HYS} below V_{IT+} will the receiver output transition to a low state. Therefore, the noise immunity of the receiver inputs during a bus fault condition includes the receiver hysteresis value, V_{HYS}, as well as the value of V_{IT+}.

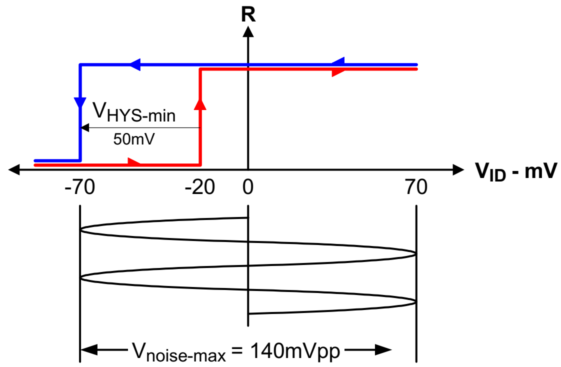


Figure 18. Noise Immunity

9.2.1.5 Transient Protection

The bus pins of the SN55HVD75-EP transceiver family possess on-chip ESD protection against ±15-kV human body model (HBM) and ±12-kV IEC 61000-4-2 contact discharge. The IEC-ESD test is far more severe than the HBM-ESD test. The 50% higher charge capacitance, C_S, and 78% lower discharge resistance, R_D, of the IEC-model produce significantly higher discharge currents than the HBM-model.

As stated in the IEC 61000-4-2 standard, contact discharge is the preferred test method; although IEC air-gap testing is less repeatable than contact testing, air discharge protection levels are inferred from the contact discharge test results.

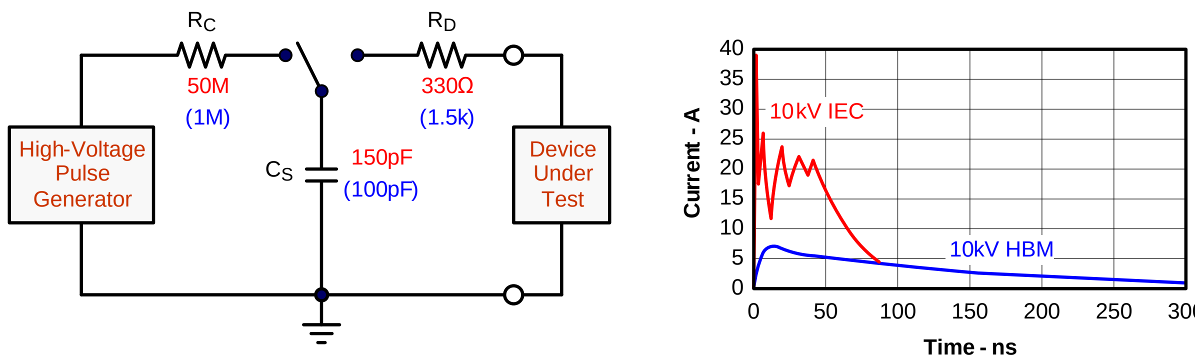


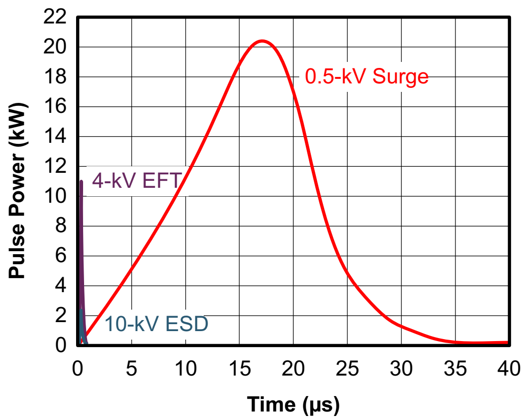
Figure 19. HBM and IEC-ESD Models and Currents in Comparison (HBM Values in Parenthesis)

The on-chip implementation of IEC ESD protection significantly increases the robustness of equipment. Common discharge events occur due to human contact with connectors and cables. Designers may choose to implement protection against longer duration transients, typically referred to as surge transients.

EFTs are generally caused by relay-contact bounce or the interruption of inductive loads. Surge transients often result from lightning strikes (direct strike or an indirect strike which induce voltages and currents), or the switching of power systems, including load changes and short circuit switching. These transients are often encountered in industrial environments, such as factory automation and power-grid systems.

Figure 20 compares the pulse-power of the EFT and surge transients with the power caused by an IEC ESD transient. The left-hand diagram shows the relative pulse-power for a 0.5-kV surge transient and 4-kV EFT transient, both of which dwarf the 10-kV ESD transient visible in the lower-left corner. 500-V surge transients are representative of events that may occur in factory environments in industrial and process automation.

The right-hand diagram shows the pulse-power of a 6-kV surge transient, relative to the same 0.5-kV surge transient. 6-kV surge transients are most likely to occur in power generation and power-grid systems.



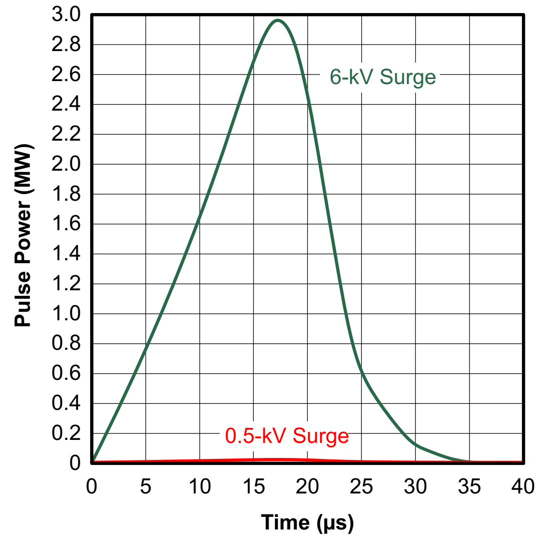


Figure 20. Power Comparison of ESD, EFT, and Surge Transients

In the case of surge transients, high-energy content is characterized by long pulse duration and slow decaying pulse power. The electrical energy of a transient that is dumped into the internal protection cells of a transceiver is converted into thermal energy which heats and destroys the protection cells, thus destroying the transceiver. Figure 21 shows the large differences in transient energies for single ESD, EFT, and surge transients, as well as for an EFT pulse train, commonly applied during compliance testing.

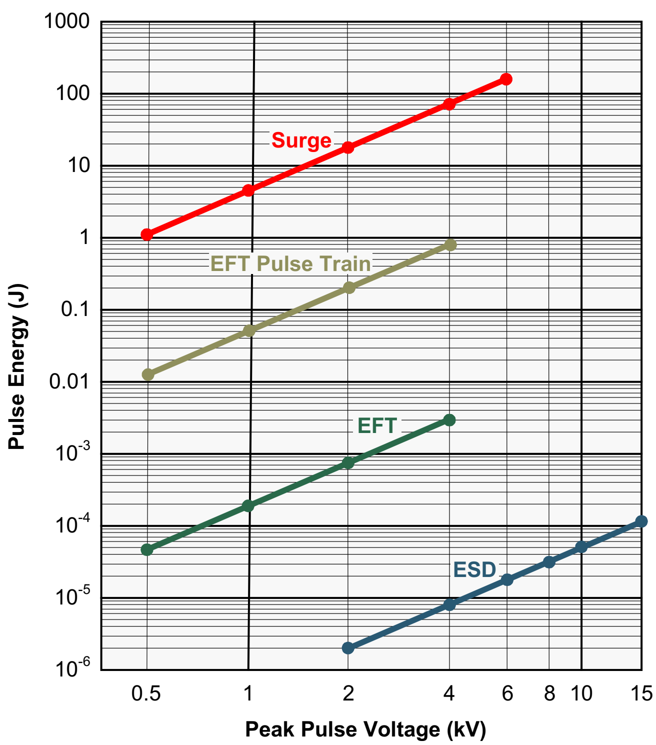


Figure 21. Comparison of Transient Energies

9.2.2 Detailed Design Procedure

9.2.2.1 External Transient Protection

To protect bus nodes against high-energy transients, the implementation of external transient protection devices is necessary. Figure 22 suggests two circuits that provide protection against light and heavy surge transients, in addition to ESD and EFT transients. Table 4 presents the associated bill of materials.

Table 4. Bill of Materials

DEVICE	FUNCTION	ORDER NUMBER	MANUFACTURER
XCVR	3.3-V, 250-kbps RS-485 transceiver	SN55HVD75DRBREP	TI
R1, R2	10-Ω, pulse-proof thick-film resistor	CRCW060310RJNEAHP	Vishay
TVS	Bidirectional 400-W transient suppressor	CDSOT23-SM712	Bourns
TBU1, TBU2	Bidirectional surge suppressor	TBU-CA-065-200-WH	Bourns
MOV1, MOV2	200-mA Transient blocking unit, 200-V, metal-oxide varistor	MOV-10D201K	Bourns

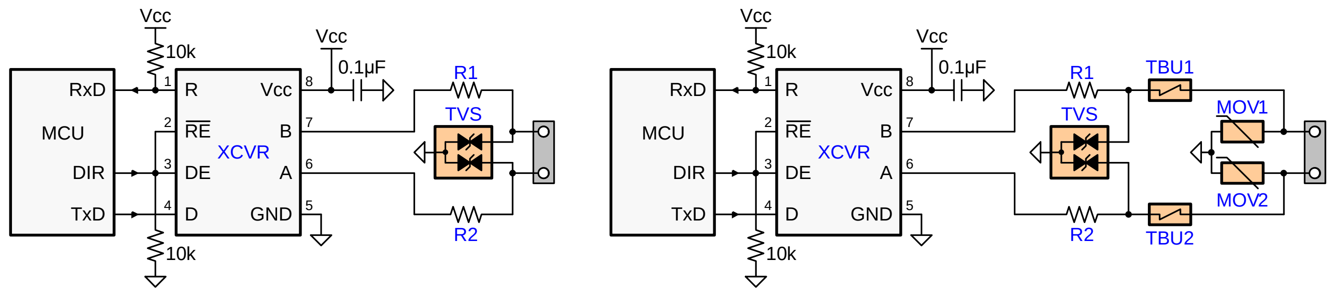


Figure 22. Transient Protections against ESD, EFT, and Surge Transients

The left-hand circuit provides surge protection of ≥500-V surge transients, while the right-hand circuit can withstand surge transients of up to 5 kV.

9.2.2.2 Isolated Bus Node Design

Many RS-485 networks use isolated bus nodes to prevent the creation of unintended ground loops and their disruptive impact on signal integrity. An isolated bus node typically includes a microcontroller that connects to the bus transceiver via a multi-channel, digital isolator (Figure 23).

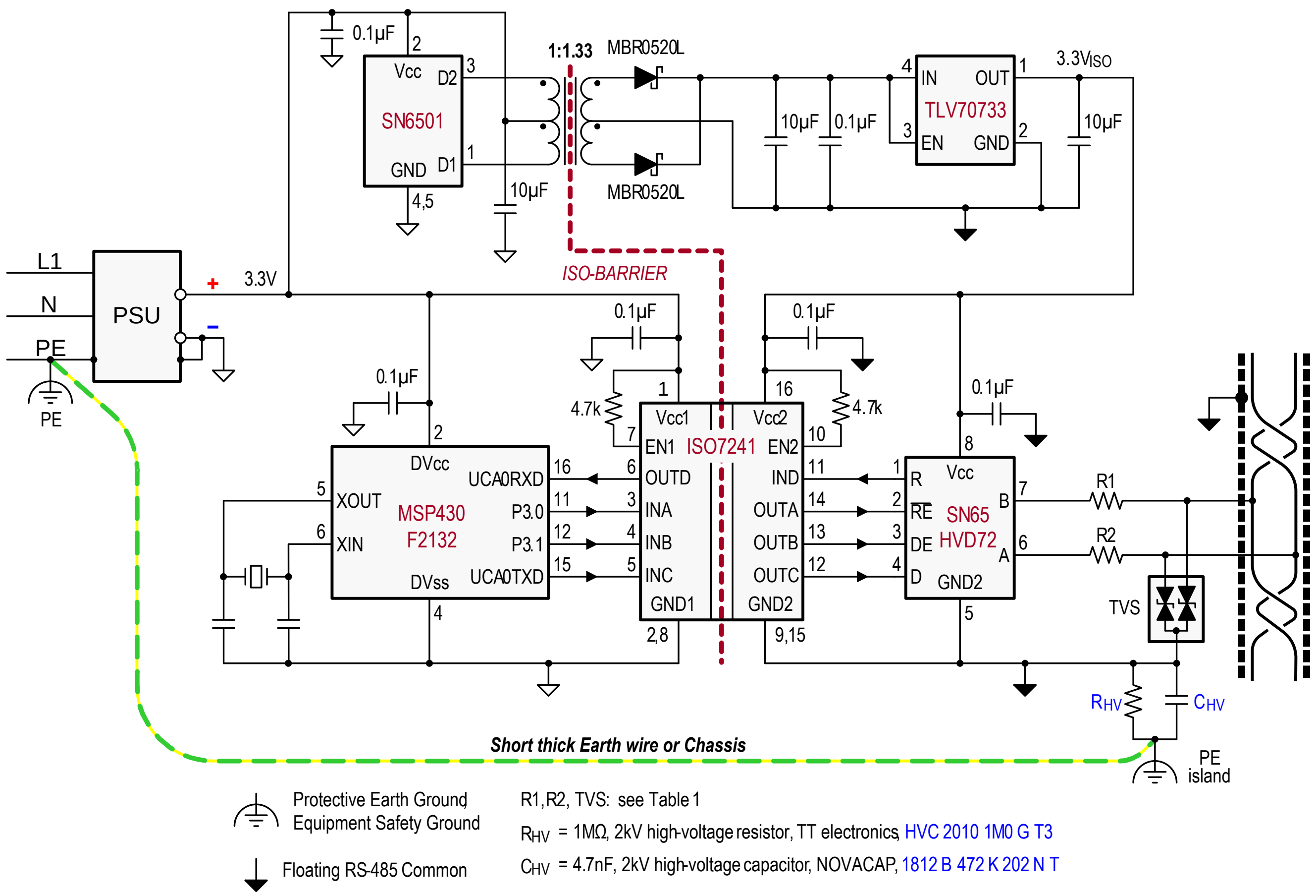


Figure 23. Isolated Bus Node with Transient Protection

Power isolation is accomplished using the push-pull transformer driver SN6501 and a low-cost LDO, TLV70733.

Signal isolation uses the quadruple digital isolator ISO7241. Notice that both enable inputs, EN_1 and EN_2, are pulled up via 4.7-kΩ resistors to limit their input currents during transient events.

While the transient protection is similar to the one in Figure 22 (left circuit), an additional high-voltage capacitor is used to divert transient energy from the floating RS-485 common further toward Protective Earth (PE) ground. This is necessary as noise transients on the bus are usually referred to Earth potential.

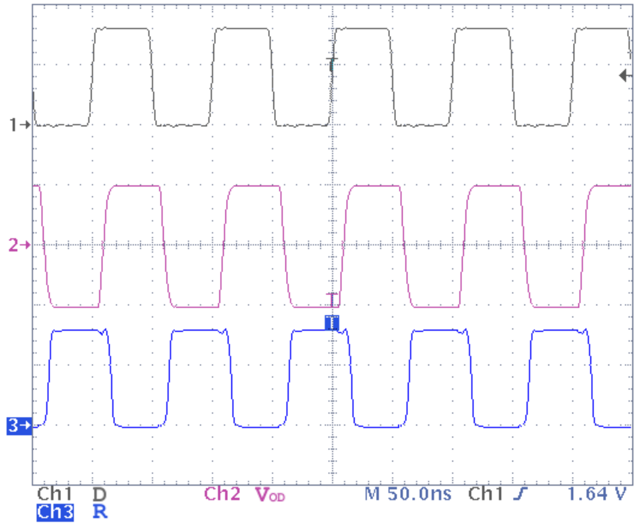
R_{HV} refers to a high voltage resistor, and in some applications even a varistor. This resistance is applied to prevent charging of the floating ground to dangerous potentials during normal operation.

Occasionally varistors are used instead of resistors to rapidly discharge C_{HV}, if it is expected that fast transients might charge C_{HV} to high-potentials.

Note that the PE island represents a copper island on the PCB for the provision of a short, thick Earth wire connecting this island to PE ground at the entrance of the power supply unit (PSU).

In equipment designs using a chassis, the PE connection is usually provided through the chassis itself. Typically the PE conductor is tied to the chassis at one end while the high-voltage components, C_{HV} and R_{HV}, are connecting to the chassis at the other end.

9.2.3 Application Curve



R_L = 60 Ω

Figure 24. 20 Mbps

10 Power Supply Recommendations

To assure reliable operation at all data rates and supply voltages, each supply should be buffered with a 100-nF ceramic capacitor located as close to the supply pins as possible. The TPS76333 is a linear voltage regulator suitable for the 3.3-V supply.

See *SN6501 Transformer Driver for Isolated Power Supplies* (SLLSEA0) for isolated power supply designs.

11 Layout

11.1 Layout Guidelines

On-chip IEC ESD protection is sufficient for laboratory and portable equipment but often insufficient for EFT and surge transients occurring in industrial environments. Therefore, robust and reliable bus node design requires the use of external transient protection devices.

Because ESD and EFT transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high-frequency layout techniques must be applied during PCB design.

For a successful PCB design, start with the design of the protection circuit in mind.

- Place the protection circuitry close to the bus connector to prevent noise transients from entering the board.
- Use V_{CC} and ground planes to provide low-inductance. Note that high-frequency currents follow the path of least inductance and not the path of least impedance.
- Design the protection components into the direction of the signal path. Do not force the transients currents to divert from the signal path to reach the protection device.
- Apply 100-nF to 220-nF bypass capacitors as close as possible to the V_{CC} pins of transceiver, UART, and controller ICs on the board.
- Use at least two vias for V_{CC} and ground connections of bypass capacitors and protection devices to minimize effective via-inductance.
- Use 1-kΩ to 10-kΩ pullup or pulldown resistors for enable lines to limit noise currents in these lines during transient events.
- Insert pulse-proof series resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus pins. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
- While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to 200 mA.

11.2 Layout Example

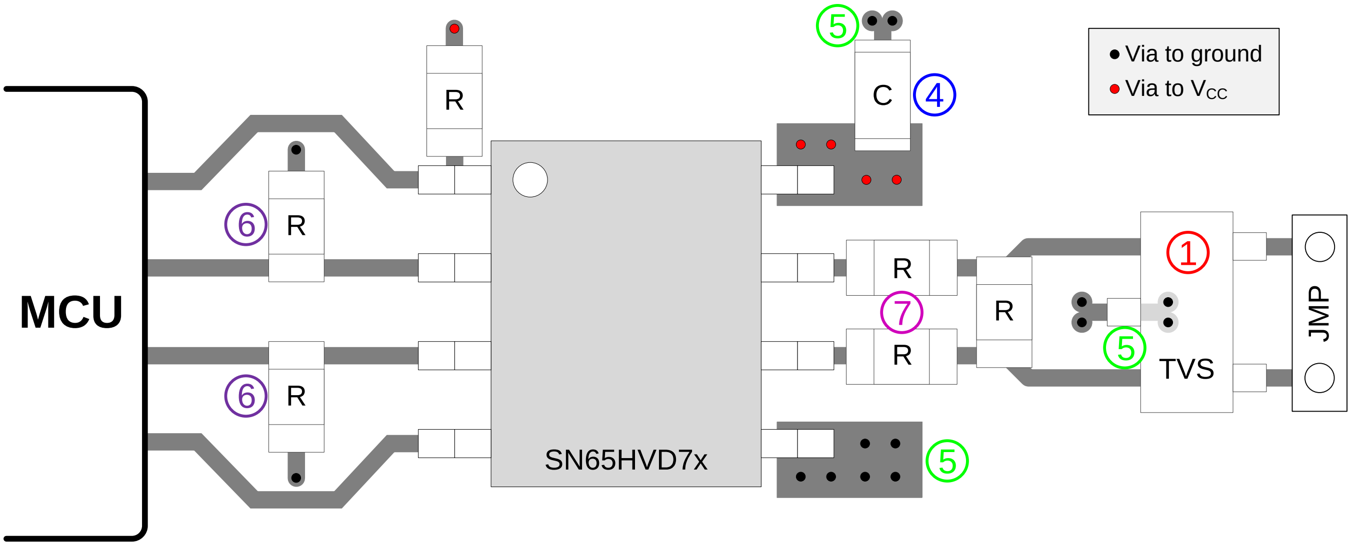


Figure 25. SN55HVD75-EP Half-Duplex Layout Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN55HVD75DRBREP	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	HVD75M
SN55HVD75DRBREP.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	HVD75M
SN55HVD75DRBREP.B	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	HVD75M
V62/15608-01XE	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	HVD75M

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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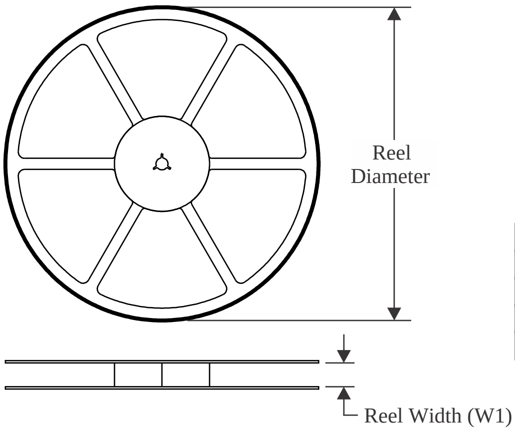
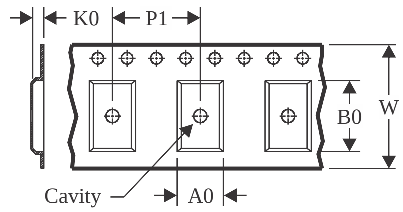
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

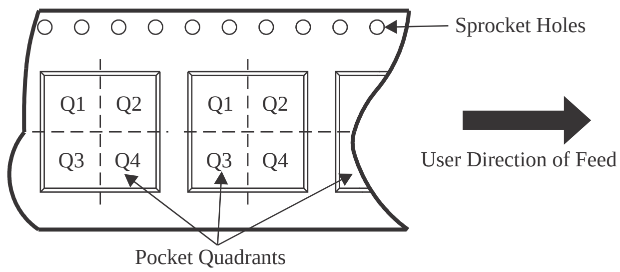


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

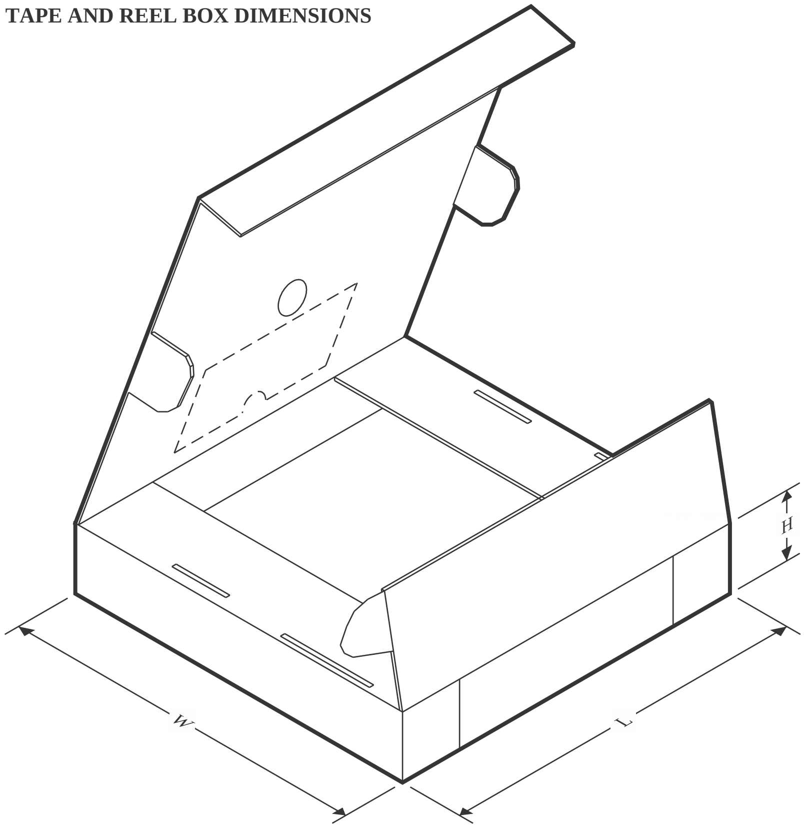
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN55HVD75DRBREP	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

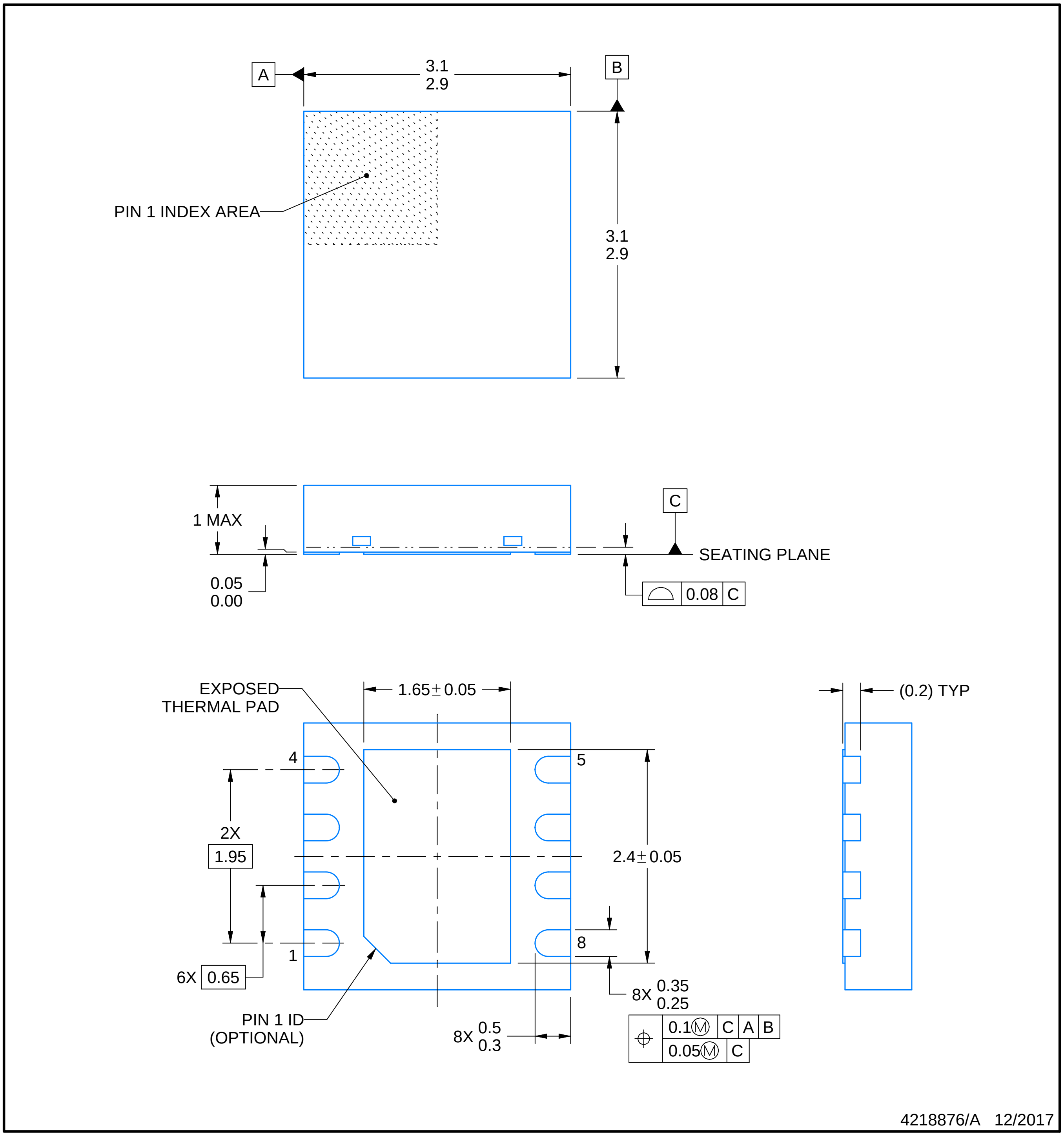
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

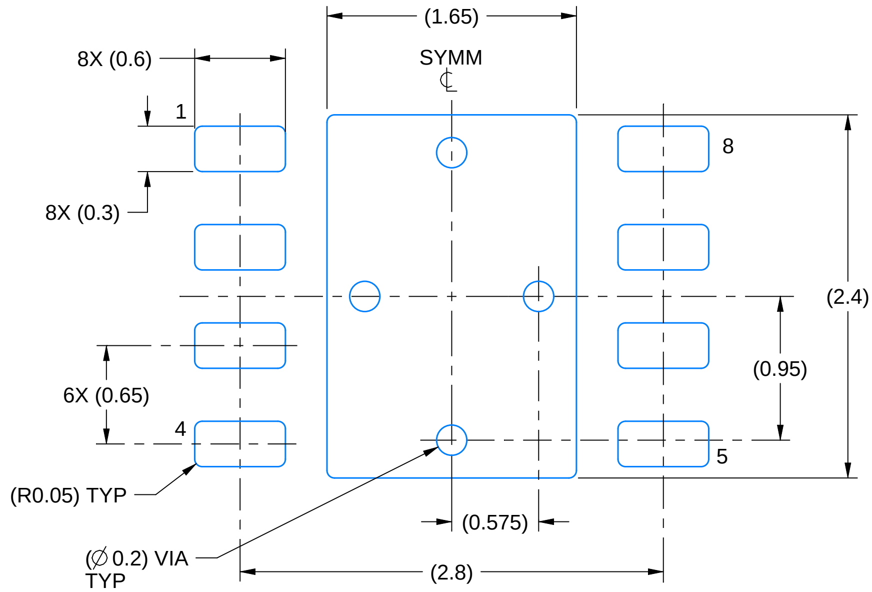
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN55HVD75DRBREP	SON	DRB	8	3000	346.0	346.0	33.0

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

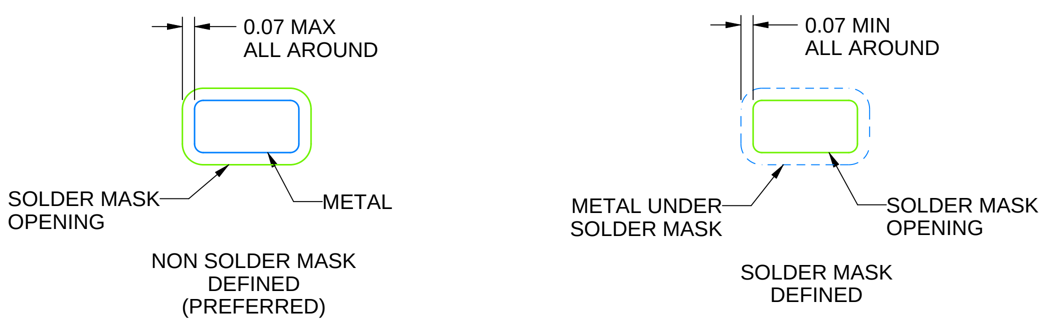


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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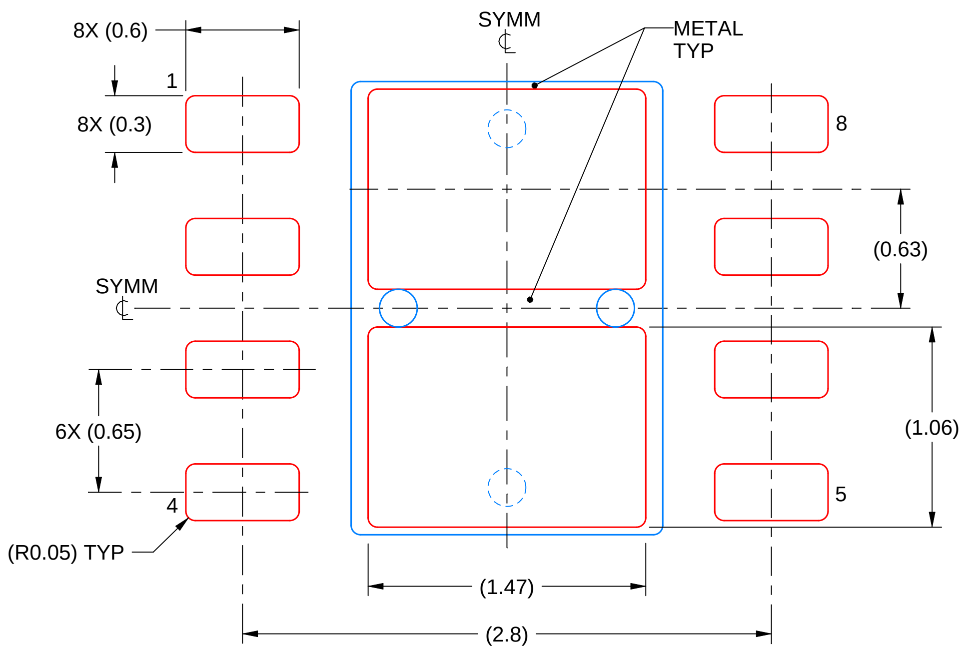
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.