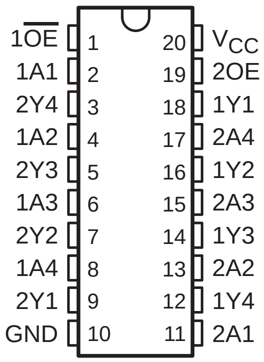
SN54ABT2241, SN74ABT2241
OCTAL BUFFERS AND LINE/MOS DRIVERS
WITH 3-STATE OUTPUTS

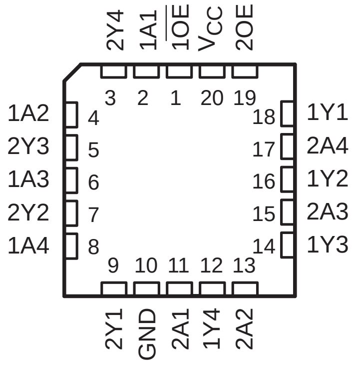
SCBS233B – JANUARY 1991 – REVISED JANUARY 1997

- **Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Plastic (N) and Ceramic (J) DIPs**

SN54ABT2241 . . . J PACKAGE
SN74ABT2241 . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54ABT2241 . . . FK PACKAGE
(TOP VIEW)



description

These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Together with the SN54ABT2240, SN74ABT2240A and ’ABT2244A, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical active-low output-enable ($\overline{\text{OE}}$) inputs, and complementary OE and $\overline{\text{OE}}$ inputs. These devices feature high fan-out and improved fan-in.

The outputs, which are designed to sink up to 12 mA, include equivalent 25-Ω series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

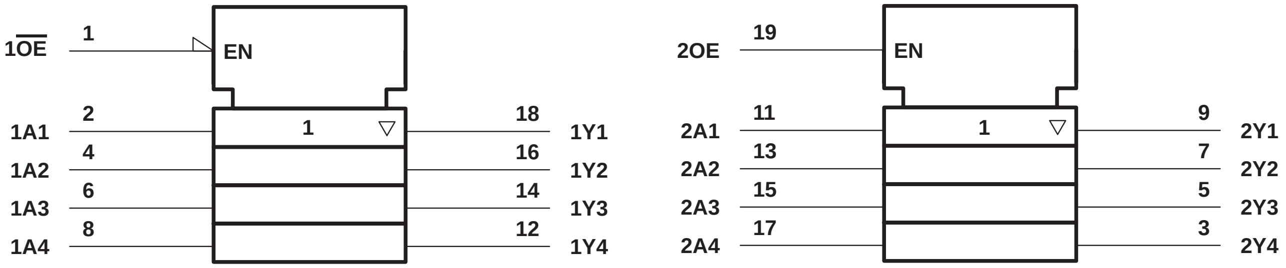
The SN54ABT2241 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT2241 is characterized for operation from –40°C to 85°C.

FUNCTION TABLES

INPUTS		OUTPUT
$1\overline{OE}$	1A	1Y
L	H	H
L	L	L
H	X	Z

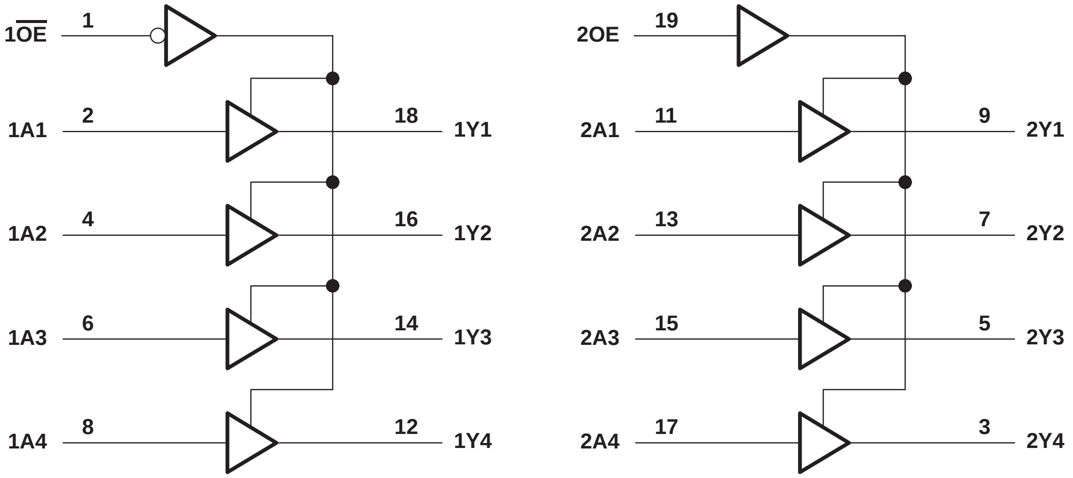
INPUTS		OUTPUT
2OE	2A	2Y
H	H	H
H	L	L
L	X	Z

logic symbol†

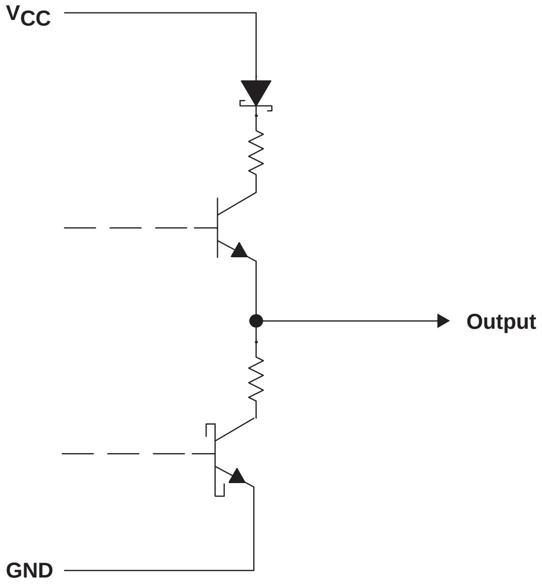


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic of Y outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		–0.5 V to 7 V
Input voltage range, V_I (see Note 1)		–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O		–0.5 V to 5.5 V
Current into any output in the low state, I_O		30 mA
Input clamp current, I_{IK} ($V_I < 0$)		–18 mA
Output clamp current, I_{OK} ($V_O < 0$)		–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DB package	115°C/W
	DW package	97°C/W
	N package	67°C/W
	PW package	128°C/W
Storage temperature range, T_{stg}		–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions (see Note 3)

			SN54ABT2241		SN74ABT2241		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			–24		–32	mA
I_{OL}	Low-level output current			12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		$T_A = 25°C$			SN54ABT2241		SN74ABT2241		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}		$V_{CC} = 4.5$ V,	$I_I = –18$ mA			–1.2		–1.2		–1.2	V
V_{OH}		$V_{CC} = 4.5$ V,	$I_{OH} = –3$ mA	2.5			2.5		2.5		V
		$V_{CC} = 5$ V,	$I_{OH} = –3$ mA	3			3		3		
		$V_{CC} = 4.5$ V	$I_{OH} = –24$ mA	2			2				
			$I_{OH} = –32$ mA	2*					2		
V_{OL}		$V_{CC} = 4.5$ V,	$I_{OL} = 12$ mA			0.8		0.8		0.8	V
V_{hys}					100						mV
I_I		$V_{CC} = 5.5$ V,	$V_I = V_{CC}$ or GND			±1		±1		±1	µA
I_{OZH}		$V_{CC} = 5.5$ V,	$V_O = 2.7$ V			50		50		50	µA
I_{OZL}		$V_{CC} = 5.5$ V,	$V_O = 0.5$ V			–50		–50		–50	µA
I_{off}		$V_{CC} = 0$,	V_I or $V_O \leq 4.5$ V			±100				±100	µA
I_{CEX}		$V_{CC} = 5.5$ V, $V_O = 5.5$ V	Outputs high			50		50		50	µA
I_O‡		$V_{CC} = 5.5$ V,	$V_O = 2.5$ V	–50	–100	–180	–50	–180	–50	–180	mA
I_{CC}		$V_{CC} = 5.5$ V, $I_O = 0$, $V_I = V_{CC}$ or GND	Outputs high		1	250		250		250	µA
			Outputs low		24	30		30		30	mA
			Outputs disabled		0.5	250		250		250	µA
ΔI_{CC}§	Data inputs	$V_{CC} = 5.5$ V, One input at 3.4 V, Other inputs at V_{CC} or GND	Outputs enabled			1.5		1.5		1.5	mA
			Outputs disabled			0.05		0.05		0.05	
	Control inputs	$V_{CC} = 5.5$ V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	
C_i	C_i	$V_I = 2.5$ V or 0.5 V			3						pF
C_o	C_o	$V_O = 2.5$ V or 0.5 V			8.5						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at $V_{CC} = 5$ V.

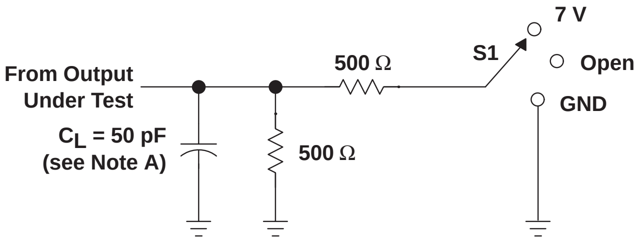
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

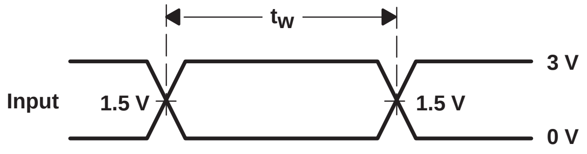
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT2241		SN74ABT2241		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1	3	4.3	1	4.8	1	4.7	ns
t_{PHL}			1	4.3	5.3	1	5.7	1	5.6	
t_{PZH}	OE or $\overline{OE}$	Y	1.1	3.5	4.8	1.1	6.1	1.1	5.8	ns
t_{PZL}			2.1	6.2	7.6	2.1	8.6	2.1	8.4	
t_{PHZ}	OE or $\overline{OE}$	Y	1.7	4.2	5.6	1.7	6.7	1.7	6.6	ns
t_{PLZ}			1.7	3.9	5.8	1.7	6.9	1.7	6.4	

PARAMETER MEASUREMENT INFORMATION

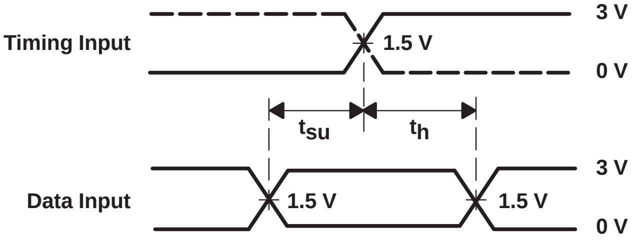


LOAD CIRCUIT

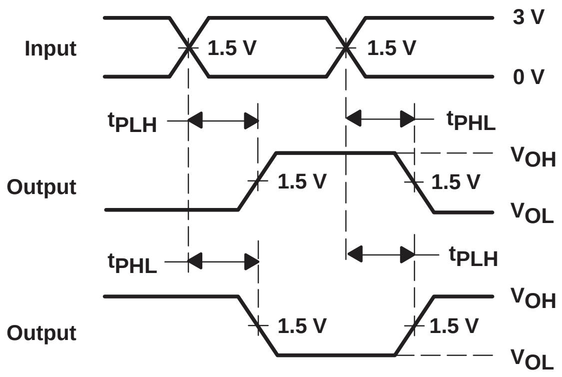
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



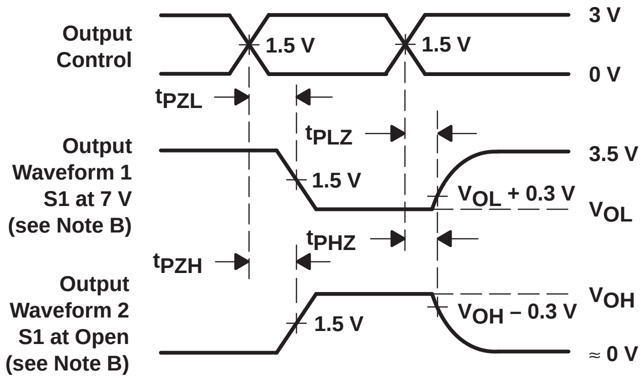
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74ABT2241DBR	Active	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AA241
SN74ABT2241DBR.B	Active	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AA241
SN74ABT2241DW	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT2241
SN74ABT2241DW.B	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT2241
SN74ABT2241DWR	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT2241
SN74ABT2241DWR.B	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT2241
SN74ABT2241PWR	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AA241
SN74ABT2241PWR.B	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AA241

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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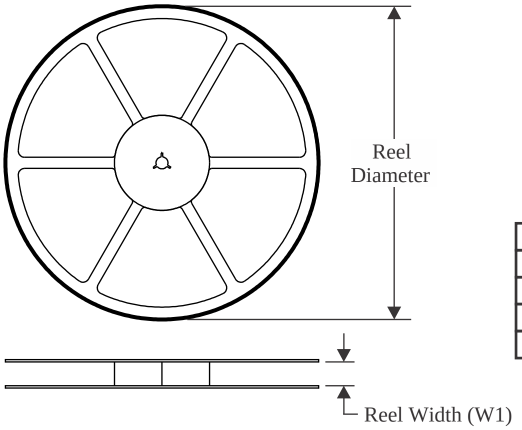
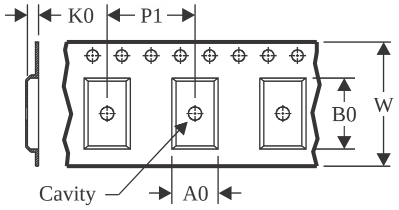
TAPE AND REEL INFORMATION

REEL DIMENSIONS

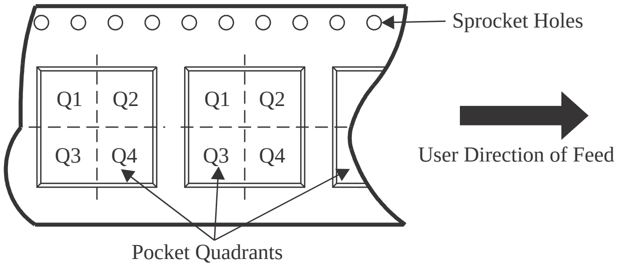


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

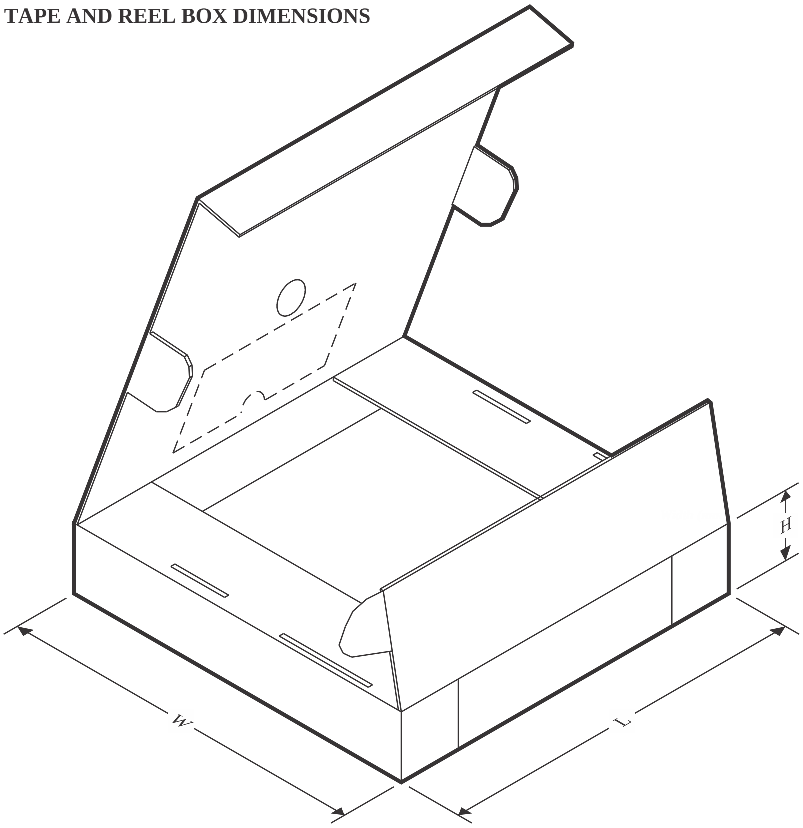
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT2241DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74ABT2241DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74ABT2241PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

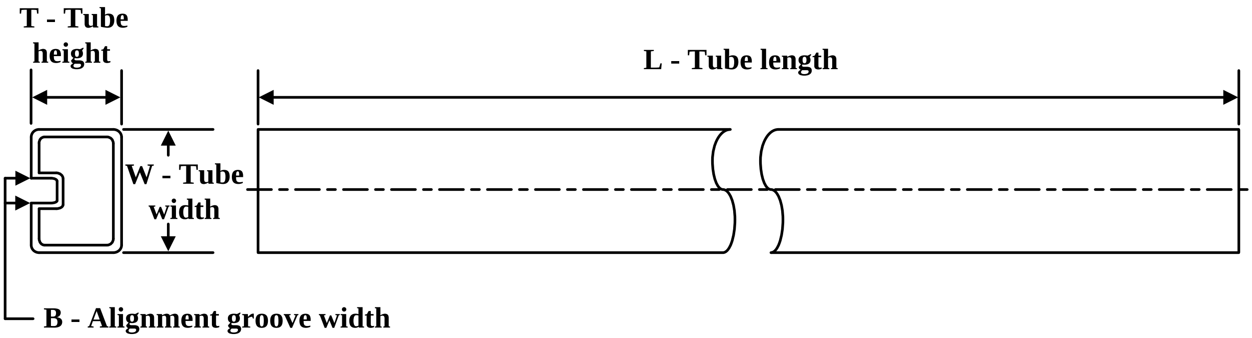
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

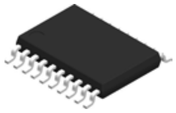
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT2241DBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74ABT2241DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74ABT2241PWR	TSSOP	PW	20	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

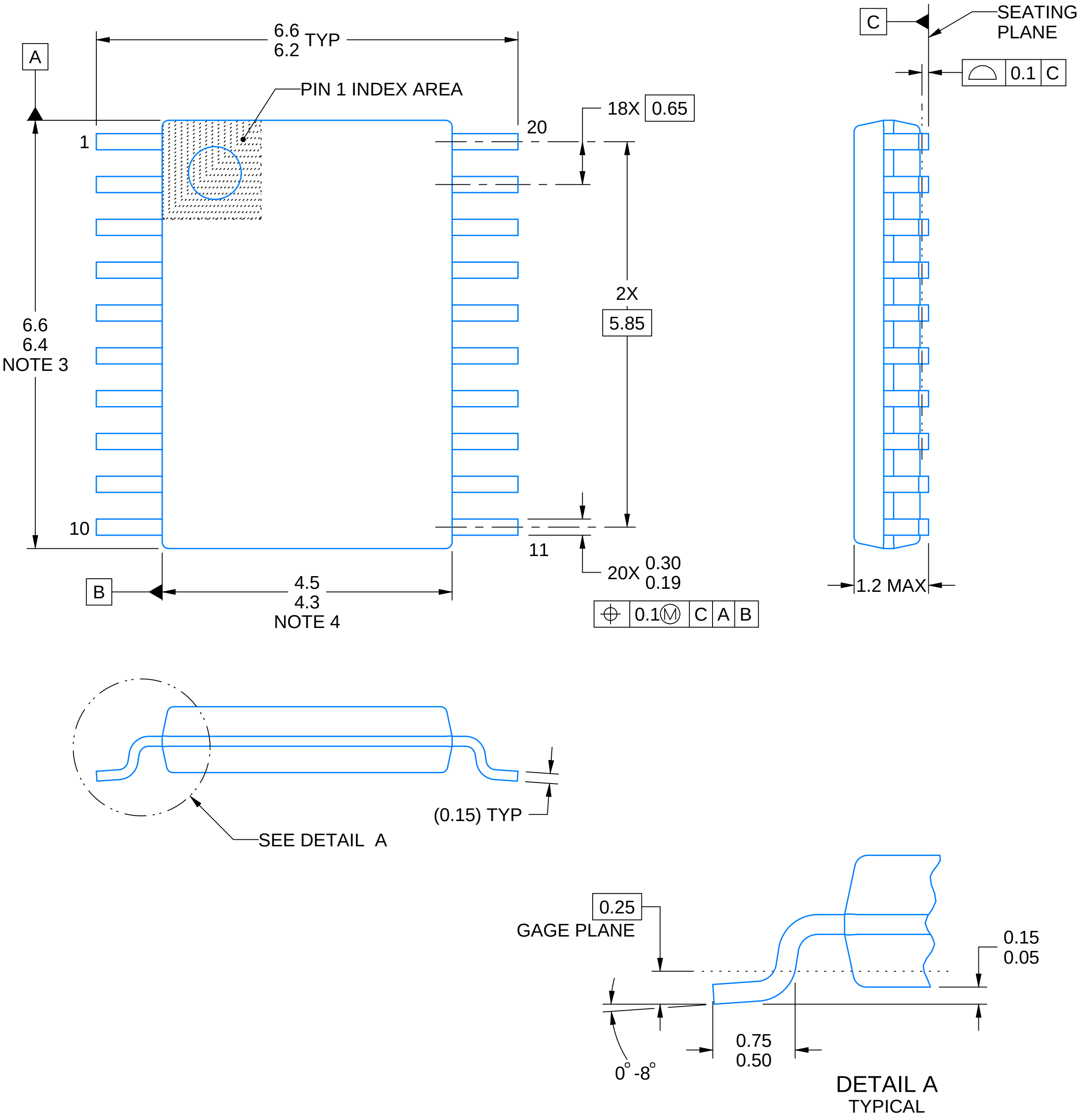
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74ABT2241DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ABT2241DW.B	DW	SOIC	20	25	507	12.83	5080	6.6



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

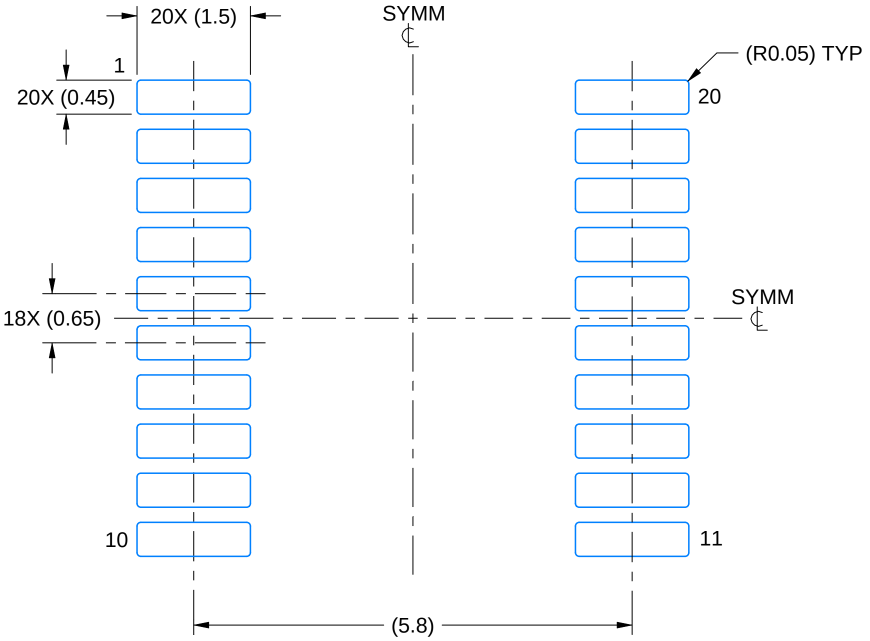
SMALL OUTLINE PACKAGE



4220206/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

NON-SOLDER MASK
DEFINED
(PREFERRED)

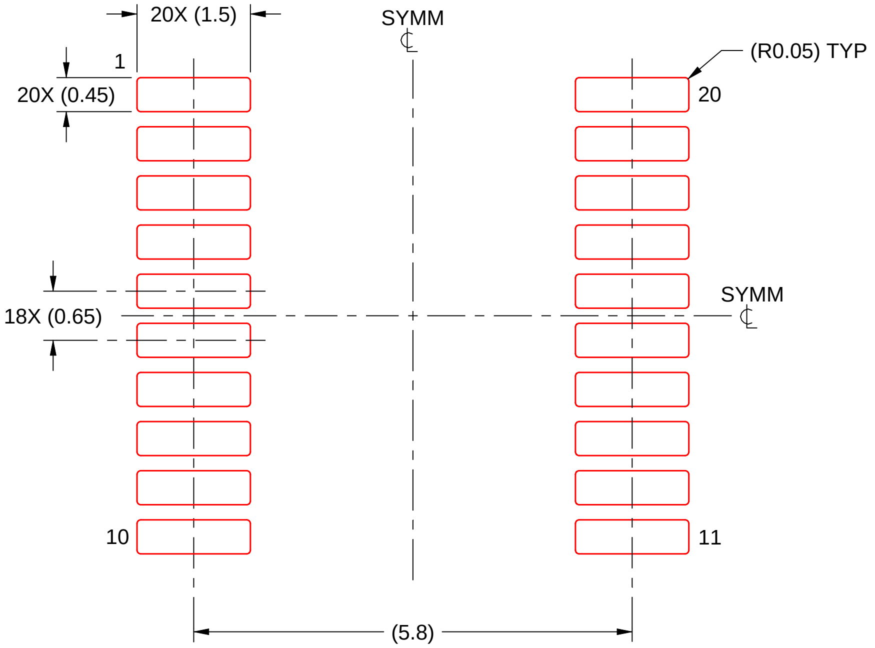
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

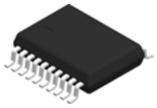


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

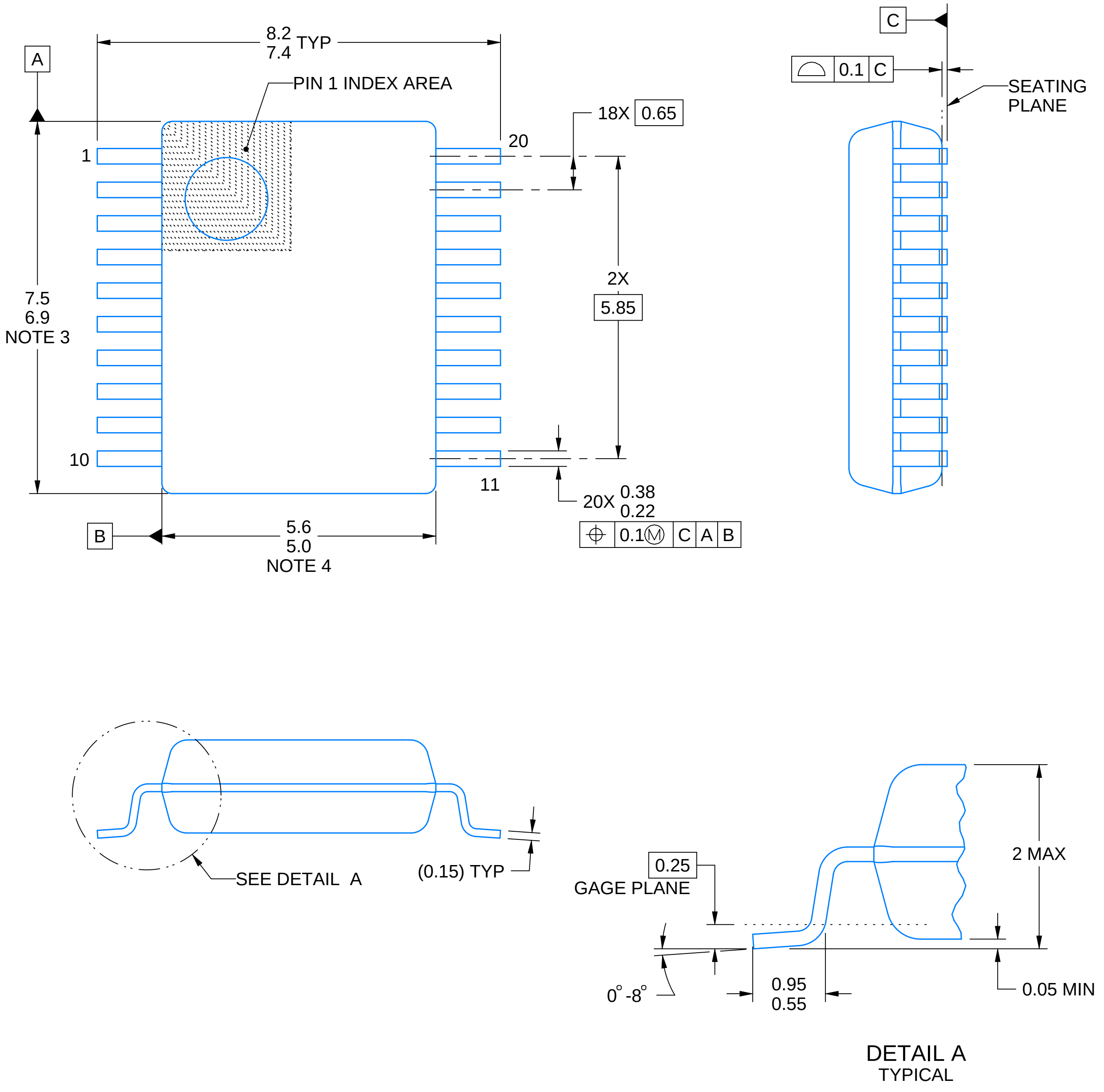
DB0020A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

NOTES:

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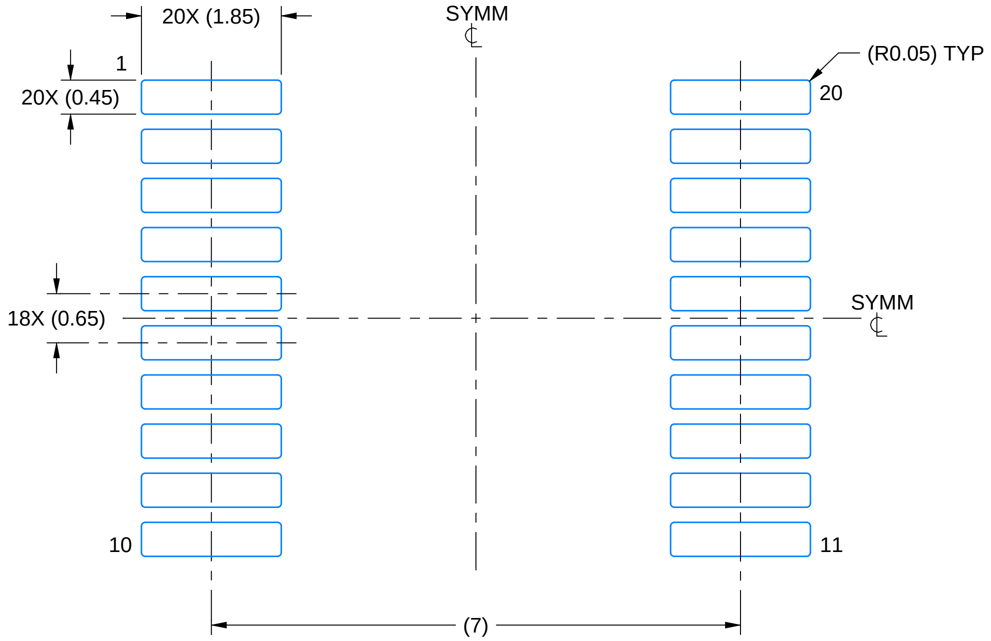
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

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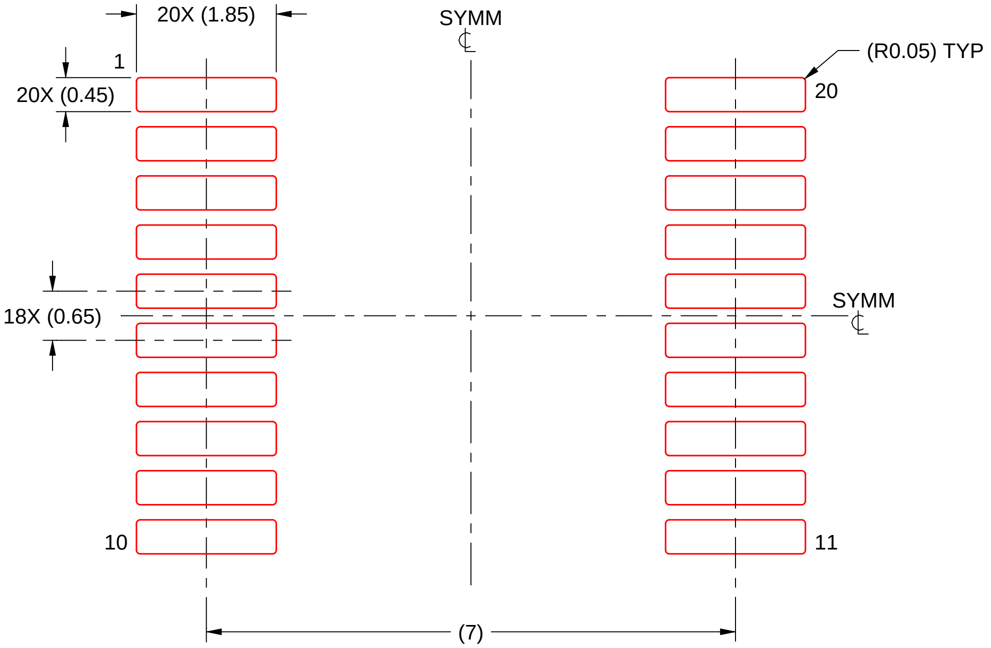
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

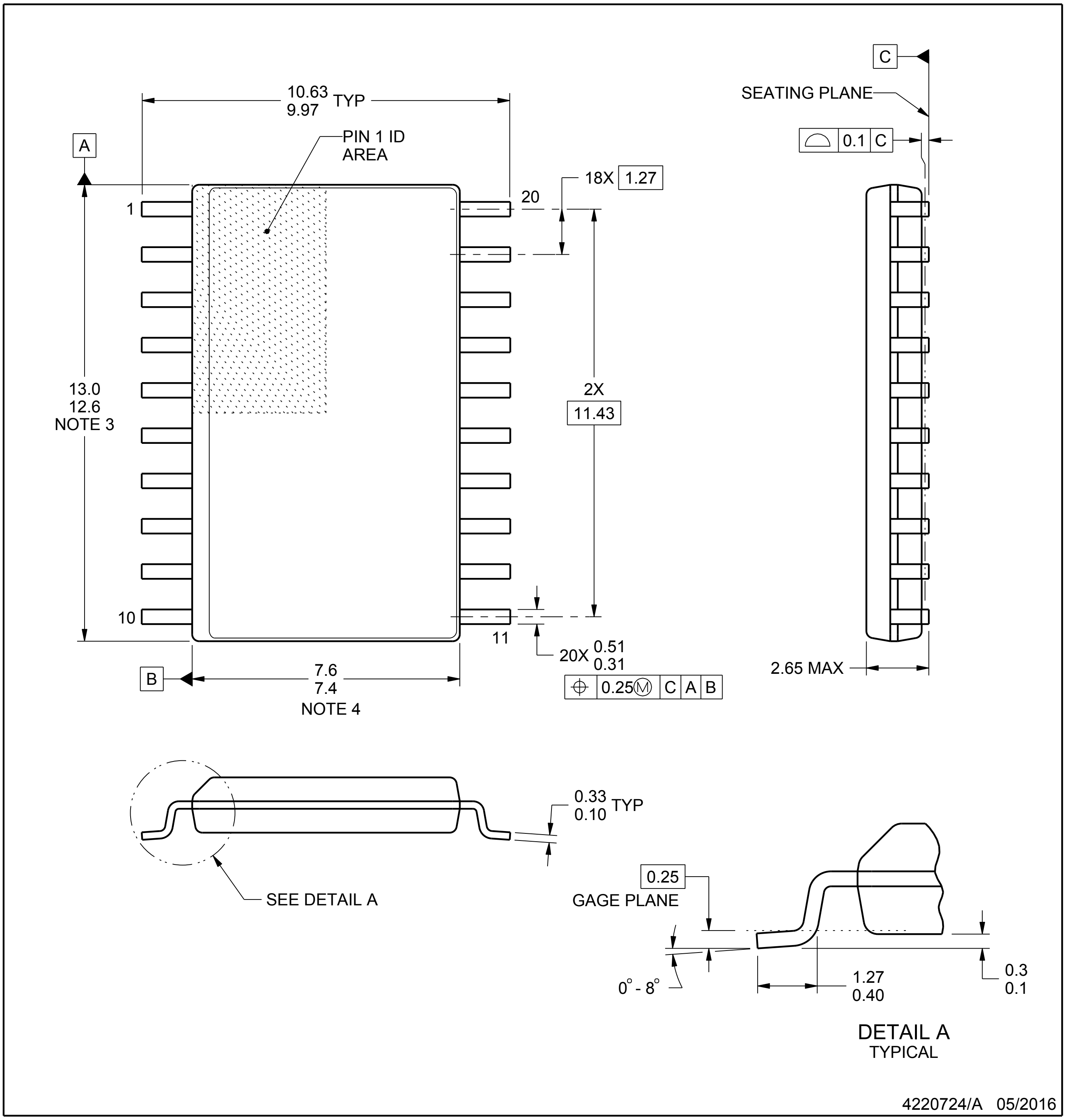


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

SOIC



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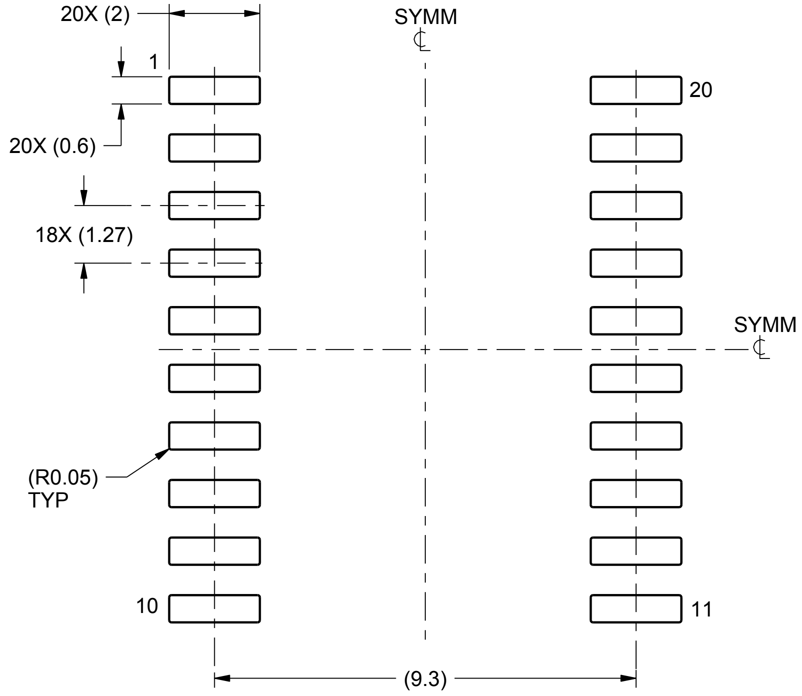
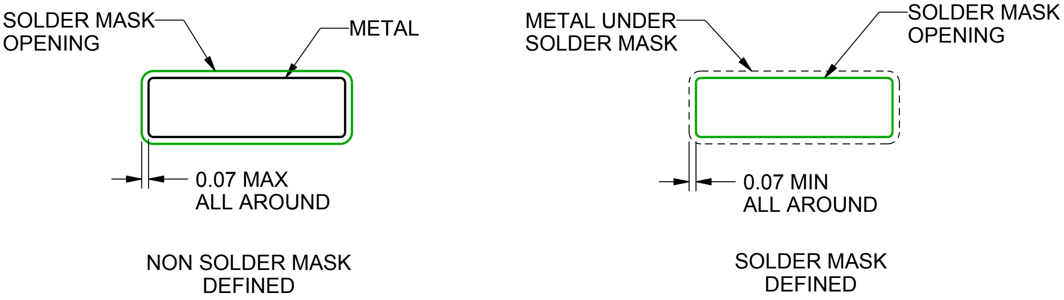
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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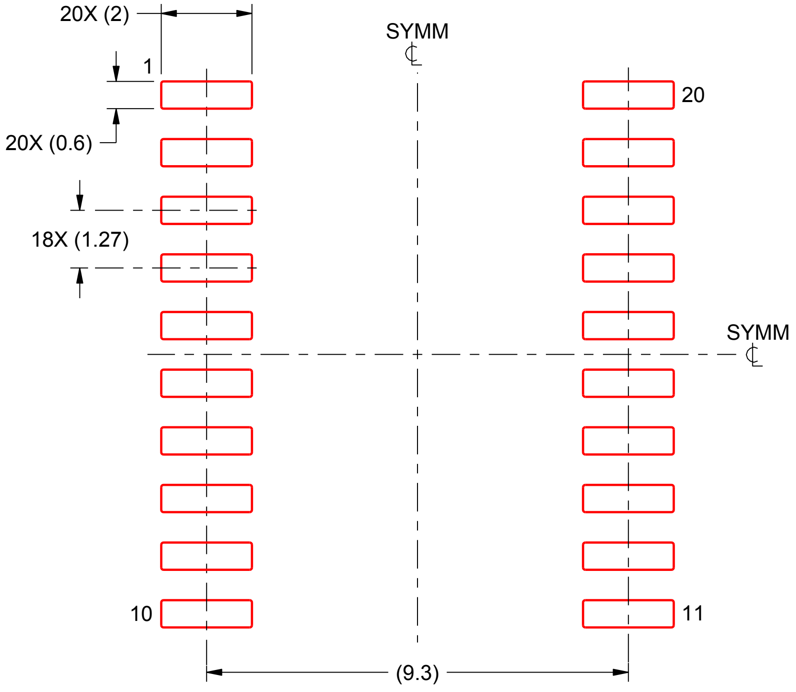
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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