

SN54ACT563, SN74ACT563 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

SCAS550B – NOVEMBER 1995 – REVISED OCTOBER 2002

- 4.5-V to 5.5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 8.5 ns at 5 V
- Inputs Are TTL-Voltage Compatible
- 3-State Inverted Outputs Drive Bus Lines Directly
- Flow-Through Architecture to Optimize PCB Layout

description/ordering information

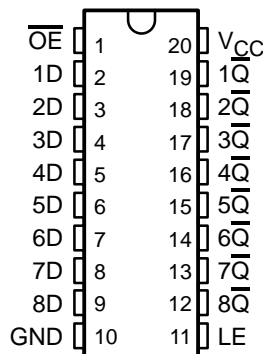
The 'ACT563 devices are octal D-type transparent latches with 3-state outputs. When the latch-enable (LE) input is high, the \bar{Q} outputs are set to the complements of the data (D) inputs. When LE is taken low, the \bar{Q} outputs are latched at the inverse logic levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input places the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased high logic level provide the capability to drive bus lines without interface or pullup components.

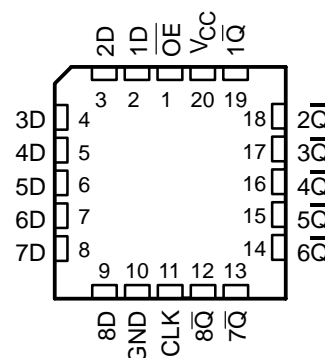
\overline{OE} does not affect internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

SN54ACT563 . . . J OR W PACKAGE SN74ACT563 . . . DB, DW, N, NS, OR PW PACKAGE (TOP VIEW)



SN54ACT563 . . . FK PACKAGE (TOP VIEW)



ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube	SN74ACT563N	SN74ACT563N
	SOIC – DW	Tube	SN74ACT563DW	ACT563
		Tape and reel	SN74ACT563DWR	
	SOP – NS	Tape and reel	SN74ACT563NSR	ACT563
	SSOP – DB	Tape and reel	SN74ACT563DBR	AD563
-55°C to 125°C	TSSOP – PW	Tape and reel	SN74ACT563PWR	AD563
	CDIP – J	Tube	SNJ54ACT5634J	SNJ54ACT563J
	CFP – W	Tube	SNJ54ACT563W	SNJ54ACT563W
	LCCC – FK	Tube	SNJ54ACT563FK	SNJ54ACT563FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2002, Texas Instruments Incorporated

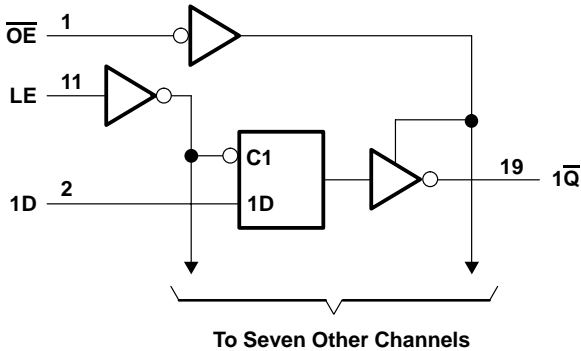
SN54ACT563, SN74ACT563 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

SCAS550B – NOVEMBER 1995 – REVISED OCTOBER 2002

FUNCTION TABLE
(each latch)

INPUTS			OUTPUT \overline{Q}
\overline{OE}	LE	D	
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q_0}$
H	X	X	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±200 mA
Package thermal impedance, θ_{JA} (see Note 2):	
DB package	70°C/W
DW package	58°C/W
N package	69°C/W
NS package	60°C/W
PW package	83°C/W

Storage temperature range, T_{stg}	–65°C to 150°C
--------------------------------------	----------------

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

SN54ACT563, SN74ACT563 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

SCAS550B – NOVEMBER 1995 – REVISED OCTOBER 2002

recommended operating conditions (see Note 3)

		SN54ACT563		SN74ACT563		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		-24		-24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		8		8	ns/V
T_A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			SN54ACT563		SN74ACT563		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$I_{OH} = -50\ \mu\text{A}$	4.5 V	4.4	4.49		4.4		4.4		V
		5.5 V	5.4	5.49		5.4		5.4		
	$I_{OH} = -24\ \text{mA}$	4.5 V	3.86			3.7		3.76		
		5.5 V	4.86			4.7		4.76		
	$I_{OH} = -50\ \text{mA}^\dagger$	5.5 V				3.85				
V_{OL}	$I_{OL} = 50\ \mu\text{A}$	4.5 V		0.001	0.1		0.1		0.1	V
		5.5 V		0.001	0.1		0.1		0.1	
	$I_{OL} = 24\ \text{mA}$	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	$I_{OL} = 50\ \text{mA}^\dagger$	5.5 V					1.65			
	$I_{OL} = 75\ \text{mA}^\dagger$	5.5 V							1.65	
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			± 0.25		± 5		± 2.5	μA
I_I	$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 1		± 1	μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			4		80		40	μA
ΔI_{CC}^\ddagger	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V		0.6			1.6		1.5	mA
C_i	$V_I = V_{CC}$ or GND	5 V		4.5						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC} .

timing requirements over recommended operating free-air temperature range, $V_{CC} = 5\ \text{V} \pm 0.5\ \text{V}$ (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		SN54ACT563		SN74ACT563		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	3		5		3		ns
t_{su}	Setup time, data before LE \downarrow	4		4.5		4.5		ns
t_h	Hold time, data after LE \downarrow	0		1.5		0		ns

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54ACT563, SN74ACT563

OCTAL D-TYPE TRANSPARENT LATCHES

WITH 3-STATE OUTPUTS

SCAS550B – NOVEMBER 1995 – REVISED OCTOBER 2002

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			SN54ACT563		SN74ACT563		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	\overline{Q}	3	7	11.5	1	14.5	2.5	12.5	ns
t_{PHL}			3	6	10	1	12	2.5	11	
t_{PLH}	LE	\overline{Q}	3	6.5	10.5	1	12.5	2.5	11.5	ns
t_{PHL}			2.5	5.5	9.5	1	11.5	2	10.5	
t_{PZH}	\overline{OE}	\overline{Q}	2.5	5.5	9	1	11.5	2	10	ns
t_{PZL}			2	5.5	8.5	1	11	2	9.5	
t_{PHZ}	\overline{OE}	\overline{Q}	3.5	6.5	10.5	1	12	2.5	11.5	ns
t_{PLZ}			2	4.5	8	1	9.5	1	8.5	

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 1\text{ MHz}$	50	pF

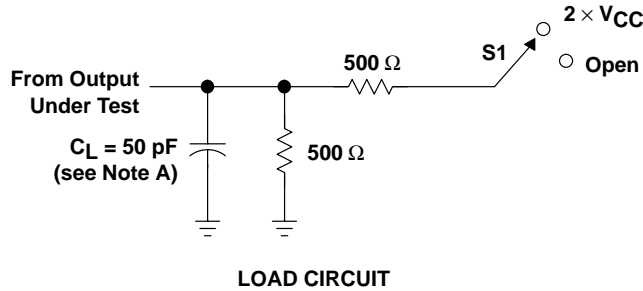
PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



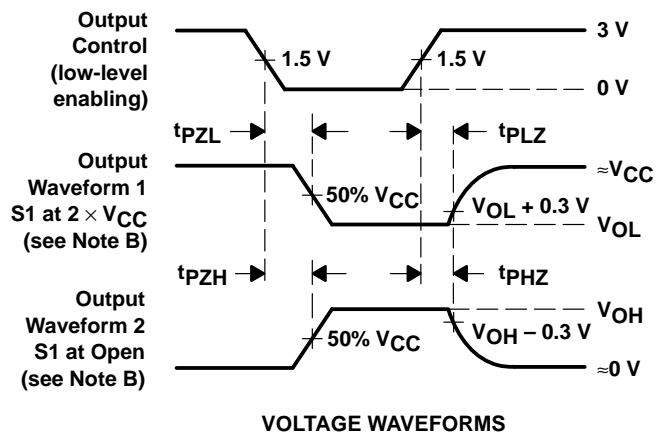
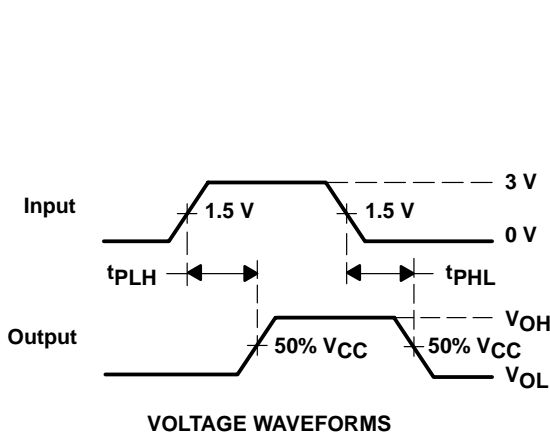
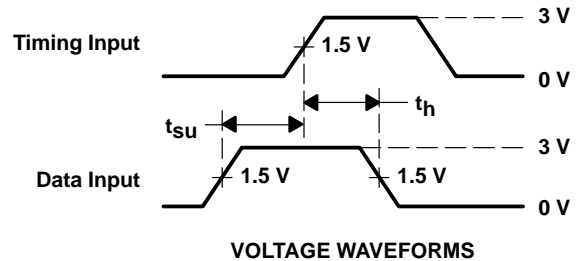
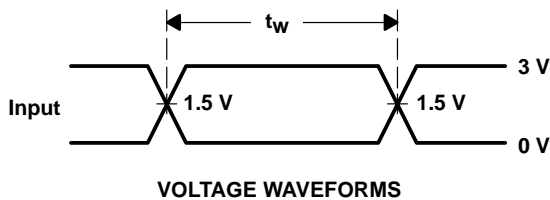
SN54ACT563, SN74ACT563 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

SCAS550B – NOVEMBER 1995 – REVISED OCTOBER 2002

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	Open



NOTES: A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.

D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74ACT563DW	Obsolete	Production	SOIC (DW) 20	-	-	Call TI	Call TI	-40 to 85	ACT563
SN74ACT563DWR	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT563
SN74ACT563DWR.A	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT563
SN74ACT563N	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74ACT563N
SN74ACT563N.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74ACT563N
SN74ACT563PW	Obsolete	Production	TSSOP (PW) 20	-	-	Call TI	Call TI	-40 to 85	AD563
SN74ACT563PWR	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD563
SN74ACT563PWR.A	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD563

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ACT563DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74ACT563PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ACT563DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74ACT563PWR	TSSOP	PW	20	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74ACT563N	N	PDIP	20	20	506	13.97	11230	4.32
SN74ACT563N.A	N	PDIP	20	20	506	13.97	11230	4.32

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025