

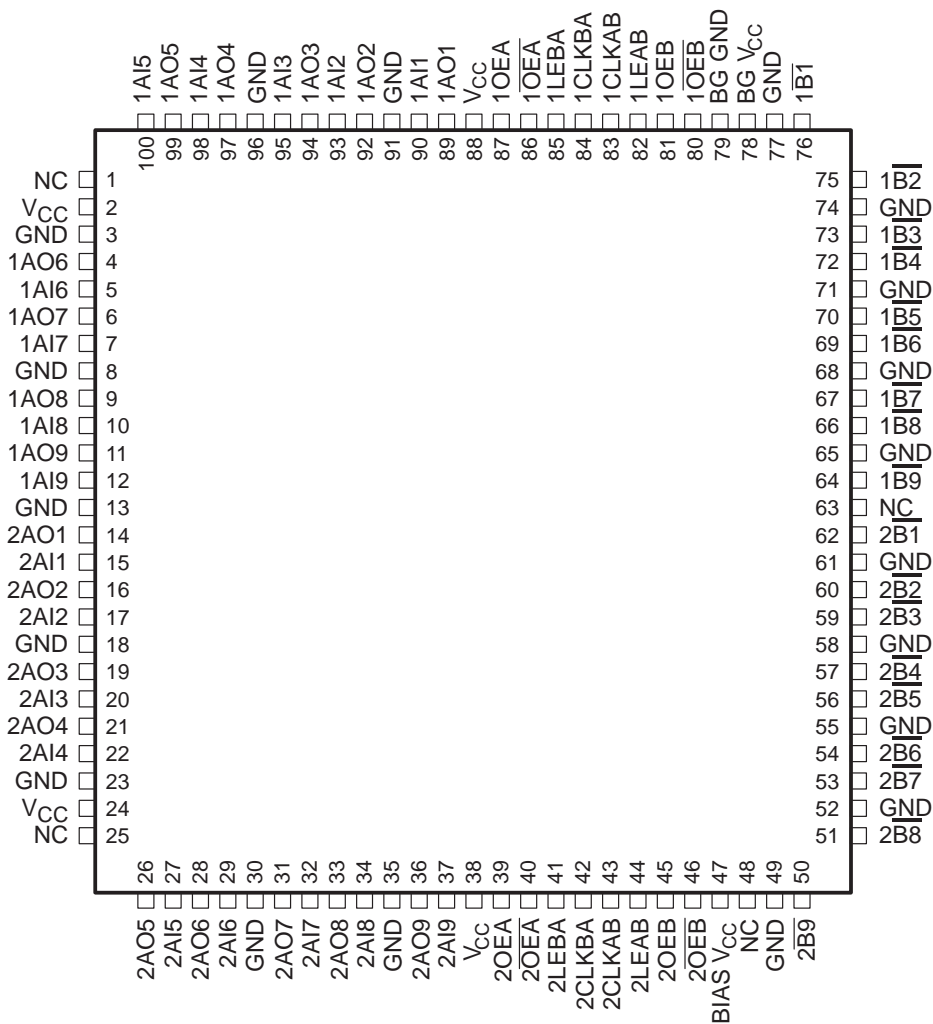
SN74FB1650

18-BIT TTL/BTL UNIVERSAL STORAGE TRANSCEIVER

SCBS1780 – AUGUST 1992 – REVISED MARCH 2004

- Compatible With IEEE Std 1194.1-1991 (BTL)
- TTL A Port, Backplane Transceiver Logic (BTL) \bar{B} Port
- Open-Collector \bar{B} -Port Outputs Sink 100 mA
- BIAS V_{CC} Minimizes Signal Distortion During Live Insertion or Withdrawal
- High-Impedance State During Power Up and Power Down
- \bar{B} -Port Biasing Network Preconditions the Connector and PC Trace to the BTL High-Level Voltage
- TTL-Input Structures Incorporate Active Clamping to Aid in Line Termination

PCA PACKAGE
(TOP VIEW)



NC – No internal connection



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description/ordering information

The SN74FB1650 contains two 9-bit transceivers designed to translate signals between TTL and backplane transceiver-logic (BTL) environments. The device is designed specifically to be compatible with IEEE Std 1194.1-1991.

The \bar{B} port operates at BTL-signal levels. The open-collector \bar{B} ports are specified to sink 100 mA. Two output enables (OEB and \overline{OEB}) are provided for the \bar{B} outputs. When OEB is low, \overline{OEB} is high, or V_{CC} is less than 2.1 V, the \bar{B} port is turned off.

The A port operates at TTL-signal levels. The A outputs reflect the inverse of the data at the \bar{B} port when the A-port output enable (OEA) is high. When OEA is low or when V_{CC} is less than 2.1 V, the A outputs are in the high-impedance state.

BIAS V_{CC} establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V_{CC} is not connected.

BG V_{CC} and BG GND are the supply inputs for the bias generator.

ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	TQFP – PCA	Tube	SN74FB1650PCA	FB1650

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Function Tables

TRANSCEIVER

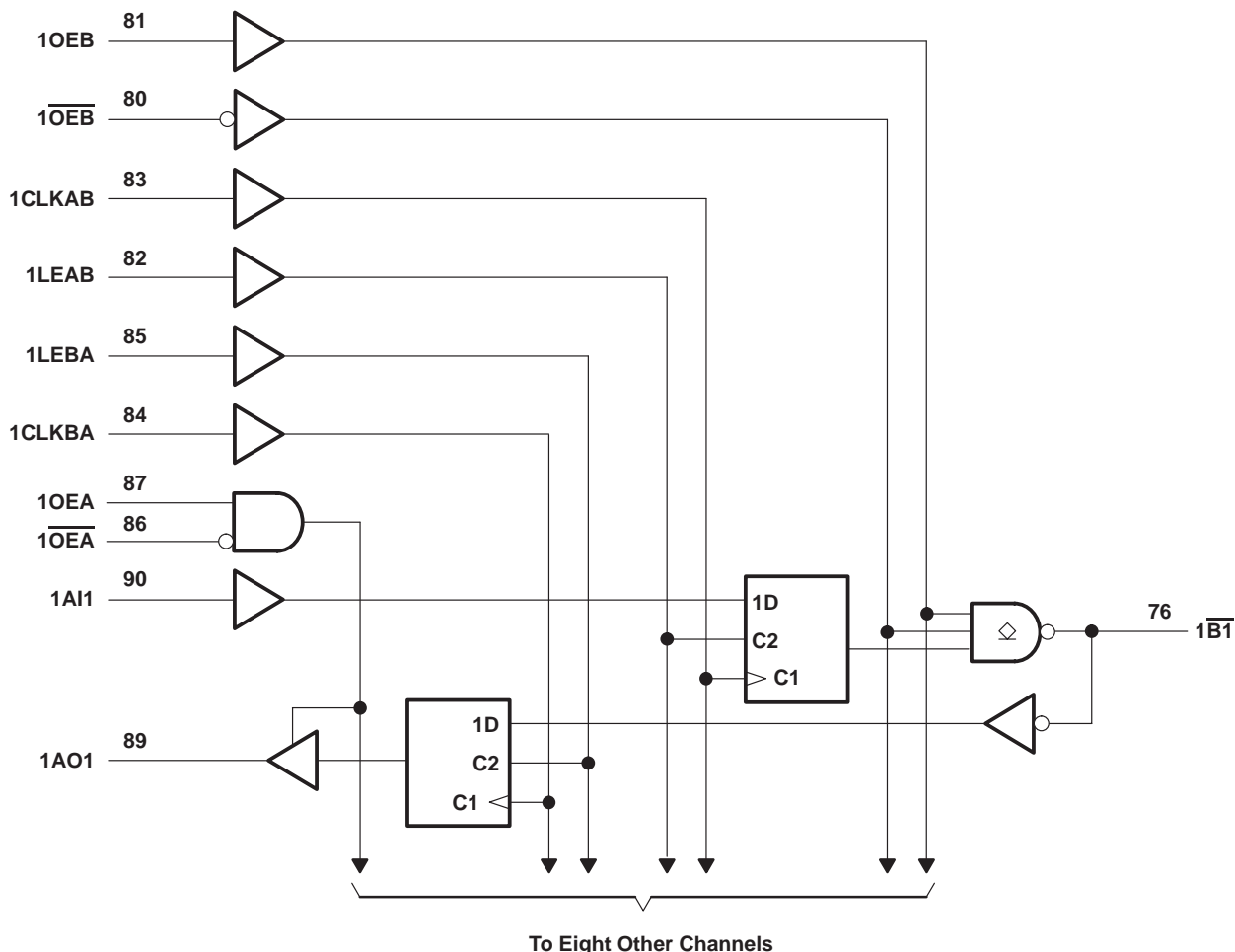
INPUTS				FUNCTION
\overline{OEA}	OEA	OEB	\overline{OEB}	
X	X	H	L	\bar{A} data to B bus
L	H	X	X	\bar{B} data to A bus
L	H	H	L	\bar{A} data to B bus, \bar{B} data to A bus
X	X	L	X	B-bus isolation
X	X	X	H	
H	X	X	X	A-bus isolation
X	L	X	X	

STORAGE MODE

INPUTS		FUNCTION
LE	CLK	
H	X	Transparent
L	↑	Store data
L	L	Storage



functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} , BIAS V_{CC} , BG V_{CC}	-0.5 V to 7 V
Input voltage range, V_I : Except \bar{B} port	-1.2 V to 7 V
\bar{B} port	-1.2 V to 3.5 V
Voltage range applied to any \bar{B} output in the disabled or power-off state, V_O	-0.5 V to 3.5 V
Voltage range applied to any output in the high state, V_O	-0.5 V to V_{CC}
Input clamp current, I_{IK} : Except \bar{B} port	-40 mA
\bar{B} port	-18 mA
Current applied to any single output in the low state, I_O : A port	48 mA
B port	200 mA
Package thermal impedance, θ_{JA} (see Note 1)	22°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

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recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC} , BG V_{CC} , BIAS V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	\overline{B} port	1.62	2.3	V
		Except \overline{B} port	2		
V_{IL}	Low-level input voltage	\overline{B} port	0.75	1.47	V
		Except \overline{B} port		0.8	
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current	A port		24	mA
		\overline{B} port		100	
T_A	Operating free-air temperature	0		70	°C

NOTE 2: To ensure proper device operation, all unused inputs must be terminated as follows: A and control inputs to V_{CC} (5 V) or GND, and B inputs to GND only. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	\overline{B} port	$V_{CC} = 4.5$ V,	$I_I = -18$ mA			-1.2	V
	Except \overline{B} port	$V_{CC} = 4.5$ V,	$I_I = -40$ mA			-0.5	
V_{OH}	AO port	$V_{CC} = 4.5$ V,	$I_{OH} = -3$ mA	2.5	3.3		V
V_{OL}	AO port	$V_{CC} = 4.5$ V,	$I_{OL} = 24$ mA		0.35	0.5	V
	\overline{B} port	$V_{CC} = 4.5$ V	$I_{OL} = 80$ mA	0.75	1.1		
			$I_{OL} = 100$ mA		1.15		
I_I	Except \overline{B} port	$V_{CC} = 5.5$ V,	$V_I = 5.5$ V			50	μA
$I_{IH}‡$	Except \overline{B} port	$V_{CC} = 5.5$ V,	$V_I = 2.7$ V			50	μA
$I_{IL}‡$	Except \overline{B} port	$V_{CC} = 5.5$ V,	$V_I = 0.5$ V			-50	μA
	\overline{B} port	$V_{CC} = 5.5$ V,	$V_I = 0.75$ V			-100	
I_{OZH}	AO port	$V_{CC} = 5.5$ V,	$V_O = 2.7$ V			50	μA
I_{OZL}	AO port	$V_{CC} = 5.5$ V,	$V_O = 0.5$ V			-50	μA
I_{OZPU}	AO port	$V_{CC} = 0$ to 2.1 V,	$V_O = 0.5$ V to 2.7 V			50	μA
I_{OZPD}	AO port	$V_{CC} = 2.1$ V to 0,	$V_O = 0.5$ V to 2.7 V			-50	μA
I_{OH}	\overline{B} port	$V_{CC} = 0$ to 5.5 V,	$V_O = 2.1$ V			100	μA
$I_{OS}§$	A port	$V_{CC} = 5.5$ V,	$V_O = 0$	-30		-150	mA
I_{CC}	A port to \overline{B} port	$V_{CC} = 5.5$ V,	$I_O = 0$			100	mA
	\overline{B} port to A port					120	
C_i	A1 port	$V_I = V_{CC}$ or GND			5.5		pF
	Control inputs				5.5		
C_O	AO ports	$V_O = V_{CC}$ or GND			5.5		pF
C_{io}	\overline{B} port per IEEE Std 1194.1-1991	$V_{CC} = 0$ to 5.5 V				5.5	pF

† All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.



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live-insertion specifications over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
I_{CC} (BIAS V_{CC})	$V_{CC} = 0$ to 4.5 V	$V_B = 0$ to 2 V,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V	450		μA
	$V_{CC} = 4.5$ V to 5.5 V			10		
V_O	\overline{B} port	$V_{CC} = 0$,	V_I (BIAS V_{CC}) = 5 V	1.62	2.1	V
I_O	\overline{B} port	$V_{CC} = 0$,	$V_B = 1$ V,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V		μA
		$V_{CC} = 0$ to 2.2 V,	OEB = 0 to 5 V	100		
		$V_{CC} = 0$ to 5.5 V,	OEB = 0 to 0.8 V	1		mA

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			$V_{CC} = 5$ V, $T_A = 25^\circ C$		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency		150			150	MHz
t_w	Pulse duration	CLK or LE	3.3		3.3		ns
t_{su}	Setup time	Data before LE	4.8		4.8		ns
		Data before CLK \uparrow	4.9		4.9		
t_h	Hold time	Data after LE	1.8		1.8		ns
		Data after CLK \uparrow	1.1		1.1		



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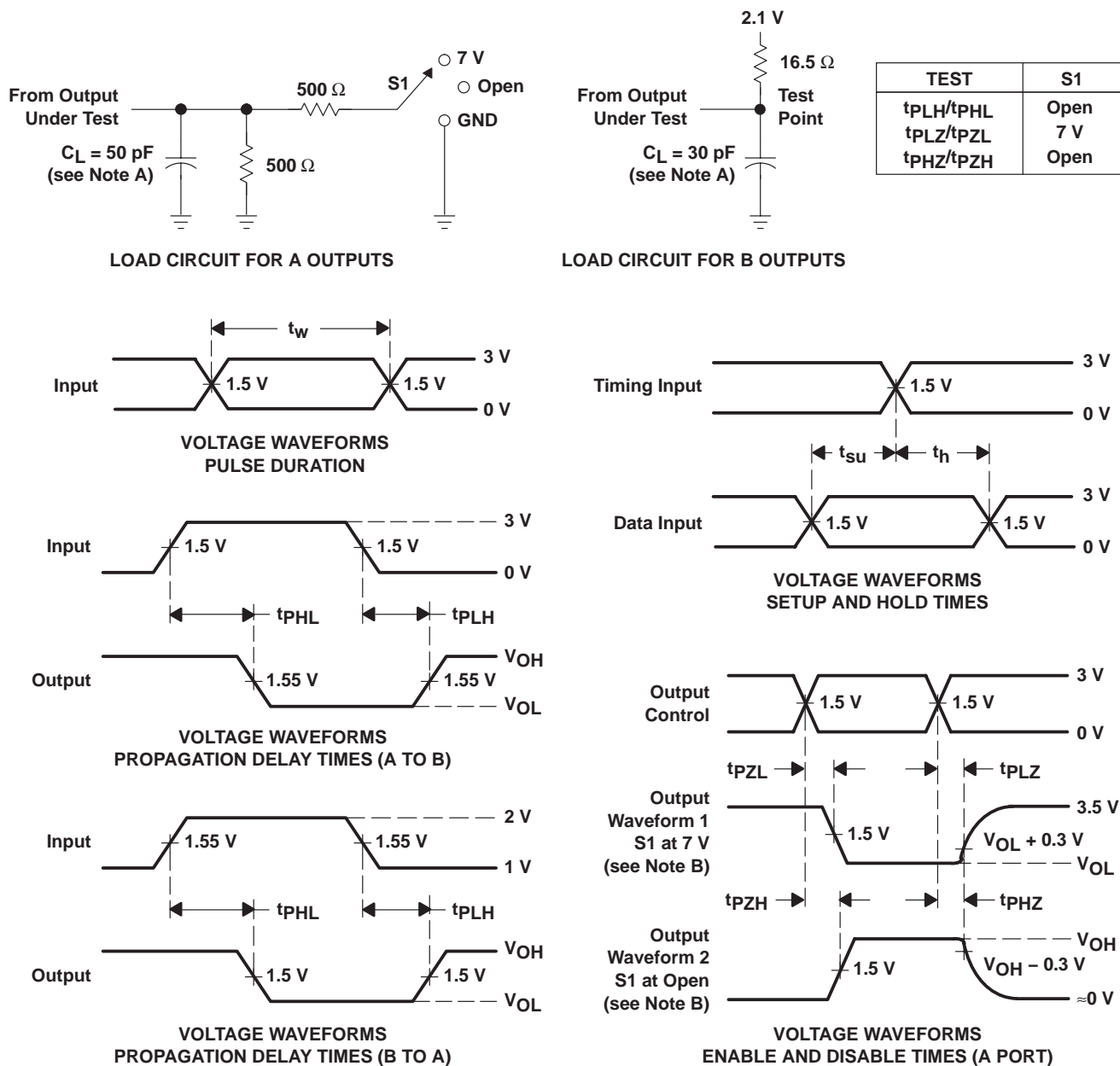
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f _{max}			150			150		MHz
t _{PLH}	AI	\overline{B}	1.8	3.7	5.3	1.8	6.2	ns
t _{PHL}			2.9	4.4	6	2.9	7.2	
t _{PLH}	LEAB	\overline{B}	2.7	4.2	5.8	2.7	6.4	ns
t _{PHL}			3.5	5	6.5	3.5	7.3	
t _{PLH}	CLKAB	\overline{B}	2.3	3.9	5.5	2.3	6	ns
t _{PHL}			2.9	4.5	6.1	2.9	6.7	
t _{PLH}	\overline{B}	AO	3.5	5.9	7.9	3.5	8.6	ns
t _{PHL}			2.2	3.7	5.3	2.2	5.7	
t _{PLH}	LEBA	AO	1.8	3.2	4.6	1.8	5.1	ns
t _{PHL}			1.7	3	4.4	1.7	4.7	
t _{PLH}	CLKBA	AO	1.8	3.1	4.6	1.8	5.1	ns
t _{PHL}			1.7	3.1	4.6	1.7	4.9	
t _{PLH}	OEB	\overline{B}	2.7	4.6	6.4	2.7	6.7	ns
t _{PHL}			2.9	4.1	5.9	2.9	6.6	
t _{PLH}	\overline{OEB}	\overline{B}	2.6	4.3	6.2	2.6	6.6	ns
t _{PHL}			3.4	4.6	6.4	3.4	7	
t _{PZH}	OEA	AO	1.4	2.9	4.4	1.4	4.9	ns
t _{PZL}			1.4	2.6	4	1.4	4.6	
t _{PHZ}	OEA	AO	1.7	3.4	5.1	1.7	5.8	ns
t _{PLZ}			2.2	3.6	5	2.2	5.5	
t _{PZH}	\overline{OEA}	AO	1.7	3.3	4.7	1.7	5.5	ns
t _{PZL}			1.7	3.1	4.4	1.7	5.1	
t _{PHZ}	\overline{OEA}	AO	1.5	2.9	4.5	1.5	5.1	ns
t _{PLZ}			2	3.1	4.6	2	4.8	
t _{sk(p)} [†]	Pulse skew, AI to \overline{B} or \overline{B} to AO		1					ns
t _{sk(o)} [†]	Output skew, AI to \overline{B} or \overline{B} to AO		0.5					ns
t _t Transition time	\overline{B} outputs (1.3 V to 1.8 V)		0.9	1.7	3.1	0.5	4.6	ns
	AO outputs (10% to 90%)		0.5	2	3.6	0.4	4.2	
t _(pr)	\overline{B} -port input pulse rejection		1			1		ns

[†] Skew values are applicable for through mode only.



PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: TTL inputs: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns; BTL inputs: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74FB1650PCA	Active	Production	HLQFP (PCA) 100	90 JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	0 to 70	FB1650
SN74FB1650PCA.B	Active	Production	HLQFP (PCA) 100	90 JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	0 to 70	FB1650

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TRAY



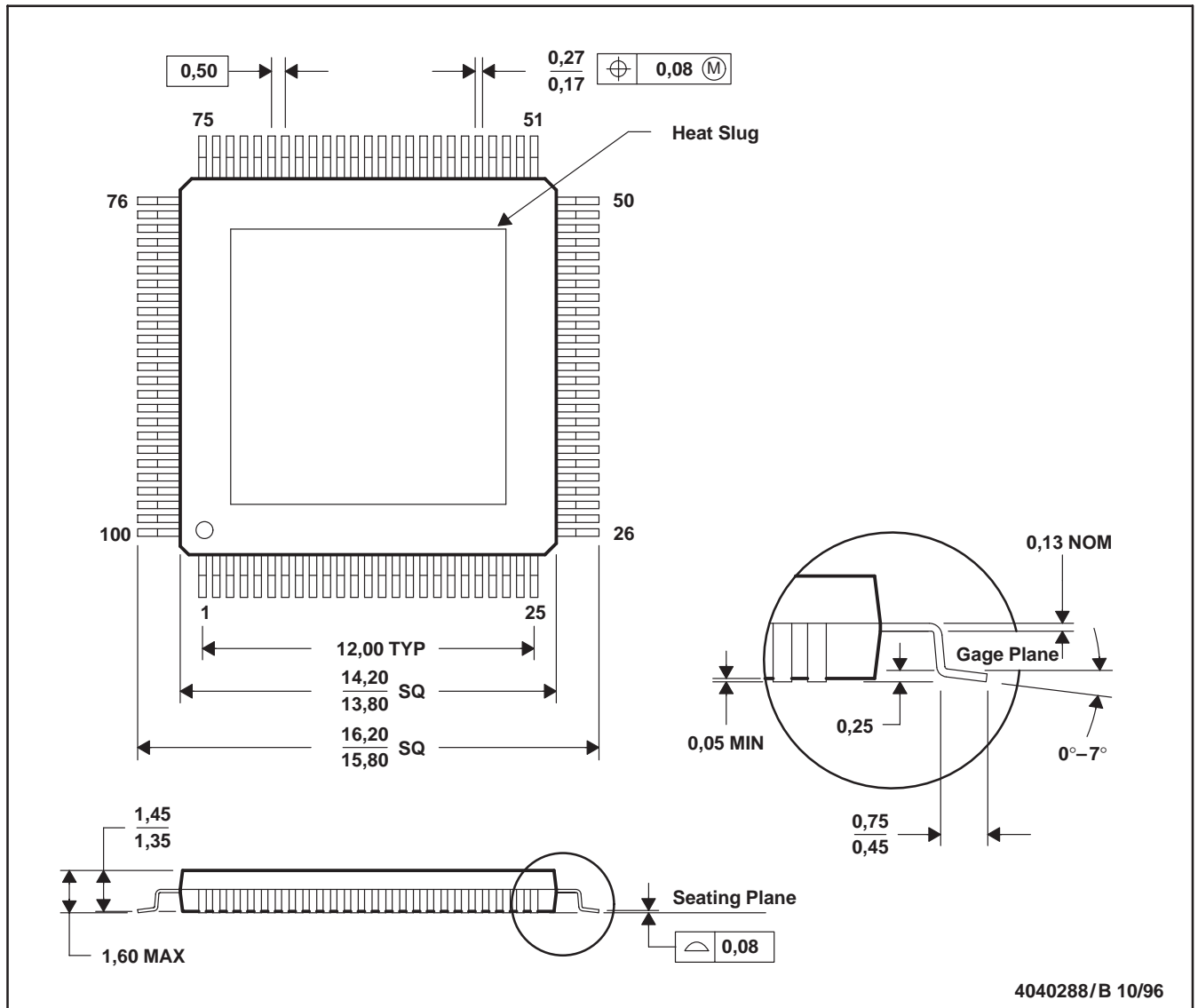
Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
SN74FB1650PCA	PCA	HLQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.45
SN74FB1650PCA.B	PCA	HLQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.45

PCA (S-PQFP-G100)

PLASTIC QUAD FLATPACK (DIE DOWN)



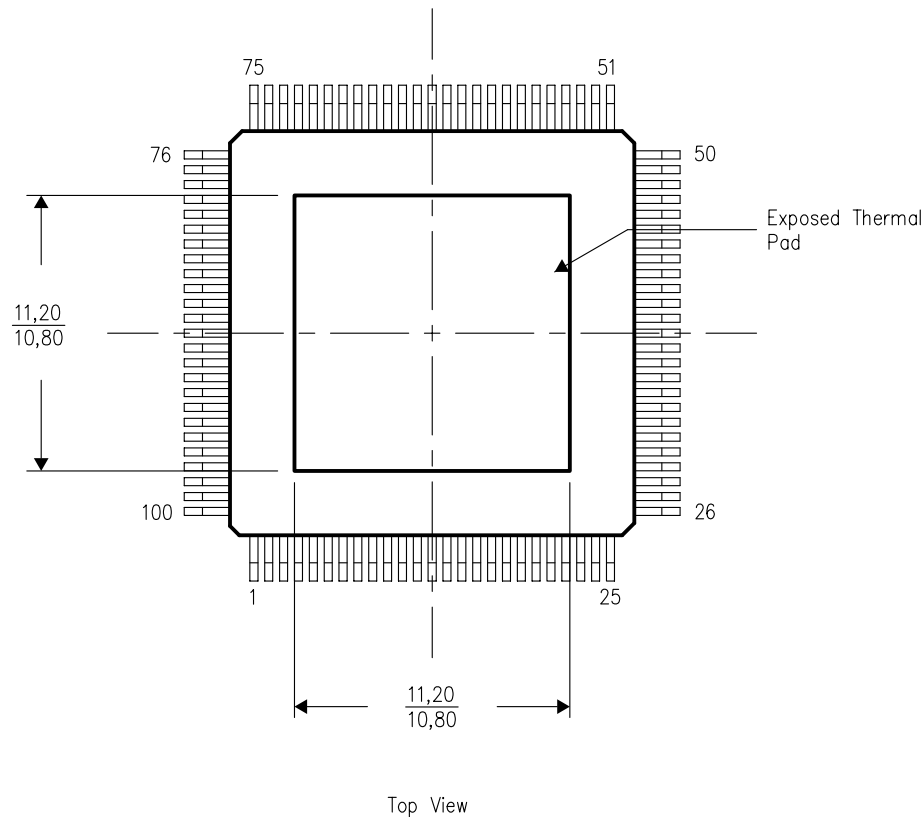
- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Thermally enhanced molded plastic package with a heat slug (HSL)
 D. Falls within JEDEC MS-026

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

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