# SNx4HC112 Dual J-K Negative-Edge-Triggered Flip-Flops With Clear and Preset

## 1 Features

- Wide operating voltage range of 2V to 6V
- Outputs can drive up to 10 LSTTL loads
- Low power consumption, 40µA max $I_{CC}$
- Typical $t_{pd}$ = 13ns
- ±4mA output drive at 5V
- Low input current of 1µA max

## 2 Applications

- Servers
- LED displays
- Network switch
- Telecom infrastructure
- Motor drivers
- I/O expanders

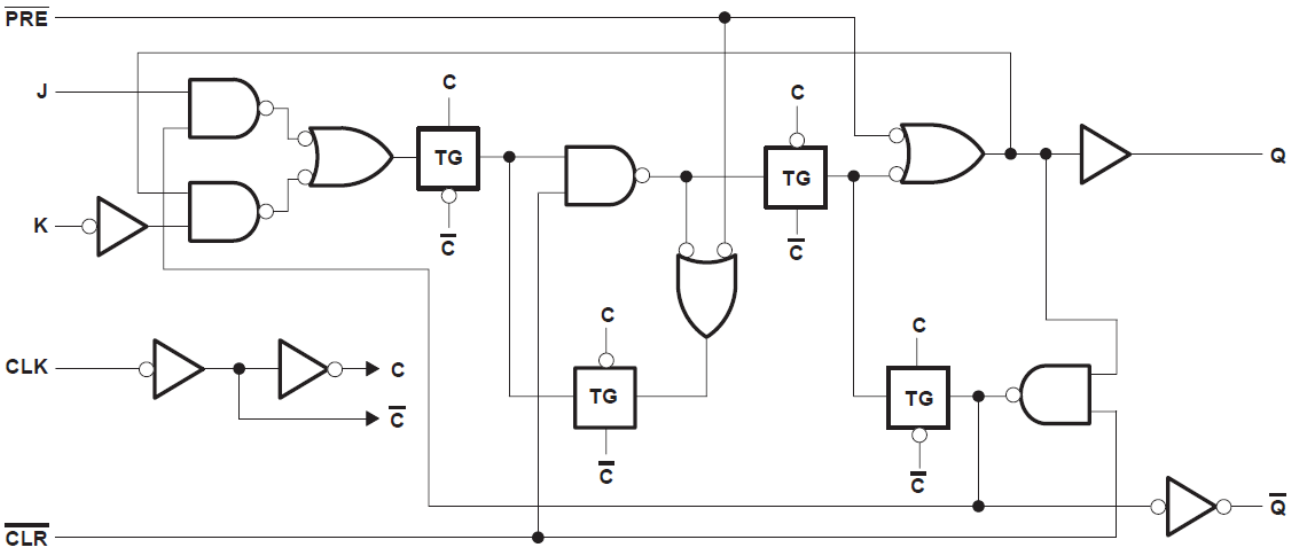
## 3 Description

The SNx4HC112 devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) inputs sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not directly related to the fall time of the CLK pulse. Following the hold-time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops perform as toggle flip-flops by tying J and K high.

**Device Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) | BODY SIZE (NOM)(3) |
|---|---|---|---|
| SNx4HC112 | J (CDIP, 16) | 19.56mm × 6.92mm | 19.56mm × 6.92mm |
| | D (SOIC, 16) | 9.9mm × 6mm | 9.9mm × 3.9mm |
| | N (PDIP, 16) | 19.3mm × 9.4mm | 19.3mm × 6.35mm |
| | FK (LCCC, 20) | 8.89mm × 8.89mm | 8.89mm × 8.89mm |
| | W (CFP, 16) | 10.3mm × 6.73mm | 10.3mm × 6.73mm |

(1) For more information, see Section 11
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.




**Functional Block Diagram**

## Table of Contents



## 4 Pin Configuration and Functions

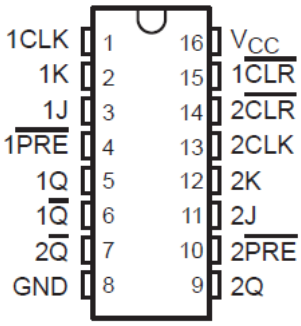
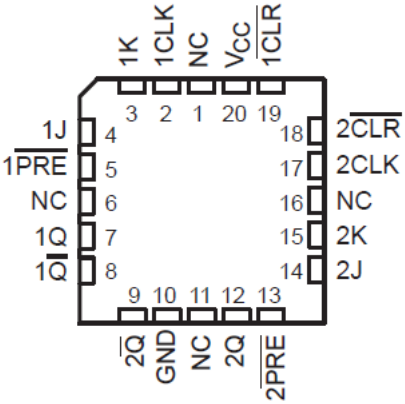



**Figure 4-1. J, D, N, W Package, 16-Pin CDIP, SOIC, PDIP, CFP (Top View)**




NC – No internal connection

**Figure 4-2. FK Package, 20-Pin LCCC (Top View)**

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | –0.5 | 7 | V |
| $I_{IK}$ | Input clamp current(2) | $V_I < 0$ or $V_I > V_{CC}$ | | ±20 | mA |
| $I_{OK}$ | Output clamp current(2) | $V_O < 0$ or $V_O > V_{CC}$ | | ±20 | mA |
| $I_O$ | Continuous output current | $V_O = 0$ to $V_{CC}$ | | ±25 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±50 | mA |
| $T_J$ | Junction temperature | | | 150 | ℃ |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | ℃ |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 5.2 Recommended Operating Conditions (2)

| | | | SN54HC112 | | | SN74HC112 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5 | 6 | 2 | 5 | 6 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2V | 1.5 | | | 1.5 | | | V |
| | | $V_{CC}$ = 4.5V | 3.15 | | | 3.15 | | | |
| | | $V_{CC}$ = 6V | 4.2 | | | 4.2 | | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2V | | | 0.5 | | | 0.5 | V |
| | | $V_{CC}$ = 4.5V | | | 1.35 | | | 1.35 | |
| | | $V_{CC}$ = 6V | | | 1.8 | | | 1.8 | |
| $V_I$ | Input voltage | | 0 | | $V_{CC}$ | 0 | | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | | $V_{CC}$ | 0 | | $V_{CC}$ | V |
| $t_t$ (1) | Input transition (rise and fall) time | $V_{CC}$ = 2V | | | 1000 | | | 1000 | ns |
| | | $V_{CC}$ = 4.5V | | | 500 | | | 500 | |
| | | $V_{CC}$ = 6V | | | 400 | | | 400 | |
| $T_A$ | Operating free-air temperature | | −55 | | 125 | −40 | | 85 | °C |

(1) If this device is used in the threshold region (from $V_{IL}$max = 0.5V to $V_{IH}$min = 1.5V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at $t_t$ = 1000ns and $V_{CC}$ = 2V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.
(2) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## 5.3 Thermal Information

| THERMAL METRIC | | D (SOIC) | N (PDIP) | UNIT |
|---|---|---|---|---|
| | | 16 PINS | 16 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance (1) | 117.2 | 89.1 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 77.2 | 46.9 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 75.6 | 47.4 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 38.1 | 11.8 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 75.3 | 47 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

## 5.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | $V_{CC}$ | $T_A$ = 25°C | | | SN54HC112 | | SN74HC112 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $V_I$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = −20μA | 2V | 1.9 | 1.998 | | 1.9 | | 1.9 | | V |
| | | | 4.5V | 4.4 | 4.499 | | 4.4 | | 4.4 | | |
| | | | 6V | 5.9 | 5.999 | | 5.9 | | 5.9 | | |
| | | $I_{OH}$ = −4mA | 4.5V | 3.98 | 4.3 | | | 3.7 | | 3.84 | |
| | | $I_{OH}$ = −5.2mA | 6V | 5.48 | 5.8 | | | 5.2 | | 5.34 | |
| $V_{OL}$ | $V_I$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 20μA | 2V | | 0.002 | 0.1 | | 0.1 | | 0.1 | V |
| | | | 4.5V | | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| | | | 6V | | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| | | $I_{OL}$ = 4mA | 4.5V | | 0.17 | 0.26 | | 0.4 | | 0.33 | |
| | | $I_{OL}$ = 5.2mA | 6V | | 0.15 | 0.26 | | 0.4 | | 0.33 | |
| $I_I$ | $V_I$ = $V_{CC}$ or 0 | | 6V | | ±0.1 | ±100 | | ±1000 | | ±1000 | nA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or 0, | $I_O$ = 0 | 6V | | | 4 | | 80 | | 40 | μA |
| $C_i$ | | | 2V to 6V | | 3 | 10 | | 10 | | 10 | pF |

## 5.5 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

| | | | $V_{CC}$ | $T_A$ = 25°C | | SN54HC112 | | SN74HC112 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | 2V | | 5 | | 3.4 | | 4 | MHz |
| | | | 4.5V | | 25 | | 17 | | 20 | |
| | | | 6V | | 29 | | 20 | | 24 | |
| $t_w$ | Pulse duration | $\overline{PRE}$ or $\overline{CLR}$ low | 2V | 100 | | 150 | | 125 | | ns |
| | | | 4.5V | 20 | | 30 | | 25 | | |
| | | | 6V | 17 | | 25 | | 21 | | |
| | | CLK high or low | 2V | 100 | | 150 | | 125 | | |
| | | | 4.5V | 20 | | 30 | | 25 | | |
| | | | 6V | 17 | | 25 | | 21 | | |

## 5.5 Timing Requirements (continued)

over recommended operating free-air temperature range (unless otherwise noted)

| | | | $V_{CC}$ | $T_A$ = 25°C | | SN54HC112 | | SN74HC112 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{su}$ | Setup time before CLK↓ | Data (J, K) | 2V | 100 | | 150 | | 125 | | ns |
| | | | 4.5V | 20 | | 30 | | 25 | | |
| | | | 6V | 17 | | 25 | | 21 | | |
| | | $\overline{PRE}$ or $\overline{CLR}$ inactive | 2V | 100 | | 150 | | 125 | | |
| | | | 4.5V | 20 | | 30 | | 25 | | |
| | | | 6V | 17 | | 25 | | 21 | | |
| $t_h$ | Hold time, data after CLK↓ | | 2V | 0 | | 0 | | 0 | | ns |
| | | | 4.5V | 0 | | 0 | | 0 | | |
| | | | 6V | 0 | | 0 | | 0 | | |

## 5.6 Switching Characteristics

over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Parameter Measurement Information)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | $T_A$ = 25°C | | | SN54HC112 | | SN74HC112 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | 2V | 5 | 10 | | 3.4 | | 4 | | MHz |
| | | | 4.5V | 25 | 50 | | 17 | | 20 | | |
| | | | 6V | 29 | 60 | | 20 | | 24 | | |
| $t_{pd}$ | $\overline{PRE}$ or $\overline{CLR}$ | Q or $\overline{Q}$ | 2V | | 54 | 165 | | 245 | | 205 | ns |
| | | | 4.5V | | 16 | 33 | | 49 | | 41 | |
| | | | 6V | | 13 | 28 | | 42 | | 35 | |
| | CLK | Q or $\overline{Q}$ | 2V | | 56 | 125 | | 185 | | 155 | |
| | | | 4.5V | | 16 | 25 | | 37 | | 31 | |
| | | | 6V | | 13 | 21 | | 31 | | 26 | |
| $t_t$ | | Q or $\overline{Q}$ | 2V | | 29 | 75 | | 110 | | 95 | ns |
| | | | 4.5V | | 9 | 15 | | 22 | | 19 | |
| | | | 6V | | 8 | 13 | | 19 | | 16 | |

## 5.7 Operating Characteristics

$T_A$ = 25°C

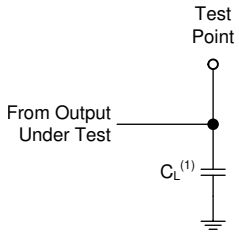
| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load | 35 | pF |

## 6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, $Z_O$ = 50Ω, $t_t$ < 6ns.

For clock inputs, $f_{max}$ is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.




(1) $C_L$ includes probe and test-fixture capacitance.

**Figure 6-1. Load Circuit for Push-Pull Outputs**

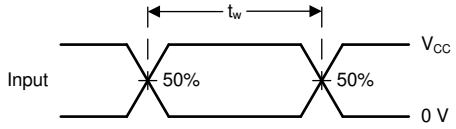



**Figure 6-2. Voltage Waveforms, Standard CMOS Inputs Pulse Duration**

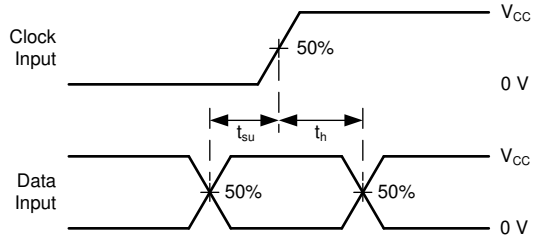
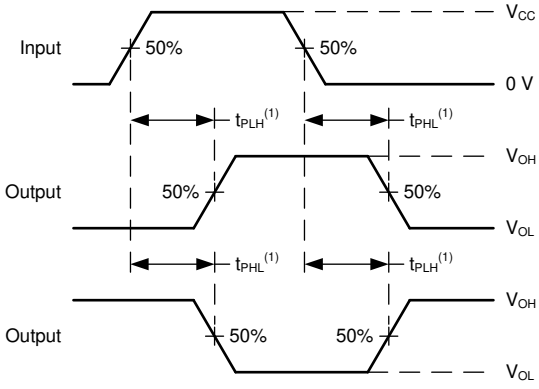
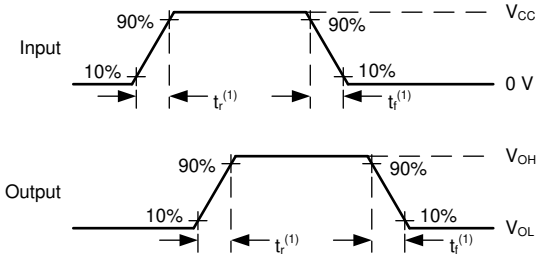



**Figure 6-3. Voltage Waveforms, Standard CMOS Inputs Setup and Hold Times**




(1) The greater between $t_{PLH}$ and $t_{PHL}$ is the same as $t_{pd}$.

**Figure 6-4. Voltage Waveforms, Propagation Delays for Standard CMOS Inputs**




(1) The greater between $t_r$ and $t_f$ is the same as $t_t$.

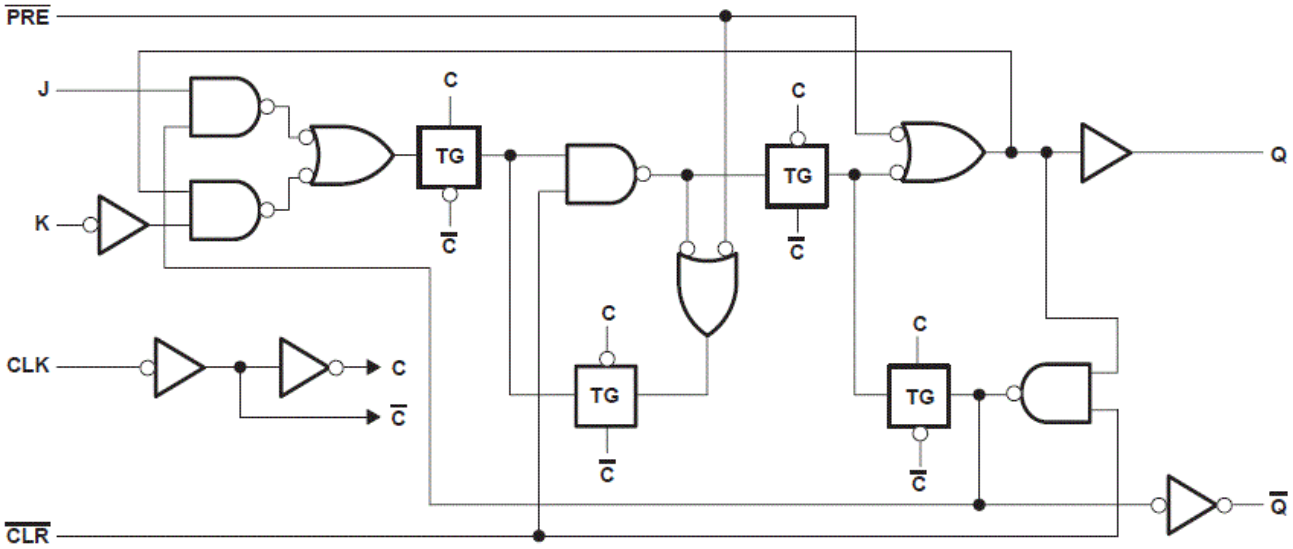
**Figure 6-5. Voltage Waveforms, Input and Output Transition Times for Standard CMOS Inputs**

# 7 Detailed Description

## 7.1 Overview

The SNx4HC112 devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) inputs sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not directly related to the fall time of the CLK pulse. Following the hold-time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops perform as toggle flip-flops by tying J and K high.

## 7.2 Functional Block Diagram




## 7.3 Device Functional Modes

**Table 7-1. Function Table**

| INPUTS | | | | | OUTPUTS | |
|---|---|---|---|---|---|---|
| $\overline{PRE}$ | $\overline{CLR}$ | CLK | J | K | Q | $\overline{Q}$ |
| L | H | X | X | X | H | H |
| H | L | X | X | X | L | H |
| L | L | X | X | X | H(1) | H(1) |
| H | H | ↓ | L | L | $Q_0$ | $\overline{Q}_0$ |
| H | H | ↓ | H | L | H | L |
| H | H | ↓ | L | H | L | H |
| H | H | ↓ | H | H | Toggle | |
| H | H | H | X | X | $Q_0$ | $\overline{Q}_0$ |

(1) This configuration is non stable; that is, it does not persist when either $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

# 8 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 8.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each $V_{CC}$ terminal should have a good bypass capacitor to prevent power disturbance. A 0.1µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 8.2 Layout

### *8.2.1 Layout Guidelines*

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or $V_{CC}$, whichever makes more sense for the logic function or is more convenient.

# 9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

## 9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.5 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision H (June 2022) to Revision I (September 2024) | Page |
|---|---|
| • Updated the *Device Information* table to include package lead frame and body size | 1 |
| • Changed $V_{CC}$ unit from: mA to: V in the *Absolute Maximum Ratings* section | 3 |

| Changes from Revision G (February 2022) to Revision H (June 2022) | Page |
|---|---|
| • Junction-to-ambient thermal resistance values increased. D was 73 is now 117.2, N was 67 is now 89.1 | 4 |

# 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| 84088012A | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 84088012A SNJ54HC 112FK |
| 8408801EA | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8408801EA SNJ54HC112J |
| 8408801FA | Active | Production | CFP (W) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8408801FA SNJ54HC112W |
| JM38510/65305BEA | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 65305BEA |
| JM38510/65305BEA.A | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 65305BEA |
| M38510/65305BEA | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 65305BEA |
| SN54HC112J | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SN54HC112J |
| SN54HC112J.A | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SN54HC112J |
| SN74HC112D | Obsolete | Production | SOIC (D) \| 16 | - | - | Call TI | Call TI | -40 to 85 | HC112 |
| SN74HC112DR | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 85 | HC112 |
| SN74HC112DR.A | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC112 |
| SN74HC112DRG4 | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC112 |
| SN74HC112DRG4.A | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC112 |
| SN74HC112DT | Obsolete | Production | SOIC (D) \| 16 | - | - | Call TI | Call TI | -40 to 85 | HC112 |
| SN74HC112N | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | SN74HC112N |
| SN74HC112N.A | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | SN74HC112N |
| SNJ54HC112FK | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 84088012A SNJ54HC 112FK |
| SNJ54HC112FK.A | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 84088012A SNJ54HC 112FK |
| SNJ54HC112J | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8408801EA SNJ54HC112J |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| SNJ54HC112J.A | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8408801EA SNJ54HC112J |
| SNJ54HC112W | Active | Production | CFP (W) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8408801FA SNJ54HC112W |
| SNJ54HC112W.A | Active | Production | CFP (W) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8408801FA SNJ54HC112W |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.



**OTHER QUALIFIED VERSIONS OF SN54HC112, SN74HC112 :**

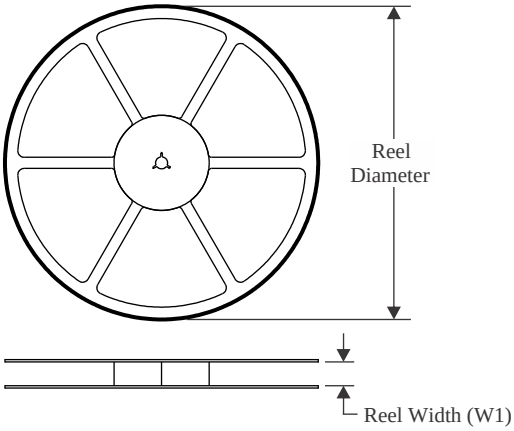
- Catalog : SN74HC112
- Military : SN54HC112

NOTE: Qualified Version Definitions:

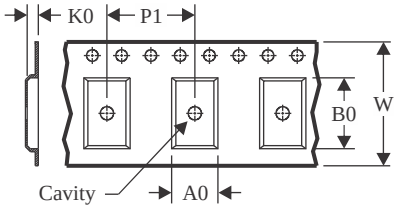
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

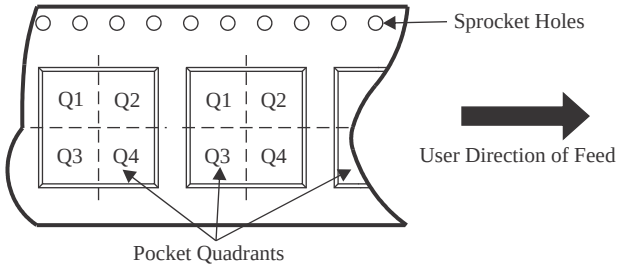



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

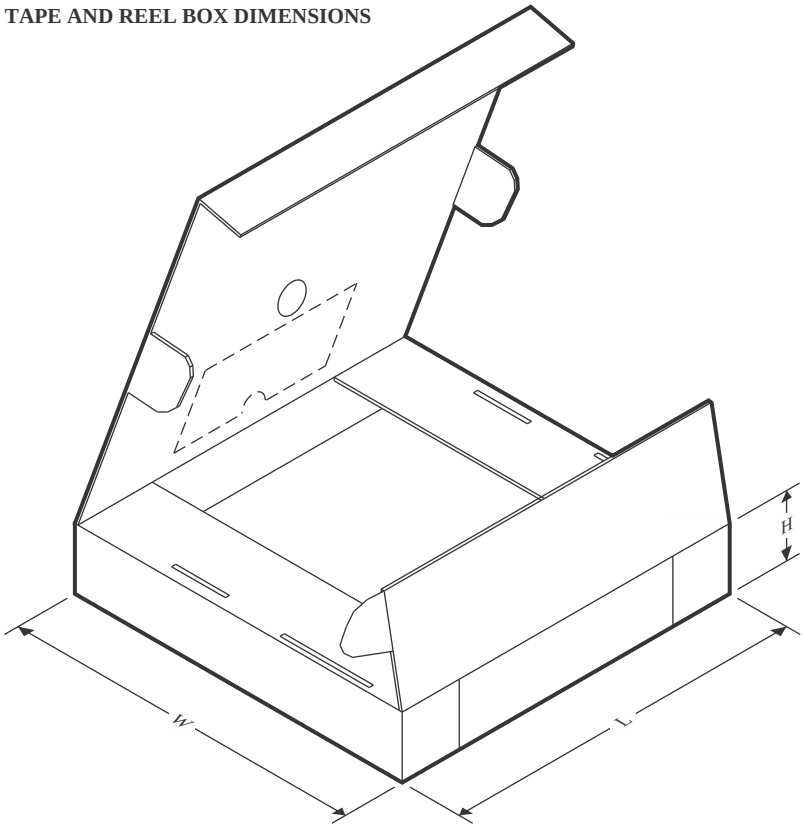
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74HC112DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HC112DRG4 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |

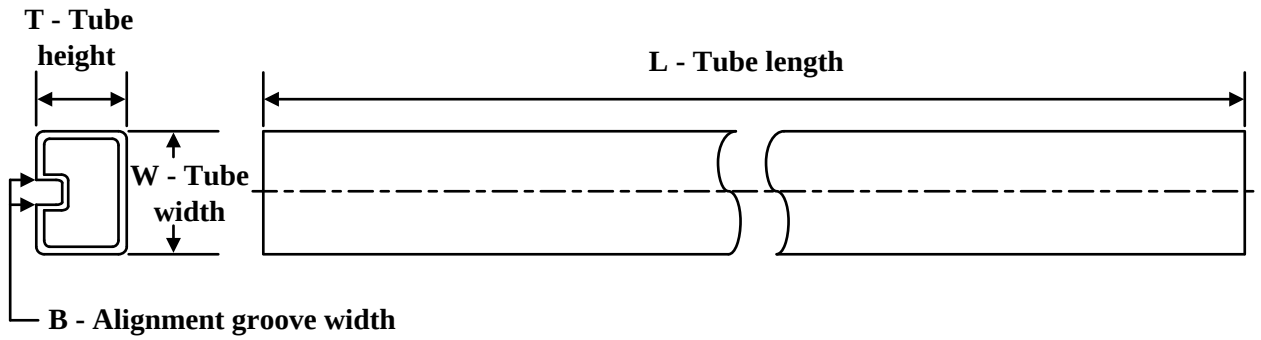
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74HC112DR | SOIC | D | 16 | 2500 | 353.0 | 353.0 | 32.0 |
| SN74HC112DRG4 | SOIC | D | 16 | 2500 | 353.0 | 353.0 | 32.0 |

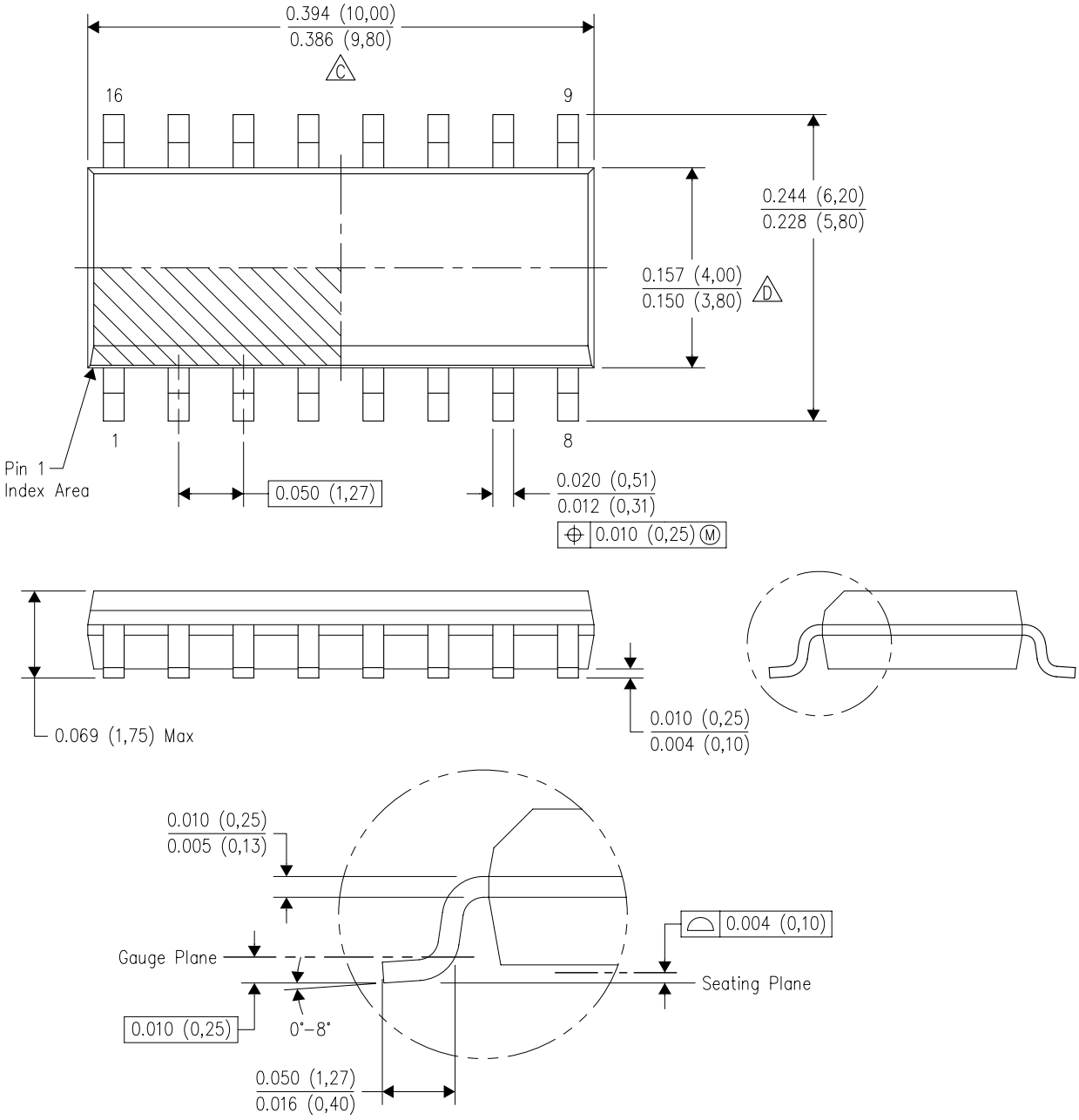
## TUBE




*All dimensions are nominal

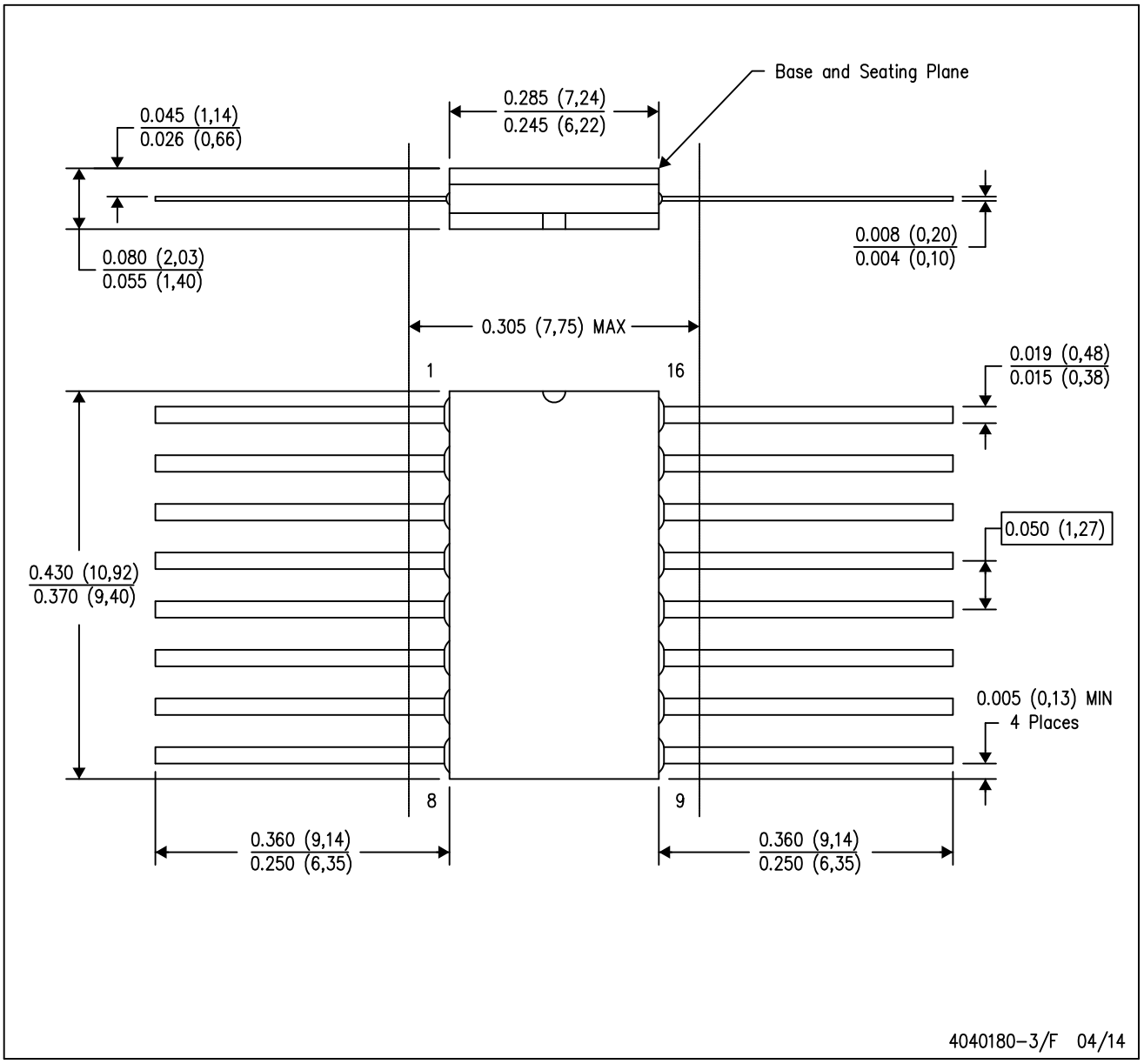
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| 84088012A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| 8408801FA | W | CFP | 16 | 25 | 506.98 | 26.16 | 6220 | NA |
| SN74HC112N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HC112N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HC112N.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HC112N.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SNJ54HC112FK | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54HC112FK.A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54HC112W | W | CFP | 16 | 25 | 506.98 | 26.16 | 6220 | NA |
| SNJ54HC112W.A | W | CFP | 16 | 25 | 506.98 | 26.16 | 6220 | NA |

D (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

W (R–GDFP–F16) CERAMIC DUAL FLATPACK




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP2–F16

# GENERIC PACKAGE VIEW

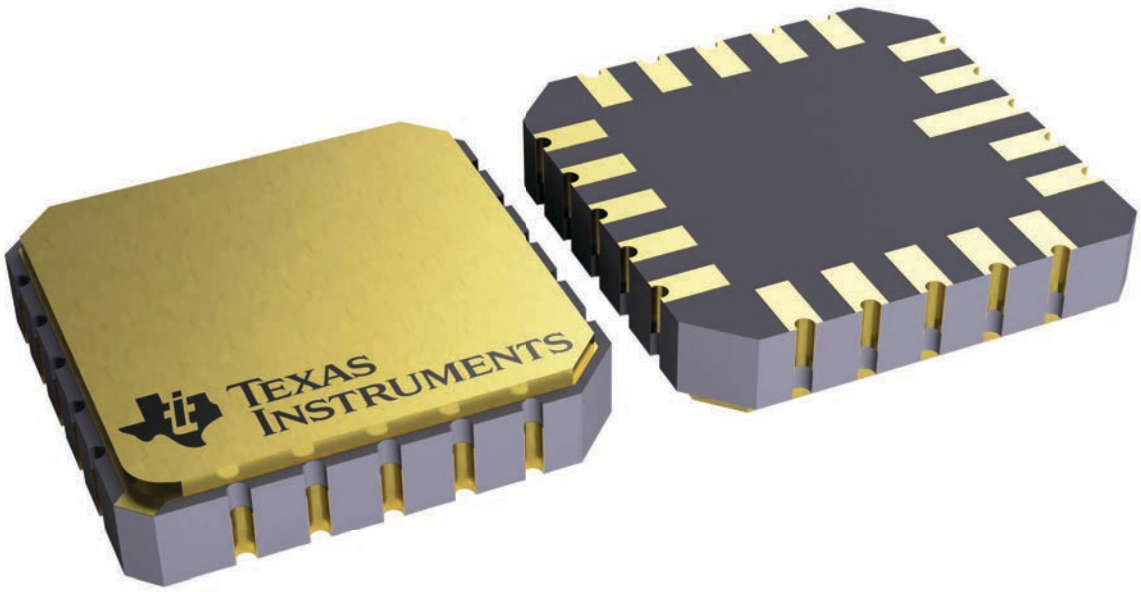
## FK 20

## LCCC - 2.03 mm max height

**8.89 x 8.89, 1.27 mm pitch**

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

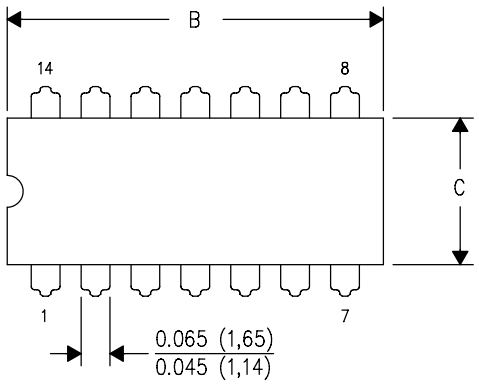



4229370VA\

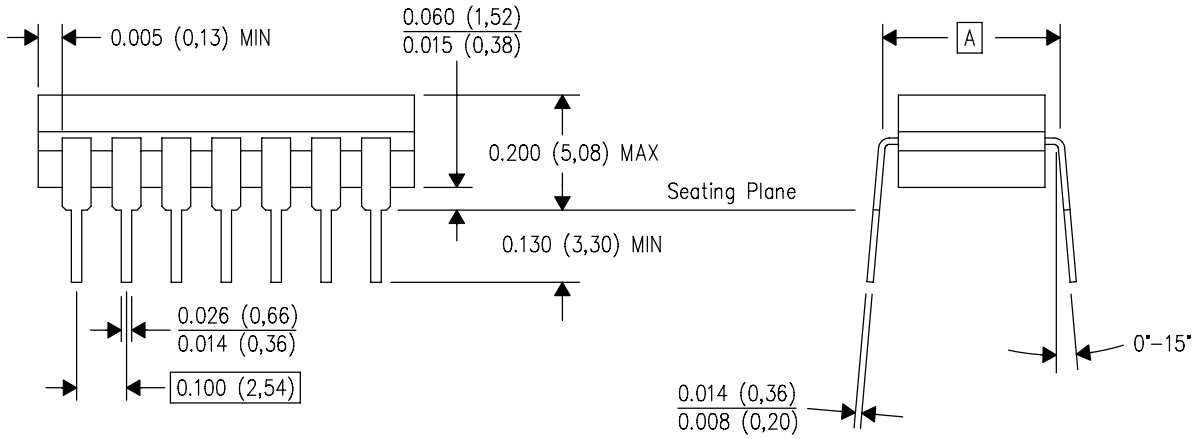
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



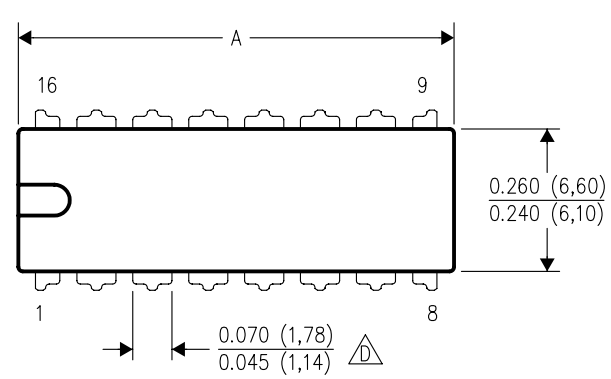

4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

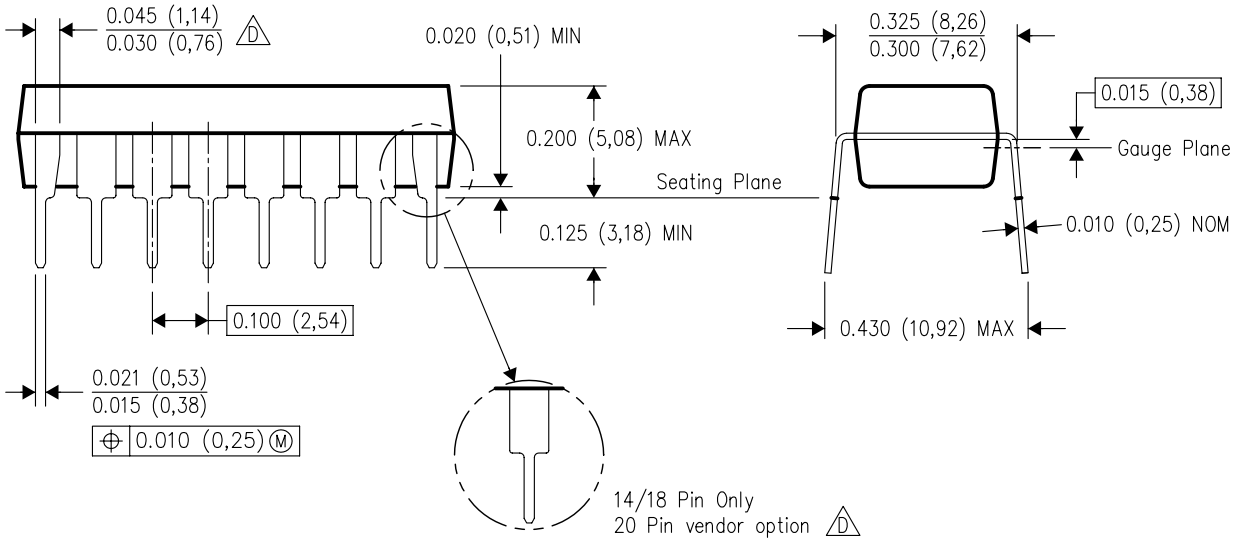
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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