

SN54HC688, SN74HC688 8-Bit Identity Comparators

1 Features

- Wide operating voltage range of 2 V to 6 V
- High-current outputs drive up to 10 LSTTL loads
- Low power consumption, 80- μ A max I_{CC}
- Typical $t_{pd} = 14$ ns
- ± 4 -mA output drive at 5 V
- Low input current of 1 μ A max
- Compare two 8-bit words

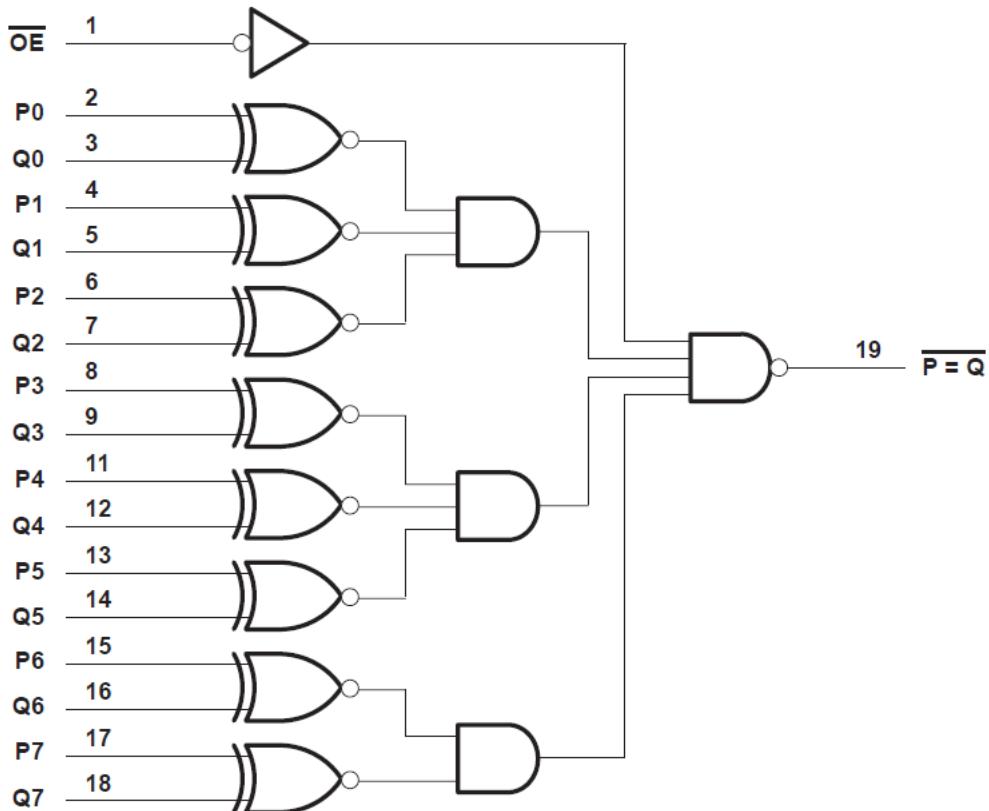
2 Description

These identity comparators perform comparisons of two 8-bit binary or BCD words. An output-enable (\overline{OE}) input may be used to force the output to the high level.

Device Information

PART NUMBER	PACKAGE ⁽¹⁾	BODY SIZE (NOM)
SN74HC688DW	SOIC (20)	12.80 mm \times 7.50 mm
SN74HC688N	PDIP (20)	25.40 mm \times 6.35 mm
SN74HC688PWR	TSSOP (20)	6.50 mm \times 4.40 mm
SN54HC688J	CDIP (20)	26.92 mm \times 6.92 mm
SNJ54HC688FK	LCCC (20)	8.89 mm \times 8.45 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Functional Block Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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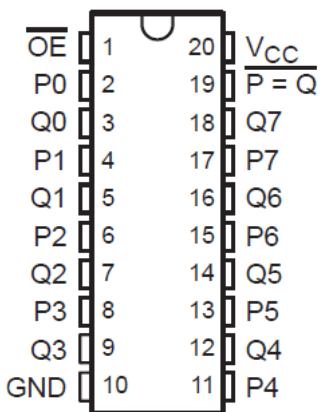
3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

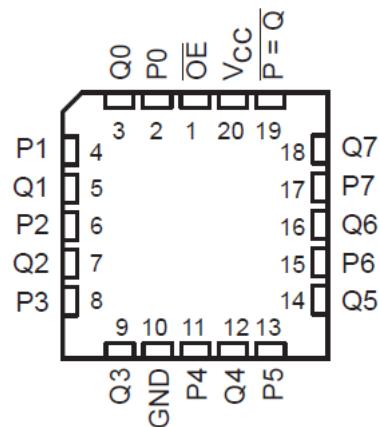
Changes from Revision E (February 2022) to Revision F (May 2022)	Page
• Junction-to-ambient thermal resistance values increased. DW was 58 is now 109.1, N was 69 is now 84.6, PW was 83 is now 131.8.....	4

Changes from Revision D (August 2003) to Revision E (February 2022)	Page
• Updated the numbering, formatting, tables, figures, and cross-references throughout the document to reflect modern data sheet standards.....	1

4 Pin Configuration and Functions



J, DW, N or PW package
20-Pin CDIP, SOIC, PDIP, TSSOP
Top View



FK Package
20-Pin LCCC
Top View

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	7	V
I _{IK}	Input clamp current ⁽²⁾	V _I < 0 or V _I > V _{CC}		±20	mA
I _{OK}	Output clamp current ⁽²⁾	V _O < 0 or V _O > V _{CC}		±20	mA
I _O	Continuous output current	V _O = 0 to V _{CC}		±25	mA
	Continuous current through V _{CC} or GND			±50	mA
T _J	Junction temperature			150	°C
T _{stg}	Storage temperature range		-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 Recommended Operating Conditions⁽¹⁾

		SN54HC688			SN74HC688			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	2	5	6	2	5	6	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		1.5			V
		V _{CC} = 4.5 V	3.15		3.15			
		V _{CC} = 6 V	4.2		4.2			
V _{IL}	Low-level input voltage	V _{CC} = 2 V		0.5		0.5		V
		V _{CC} = 4.5 V		1.35		1.35		
		V _{CC} = 6 V		1.8		1.8		
V _I	Input voltage	0	V _{CC}		0	V _{CC}		V
V _O	Output voltage	0	V _{CC}		0	V _{CC}		V
t _l	Input transition (rise and fall) time	V _{CC} = 2 V		1000		1000		ns
		V _{CC} = 4.5 V		500		500		
		V _{CC} = 6 V		400		400		
T _A	Operating free-air temperature	-55		125	-40		85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

5.3 Thermal Information

THERMAL METRIC		DW (SOIC)	N (PDIP)	PW (TSSOP)	UNIT
		20 PINS	20 PINS	20 PINS	
R _{θJA}	Junction-to-ambient thermal resistance ⁽¹⁾	109.1	84.6	131.8	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	76	72.5	72.2	°C/W
R _{θJB}	Junction-to-board thermal resistance	77.6	65.3	82.8	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	51.5	55.3	21.5	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	77.1	65.2	82.4	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

5.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54HC688		SN74HC688		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = -20 µA	2 V	1.9	1.998	1.9		1.9		V
			4.5 V	4.4	4.499	4.4		4.4		
			6 V	5.9	5.999	5.9		5.9		
		I _{OH} = -4 mA	4.5 V	3.98	4.3	3.7		3.84		
		I _{OH} = -5.2 mA	6 V	5.48	5.8	5.2		5.34		
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 20 µA	2 V		0.002	0.1		0.1		V
			4.5 V		0.001	0.1		0.1		
			6 V		0.001	0.1		0.1		
		I _{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33
		I _{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33
I _I	V _I = V _{CC} or 0		6 V		±0.1	±100		±1000		nA
I _{CC}	V _I = V _{CC} or 0, I _O = 0		6 V			8		160		80 µA
C _i			2 V to 6 V		3	10		10		10 pF

5.5 Switching Characteristics

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see [Parameter Measurement Information](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			SN54HC688		SN74HC688		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	P or Q	P = Q	2 V		113	210		313		265	ns
			4.5 V		30	42		63		53	
			6 V		24	36		53		45	
	OE	P = Q	2 V		66	120		179		151	ns
			4.5 V		16	24		36		30	
			6 V		14	20		30		26	
t _t		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

5.6 Operating Characteristics

T_A = 25°C

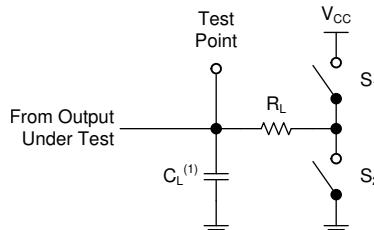
PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance	No load	40 pF

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_t < 6$ ns.

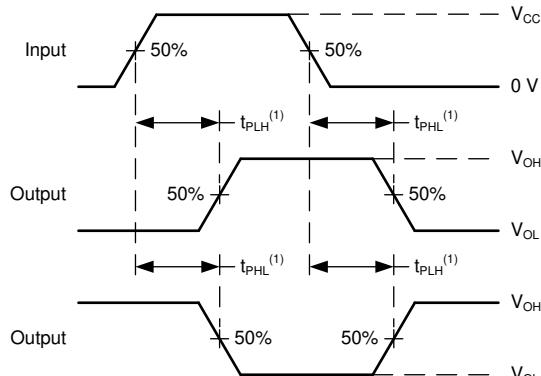
For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



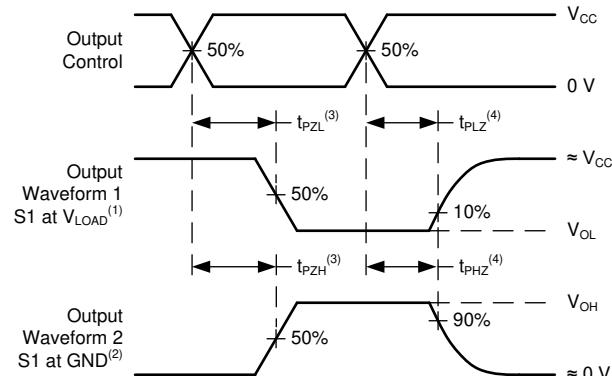
(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for 3-State Outputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd} .

Figure 6-2. Voltage Waveforms, Propagation Delays for Standard CMOS Inputs



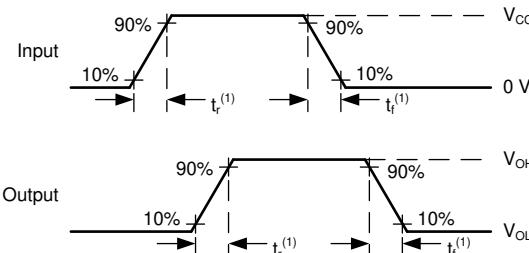
(1) S1 = CLOSED; S2 = OPEN.

(2) S1 = OPEN; S2 = CLOSED.

(3) t_{PLZ} and t_{PHZ} are the same as t_{dis} .

(4) t_{PLZ} and t_{PHZ} are the same as t_{en} .

Figure 6-3. Voltage Waveforms, Standard CMOS Inputs Propagation Delays



(1) The greater between t_r and t_f is the same as t_t .

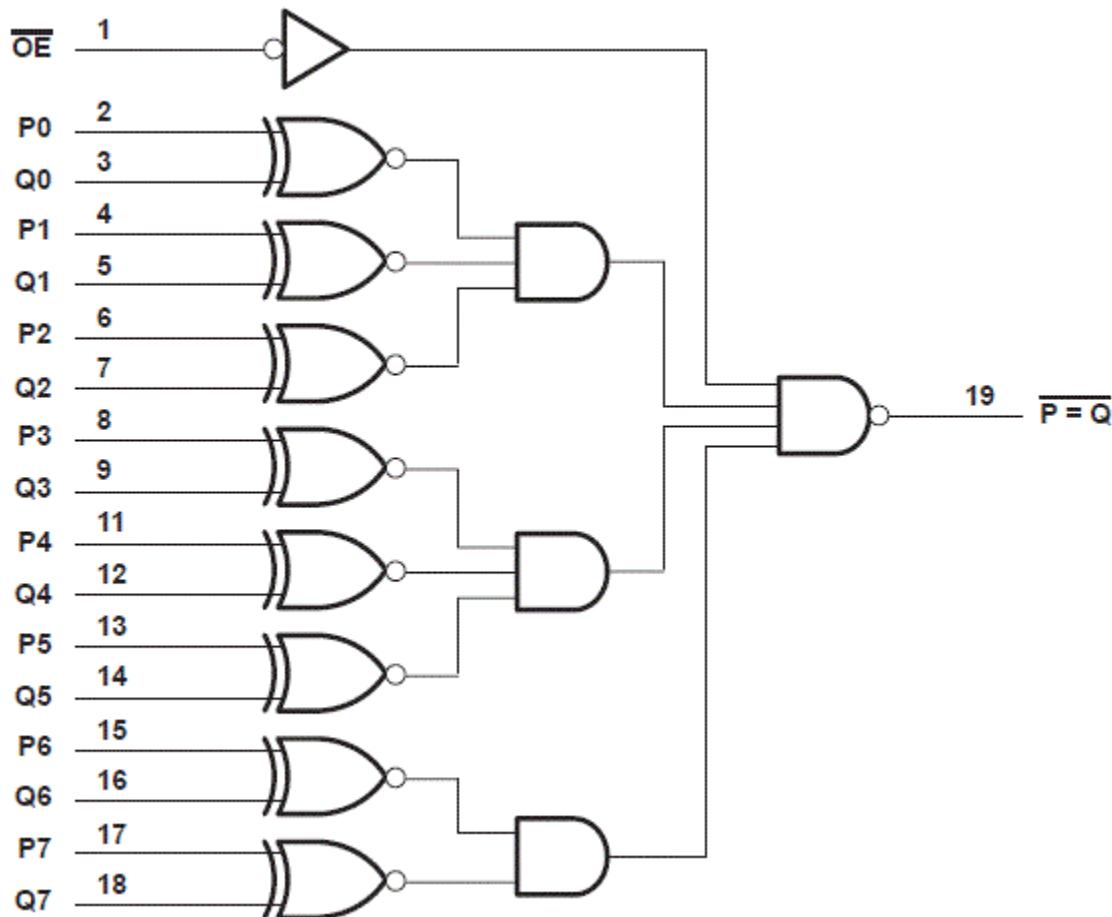
Figure 6-4. Voltage Waveforms, Input and Output Transition Times for Standard CMOS Inputs

7 Detailed Description

7.1 Overview

These identity comparators perform comparisons of two 8-bit binary or BCD words. An output-enable (\overline{OE}) input may be used to force the output to the high level.

7.2 Functional Block Diagram



7.3 Device Functional Modes

Table 7-1. Function Table

INPUTS		OUTPUT $\overline{P = Q}$
DATA P, Q	\overline{OE}	
P = Q	L	L
P > Q	X	H
P < Q	X	H
X	H	H

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-86818012A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 86818012A SNJ54HC 688FK
5962-8681801RA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8681801RA SNJ54HC688J
SN54HC688J	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HC688J
SN54HC688J.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HC688J
SN74HC688DW	Obsolete	Production	SOIC (DW) 20	-	-	Call TI	Call TI	-40 to 85	HC688
SN74HC688DWR	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC688
SN74HC688DWR.A	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC688
SN74HC688DWRE4	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC688
SN74HC688DWRG4	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC688
SN74HC688N	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC688N
SN74HC688N.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC688N
SN74HC688PWR	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC688
SN74HC688PWR.A	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC688
SN74HC688PWRE4	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC688
SN74HC688PWT	Obsolete	Production	TSSOP (PW) 20	-	-	Call TI	Call TI	-40 to 85	HC688
SNJ54HC688FK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 86818012A SNJ54HC 688FK
SNJ54HC688FK.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 86818012A SNJ54HC 688FK
SNJ54HC688J	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8681801RA SNJ54HC688J
SNJ54HC688J.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8681801RA SNJ54HC688J

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

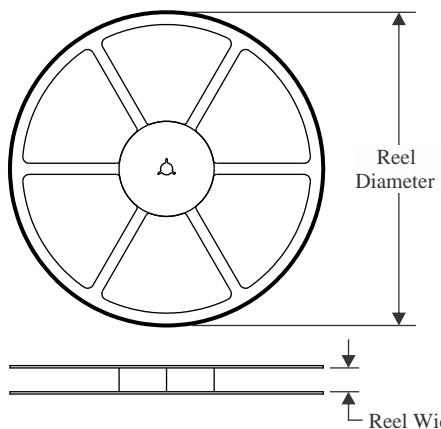
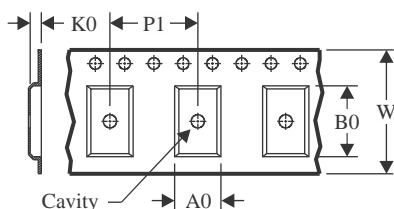
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54HC688, SN74HC688 :

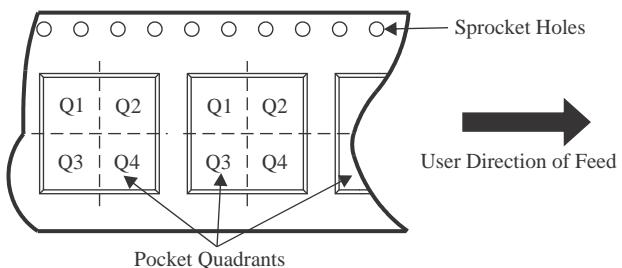
- Catalog : [SN74HC688](#)
- Military : [SN54HC688](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

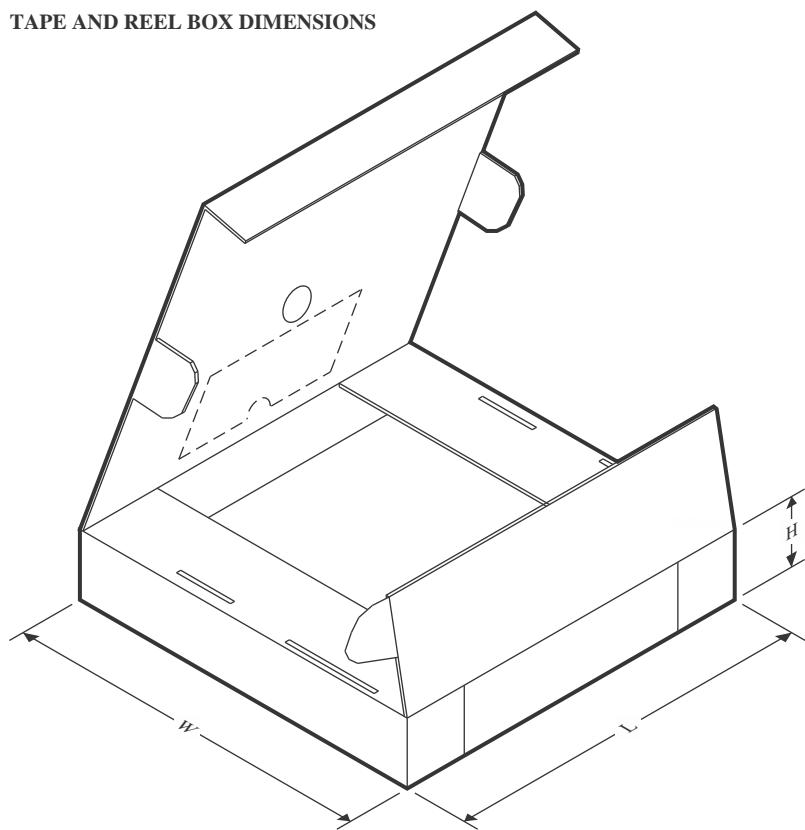
TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


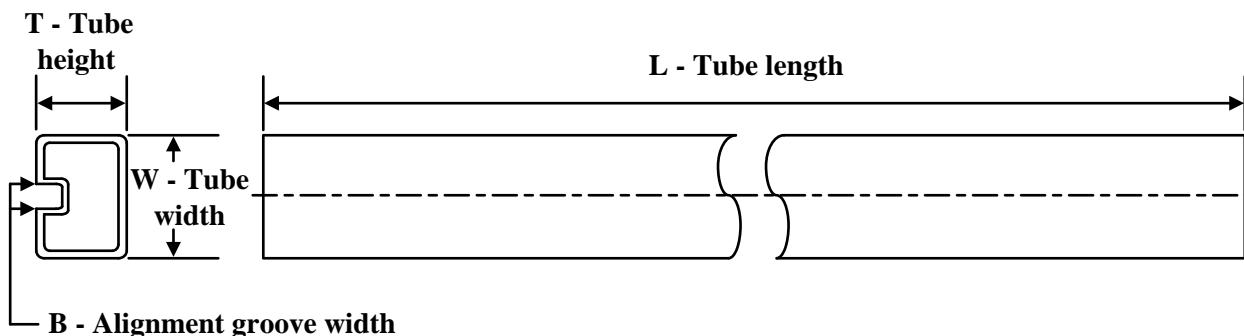
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC688DWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74HC688PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC688DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74HC688PWR	TSSOP	PW	20	2000	353.0	353.0	32.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μ m)	B (mm)
5962-86818012A	FK	LCCC	20	55	506.98	12.06	2030	NA
SN74HC688N	N	PDIP	20	20	506	13.97	11230	4.32
SN74HC688N.A	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54HC688FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54HC688FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA

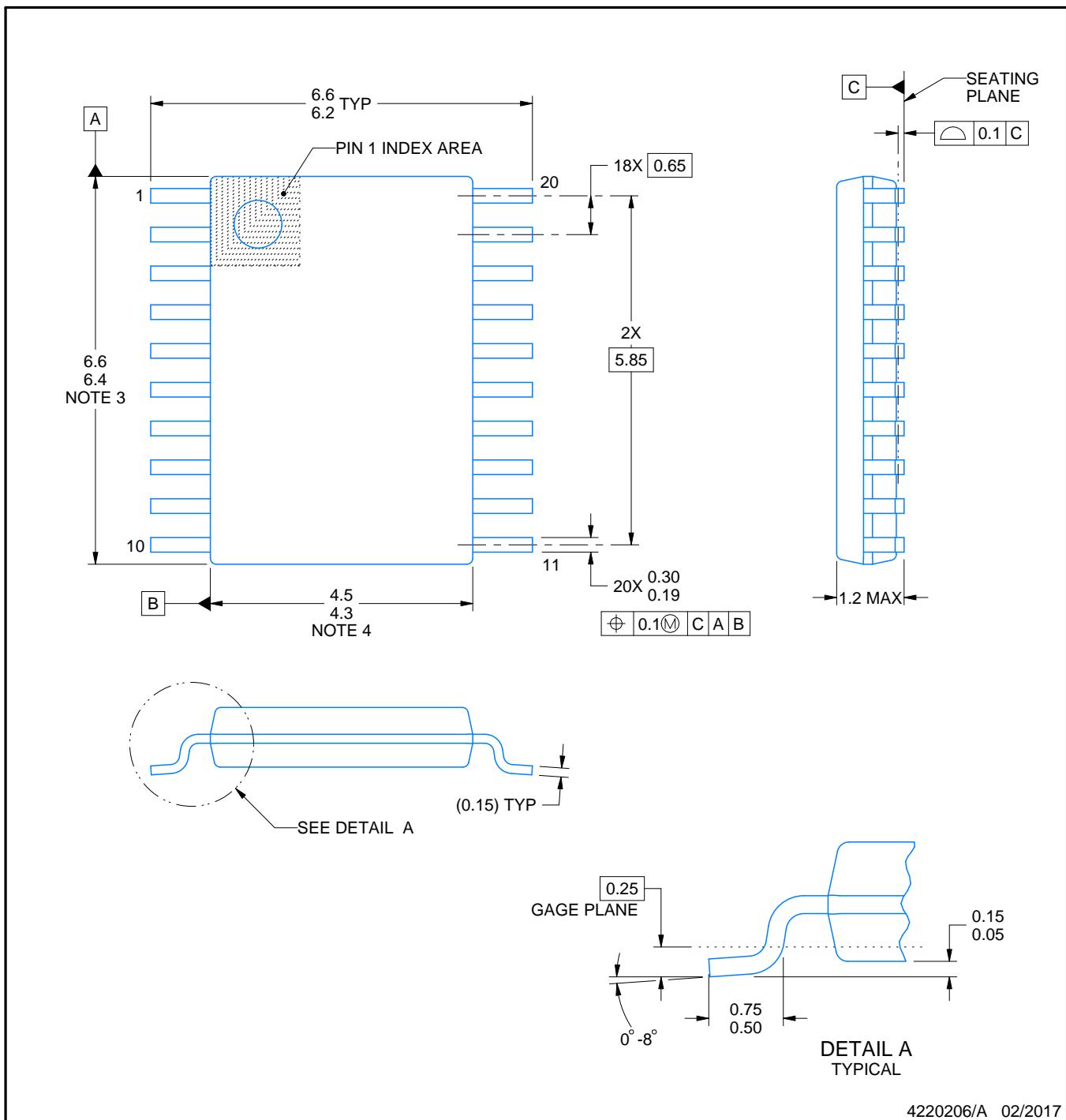
PACKAGE OUTLINE

PW0020A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

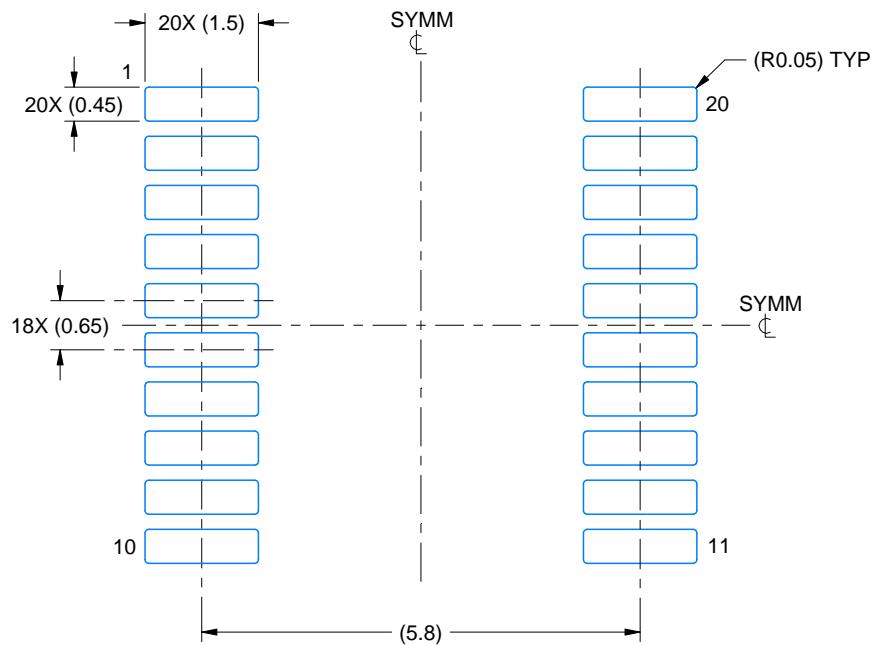
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

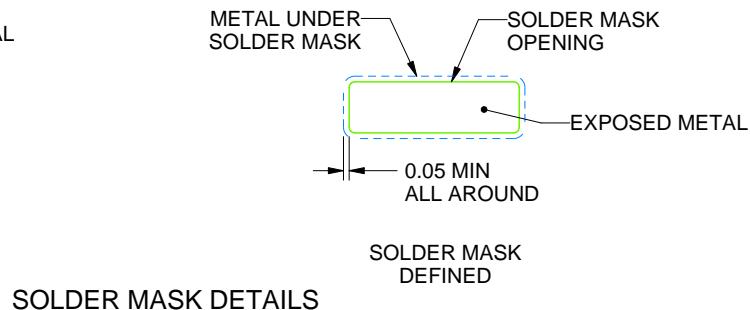
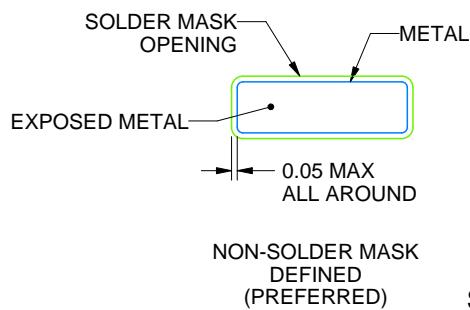
PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

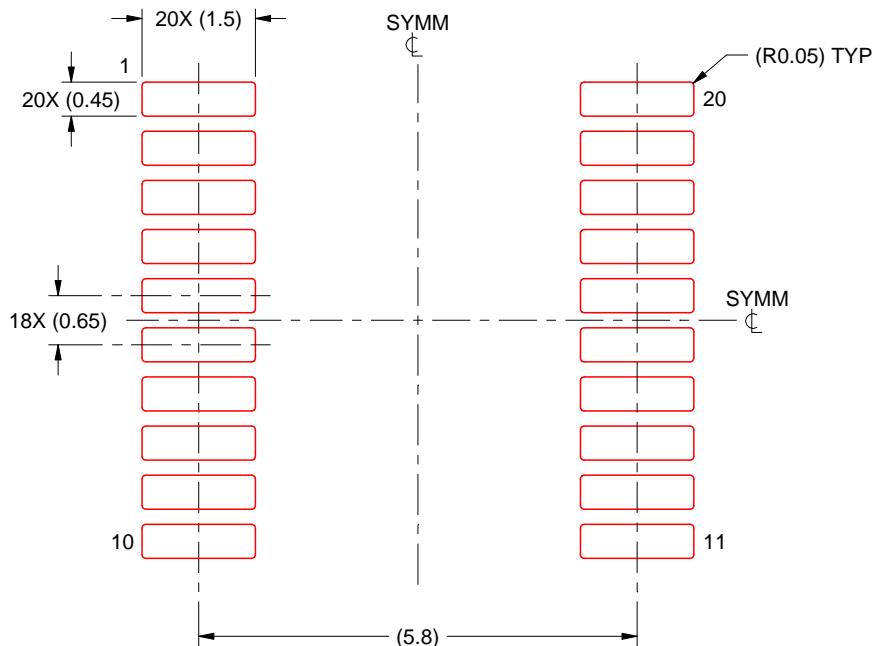
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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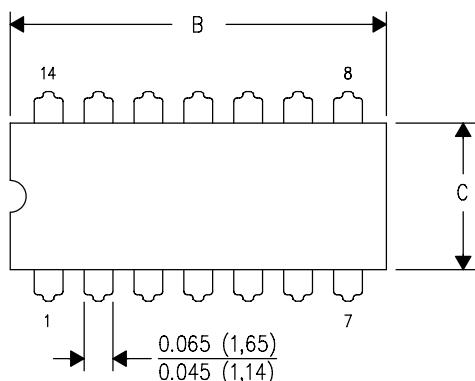
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

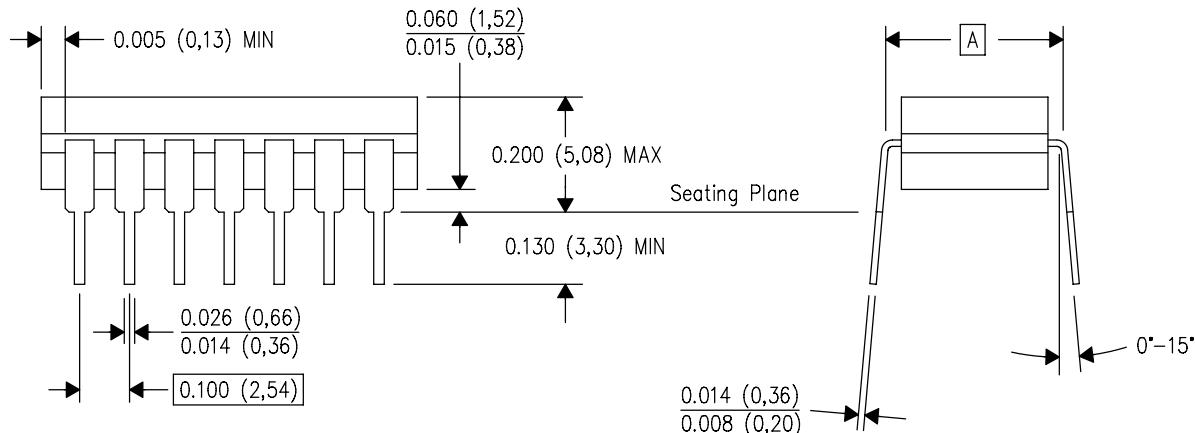
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



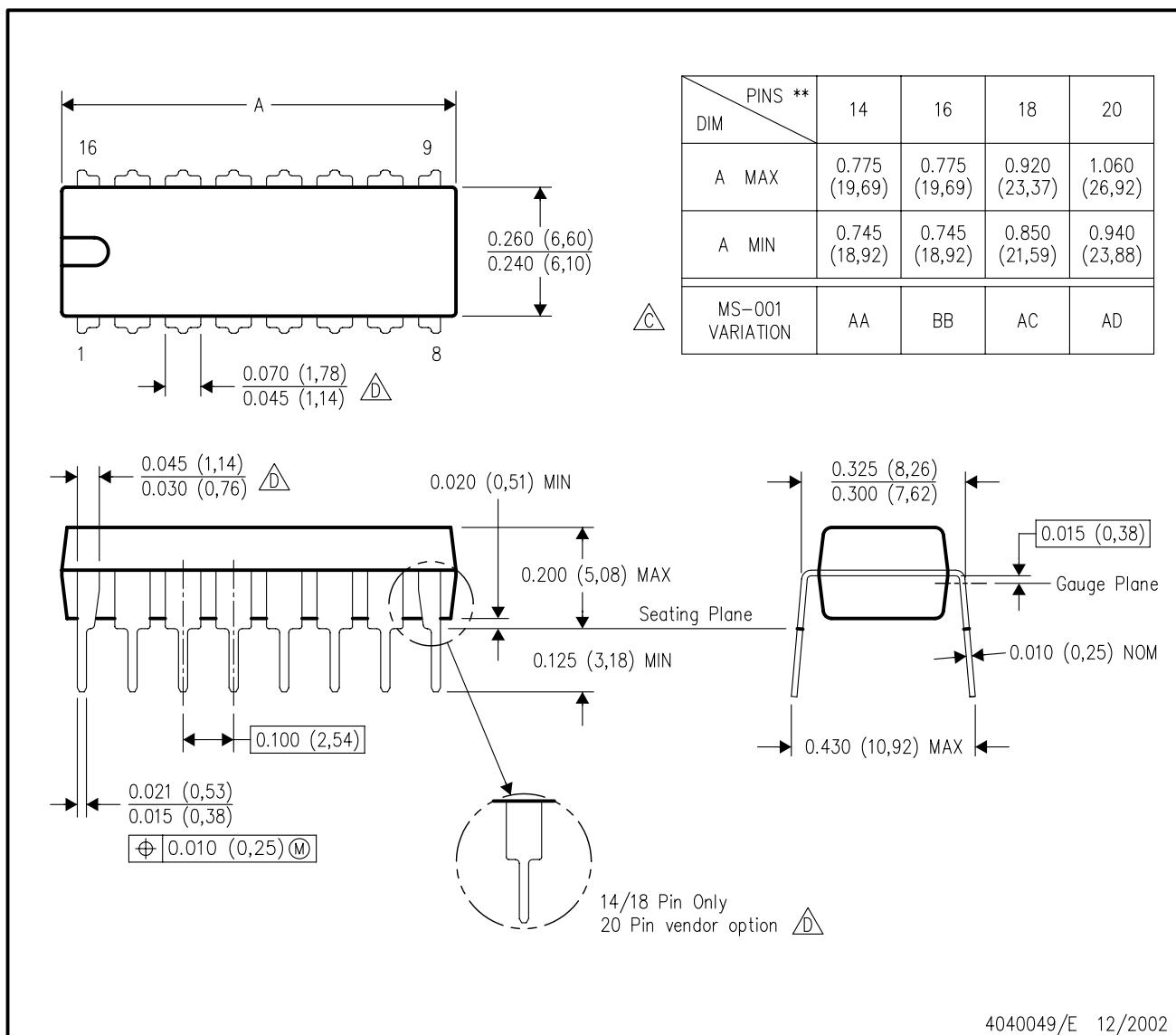
4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

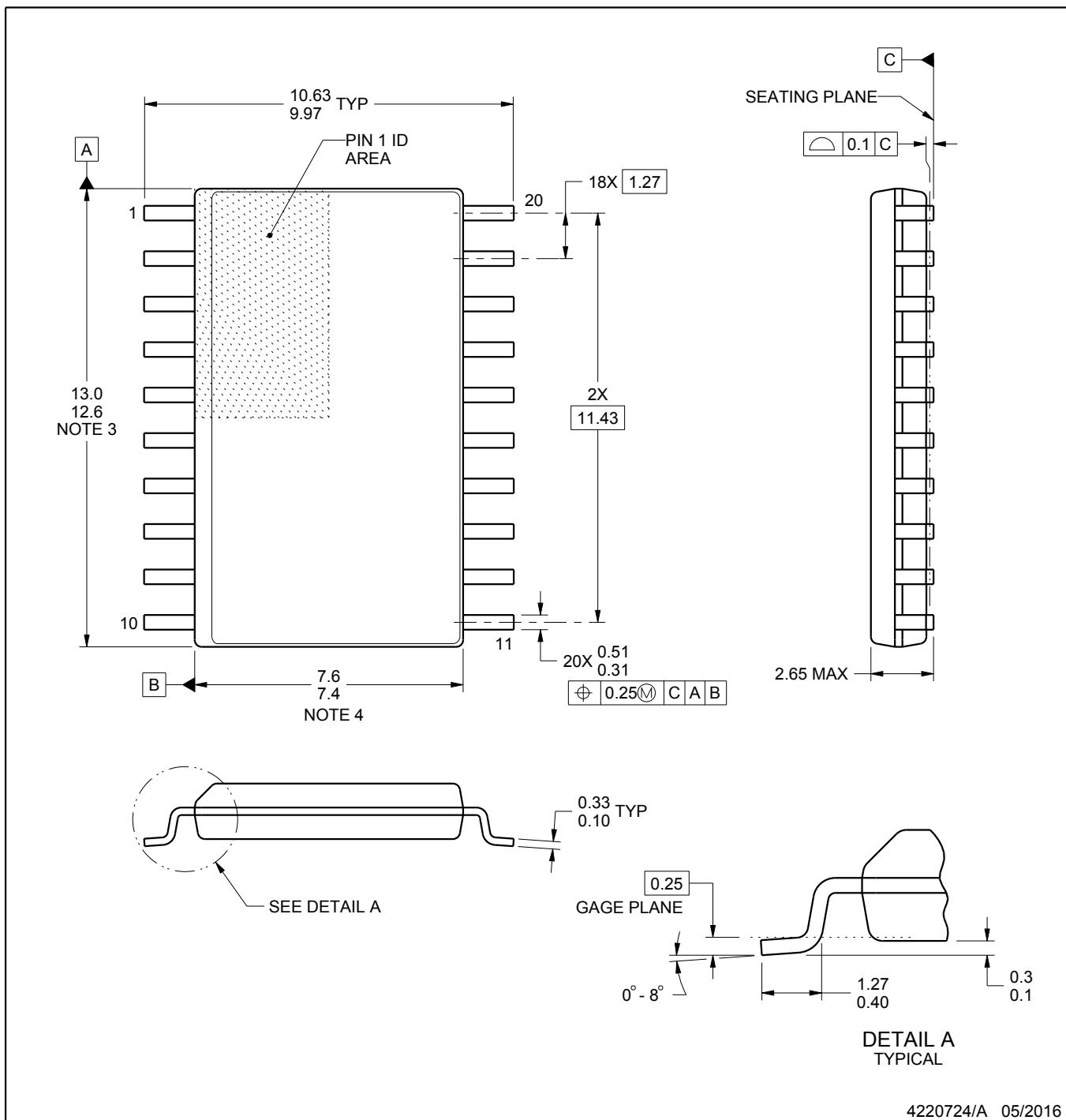
PACKAGE OUTLINE

DW0020A



SOIC - 2.65 mm max height

SOIC



NOTES:

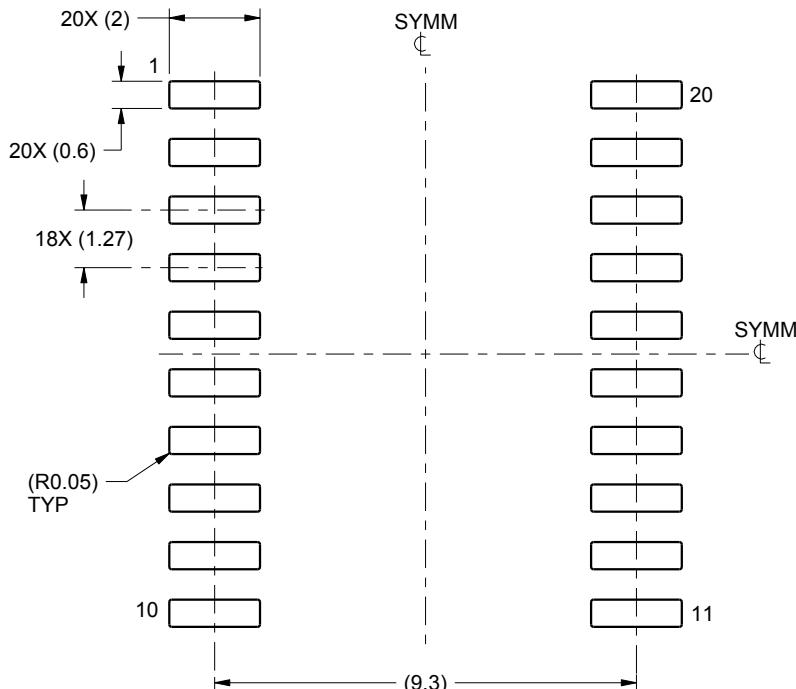
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

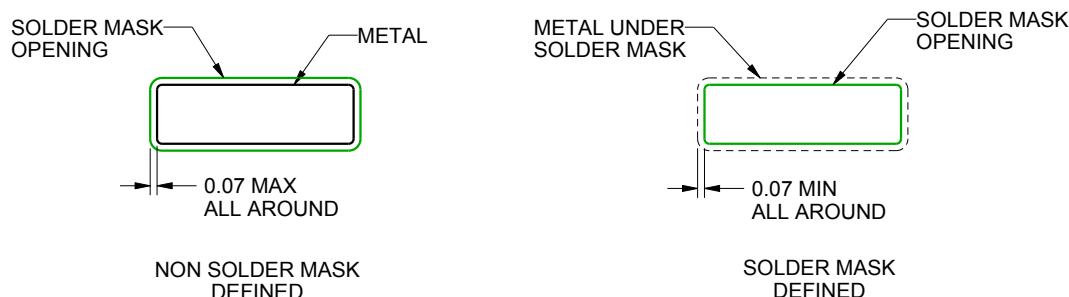
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

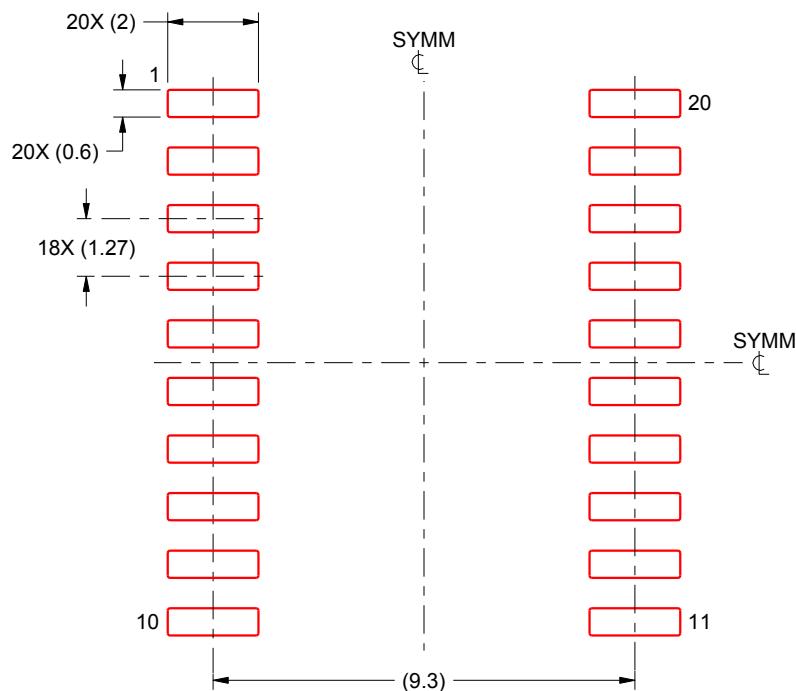
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

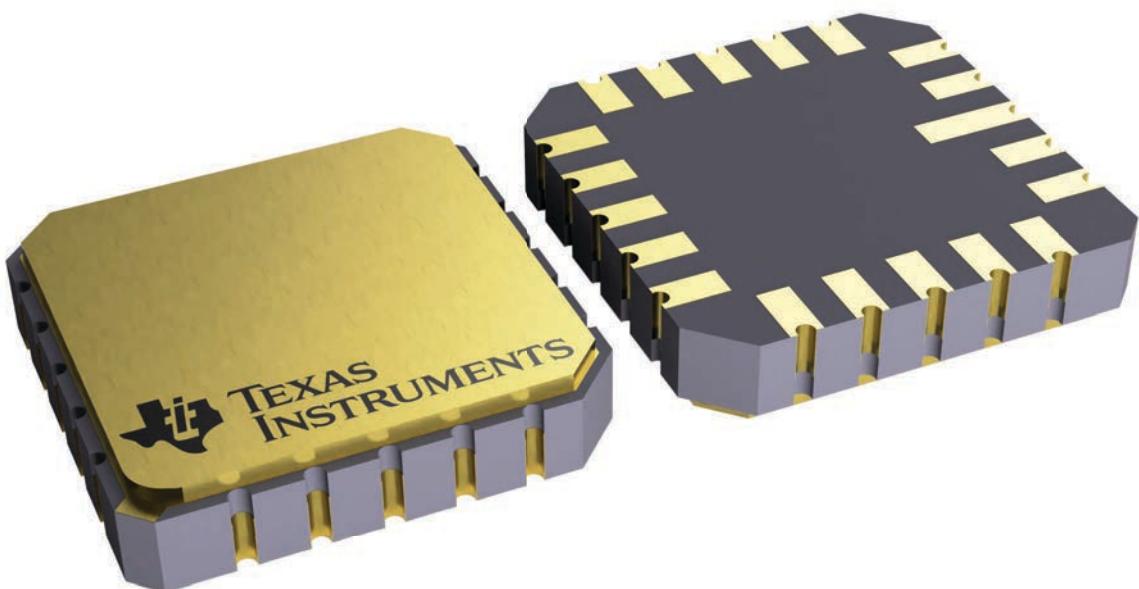
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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Last updated 10/2025