SN74HCS11 Triple 3-Input AND Gates With Schmitt-Trigger Inputs

1 Features

- Wide operating voltage range: 2V to 6V
- Schmitt-trigger inputs allow for slow or noisy input signals
- Low power consumption
  - Typical I_{CC} of 100nA
  - Typical input leakage current of ±100nA
- ±7.8mA output drive at 5V
- Extended ambient temperature range: –40°C to +125°C, T_A

2 Applications

- Combine power good signals
- Combine enable signals

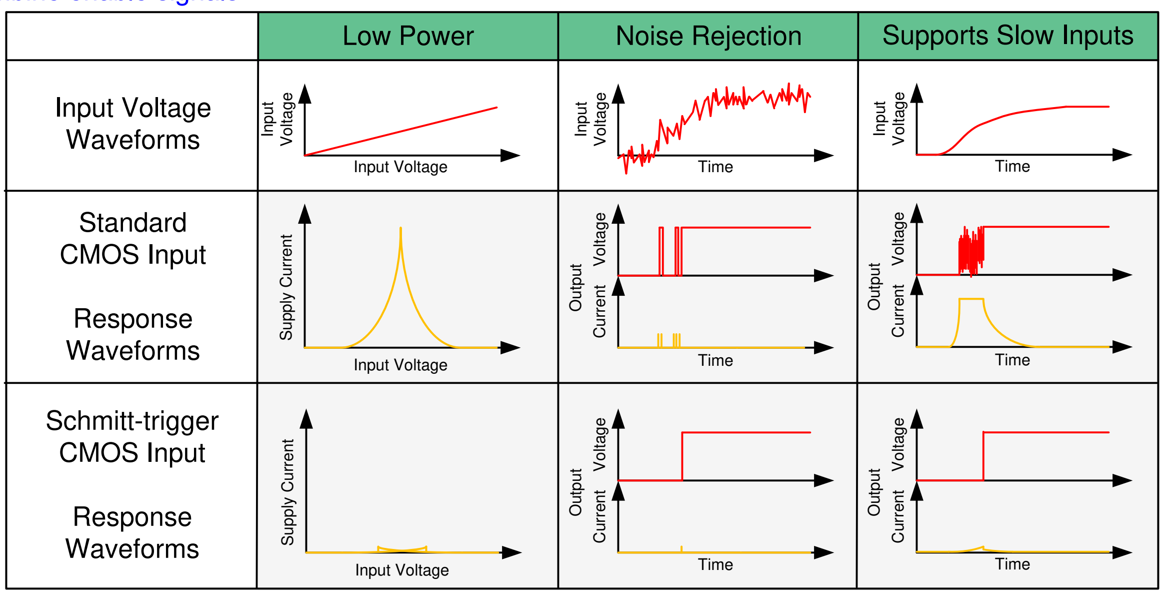
3 Description

This device contains three independent 3-input AND Gates with Schmitt-trigger inputs. Each gate performs the Boolean function Y = A ● B ● C in positive logic.

Package Information

PART NUMBER	PACKAGE[1]	PACKAGE SIZE[2]
SN74HCS11QDR	SOIC (14)	8.70mm × 3.90mm
SN74HCS11PWR	TSSOP (14)	5.00mm × 4.40mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Benefits of Schmitt-trigger Inputs

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4 Pin Configuration and Functions

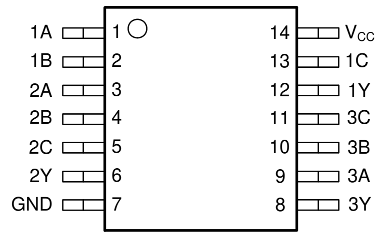


Figure 4-1. D or PW Package 14-Pin SOIC or TSSOP Top View

PIN		TYPE	DESCRIPTION
NAME	NO.		
1A	1	Input	Channel 1, Input A
1B	2	Input	Channel 1, Input B
1C	13	Input	Channel 1, Input C
1Y	12	Output	Channel 1, Output Y
2A	3	Input	Channel 2, Input A
2B	4	Input	Channel 2, Input B
2C	5	Input	Channel 2, Input C
2Y	6	Output	Channel 2, Output Y
3A	9	Input	Channel 3, Input A
3B	10	Input	Channel 3, Input B
3C	11	Input	Channel 3, Input C
3Y	8	Output	Channel 3, Output Y
GND	7	—	Ground
V_{CC}	14	—	Positive Supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
I_{IK}	Input clamp current[(2)]	$V_I < –0.5$ or $V_I > V_{CC} + 0.5$		±20	mA
I_{OK}	Output clamp current[(2)]	$V_O < –0.5$ or $V_O > V_{CC} + 0.5$		±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±35	mA
	Continuous current through V_{CC} or GND			±70	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	±1500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2	5	6	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
Δt/Δv	Input transition rise and fall rate			Unlimited	ns/V
T_A	Ambient temperature	–40		125	°C

5.4 Thermal Information

THERMAL METRIC[(1)]		SN74HCS11 PW (TSSOP) 14 PINS	SN74HCS11 D (SOIC) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	151.7	133.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	79.4	89.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	94.7	89.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	25.2	45.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	94.1	89.1	°C/W

THERMAL METRIC[(1)]		SN74HCS11 PW (TSSOP) 14 PINS	SN74HCS11 D (SOIC) 14 PINS	UNIT
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

over operating free-air temperature range; typical ratings measured at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
V_{T+}	Positive switching threshold			2V	1.18		1.3	V
				4.5V	2.39		2.58	
				6V	3.11		3.32	
V_{T-}	Negative switching threshold			2V	0.61		0.66	V
				4.5V	1.31		1.42	
				6V	1.72		1.87	
ΔV_T	V_{T+} - V_{T-}			2V	0.55		0.67	V
				4.5V	1.04		1.21	
				6V	1.34		1.49	
V_{OH}	High-level output voltage	$V_I = V_{IH}$ or V_{IL}	I_{OH} = -20µA	2V to 6V	V_{CC} - 0.1	V_{CC} - 0.002		V
			I_{OH} = -6mA	4.5V	4.0	4.3		
			I_{OH} = -7.8mA	6V	5.4	5.75		
V_{OL}	Low-level output voltage	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20µA	2V to 6V		0.002	0.1	V
			I_{OL} = 4mA	4.5V		0.18	0.30	
			I_{OL} = 7.8mA	6V		0.22	0.33	
I_I	Input leakage current	$V_I = V_{CC}$ or 0		6V		±100	±1000	nA
I_{CC}	Supply current	$V_I = V_{CC}$ or 0, I_O = 0		6V		0.1	2	µA
C_i	Input capacitance			2V to 6V			5	pF
C_{pd}	Power dissipation capacitance per gate	No load		2V to 6V		10		pF

5.6 Switching Characteristics

over operating free-air temperature range; typical ratings measured at T_A = 25°C (unless otherwise noted). See Section 6.

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	TYP	MAX	UNIT
t_{pd}	Propagation delay	A or B or C	Y	2V		13	40	ns
				4.5V		6	17	
				6V		5	16	
t_t	Transition-time		Y	2V		9	17	ns
				4.5V		5	8	
				6V		4	7	

5.7 Typical Characteristics

$T_A = 25°C$

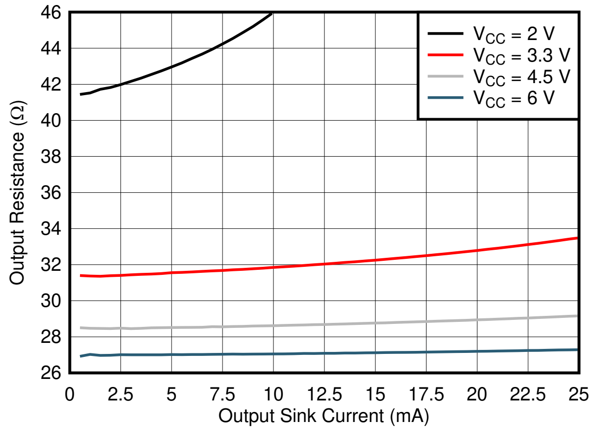


Figure 5-1. Output driver resistance in Low state

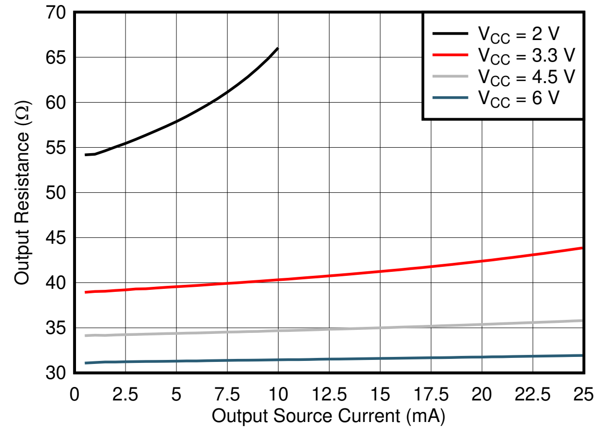


Figure 5-2. Output driver resistance in High state

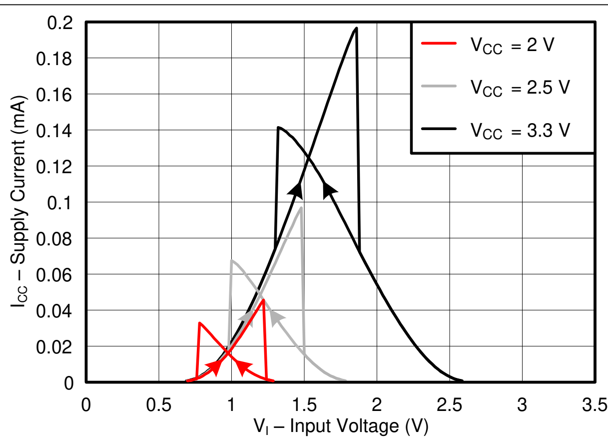


Figure 5-3. Typical supply current versus input voltage across common supply values (2V to 3.3V)

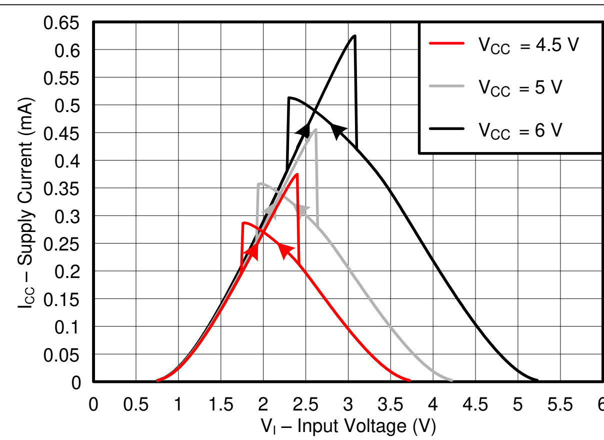
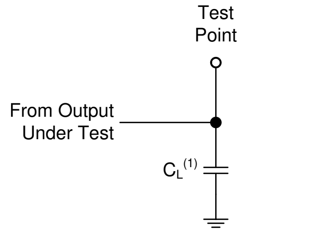


Figure 5-4. Typical supply current versus input voltage across common supply values (4.5V to 6V)

6 Parameter Measurement Information

- Phase relationships between waveforms are chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50Ω, t_t < 2.5ns.
- The outputs are measured one at a time, with one input transition per measurement.



A. C_L= 50pF and includes probe and jig capacitance.

Figure 6-1. Load Circuit

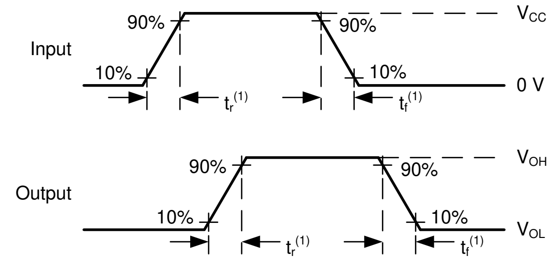
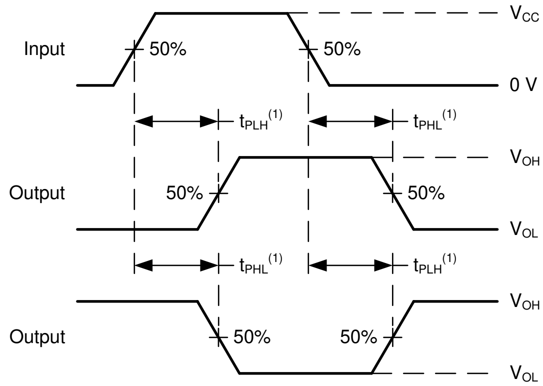


Figure 6-2. Voltage Waveforms Transition Times



A. The maximum between t_{PLH} and T_{PHL} is used for t_{pd}.

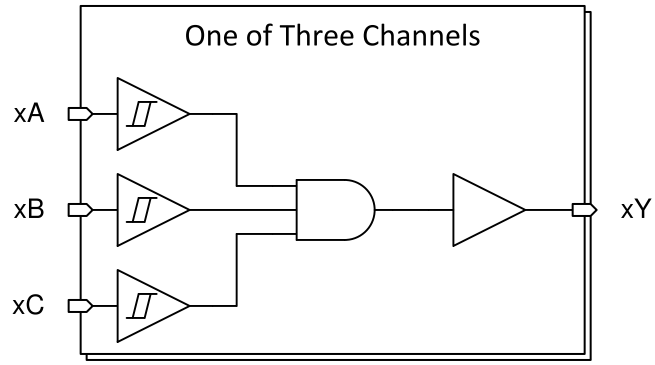
Figure 6-3. Voltage Waveforms Propagation Delays

7 Detailed Description

7.1 Overview

This device contains three independent 3-input AND Gates with Schmitt-trigger inputs. Each gate performs the Boolean function Y = A ● B ● C in positive logic.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Balanced CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to over-current. The electrical and thermal limits defined in the *Section 5.1* must be followed at all times.

7.3.2 CMOS Schmitt-Trigger Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Section 5.5*. The worst case resistance is calculated with the maximum input voltage, given in the *Section 5.1*, and the maximum input leakage current, given in the *Section 5.5*, using ohm's law (R = V ÷ I).

The Schmitt-trigger input architecture provides hysteresis as defined by ΔV_T in the *Section 5.5*, which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs slowly will also increase dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see Understanding Schmitt Triggers.

7.3.3 Clamp Diode Structure

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in Figure 7-1.

CAUTION

Voltages beyond the values specified in the Section 5.1 table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

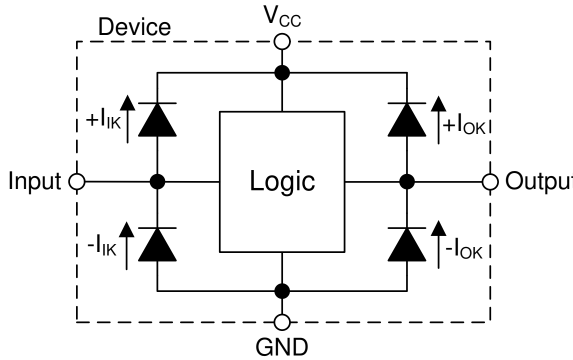


Figure 7-1. Electrical Placement of Clamping Diodes for Each Input and Output

7.4 Device Functional Modes

Table 7-1. Function Table

INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The SN74HCS11 includes three 3-input AND gates with Schmitt-trigger inputs. These 3-input AND gates work independently, but can be combined to get up to a 7-input AND gate. It can be used with all three inputs active, or one input can be disabled by directly connecting them to V_{CC} to turn the device into a 2-input AND gate.

The SN74HCS11 is used to control the $\overline{\text{RESET}}$ pin of a motor controller. This system requires three input signals to all be HIGH before the controller is enabled, and should be disabled in the event that any one signal goes LOW. The 3-input AND gate combines the 3 individual reset signals into a single active-low reset signal.

Many power good signals utilize open-drain outputs which can produce slow input transition rates when they transition from LOW to Hi-Z mode. This makes the SN74HCS11 ideal for the application because it has Schmitt-trigger inputs that do not have input transition rate requirements.

8.2 Typical Application

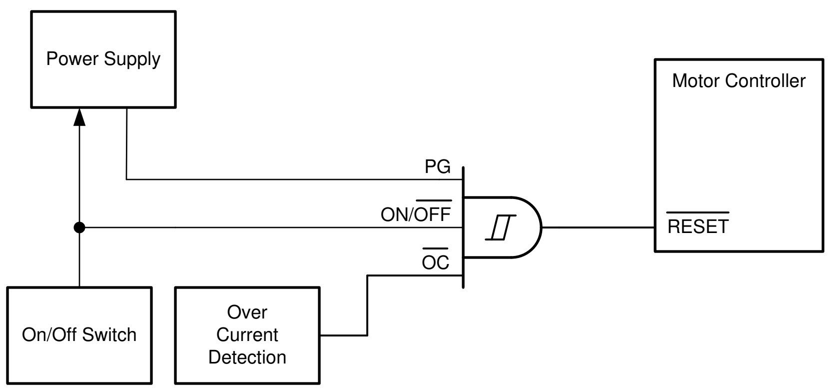


Figure 8-1. Typical application block diagram

8.2.1 Design Requirements

- All signals in the system operate at 5V
- The motor controller should be disabled if any of these conditions apply:
  – Power Supply is not ready (PG)
  – Excessive current is detected (OC)
  – The power switch is in the OFF position (ON/ $\overline{\text{OFF}}$)

8.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Section 5.3*. The supply voltage sets the device's electrical characteristics as described in the *Section 5.5*.

The supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74HCS11 plus the maximum supply current, I_{CC}, listed in the *Section 5.5*. The logic device can only source or sink as much current as it is provided at the supply and ground pins, respectively. Be sure not to exceed the maximum total current through GND or V_{CC} listed in the *Section 5.1*.

The SN74HCS11 can drive a load with a total capacitance less than or equal to 50pF connected to a high-impedance CMOS input while still meeting all of the datasheet specifications. Larger capacitive loads can be applied, however it is not recommended to exceed 70pF.

Total power consumption can be calculated using the information provided in CMOS Power Consumption and C_{pd} Calculation.

Thermal increase can be calculated using the information provided in Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices.

> **CAUTION**
>
> The maximum junction temperature, T_J(max) listed in the *Section 5.1*, is an *additional limitation* to prevent damage to the device. Do not violate any values listed in the *Section 5.1*. These limits are provided to prevent damage to the device.

8.2.1.2 Input Considerations

Input signals must cross V_{t-}(min) to be considered a logic LOW, and V_{t+}(max) to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Section 5.1*.

Unused inputs must be terminated to either V_{CC} or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the SN74HCS11, as specified in the *Section 5.5*, and the desired input transition rate. A 10kΩ resistor value is often used due to these factors.

The SN74HCS11 has no input signal transition rate requirements because it has Schmitt-trigger inputs.

Another benefit to having Schmitt-trigger inputs is the ability to reject noise. Noise with a large enough amplitude can still cause issues. To know how much noise is too much, please refer to the ΔV_T(min) in the *Section 5.5*. This hysteresis value will provide the peak-to-peak limit.

Unlike what happens with standard CMOS inputs, Schmitt-trigger inputs can be held at any valid value without causing huge increases in power consumption. The typical additional current caused by holding an input at a value other than V_{CC} or ground is plotted in the *Section 5.7*.

Refer to the *Section 7.3* for additional information regarding the inputs for this device.

8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output decreases the output voltage as specified by the V_{OH} specification in the *Section 5.5*. Similarly, the ground voltage is used to produce the output LOW voltage. Sinking current into the output increases the output voltage as specified by the V_{OL} specification in the *Section 5.5*. The plots in MISSING LINK and MISSING LINK provide a typical relationship between output voltage and current for this device.

Unused outputs can be left floating.

Refer to *Section 7.3* for additional information regarding the outputs for this device.

8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Section 8.4*.
2. Ensure the capacitive load at the output is ≤ 70pF. This is not a hard limit, however it will ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74HCS11 to the receiving device.
3. Ensure the resistive load at the output is larger than (V_{CC} / 25mA) Ω. This will ensure that the maximum output current from the *Section 5.1* is not violated. Most CMOS inputs have a resistive load measured in megaohms; much larger than the minimum calculated above.

4. Thermal issues are rarely a concern for logic gates, however the power consumption and thermal increase can be calculated using the steps provided in the application report, CMOS Power Consumption and Cpd Calculation

8.2.3 Application Curves

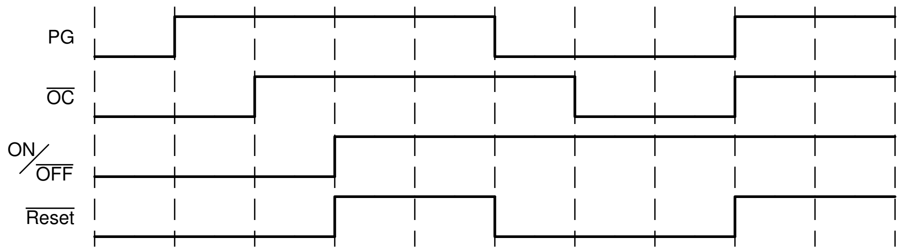


Figure 8-2. Application timing diagram

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. A 0.1µF capacitor is recommended for this device. Multiple bypass capacitors can be placed in parallel to reject different frequencies of noise. The 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power terminal as possible for best results, as shown in the following layout example.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or VCC, whichever makes more sense for the logic function or is more convenient.

8.4.2 Layout Example

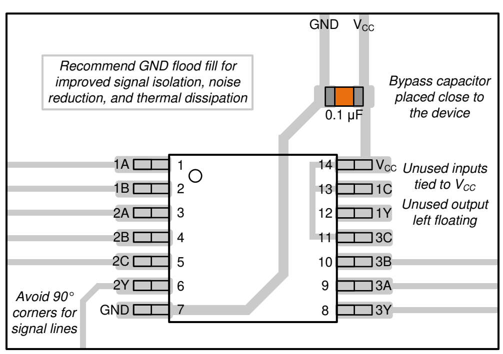


Figure 8-3. Example layout for the SN74HCS11

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- HCMOS Design Considerations
- CMOS Power Consumption and CPD Calculation
- Designing with Logic

9.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

9.3 Community Resources

9.4 Trademarks

All trademarks are the property of their respective owners.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from August 1, 2019 to March 18, 2026 (from Revision A (August 2019) to Revision B (March 2026)) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document................. 1
- Changed V_{T+} limits at 2V V_{CC} from 0.7V (min), 1.5V (max) to 1.18V (min), 1.3V (max) 5
- Changed V_{T+} limits at 4.5V V_{CC} from 1.7V (min), 3.15V (max) to 2.39V (min), 2.58V (max) 5
- Changed V_{T+} limits at 6V V_{CC} from 2.1V (min), 4.2V (max) to 3.11V (min), 3.32V (max) 5
- Changed V_{T-} limits at 2V V_{CC} from 0.3V (min), 1.0V (max) to 0.61V (min), 0.66V (max)..................................5
- Changed V_{T-} limits at 4.5V V_{CC} from 0.9V (min), 2.2V (max) to 1.31V (min), 1.42V (max) 5
- Changed V_{T-} limits at 6V V_{CC} from 1.2V (min), 3.0V (max) to 1.72V (min), 1.87V (max)..................................5
- Changed ΔV_T limits at 2V V_{CC} from 0.2V (min), 1.0V (max) to 0.55V (min), 0.67V (max)................................5
- Changed ΔV_T limits at 4.5V V_{CC} from 0.4V (min), 1.4V (max) to 1.04V (min), 1.21V (max).............................5
- Changed ΔV_T limits at 6V V_{CC} from 0.6V (min), 1.6V (max) to 1.34V (min), 1.49V (max)................................5

Changes from Revision * (August 2019) to Revision A (October 2019) **Page**

- Added D Package to data sheet...1
- Added D package information to Pin Configuration and Functions...3
- Added D package column to *Thermal Information* table... 4

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74HCS11DR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	HCS11
SN74HCS11DR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS11
SN74HCS11PWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	HCS11
SN74HCS11PWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS11

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74HCS11 :

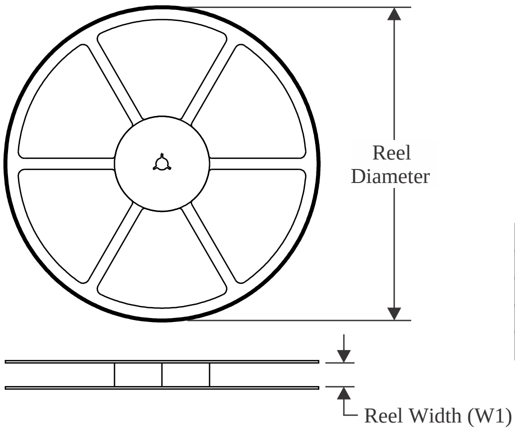
- Automotive : SN74HCS11-Q1

NOTE: Qualified Version Definitions:

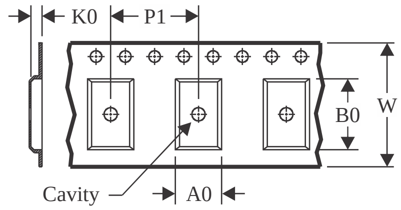
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

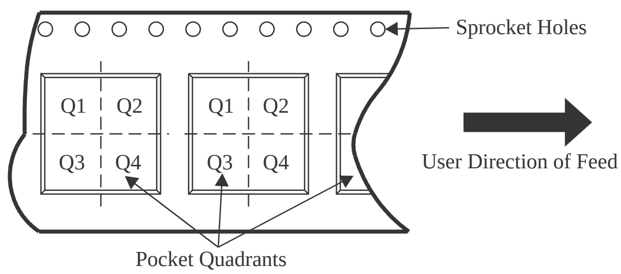


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

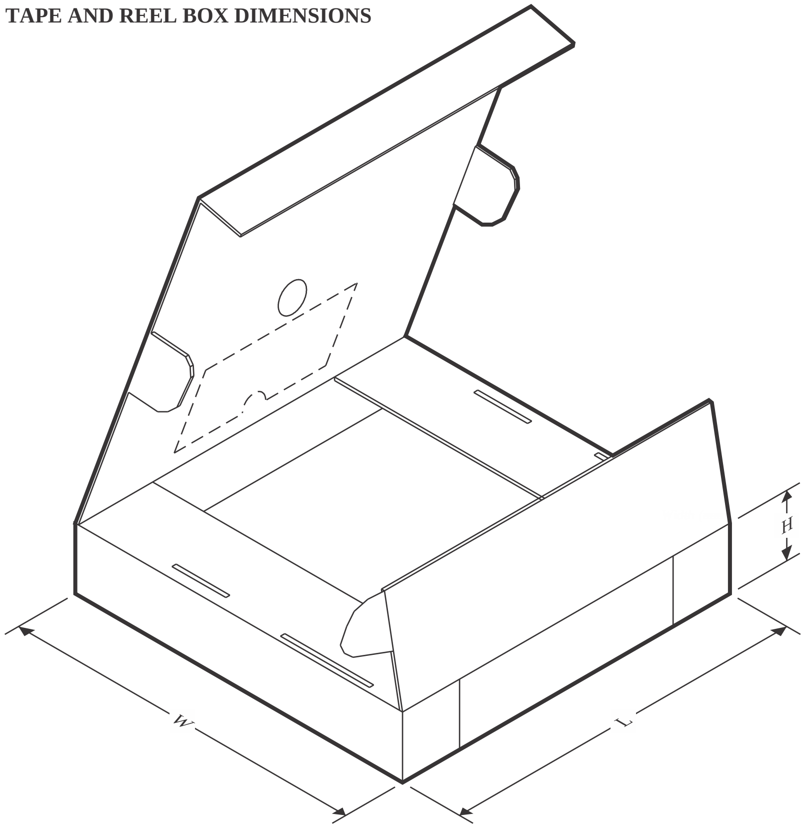
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

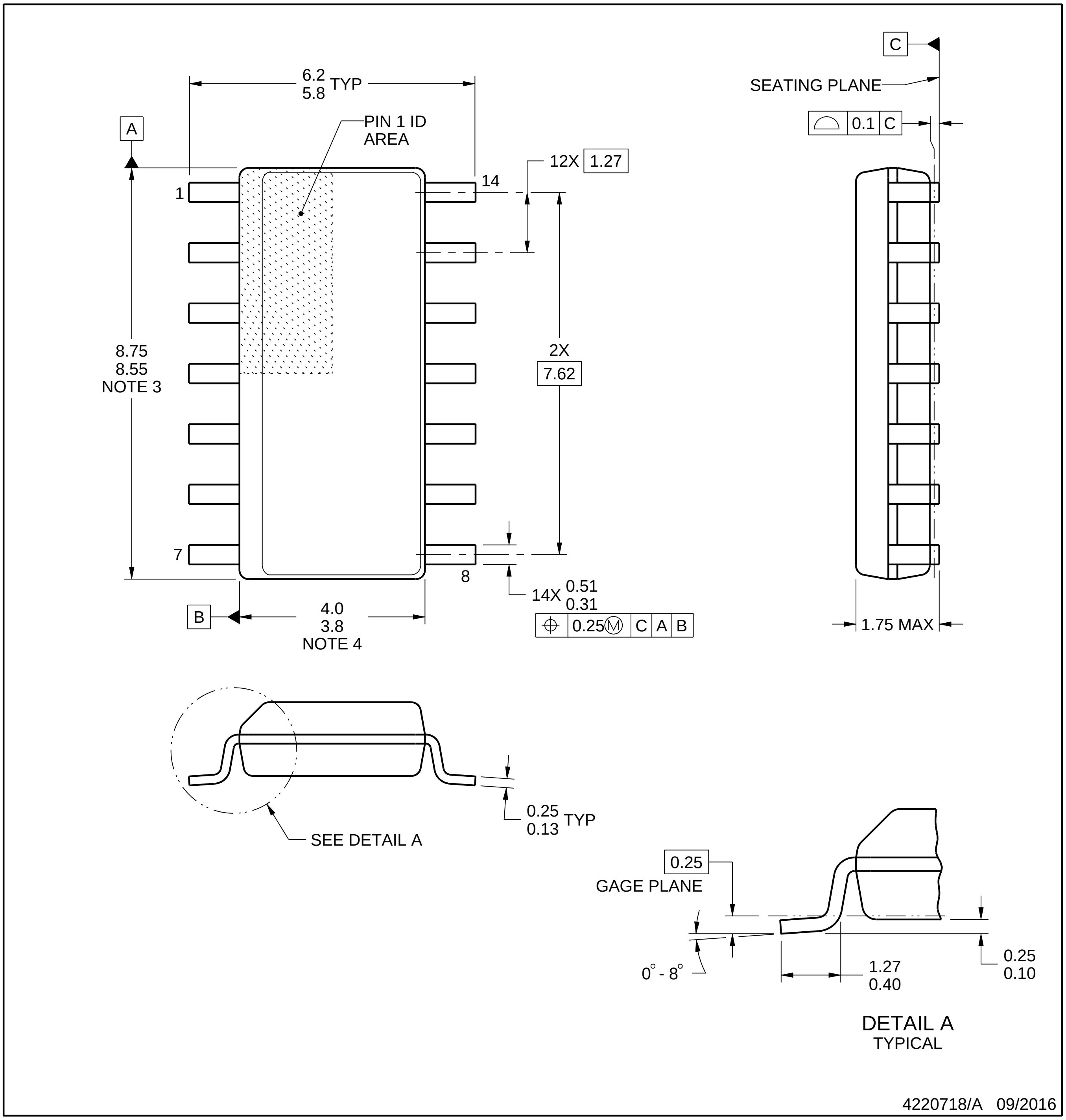
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCS11DR	SOIC	D	14	2500	330.0	16.4	6.6	9.3	2.1	8.0	16.0	Q1
SN74HCS11DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HCS11PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



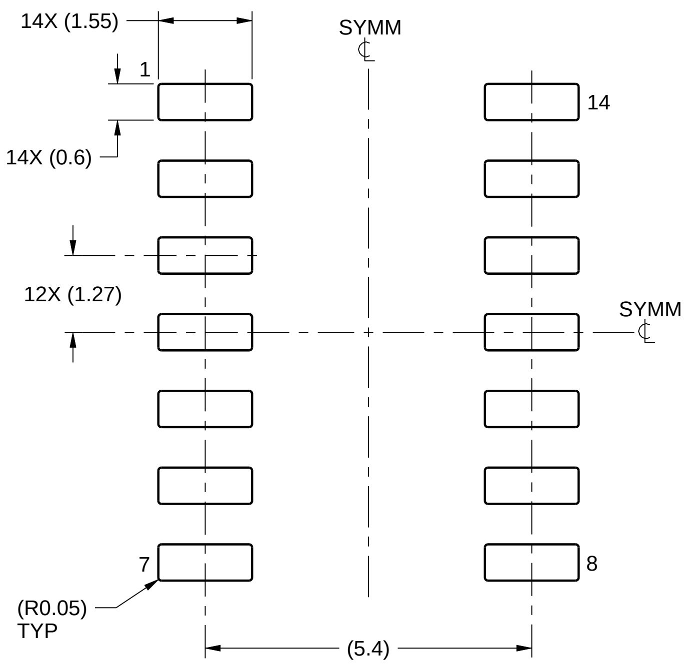
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCS11DR	SOIC	D	14	2500	366.0	364.0	50.0
SN74HCS11DR	SOIC	D	14	2500	353.0	353.0	32.0
SN74HCS11PWR	TSSOP	PW	14	2000	356.0	356.0	35.0

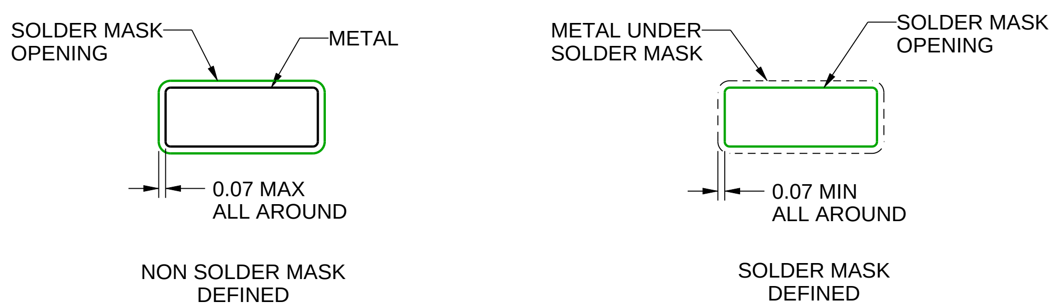


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X

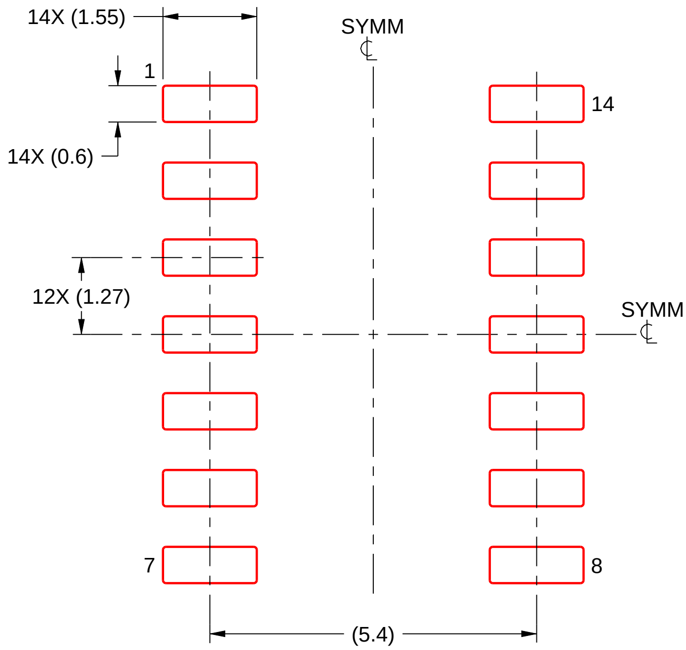


SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

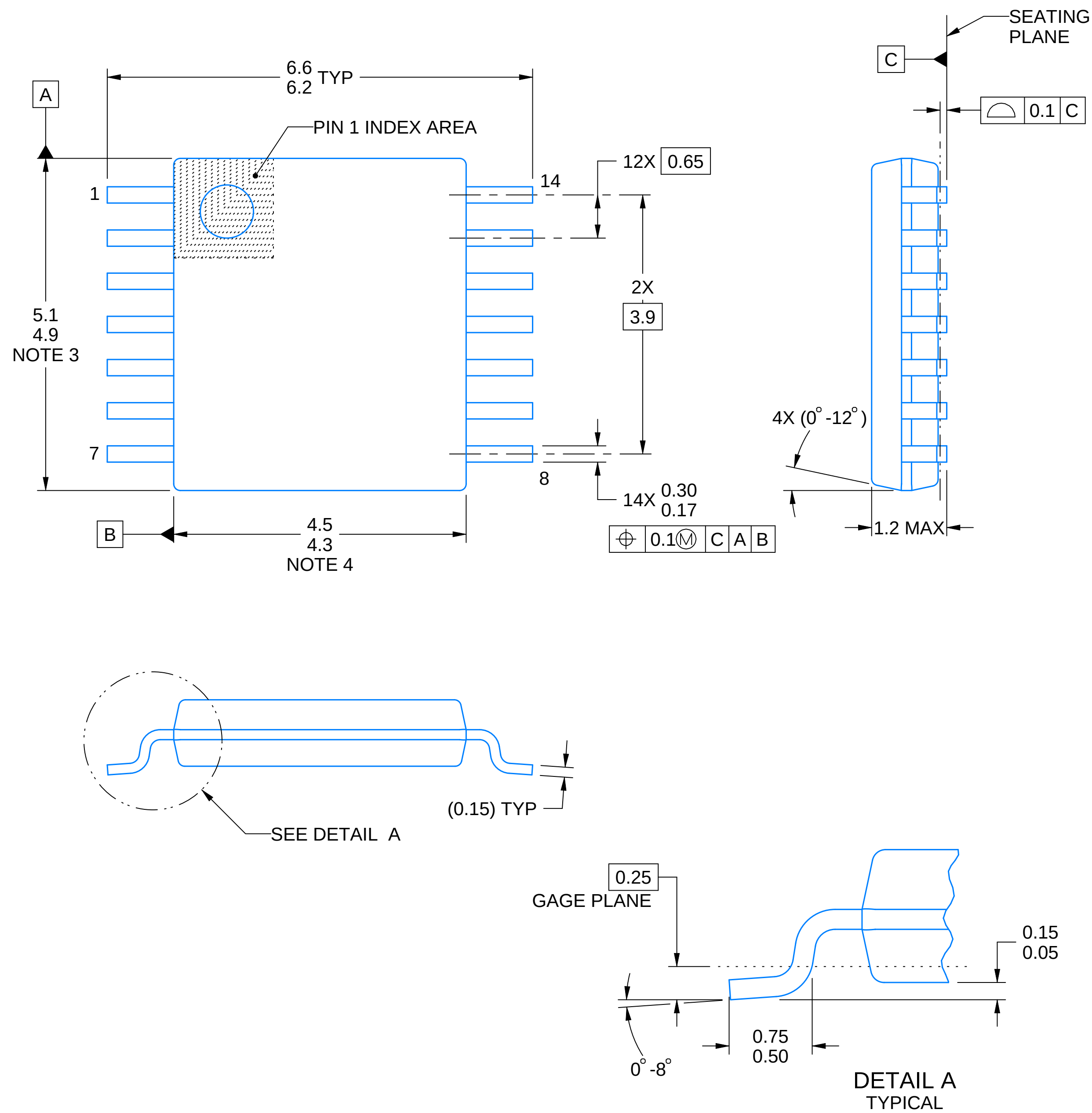


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

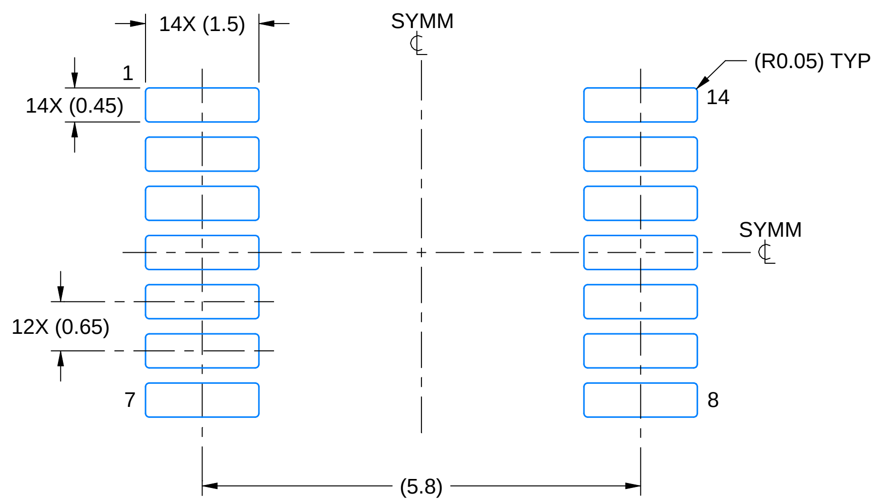
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



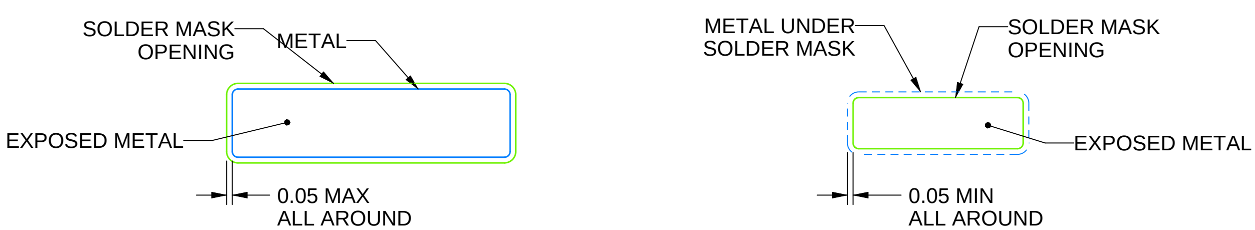
4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



NON-SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

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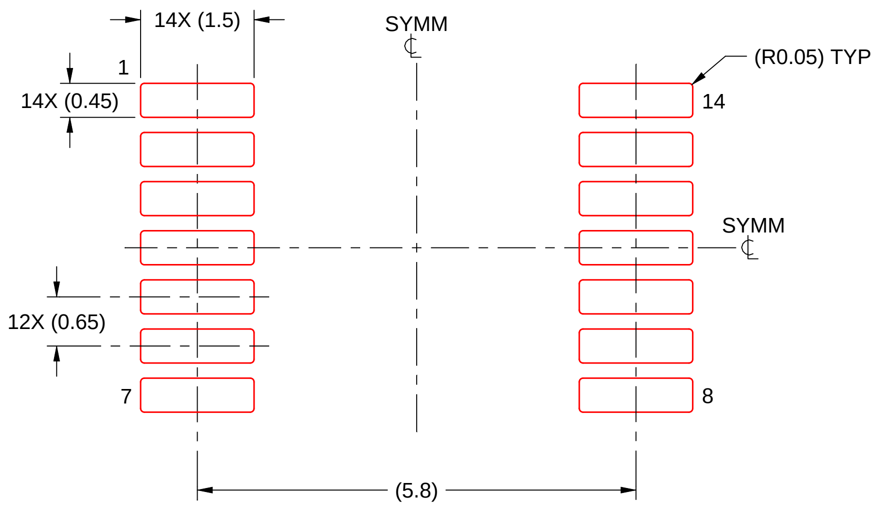
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

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9. Board assembly site may have different recommendations for stencil design.