- **Operating Voltage Range of 4.5 V to 5.5 V**
- **Low Power Consumption, 80-μA Max I_{CC}**
- **Typical t_{pd} = 12 ns**
- **$\pm$6-mA Output Drive at 5 V**
- **Low Input Current of 1 μA Max**
- **Inputs Are TTL-Voltage Compatible**
- **High-Current 3-State Outputs Interface Directly With System Bus or Can Drive Up To 15 LSTTL Loads**
- **Data Flow-Through Pinout (All Inputs on Opposite Side From Outputs)**

SN54HCT540 . . . J PACKAGE
SN74HCT540 . . . DW OR N PACKAGE
(TOP VIEW)

$\overline{OE1}$	1		20	V_{CC}
A1	2		19	$\overline{OE2}$
A2	3		18	Y1
A3	4		17	Y2
A4	5		16	Y3
A5	6		15	Y4
A6	7		14	Y5
A7	8		13	Y6
A8	9		12	Y7
GND	10		11	Y8
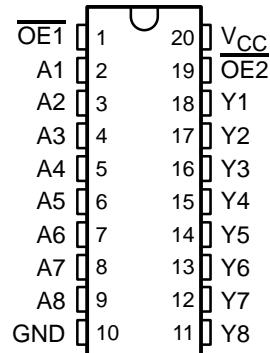
description/ordering information

These octal buffers and line drivers are designed to have the performance of the 'HCT240 devices and a pinout with inputs and outputs on opposite sides of the package. This arrangement greatly facilitates printed circuit board layout.

The 3-state control gate is a 2-input NOR. If either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all eight outputs are in the high-impedance state. The 'HCT540 devices provide inverted data at the outputs.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	PDIP – N	Tube	SN74HCT540N	SN74HCT540N
	SOIC – DW	Tube	SN74HCT540DW	HCT540
		Tape and reel	SN74HCT540DWR	
−55°C to 125°C	CDIP – J	Tube	SNJ54HCT540J	SNJ54HCT540J

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each buffer/driver)

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

SN54HCT540, SN74HCT540
OCTAL BUFFERS AND LINE DRIVERS
WITH 3-STATE OUTPUTS

SCLS008C – MARCH 1984 – REVISED MARCH 2003

logic diagram (positive logic)

To Seven Other Channels
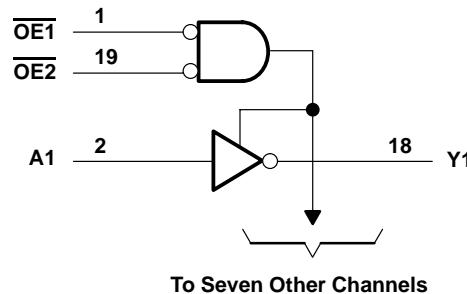
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) .... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) .... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) .... ±35 mA
Continuous current through V_{CC} or GND .... ±70 mA
Package thermal impedance, θ_{JA} (see Note 2): DW package .... 58°C/W
　　　　　　　　　　　　　　　　　　　　　　N package .... 69°C/W
Storage temperature range, T_{stg} .... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
　　　　2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			SN54HCT540			SN74HCT540			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V			0.8			0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time				500			500	ns
T_A	Operating free-air temperature		–55		125	–40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	$T_A = 25°C$			SN54HCT540		SN74HCT540		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}	$I_{OH} = -20\ \mu A$	4.5 V	4.4	4.499		4.4		4.4		V
		$I_{OH} = -6\ mA$		3.98	4.3		3.7		3.84		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	$I_{OL} = 20\ \mu A$	4.5 V		0.001	0.1		0.1		0.1	V
		$I_{OL} = 6\ mA$			0.17	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0		5.5 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	$V_O = V_{CC}$ or 0, $V_I = V_{IH}$ or V_{IL}		5.5 V		±0.01	±0.5		±10		±5	µA
I_{CC}	$V_I = V_{CC}$ or 0, $I_O = 0$		5.5 V			8		160		80	µA
ΔI_{CC}†	One input at 0.5 V or 2.4 V, Other inputs at 0 or V_{CC}		5.5 V		1.4	2.4		3		2.9	mA
C_i			4.5 V to 5.5 V		3	10		10		10	pF

† This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25°C$			SN54HCT540		SN74HCT540		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	4.5 V		13	20		30		25	ns
			5.5 V		12	18		27		23	
t_{en}	$\overline{OE}$	Y	4.5 V		20	30		45		38	ns
			5.5 V		18	27		41		34	
t_{dis}	$\overline{OE}$	Y	4.5 V		19	30		45		38	ns
			5.5 V		18	27		41		34	
t_t		Y	4.5 V		8	12		18		15	ns
			5.5 V		7	11		16		14	

switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25°C$			SN54HCT540		SN74HCT540		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	4.5 V		20	30		45		38	ns
			5.5 V		19	27		41		34	
t_{en}	$\overline{OE}$	Y	4.5 V		26	40		60		50	ns
			5.5 V		25	36		54		45	
t_t		Y	4.5 V		17	42		63		53	ns
			5.5 V		14	38		57		48	

operating characteristics, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per buffer/driver	No load	35	pF

PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT
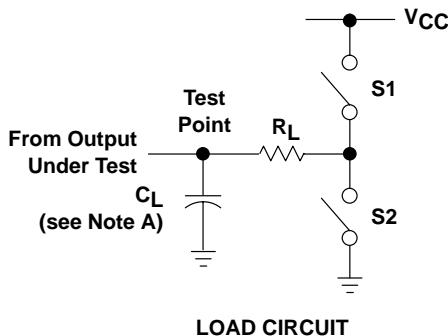
PARAMETER		R_L	C_L	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open
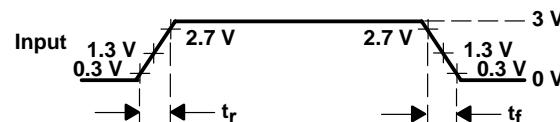
VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES
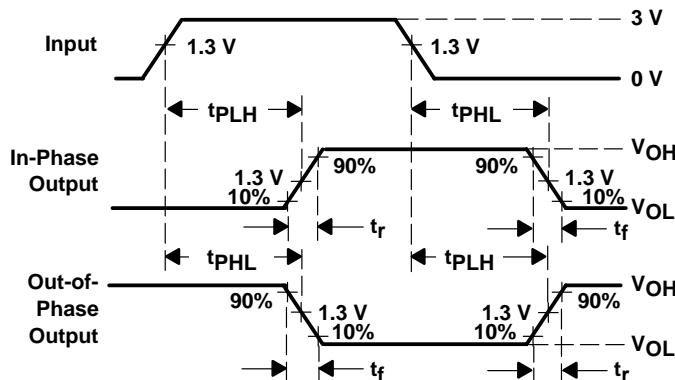
VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT RISE AND FALL TIMES
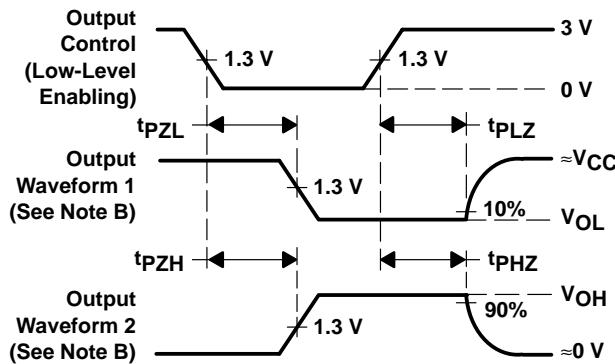
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
   B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
       Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
   C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following
       characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
   D. The outputs are measured one at a time with one input transition per measurement.
   E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
   F. t_{PZL} and t_{PZH} are the same as t_{en}.
   G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

![TEXAS INSTRUMENTS]

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
JM38510/65760BRA	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65760BRA
JM38510/65760BRA.A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65760BRA
M38510/65760BRA	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65760BRA
SN54HCT540J	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HCT540J
SN54HCT540J.A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HCT540J
SN74HCT540DWR	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT540
SN74HCT540DWR.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT540
SN74HCT540DWRG4	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT540
SN74HCT540N	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HCT540N
SN74HCT540N.A	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HCT540N
SNJ54HCT540J	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54HCT540J
SNJ54HCT540J.A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54HCT540J

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE OPTION ADDENDUM

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54HCT540, SN74HCT540 :

• Catalog : SN74HCT540

• Military : SN54HCT540

NOTE: Qualified Version Definitions:

   • Catalog - TI's standard catalog product

   • Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS
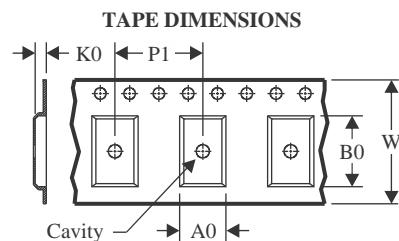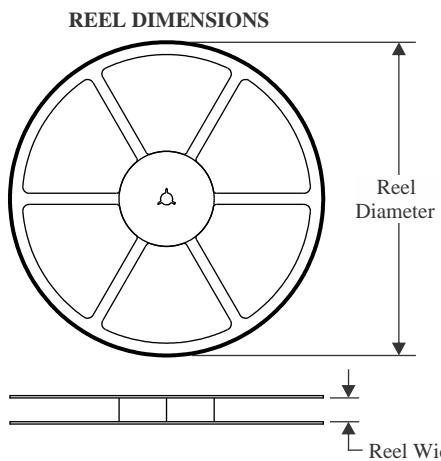
TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE
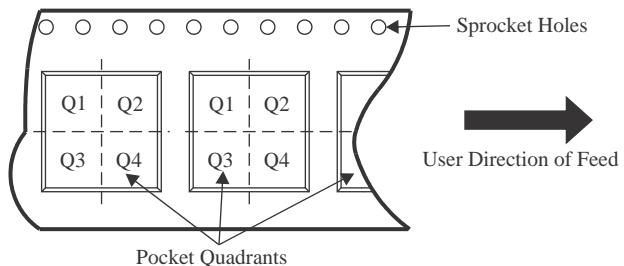
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCT540DWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74HCT540DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS
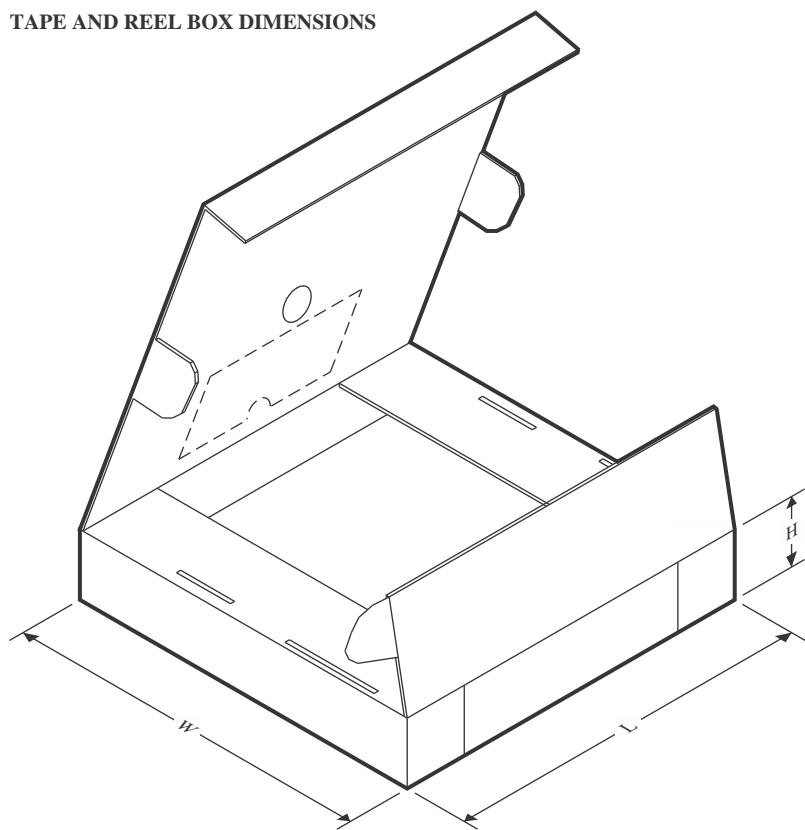
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCT540DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74HCT540DWR	SOIC	DW	20	2000	356.0	356.0	45.0

PACKAGE MATERIALS INFORMATION

TUBE

T - Tube height

L - Tube length

W - Tube width

B - Alignment groove width
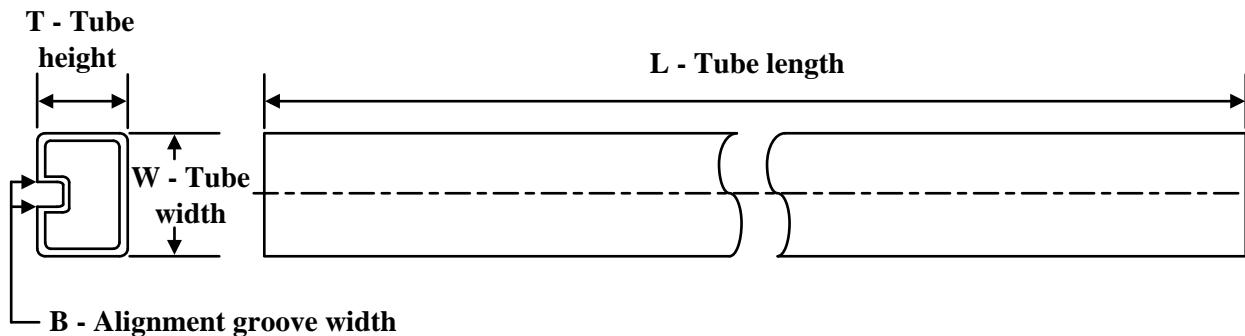
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74HCT540N	N	PDIP	20	20	506	13.97	11230	4.32
SN74HCT540N.A	N	PDIP	20	20	506	13.97	11230	4.32

J (R−GDIP−T**)   CERAMIC DUAL IN−LINE PACKAGE
14 LEADS SHOWN
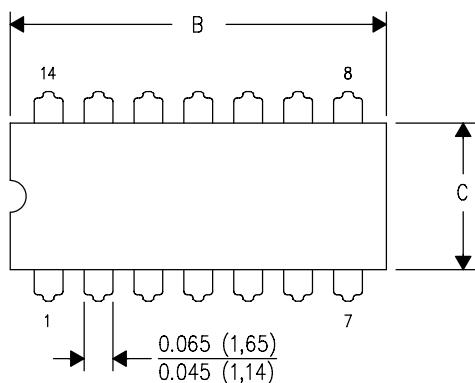
DIM / PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

C

1   7

0.065 (1,65)
―――――――――
0.045 (1,14)

0.005 (0,13) MIN

0.060 (1,52)
―――――――――
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
―――――――――
0.014 (0,36)

0.100 (2,54)

A

0°−15°

0.014 (0,36)
―――――――――
0.008 (0,20)
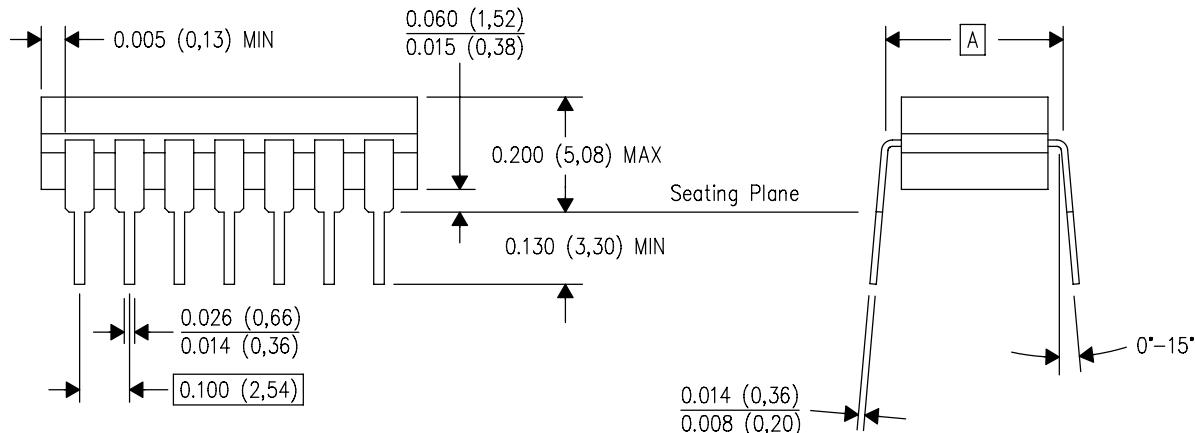
4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
          B. This drawing is subject to change without notice.
          C. This package is hermetically sealed with a ceramic lid using glass frit.
          D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
          E. Falls within MIL STD 1835 GDIP1−T14, GDIP1−T16, GDIP1−T18 and GDIP1−T20.

N (R–PDIP–T**)
16 PINS SHOWN

PLASTIC DUAL–IN–LINE PACKAGE
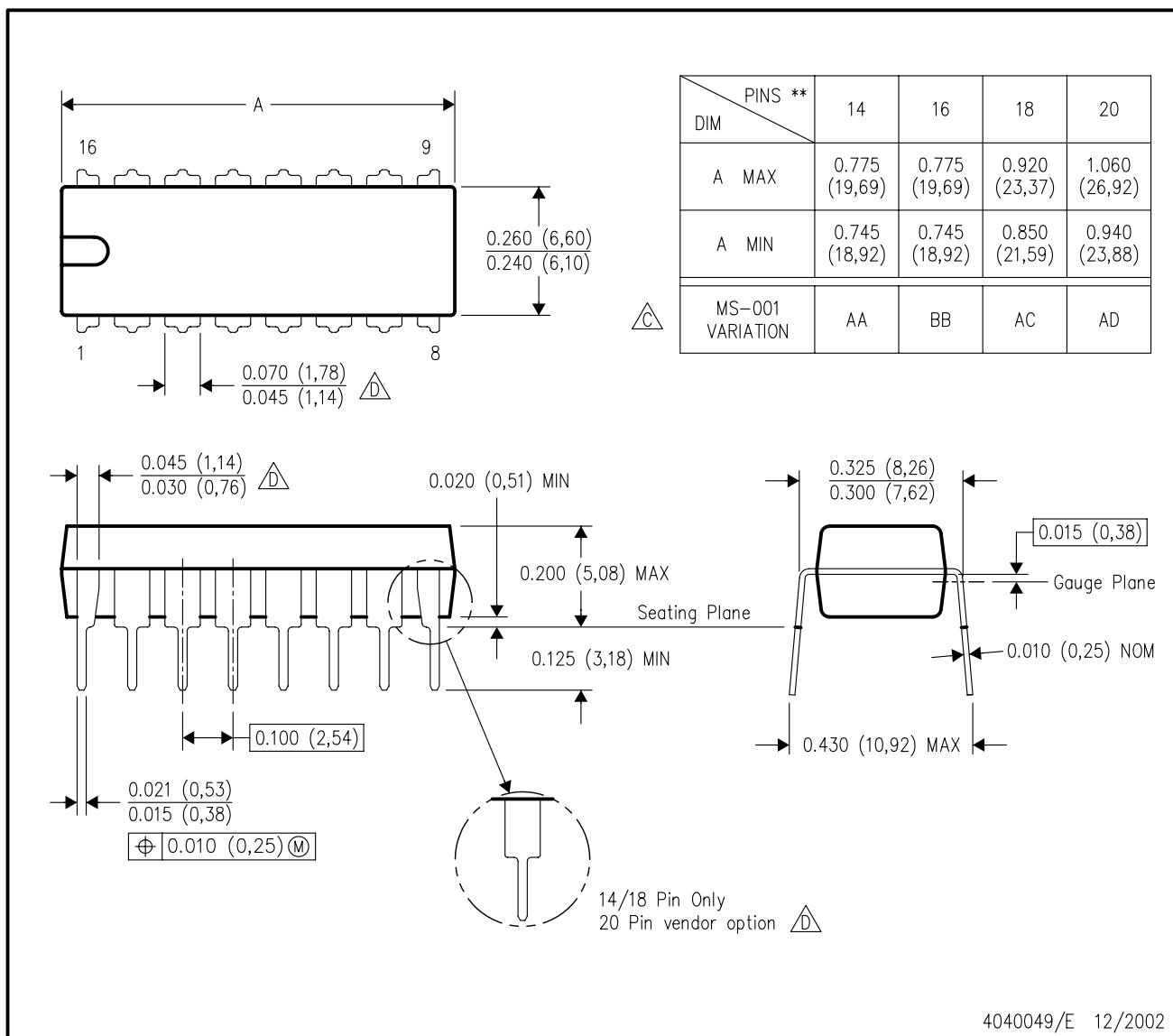
PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION	AA	BB	AC	AD

0.260 (6,60) / 0.240 (6,10)

0.070 (1,78) / 0.045 (1,14)

0.045 (1,14) / 0.030 (0,76)

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

0.010 (0,25) M

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

TEXAS INSTRUMENTS
www.ti.com

10.63 / 9.97 TYP

A

PIN 1 ID AREA

1

18X [1.27]

20

13.0 / 12.6 NOTE 3

2X [11.43]

10

11

B

7.6 / 7.4 NOTE 4

20X 0.51 / 0.31

[⊕ | 0.25Ⓜ | C | A | B]

C

SEATING PLANE

[⌒ | 0.1 | C]

2.65 MAX

0.33 / 0.10 TYP

SEE DETAIL A

[0.25]

GAGE PLANE

0° - 8°

1.27 / 0.40

0.3 / 0.1

DETAIL A
TYPICAL

4220724/A   05/2016
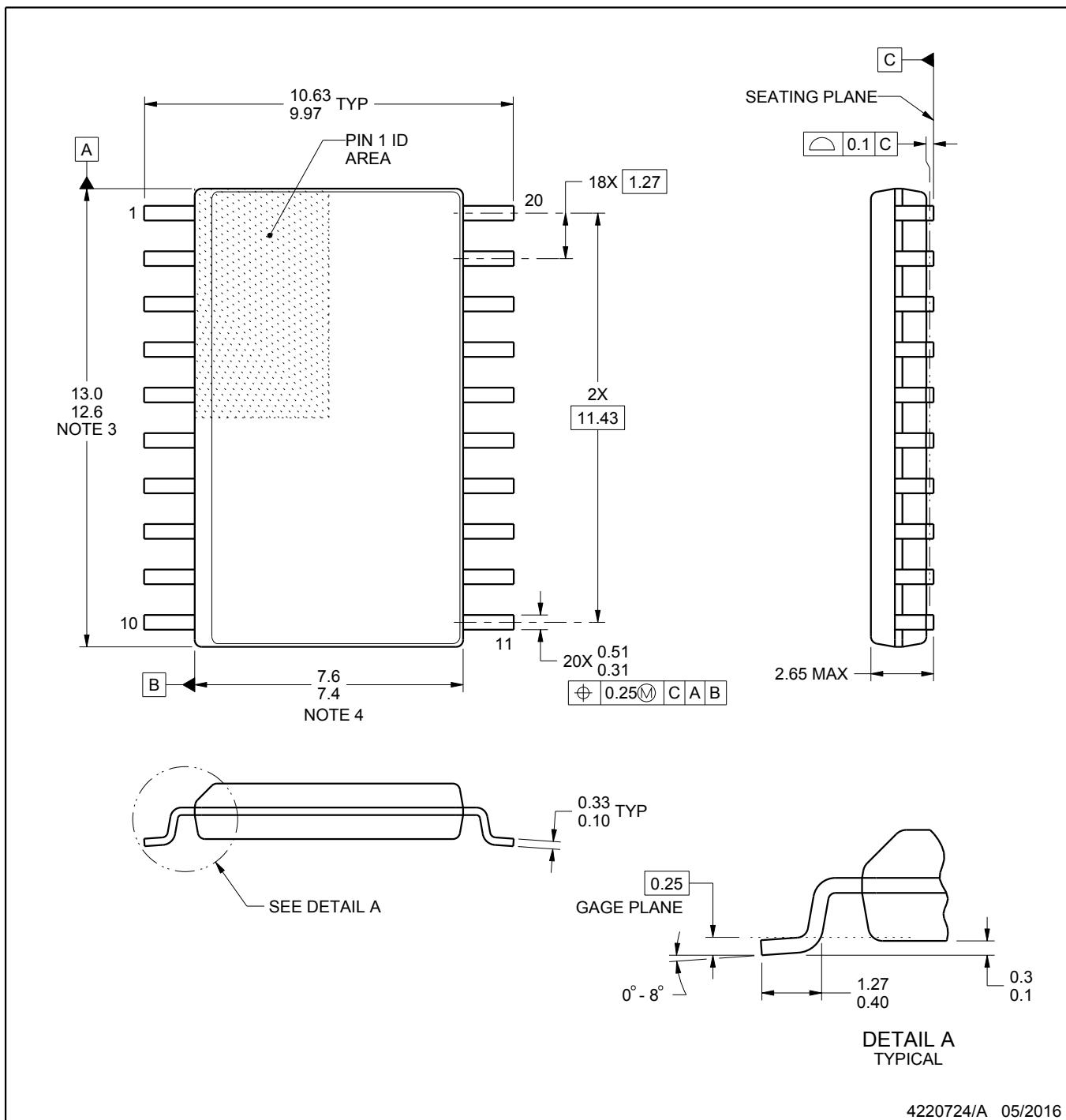
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

20X (2)

1

SYMM
₵

20

20X (0.6)

18X (1.27)

SYMM
₵

(R0.05)
TYP

10

11

(9.3)
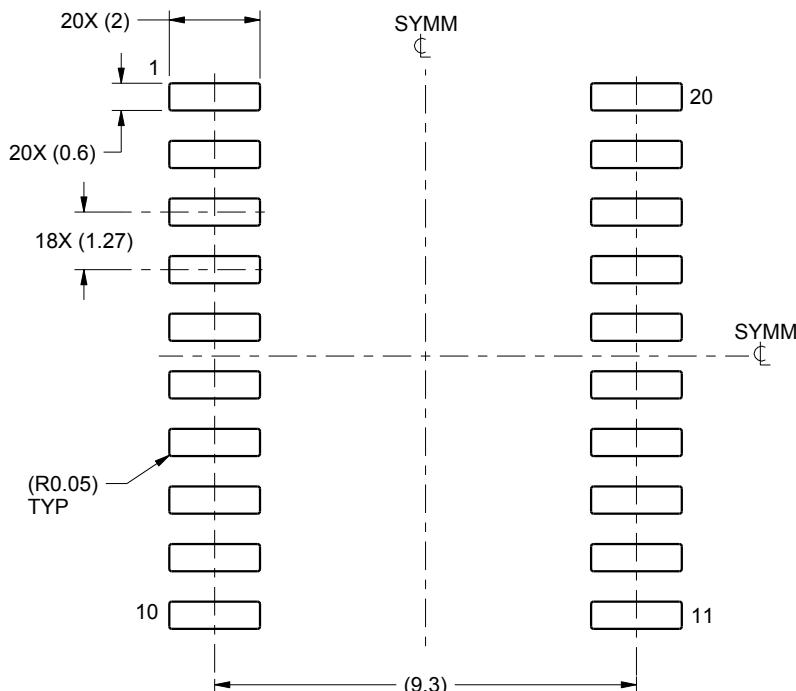
LAND PATTERN EXAMPLE
SCALE:6X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.07 MAX
ALL AROUND

0.07 MIN
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED
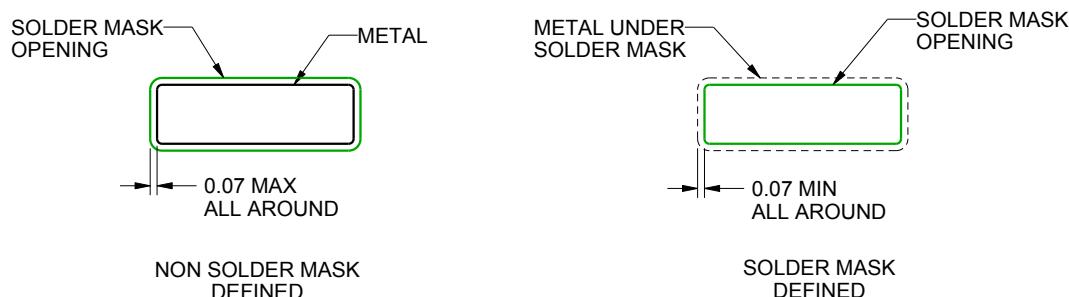
SOLDER MASK DETAILS

4220724/A   05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

20X (2)

1

20X (0.6)

18X (1.27)

SYMM

SYMM

20

10   11

(9.3)
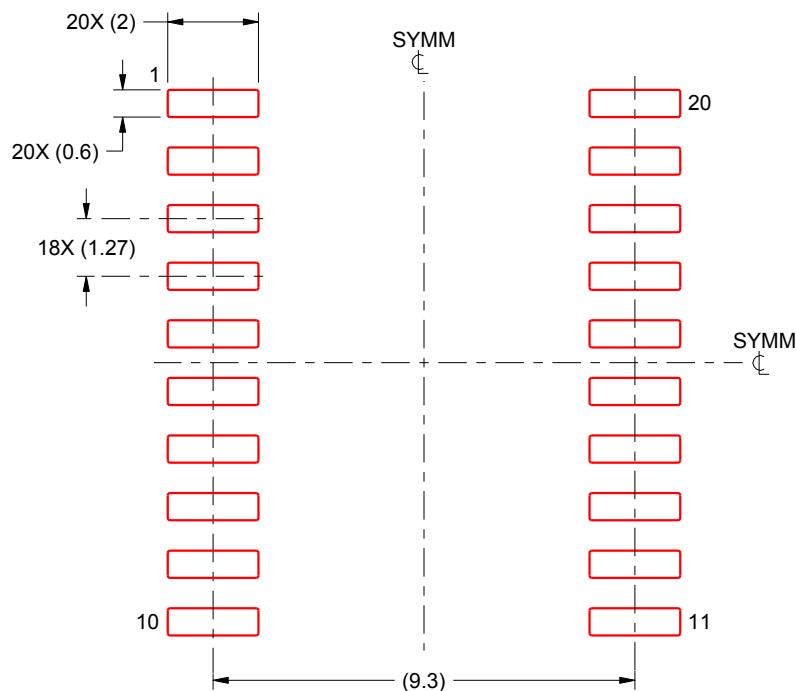
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A   05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
9. Board assembly site may have different recommendations for stencil design.

TEXAS
INSTRUMENTS
www.ti.com

IMPORTANT NOTICE AND DISCLAIMER