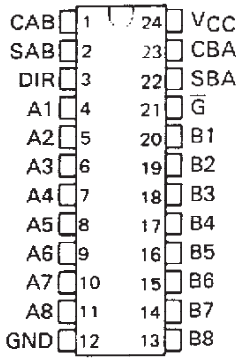
# OCTAL BUS TRANSCEIVERS AND REGISTERS

SDLS190A – DECEMBER 1982 – REVISED MAY 2004

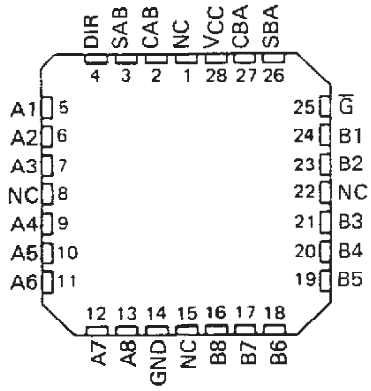
- **Independent Registers for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **Choice of True or Inverting Data Paths**
- **Choice of 3-State or Open-Collector Outputs**
- **Included Among the Package Options Are Compact 24-pin 300-mil-Wide Plastic and Ceramic DIPs, Ceramic Chip Carriers, and Plastic "Small Outline" Packages**
- **Dependable Texas Instruments Quality and Reliability**

| DEVICE | OUTPUT | LOGIC |
|---|---|---|
| 'LS646 | 3-State | True |
| 'LS647 | Open-Collector | True |
| 'LS648 | 3-State | Inverting |
| 'LS649 | Open-Collector | Inverting |

SN54LS' . . . JT PACKAGE
SN74LS' . . . DW OR NT PACKAGE
(TOP VIEW)

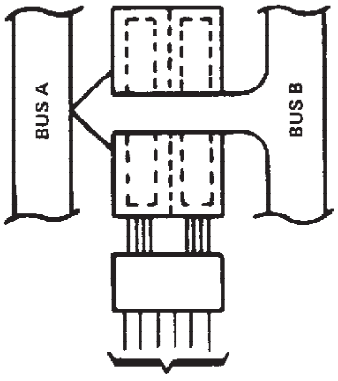



SN54LS' . . . FK PACKAGE
(TOP VIEW)



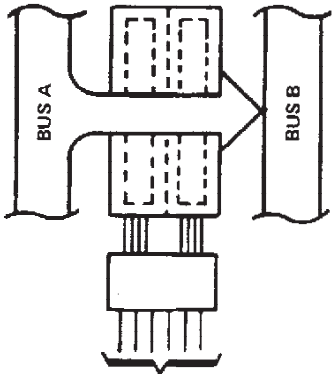

## description

These devices consist of bus transceiver circuits with 3-state or open-collector outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers on the low-to-high transition of the appropriate clock pin (CAB or CBA). The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.




| (21) $\overline{G}$ | (3) DIR | (1) CAB | (23) CBA | (2) SAB | (22) SBA |
|---|---|---|---|---|---|
| L | L | X | X | X | L |

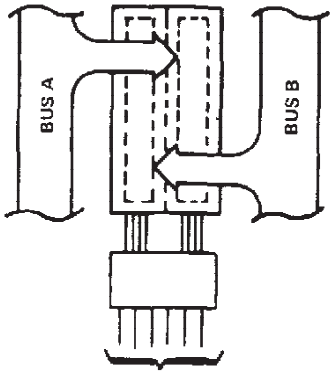
REAL-TIME TRANSFER
BUS B TO BUS A




| (21) $\overline{G}$ | (3) DIR | (1) CAB | (23) CBA | (2) SAB | (22) SBA |
|---|---|---|---|---|---|
| L | H | X | X | L | X |

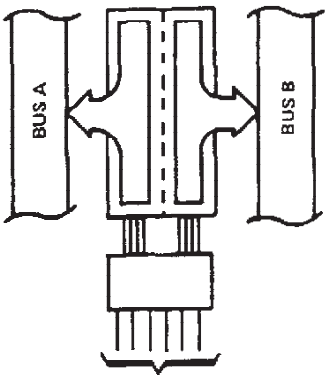
REAL-TIME TRANSFER
BUS A TO BUS B

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.




| (21) $\overline{G}$ | (3) DIR | (1) CAB | (23) CBA | (2) SAB | (22) SBA |
|---|---|---|---|---|---|
| X | X | ↑ | X | X | X |
| X | X | X | ↑ | X | X |
| H | X | ↑ | ↑ | X | X |

STORAGE FROM
A, B, OR A AND B




| (21) $\overline{G}$ | (3) DIR | (1) CAB | (23) CBA | (2) SAB | (22) SBA |
|---|---|---|---|---|---|
| L | L | X | H or L | X | H |
| L | H | H or L | X | H | X |

TRANSFER
STORED DATA
TO A OR B

Enable ($\overline{G}$) and direction (DIR) pins are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select controls (SAB and SBA) can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when enable $\overline{G}$ is active (low). In the isolation mode (control $\overline{G}$ high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The SN54' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from 0° to 70°C.

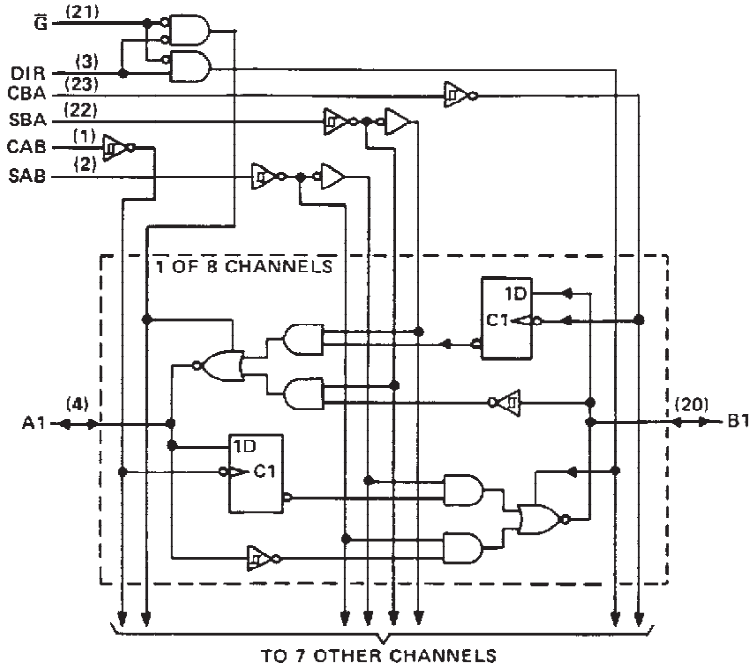
FUNCTION TABLE

| INPUTS | | | | | | DATA I/O† | | OPERATION OR FUNCTION | |
|---|---|---|---|---|---|---|---|---|---|
| $\overline{G}$ | DIR | CAB | CBA | SAB | SBA | A1 THRU A8 | B1 THRU B8 | LS646, LS647 | LS648, LS649 |
| X | X | ↑ | X | X | X | Input | Not specified | Store A, B unspecified | Store A, B unspecified |
| X | X | X | ↑ | X | X | Not specified | Input | Store B, A unspecified | Store B, A unspecified |
| H | X | ↑ | ↑ | X | X | Input | Input | Store A and B Data | Store A and B Data |
| H | X | H or L | H or L | X | X | | | Isolation, hold storage | Isolation, hold storage |
| L | L | X | X | X | L | Output | Input | Real-Time B Data to A Bus | Real-Time $\overline{B}$ Data to A Bus |
| L | L | X | H or L | X | H | | | Stored B Data to A Bus | Stored $\overline{B}$ Data to A Bus |
| L | H | X | X | L | X | Input | Output | Real-Time A Data to B Bus | Real-Time $\overline{A}$ Data to B Bus |
| L | H | H or L | X | H | X | | | Stored A Data to B Bus | Stored $\overline{A}$ Data to B Bus |

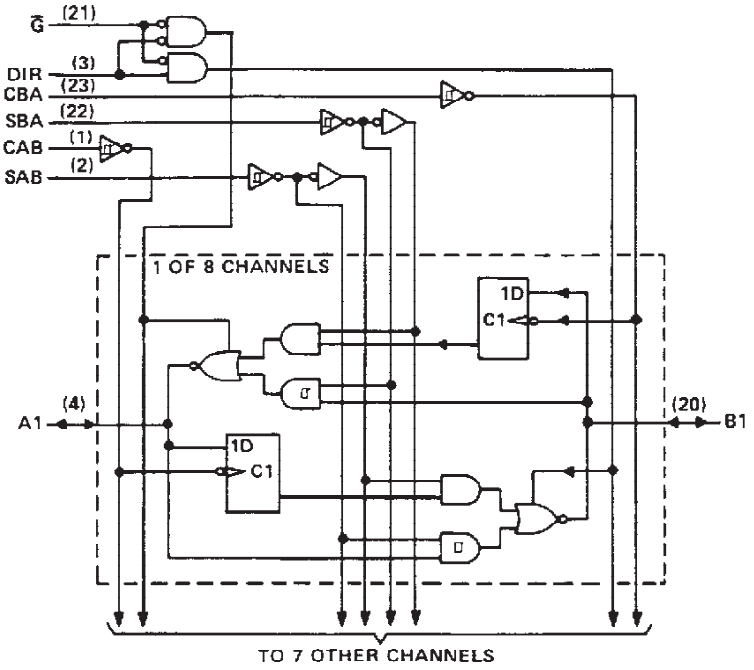
† The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

## logic diagrams (positive logic)

'LS646, 'LS647



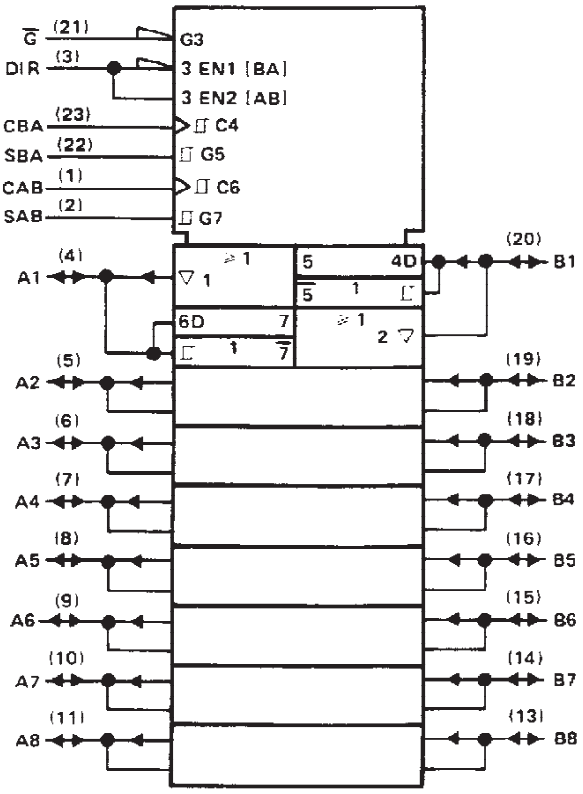

'LS648, 'LS649



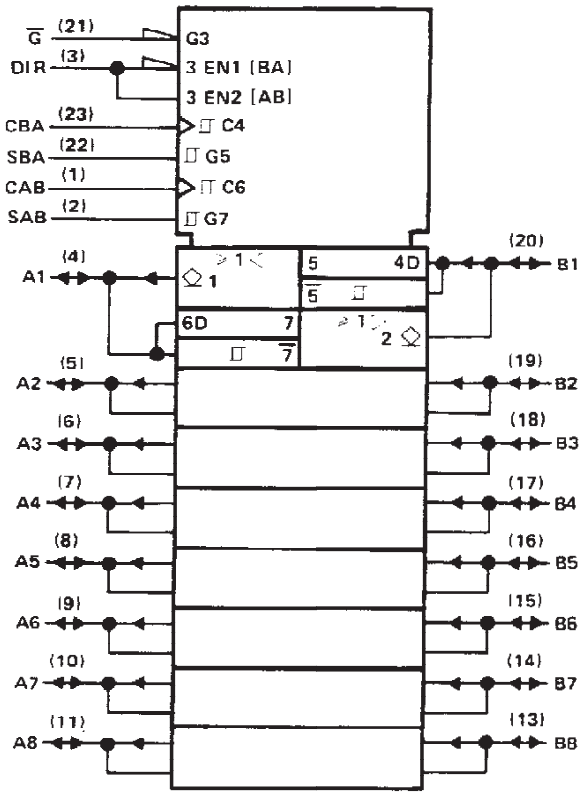

Pin numbers shown are for DW, JT, and NT packages.

**logic symbols**†

'LS646

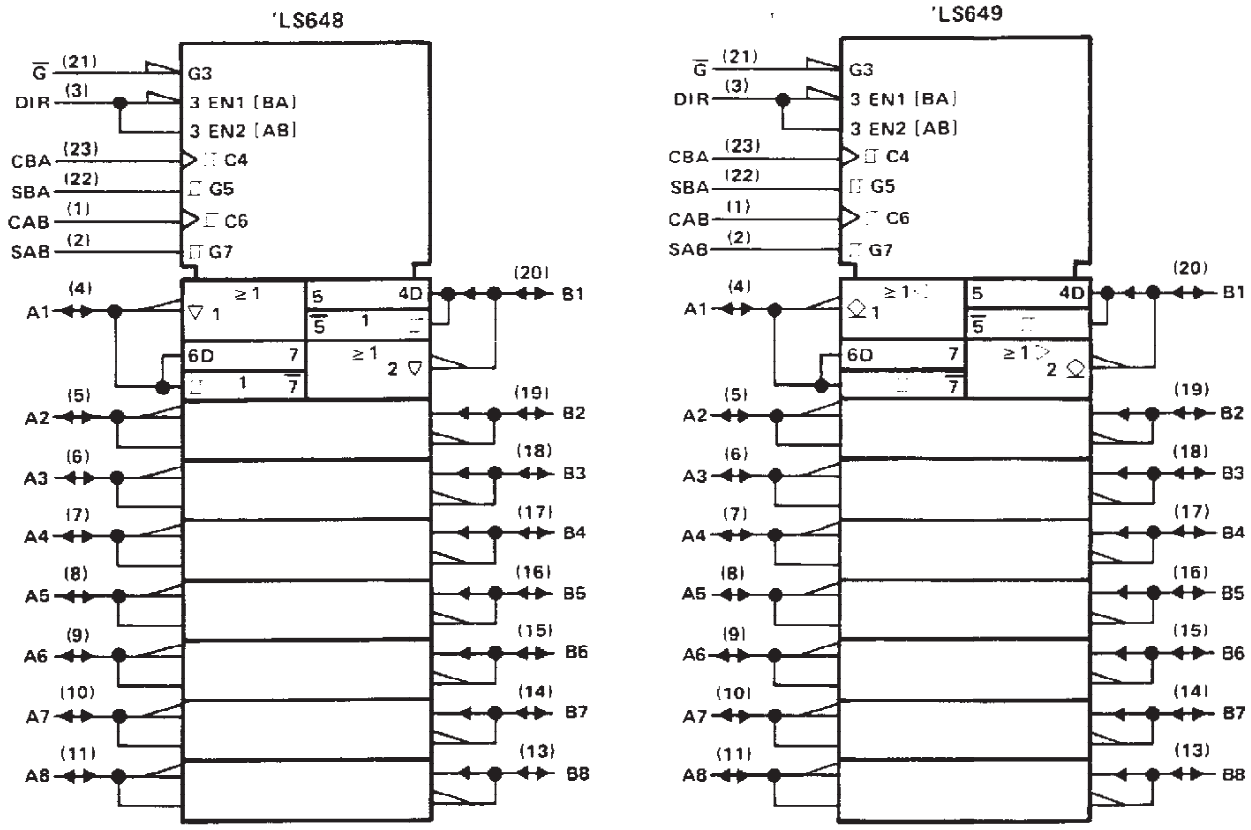



'LS647



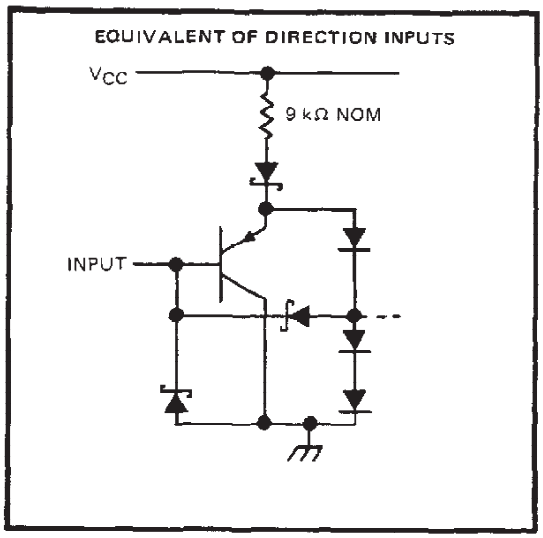

†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

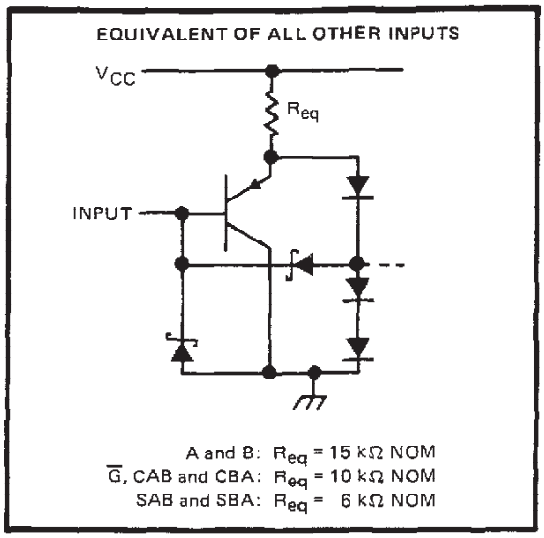
**logic symbols† (continued)**

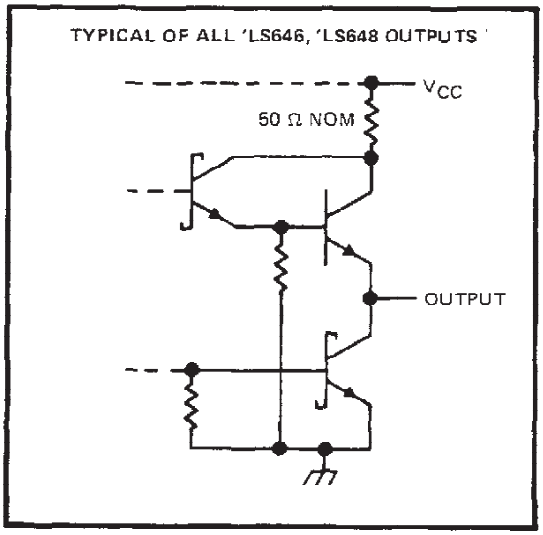


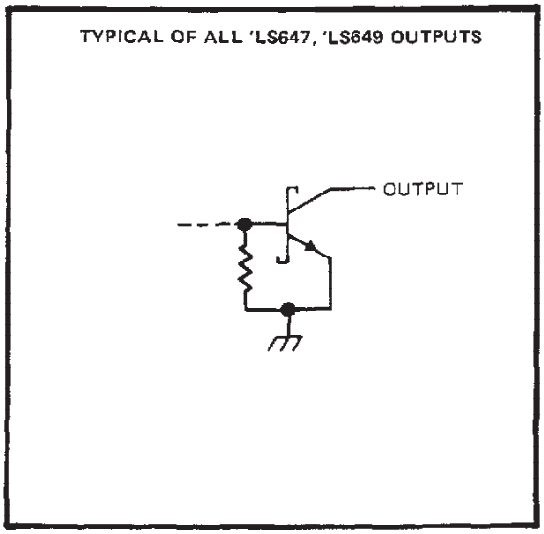

†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

## schematics of inputs and outputs



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ . . . . . 7 V
Input voltage: Control inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54LS646, SN54LS648 . . . . . −55°C to 125°C
SN74LS646, SN74LS648 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

### recommended operating conditions

| | | | SN54LS646/648 | | | SN74LS646/648 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.5 | | | 0.6 | V |
| $I_{OH}$ | High-level output current | | | | −12 | | | −15 | mA |
| $I_{OL}$ | Low-level output current | | | | 12 | | | 24 | mA |
| $t_w$ | Pulse duration | CBA or CAB high | 15 | | | 15 | | | ns |
| | | CBA or CAB low | 30 | | | 30 | | | |
| | | Data high or low | 30 | | | 30 | | | |
| $t_{su}$ | Setup time before CAB↑ or CBA↑ | A or B | 15 | | | 15 | | | ns |
| $t_h$ | Hold time after CAB↑ or CBA↑ | A or B | 0 | | | 0 | | | ns |
| $T_A$ | Operating free-air temperature | | −55 | | 125 | 0 | | 70 | °C |

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | | SN54LS646/648 | | | SN74LS646/648 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IK}$ | | $V_{CC}$ = MIN, $I_I$ = −18 mA | | | | −1.5 | | | −1.5 | V |
| Hysteresis ($V_{T+}-V_{T-}$) | A or B input | $V_{CC}$ = MIN | | 0.1 | 0.4 | | 0.2 | 0.4 | | V |
| $V_{OH}$ | | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = MAX | $I_{OH}$ = −3 mA | 2.4 | 3.4 | | 2.4 | 3.4 | | V |
| | | | $I_{OH}$ = −12 mA | 2 | | | | | | |
| | | | $I_{OH}$ = −15 mA | | | | 2 | | | |
| $V_{OL}$ | | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = MAX | $I_{OL}$ = 12 mA | | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | | | $I_{OL}$ = 24 mA | | | | | 0.35 | 0.5 | |
| $I_I$ | Control inputs | $V_{CC}$ = MAX, $V_I$ = 7 V | | | | 0.1 | | | 0.1 | mA |
| | A or B ports | $V_{CC}$ = MAX, $V_I$ = 5.5 V | | | | 0.1 | | | 0.1 | |
| $I_{IH}$ | Control inputs | $V_{CC}$ = MAX, $V_I$ = 2.7 V | | | | 20 | | | 20 | μA |
| | A or B ports¶ | | | | | 20 | | | 20 | |
| $I_{IL}$ | Control inputs | $V_{CC}$ = MAX, $V_I$ = 0.4 V | | | | −0.4 | | | −0.4 | mA |
| | A or B ports¶ | | | | | −0.4 | | | −0.4 | |
| $I_{OS}$§ | | $V_{CC}$ = MAX, $V_O$ = 0 V | | −40 | | −225 | −40 | | −225 | mA |
| $I_{CC}$ | LS646 | $V_{CC}$ = MAX | Outputs high | | 91 | 145 | | 91 | 145 | mA |
| | | | Outputs low | | 103 | 165 | | 103 | 165 | |
| | | | Outputs disabled | | 103 | 165 | | 103 | 165 | |
| | LS648 | | Outputs high | | 91 | 145 | | 91 | 145 | |
| | | | Outputs low | | 103 | 165 | | 103 | 165 | |
| | | | Outputs disabled | | 120 | 180 | | 120 | 180 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
¶ For I/O ports, the parameters $I_{IH}$ and $I_{IL}$ include the off-state output current.

**switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | 'LS646 | | | 'LS648 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_{PLH}$ | CAB or CBA | A or B | $R_L$ = 667 Ω, $C_L$ = 45 pF, See Note 2 | | 15 | 25 | | 15 | 25 | ns |
| $t_{PHL}$ | | | | | 23 | 35 | | 24 | 40 | ns |
| $t_{PLH}$ | A or B | B or A | | | 12 | 18 | | 12 | 18 | ns |
| $t_{PHL}$ | | | | | 13 | 20 | | 15 | 25 | ns |
| $t_{PLH}$ | SAB or SBA† with Bus input high | A or B | | | 26 | 40 | | 37 | 55 | ns |
| $t_{PHL}$ | | | | | 21 | 35 | | 24 | 40 | ns |
| $t_{PLH}$ | SAB or SBA† with Bus input low | | | | 33 | 50 | | 26 | 40 | ns |
| $t_{PHL}$ | | | | | 14 | 25 | | 23 | 40 | ns |
| $t_{PZH}$ | $\overline{G}$ | A or B | | | 33 | 55 | | 30 | 50 | ns |
| $t_{PZL}$ | | | | | 42 | 65 | | 37 | 55 | ns |
| $t_{PZH}$ | DIR | | | | 28 | 45 | | 23 | 40 | ns |
| $t_{PZL}$ | | | | | 39 | 60 | | 30 | 45 | ns |
| $t_{PHZ}$ | $\overline{G}$ | A or B | $R_L$ = 667 Ω, $C_L$ = 5 pF, See Note 2 | | 23 | 35 | | 28 | 45 | ns |
| $t_{PLZ}$ | | | | | 22 | 35 | | 22 | 35 | ns |
| $t_{PHZ}$ | DIR | | | | 20 | 30 | | 24 | 35 | ns |
| $t_{PLZ}$ | | | | | 19 | 30 | | 19 | 30 | ns |

† These parameters are measured with the internal output state of the storage register opposite to that of the input.
NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1) . . . . . 7 V
Input voltage (control inputs) . . . . . 7 V
Off-state output voltage (A and B ports) . . . . . 5.5 V
Operating free-air temperature range: SN54LS647, SN54LS649 . . . . . −55°C to 125°C
SN74LS647, SN74LS649 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

### recommended operating conditions

| | | | SN54LS647 SN54LS649 | | | SN74LS647 SN74LS649 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.5 | | | 0.6 | V |
| $V_{OH}$ | High-level output voltage | | | | 5.5 | | | 5.5 | V |
| $I_{OL}$ | Low-level output voltage | | | | 12 | | | 24 | mA |
| $t_w$ | Pulse duration | CBA or CAB high | 15 | | | 15 | | | ns |
| | | CBA or CAB low | 30 | | | 30 | | | |
| | | Data high or low | 30 | | | 30 | | | |
| $t_{su}$ | Setup time before CAB ↑ or CBA ↑ | A or B | 15 | | | 15 | | | ns |
| $t_h$ | Hold time after CAB ↑ or CBA ↑ | A or B | 0 | | | 0 | | | ns |
| $T_A$ | Operating free-air temperature | | −55 | | 125 | 0 | | 70 | °C |

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | | SN54LS647 SN54LS649 | | | SN74LS647 SN74LS649 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IK}$ | | $V_{CC}$ = MIN, $I_I$ = −18 mA | | | | −1.5 | | | −1.5 | V |
| Hysteresis ($V_{T+} - V_{T-}$) | A or B input | $V_{CC}$ = MIN | | 0.1 | 0.4 | | 0.2 | 0.4 | | V |
| $I_{OH}$ | | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = MAX, $V_{OH}$ = 5.5 V | | | | 0.1 | | | 0.1 | mA |
| $V_{OL}$ | | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = MAX | $I_{OL}$ = 12 mA | | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | | | $I_{OL}$ = 24 mA | | | | | 0.35 | 0.5 | |
| $I_I$ | A or B | $V_{CC}$ = MAX | $V_I$ = 5.5 V | | | 0.1 | | | 0.1 | mA |
| | All others | | $V_I$ = 7 V | | | 0.1 | | | 0.1 | |
| $I_{IH}$ | | $V_{CC}$ = MAX, $V_I$ = 2.7 V | | | | 20 | | | 20 | μA |
| $I_{IL}$ | | $V_{CC}$ = MAX, $V_I$ = 0.4 V | | | | −0.4 | | | −0.4 | mA |
| $I_{CC}$ | 'LS647 | $V_{CC}$ = MAX, Outputs open | Outputs high | | 79 | 130 | | 79 | 130 | mA |
| | | | Outputs low | | 94 | 150 | | 94 | 150 | |
| | 'LS649 | $V_{CC}$ = MAX, Outputs open | Outputs high | | 79 | 130 | | 79 | 130 | |
| | | | Outputs low | | 94 | 150 | | 94 | 150 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | 'LS647 | | | 'LS649 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_{PLH}$ | CAB or CBA | A or B | $R_L$ = 667 Ω, $C_L$ = 45 pF, See Note 2 | | 22 | 35 | | 17 | 30 | ns |
| $t_{PHL}$ | | | | | 28 | 45 | | 28 | 45 | ns |
| $t_{PLH}$ | A or B | B or A | | | 17 | 26 | | 15 | 25 | ns |
| $t_{PHL}$ | | | | | 18 | 27 | | 20 | 30 | ns |
| $t_{PLH}$ | SAB or SBA† with Bus input high | A or B | | | 33 | 50 | | 37 | 55 | ns |
| $t_{PHL}$ | | | | | 29 | 45 | | 28 | 45 | ns |
| $t_{PLH}$ | SAB or SBA† with Bus input low | | | | 39 | 60 | | 30 | 45 | ns |
| $t_{PHL}$ | | | | | 19 | 30 | | 26 | 40 | ns |
| $t_{PLH}$ | G | A or B | | | 25 | 40 | | 21 | 40 | ns |
| $t_{PHL}$ | | | | | 33 | 50 | | 34 | 50 | ns |
| $t_{PLH}$ | DIR | | | | 23 | 35 | | 19 | 30 | ns |
| $t_{PHL}$ | | | | | 25 | 40 | | 27 | 45 | ns |

† These parameters are measured with the internal outputs state of the storage register opposite to that of the bus input.
NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| SN74LS646DW | Active | Production | SOIC (DW) \| 24 | 25 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS646 |
| SN74LS646DW.A | Active | Production | SOIC (DW) \| 24 | 25 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS646 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

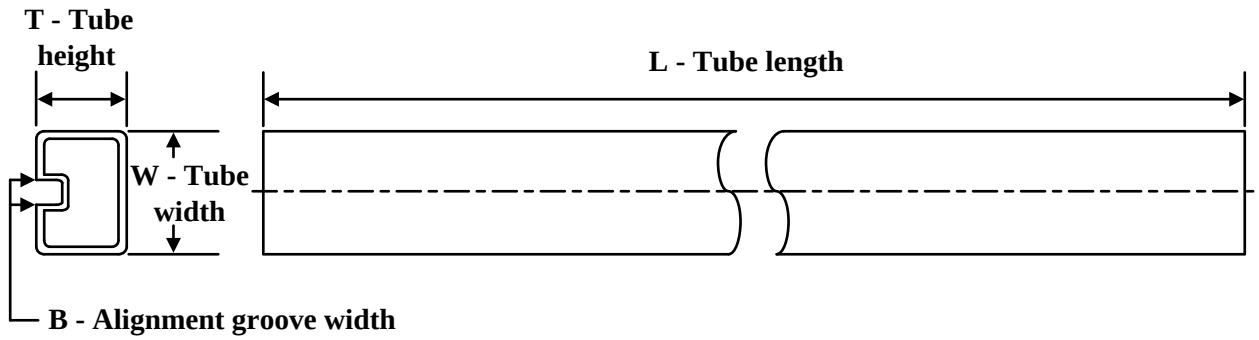
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

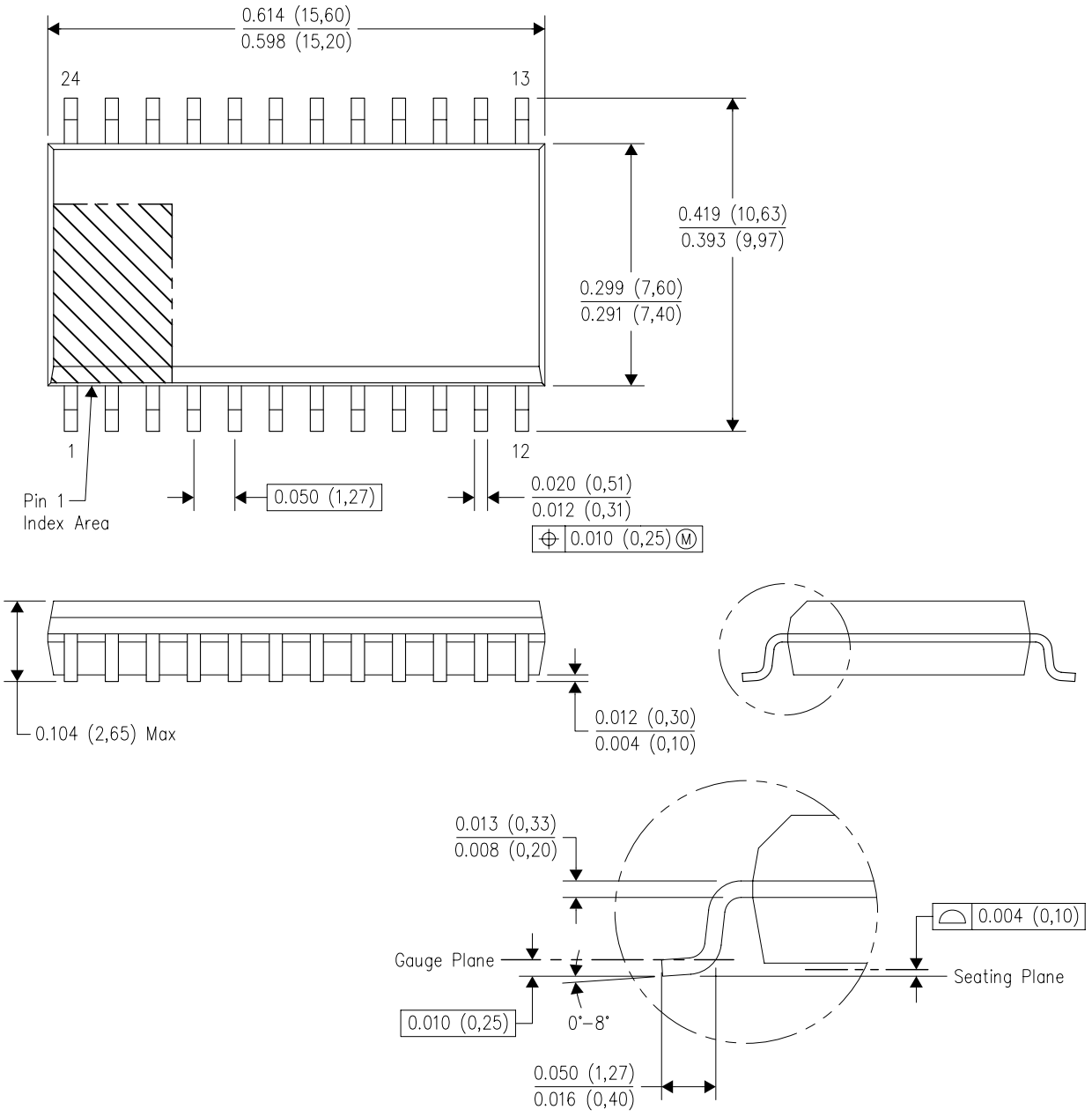
## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| SN74LS646DW | DW | SOIC | 24 | 25 | 506.98 | 12.7 | 4826 | 6.6 |
| SN74LS646DW.A | DW | SOIC | 24 | 25 | 506.98 | 12.7 | 4826 | 6.6 |

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

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