SN74LVC166A 8-Bit Parallel-Load Shift Registers with Clear

1 Features

- Operating range from 1.1V to 3.6V
- Over-voltage tolerant inputs support up to 5.5V independent of V_{CC}
- Supports partial-power-down with back drive protection (I_{off})
- High push-pull output drive strength:
  - ±24mA at 3.3V
  - ±8mA at 2.3V
  - ±4mA at 1.65V
- Maximum propagation delay of 11.2ns at 3.3V supply
- Latch-up performance exceeds 100mA per JESD78

2 Applications

- Increase the number of inputs on a microcontroller
- Read in board revision

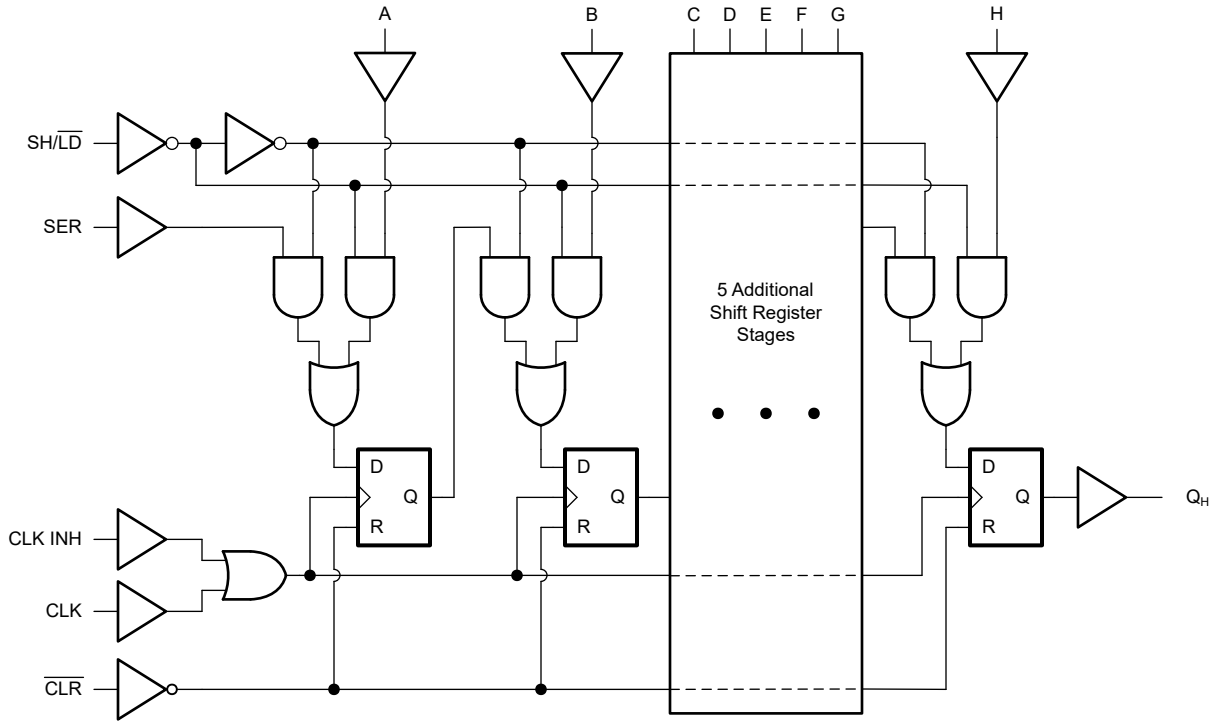
3 Description

The SN74LVC166A contains one 8-bit parallel-load shift register. Data is loaded synchronously using the shift or load (SH/$\overline{LD}$) select and clock (CLK) inputs. The device includes a serial (SER) input to allow for daisy chaining and an asynchronous clear ($\overline{CLR}$) input.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE (NOM)(3)
SN74LVC166A	BQB (WQFN, 16)	3.5mm × 2.5mm	3.5mm × 2.5mm
	D (SOIC, 16)	9.9mm × 6mm	9.9mm × 3.9mm
	PW (TSSOP, 16)	5mm × 6.4mm	5mm × 4.4mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable
(3) The body size (length × width) is a nominal value and does not include pins.



Functional Diagram

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4 Pin Configuration and Functions

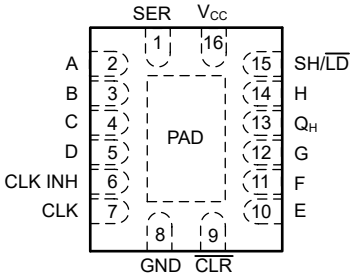


Figure 4-1. BQB Package, 16-Pin WQFN (Top View)

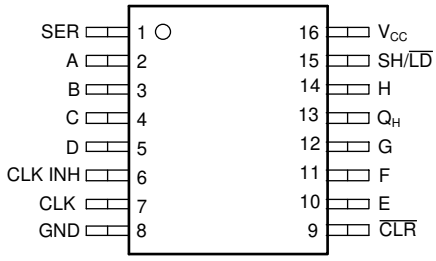


Figure 4-2. D or PW Package, 16-Pin SOIC or TSSOP (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
SER	1	I	Serial data input
A	2	I	Parallel input A
B	3	I	Parallel input B
C	4	I	Parallel input C
D	5	I	Parallel input D
CLK INH	6	I	Clock inhibit input
CLK	7	I	Clock input
GND	8	G	Ground
$\overline{CLR}$	9	I	Clock for Channel 2, rising edge triggered
E	10	O	Parallel input E
F	11	I	Parallel input F
G	12	I	Parallel input G
Q_H	13	I	Serial output
H	14	I	Parallel input H
SH/$\overline{LD}$	15	I	Enable shifting when input is high, enable loading data when input is low
V_{CC}	16	P	Positive supply
Thermal Pad[2]		—	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.
(2) BQB package only

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	6.5	V
V_I	Input voltage range(2)		-0.5	6.5	V
V_O	Output voltage range(2)		-0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0V		-50	mA
I_{OK}	Output clamp current	V_O < 0V		-50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		-65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.1	3.6	V
V_I	Input voltage		0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.8 V		-4	mA
		V_{CC} = 2.3 V		-8	
		V_{CC} = 2.7 V		-12	
		V_{CC} = 3 V		-24	
I_{OL}	Low-level output current	V_{CC} = 1.8 V		4	mA
		V_{CC} = 2.3 V		8	
		V_{CC} = 2.7 V		12	
		V_{CC} = 3 V		24	
Δt/Δv	Input transition rise or fall rate			10	ns/V
T_A	Operating free-air temperature		-40	125	°C

5.4 Thermal Information

PACKAGE	PINS	THERMAL METRIC(1)						UNIT
		$R_{\theta JA}$	$R_{\theta JC(top)}$	$R_{\theta JB}$	Ψ_{JT}	Ψ_{JB}	$R_{\theta JC(bot)}$	
PW (TSSOP)	16	141.8	74	87.1	22.3	86.6	-	°C/W
BQB (WQFN)	16	98.8	94.3	67.6	15.4	67.6	46.2	°C/W
DYY (SOT-23-THN)	16	196.3	117.4	122.9	22.3	122.7	-	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	-40°C to 125°C			UNIT
			MIN	TYP	MAX	
V_{OH}	I_{OH}= –100µA	1.1V to 3.6V	V_{CC} - 0.2	V_{CC} - 0.01		V
V_{OH}	I_{OH}= –4mA	1.65V	1.2			V
V_{OH}	I_{OH}= –8mA	2.3V	1.75			V
V_{OH}	I_{OH}= –12mA	2.7V	2.2			V
V_{OH}		3V	2.4			V
V_{OH}	I_{OH}= –24mA	3V	2.2			V
V_{OL}	I_{OL} = 100µA	1.1V to 3.6V		0.01	0.2	V
V_{OL}	I_{OL} = 4mA	1.65V			0.45	V
V_{OL}	I_{OL} = 8mA	2.3V			0.7	V
V_{OL}	I_{OL} = 12mA	2.7V			0.4	V
V_{OL}	I_{OL} = 24mA	3V			0.55	V
I_I	V_I = V_{CC} or GND	3.6V			±5	µA
I_{off}	V_I or V_O = V_{CC}	0V			±10	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	3.6V			40	µA
ΔI_{CC}	One input at V_{CC} - 0.6V, other inputs at V_{CC} or GND	2.7V to 3.6V			5000	µA
C_I	V_I = V_{CC} or GND	3.3V		4.9		pF
C_O	V_O = V_{CC} or GND	3.3V		6.3		pF
C_{PD}	f = 10MHz	1.8V		12		pF
C_{PD}	f = 10MHz	2.5V		15		pF
C_{PD}	f = 10MHz	3.3V		17		pF

5.6 Timing Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	CONDITION	V_{CC}	-40°C to 125°C		UNIT
				MIN	MAX	
F_{clock}	Clock frequency		1.2 V ± 0.1 V		59	MHz
			1.5 V ± 0.15 V		64	MHz
			1.8 V ± 0.15 V		64	MHz
			2.5 V ± 0.2 V		100	MHz
			3.3 V ± 0.3 V		104	MHz
t_W	Pulse duration	$\overline{CLR}$ low	1.2 V ± 0.1 V	6.9		ns
t_W	Pulse duration	SH/$\overline{LD}$ low	1.2 V ± 0.1 V	6.9		ns

5.6 Timing Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	CONDITION	V_{CC}	-40°C to 125°C		UNIT
				MIN	MAX	
t_W	Pulse duration	CLK	1.2 V ± 0.1 V	7		ns
t_{SU}	Setup time	SH/$\overline{LD}$ high before CLK↑	1.2 V ± 0.1 V	16.5		ns
t_{SU}	Setup time	SER before CLK↑	1.2 V ± 0.1 V	10.1		ns
t_{SU}	Setup time	CLK INH before CLK↑	1.2 V ± 0.1 V	1		ns
t_{SU}	Setup time	Data before CLK↑	1.2 V ± 0.1 V	10		ns
t_{SU}	Setup time	$\overline{CLR}$ inactive before CLK↑	1.2 V ± 0.1 V	10.1		ns
t_H	Hold time	SER data after CLK↑	1.2 V ± 0.1 V	0.4		ns
t_H	Hold time	Parallel data after SH/$\overline{LD}$↓	1.2 V ± 0.1 V	1.8		ns
t_H	Hold time	SH/$\overline{LD}$ high after CLK↑	1.2 V ± 0.1 V	0		ns
t_H	Hold time	CLK INH high after CLK↑	1.2 V ± 0.1 V	0.4		ns
t_H	Hold time	Data after CLK↑	1.2 V ± 0.1 V	1		ns
t_W	Pulse duration	$\overline{CLR}$ low	1.5 V ± 0.15 V	6.9		ns
t_W	Pulse duration	SH/$\overline{LD}$ low	1.5 V ± 0.15 V	6.9		ns
t_W	Pulse duration	CLK	1.5 V ± 0.15 V	7		ns
t_{SU}	Setup time	SH/$\overline{LD}$ high before CLK↑	1.5 V ± 0.15 V	10		ns
t_{SU}	Setup time	SER before CLK↑	1.5 V ± 0.15 V	10.1		ns
t_{SU}	Setup time	CLK INH before CLK↑	1.5 V ± 0.15 V	1		ns
t_{SU}	Setup time	Data before CLK↑	1.5 V ± 0.15 V	10		ns
t_{SU}	Setup time	$\overline{CLR}$ inactive before CLK↑	1.5 V ± 0.15 V	10.1		ns
t_H	Hold time	SER data after CLK↑	1.5 V ± 0.15 V	1.2		ns
t_H	Hold time	Parallel data after SH/$\overline{LD}$↓	1.5 V ± 0.15 V	1.9		ns
t_H	Hold time	SH/$\overline{LD}$ high after CLK↑	1.5 V ± 0.15 V	1		ns
t_H	Hold time	CLK INH high after CLK↑	1.5 V ± 0.15 V	0.6		ns
t_H	Hold time	Data after CLK↑	1.5 V ± 0.15 V	1.8		ns
t_W	Pulse duration	$\overline{CLR}$ low	1.8 V ± 0.15 V	6.9		ns
t_W	Pulse duration	SH/$\overline{LD}$ low	1.8 V ± 0.15 V	6.9		ns
t_W	Pulse duration	CLK	1.8 V ± 0.15 V	7		ns
t_{SU}	Setup time	SH/$\overline{LD}$ high before CLK↑	1.8 V ± 0.15 V	8		ns
t_{SU}	Setup time	SER before CLK↑	1.8 V ± 0.15 V	10.1		ns
t_{SU}	Setup time	CLK INH before CLK↑	1.8 V ± 0.15 V	1		ns
t_{SU}	Setup time	Data before CLK↑	1.8 V ± 0.15 V	8		ns
t_{SU}	Setup time	$\overline{CLR}$ inactive before CLK↑	1.8 V ± 0.15 V	10.1		ns
t_H	Hold time	SER data after CLK↑	1.8 V ± 0.15 V	0.2		ns
t_H	Hold time	Parallel data after SH/$\overline{LD}$↓	1.8 V ± 0.15 V	0.8		ns
t_H	Hold time	SH/$\overline{LD}$ high after CLK↑	1.8 V ± 0.15 V	0		ns
t_H	Hold time	CLK INH high after CLK↑	1.8 V ± 0.15 V	0.3		ns
t_H	Hold time	Data after CLK↑	1.8 V ± 0.15 V	1		ns
t_W	Pulse duration	$\overline{CLR}$ low	2.5 V ± 0.2 V	5.4		ns
t_W	Pulse duration	SH/$\overline{LD}$ low	2.5 V ± 0.2 V	5.4		ns
t_W	Pulse duration	CLK	2.5 V ± 0.2 V	4.5		ns
t_{SU}	Setup time	SH/$\overline{LD}$ high before CLK↑	2.5 V ± 0.2 V	4.5		ns
t_{SU}	Setup time	SER before CLK↑	2.5 V ± 0.2 V	5.9		ns
t_{SU}	Setup time	CLK INH before CLK↑	2.5 V ± 0.2 V	1		ns

5.6 Timing Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	CONDITION	V_{CC}	-40°C to 125°C		UNIT
				MIN	MAX	
t_{SU}	Setup time	Data before CLK↑	2.5 V ± 0.2 V	4.5		ns
t_{SU}	Setup time	$\overline{CLR}$ inactive before CLK↑	2.5 V ± 0.2 V	5.9		ns
t_H	Hold time	SER data after CLK↑	2.5 V ± 0.2 V	0.5		ns
t_H	Hold time	Parallel data after SH/$\overline{LD}$↓	2.5 V ± 0.2 V	0		ns
t_H	Hold time	SH/$\overline{LD}$ high after CLK↑	2.5 V ± 0.2 V	0.1		ns
t_H	Hold time	CLK INH high after CLK↑	2.5 V ± 0.2 V	0.3		ns
t_H	Hold time	Data after CLK↑	2.5 V ± 0.2 V	1.5		ns
t_W	Pulse duration	$\overline{CLR}$ low	3.3 V ± 0.3 V	4.3		ns
t_W	Pulse duration	SH/$\overline{LD}$ low	3.3 V ± 0.3 V	4.3		ns
t_W	Pulse duration	CLK	3.3 V ± 0.3 V	4.3		ns
t_{SU}	Setup time	SH/$\overline{LD}$ high before CLK↑	3.3 V ± 0.3 V	3.5		ns
t_{SU}	Setup time	SER before CLK↑	3.3 V ± 0.3 V	4		ns
t_{SU}	Setup time	CLK INH before CLK↑	3.3 V ± 0.3 V	1		ns
t_{SU}	Setup time	Data before CLK↑	3.3 V ± 0.3 V	2.9		ns
t_{SU}	Setup time	$\overline{CLR}$ inactive before CLK↑	3.3 V ± 0.3 V	4		ns
t_H	Hold time	SER data after CLK↑	3.3 V ± 0.3 V	0.5		ns
t_H	Hold time	Parallel data after SH/$\overline{LD}$↓	3.3 V ± 0.3 V	0		ns
t_H	Hold time	SH/$\overline{LD}$ high after CLK↑	3.3 V ± 0.3 V	0.2		ns
t_H	Hold time	CLK INH high after CLK↑	3.3 V ± 0.3 V	0.5		ns
t_H	Hold time	Data after CLK↑	3.3 V ± 0.3 V	1.5		ns

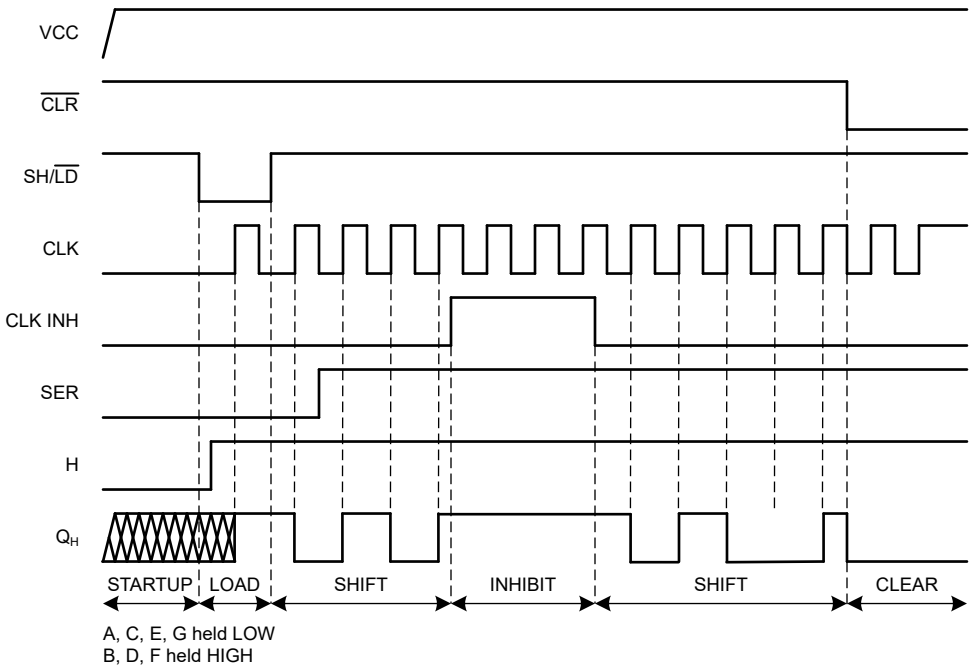


Figure 5-1. Timing Diagram

5.7 Switching Characteristics

over operating free-air temperature range(unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	-40°C to 125°C			UNIT
					MIN	TYP	MAX	
t_{pd}	CLK	Q_H	C_L = 15pF	1.2V ± 0.1V	1		27.6	ns
t_{pd}	$\overline{CLR}$	Q_H	C_L = 15pF	1.2V ± 0.1V	1		27.6	ns
t_{pd}	H	Q_H	C_L = 15pF	1.2V ± 0.1V	1		36.3	ns
t_{pd}	SH/$\overline{LD}$	Q_H	C_L = 15pF	1.2V ± 0.1V	1		40.2	ns
t_{pd}	CLK	Q_H	C_L = 30pF	1.2V ± 0.1V	1		27.6	ns
t_{pd}	$\overline{CLR}$	Q_H	C_L = 30pF	1.2V ± 0.1V	1		27.6	ns
t_{pd}	H	Q_H	C_L = 30pF	1.2V ± 0.1V	1		36.3	ns
t_{pd}	SH/$\overline{LD}$	Q_H	C_L = 30pF	1.2V ± 0.1V	1		40.2	ns
t_{pd}	CLK	Q_H	C_L = 50pF	1.2V ± 0.1V	1		32.8	ns
t_{pd}	$\overline{CLR}$	Q_H	C_L = 50pF	1.2V ± 0.1V	1		32.8	ns
t_{pd}	H	Q_H	C_L = 50pF	1.2V ± 0.1V	1		38.5	ns
t_{pd}	SH/$\overline{LD}$	Q_H	C_L = 50pF	1.2V ± 0.1V	1		45.4	ns
t_{pd}	CLK	Q_H	C_L = 15pF	1.5V ± 0.15V	1		27.6	ns
t_{pd}	$\overline{CLR}$	Q_H	C_L = 15pF	1.5V ± 0.15V	1		27.6	ns
t_{pd}	H	Q_H	C_L = 15pF	1.5V ± 0.15V	1		36.3	ns
t_{pd}	SH/$\overline{LD}$	Q_H	C_L = 15pF	1.5V ± 0.15V	1		40.2	ns
t_{pd}	CLK	Q_H	C_L = 30pF	1.5V ± 0.15V	1		27.6	ns
t_{pd}	$\overline{CLR}$	Q_H	C_L = 30pF	1.5V ± 0.15V	1		27.6	ns
t_{pd}	H	Q_H	C_L = 30pF	1.5V ± 0.15V	1		36.3	ns
t_{pd}	SH/$\overline{LD}$	Q_H	C_L = 30pF	1.5V ± 0.15V	1		40.2	ns
t_{pd}	CLK	Q_H	C_L = 50pF	1.5V ± 0.15V	1		32.8	ns
t_{pd}	$\overline{CLR}$	Q_H	C_L = 50pF	1.5V ± 0.15V	1		32.8	ns
t_{pd}	H	Q_H	C_L = 50pF	1.5V ± 0.15V	1		41.5	ns
t_{pd}	SH/$\overline{LD}$	Q_H	C_L = 50pF	1.5V ± 0.15V	1		45.4	ns
t_{pd}	CLK	Q_H	C_L = 15pF	1.8V ± 0.15V	1		27.6	ns
t_{pd}	$\overline{CLR}$	Q_H	C_L = 15pF	1.8V ± 0.15V	1		27.6	ns
t_{pd}	H	Q_H	C_L = 15pF	1.8V ± 0.15V	1		36.3	ns
t_{pd}	SH/LD	Q_H	C_L = 15pF	1.8V ± 0.15V	1		40.2	ns
t_{pd}	CLK	Q_H	C_L = 30pF	1.8V ± 0.15V	1		27.6	ns
t_{pd}	$\overline{CLR}$	Q_H	C_L = 30pF	1.8V ± 0.15V	1		27.6	ns
t_{pd}	H	Q_H	C_L = 30pF	1.8V ± 0.15V	1		36.3	ns
t_{pd}	SH/$\overline{LD}$	Q_H	C_L = 30pF	1.8V ± 0.15V	1		40.2	ns
t_{pd}	CLK	Q_H	C_L = 50pF	1.8V ± 0.15V	1		32.8	ns
t_{pd}	$\overline{CLR}$	Q_H	C_L = 50pF	1.8V ± 0.15V	1		32.8	ns
t_{pd}	H	Q_H	C_L = 50pF	1.8V ± 0.15V	1		41.5	ns
t_{pd}	SH/$\overline{LD}$	Q_H	C_L = 50pF	1.8V ± 0.15V	1		45.4	ns
t_{pd}	CLK	Q_H	C_L = 15pF	2.5V ± 0.2V	1		16	ns
t_{pd}	$\overline{CLR}$	Q_H	C_L = 15pF	2.5V ± 0.2V	1		16	ns
t_{pd}	H	Q_H	C_L = 15pF	2.5V ± 0.2V	1		21	ns
t_{pd}	SH/$\overline{LD}$	Q_H	C_L = 15pF	2.5V ± 0.2V	1		23.8	ns
t_{pd}	CLK	Q_H	C_L = 30pF	2.5V ± 0.2V	1		16	ns
t_{pd}	$\overline{CLR}$	Q_H	C_L = 30pF	2.5V ± 0.2V	1		16	ns
t_{pd}	H	Q_H	C_L = 30pF	2.5V ± 0.2V	1		21	ns

5.7 Switching Characteristics (continued)

over operating free-air temperature range(unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	-40°C to 125°C			UNIT
					MIN	TYP	MAX	
t_{pd}	SH/$\overline{LD}$	Q_H	C_L = 30pF	2.5V ± 0.2V	1		23.8	ns
t_{pd}	CLK	Q_H	C_L = 50pF	2.5V ± 0.2V	1		20	ns
t_{pd}	$\overline{CLR}$	Q_H	C_L = 50pF	2.5V ± 0.2V	1		20	ns
t_{pd}	H	Q_H	C_L = 50pF	2.5V ± 0.2V	1		25	ns
t_{pd}	SH/$\overline{LD}$	Q_H	C_L = 50pF	2.5V ± 0.2V	1		27.7	ns
t_{pd}	CLK	Q_H	C_L = 15pF	3.3V ± 0.3V	1		11.2	ns
t_{pd}	$\overline{CLR}$	Q_H	C_L = 15pF	3.3V ± 0.3V	1		11.2	ns
t_{pd}	H	Q_H	C_L = 15pF	3.3V ± 0.3V	1		14.5	ns
t_{pd}	SH/$\overline{LD}$	Q_H	C_L = 15pF	3.3V ± 0.3V	1		16.6	ns
t_{pd}	CLK	Q_H	C_L = 30pF	3.3V ± 0.3V	1		11.2	ns
t_{pd}	$\overline{CLR}$	Q_H	C_L = 30pF	3.3V ± 0.3V	1		11.2	ns
t_{pd}	H	Q_H	C_L = 30pF	3.3V ± 0.3V	1		14.5	ns
t_{pd}	SH/$\overline{LD}$	Q_H	C_L = 30pF	3.3V ± 0.3V	1		16.6	ns
t_{pd}	CLK	Q_H	C_L = 50pF	3.3V ± 0.3V	1		14.5	ns
t_{pd}	$\overline{CLR}$	Q_H	C_L = 50pF	3.3V ± 0.3V	1		14.5	ns
t_{pd}	H	Q_H	C_L = 50pF	3.3V ± 0.3V	1		17.8	ns
t_{pd}	SH/$\overline{LD}$	Q_H	C_L = 50pF	3.3V ± 0.3V	1		19.9	ns

5.8 Noise Characteristics

VCC = 3.3 V, CL = 50 pF, TA = 25°C

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}			0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}	-0.8	-0.3		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	2.2	3.3		V
$V_{IH(D)}$	High-level dynamic input voltage	2.0			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

5.9 Typical Characteristics

T_A = 25°C (unless otherwise noted)

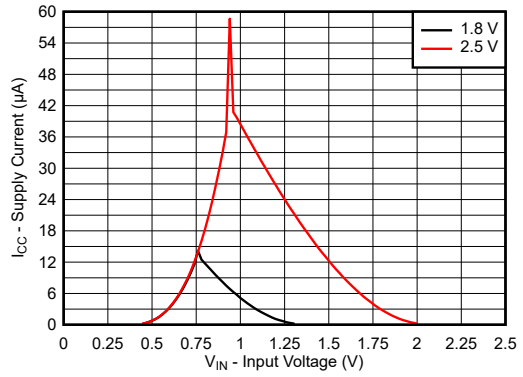


Figure 5-2. Supply Current Across Input Voltage 1.8V and 2.5V Supply

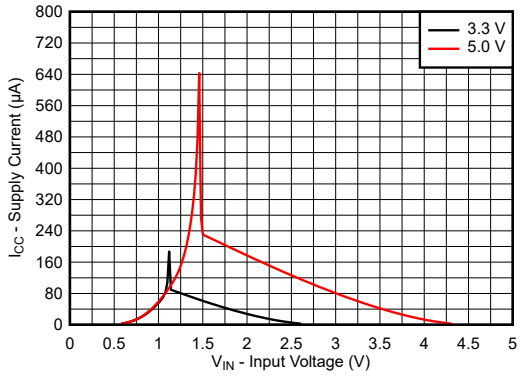


Figure 5-3. Supply Current Across Input Voltage 3.3V and 5.0V Supply

5.9 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

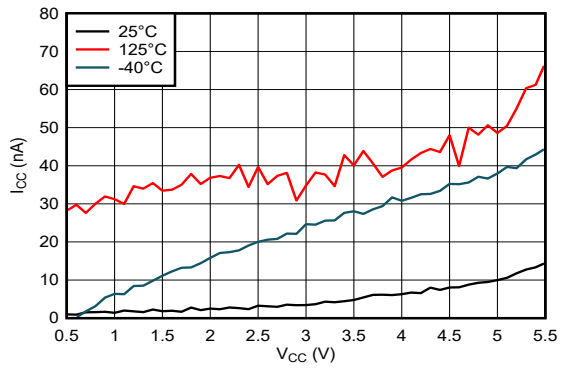


Figure 5-4. Supply Current Across Supply Voltage

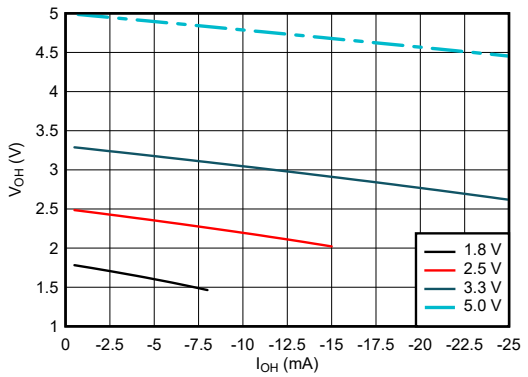


Figure 5-5. Output Voltage vs Current in HIGH State

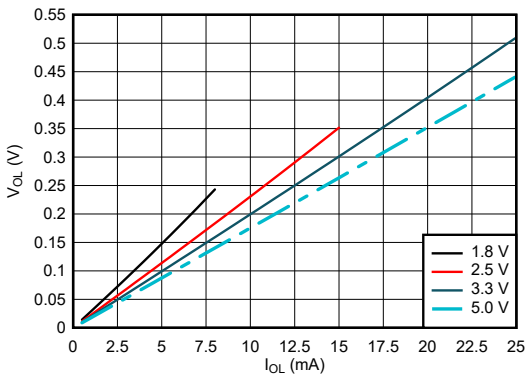


Figure 5-6. Output Voltage vs Current in LOW State

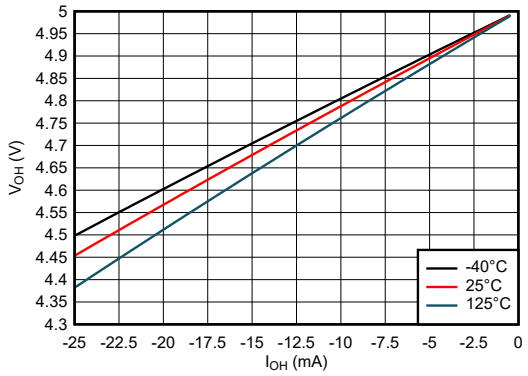


Figure 5-7. Output Voltage vs Current in HIGH State; 5V Supply

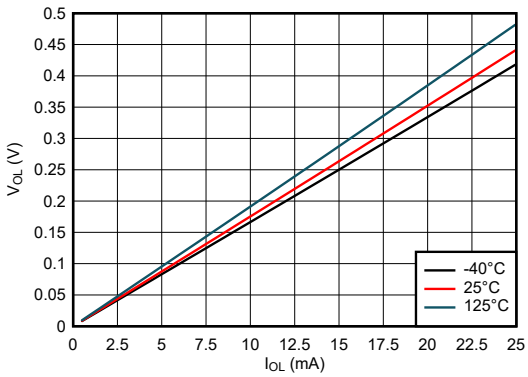


Figure 5-8. Output Voltage vs Current in LOW State; 5V Supply

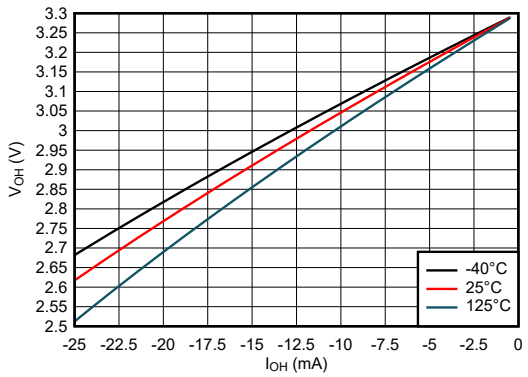


Figure 5-9. Output Voltage vs Current in HIGH State; 3.3V Supply

5.9 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

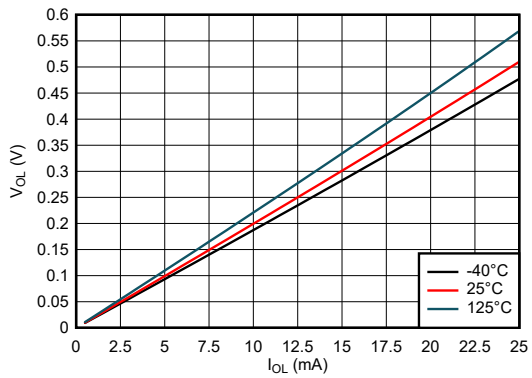


Figure 5-10. Output Voltage vs Current in LOW State; 3.3V Supply

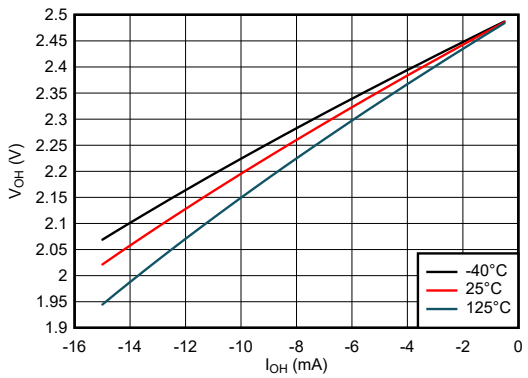


Figure 5-11. Output Voltage vs Current in HIGH State; 2.5V Supply

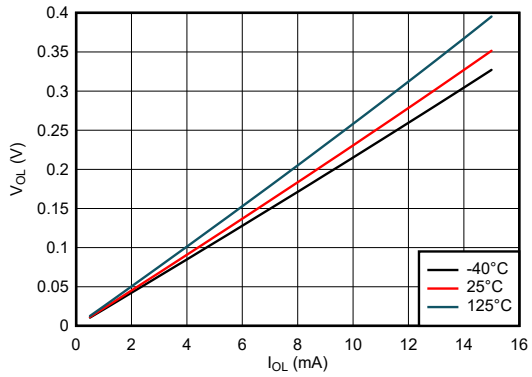


Figure 5-12. Output Voltage vs Current in LOW State; 2.5V Supply

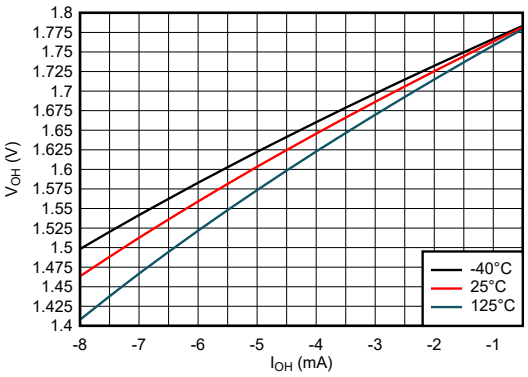


Figure 5-13. Output Voltage vs Current in HIGH State; 1.8V Supply

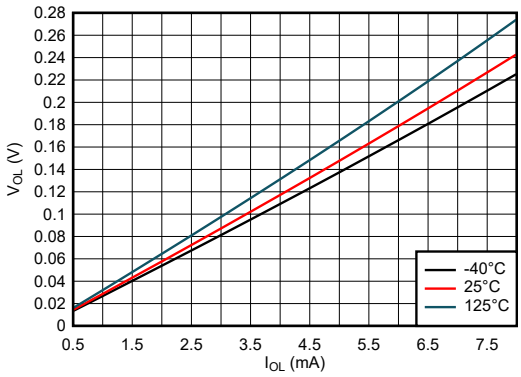


Figure 5-14. Output Voltage vs Current in LOW State; 1.8V Supply

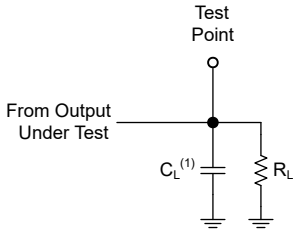
6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50Ω, t_t ≤ 2.5ns.

For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured individually with one input transition per measurement.

V_{CC}	V_t	R_L	C_L	ΔV
1.2V ± 0.1V	V_{CC}/2	2kΩ	15pF	0.1V
1.5V ± 0.12V	V_{CC}/2	2kΩ	15pF	0.1V
1.8V ± 0.15V	V_{CC}/2	1kΩ	30pF	0.15V
2.5V ± 0.2V	V_{CC}/2	500Ω	30pF	0.15V
2.7V	1.5V	500Ω	50pF	0.3V
3.3V ± 0.3V	1.5V	500Ω	50pF	0.3V



(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for Push-Pull Outputs

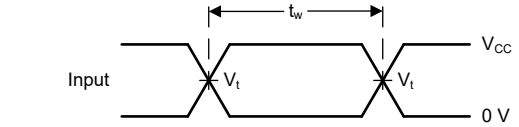


Figure 6-2. Voltage Waveforms, Pulse Duration

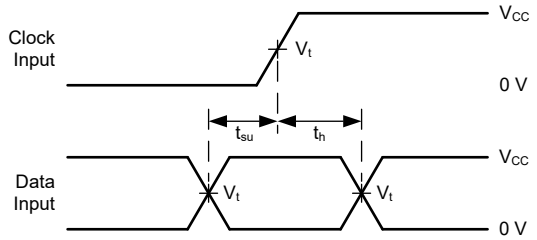
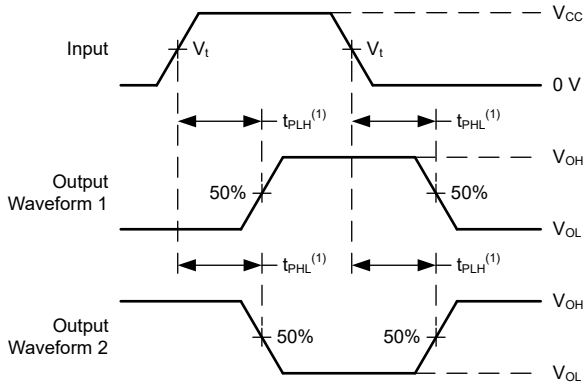
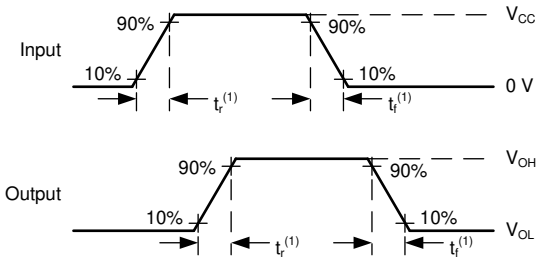


Figure 6-3. Voltage Waveforms, Setup and Hold Times



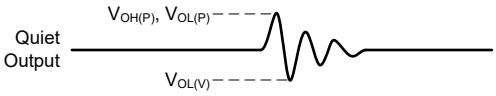
(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

Figure 6-4. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t.

Figure 6-5. Voltage Waveforms, Input and Output Transition Times



Noise values measured with all other outputs simultaneously switching.

Figure 6-6. Voltage Waveforms, Noise

7 Detailed Description

7.1 Overview

The SN74LVC166A is a parallel-load 8-bit shift register with asynchronous clear ($\overline{CLR}$). This parallel-in or serial-in, serial-out shift register features gated clock (CLK, CLK INH) inputs and an overriding clear ($\overline{CLR}$) input. The parallel-in or serial-in modes are established by the mode select (SH/$\overline{LD}$) input. When high, SH/$\overline{LD}$ enables the serial (SER) data input and couples the eight flip-flops for serial shifting with each clock (CLK) pulse. When low, the parallel (A through H) data inputs are enabled, and synchronous loading occurs on the next clock pulse.

During parallel loading, serial data flow is inhibited. Clocking is accomplished on the rising edge of CLK or CLK INH, permitting one input to be used as a clock-enable or clock-inhibit function. Holding either CLK or CLK INH high inhibits clocking; holding either low enables the other clock input. CLK INH should be changed to the high level only when CLK is high.

$\overline{CLR}$ overrides all other inputs, including CLK, and resets all flip-flops to zero.

7.2 Functional Block Diagram

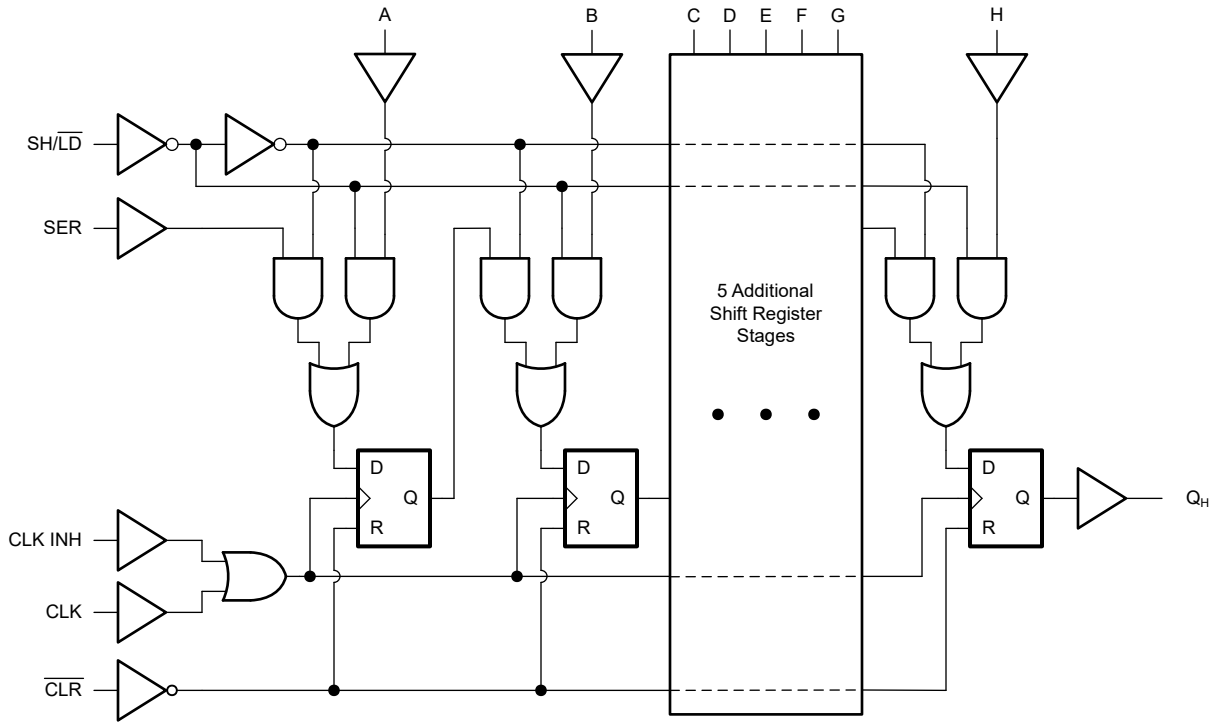


Figure 7-1. Logic Diagram (Positive Logic) for SN74LVC166A

7.3 Feature Description

7.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important to limit the output power of the device to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs must be left disconnected.

7.3.2 Latching Logic

This device includes latching logic circuitry. Latching circuits commonly include D-type latches and D-type flip-flops, but include all logic circuits that act as volatile memory.

When the device is powered on, the state of each latch is unknown. There is no default state for each latch at start-up.

The output state of each latching logic circuit only remains stable as long as power is applied to the device within the supply voltage range specified in the *Recommended Operating Conditions* table.

7.3.3 Partial Power Down (I_{off})

This device includes circuitry to disable all outputs when the supply pin is held at 0V. When disabled, the outputs will neither source nor sink current, regardless of the input voltages applied. The amount of leakage current at each output is defined by the I_{off} specification in the *Electrical Characteristics* table.

7.3.4 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in *Implications of Slow or Floating CMOS Inputs*.

Do not leave standard CMOS inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; a 10kΩ resistor, however, is recommended and will typically meet all requirements.

7.3.5 Clamp Diode Structure

Figure 7-2 shows the inputs and outputs to this device have negative clamping diodes only.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

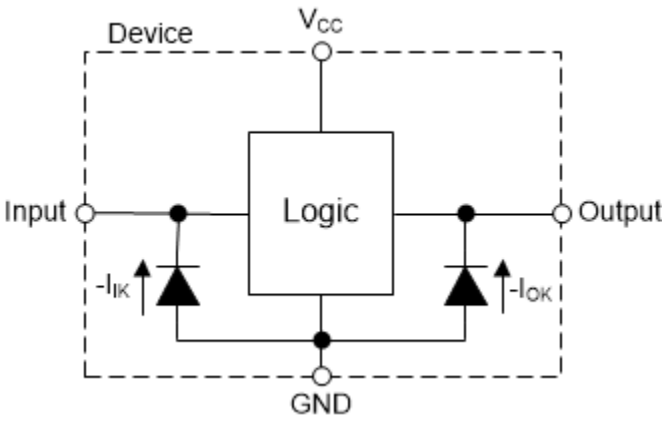


Figure 7-2. Electrical Placement of Clamping Diodes for Each Input and Output

7.4 Device Functional Modes

Table 7-1 lists the functional modes of the SN74LVC166A.

Table 7-1. Operating Mode Table

INPUTS(1)			FUNCTION
SH/$\overline{LD}$	CLK	CLK INH	
L	X	X	Parallel load(2)
H	H	X	No change
H	X	H	No change
H	L	↑	Shift(3)
H	↑	L	Shift(3)

(1) H = High voltage level, L = Low voltage level, X = Don't care, ↑ = Low to high transition
(2) Parallel load : Values at inputs A through H are loaded to respective internal registers synchronously with the clock.
(3) Shift : Content of each internal register shifts towards serial output Q_H synchronously with the clock. Data at SER is shifted into the first register.

Table 7-2. Output Function Table

INTERNAL REGISTERS(1) (2)		OUTPUTS(3)
A — G	H	Q
X	L	L
X	H	H

(1) Internal registers refer to the shift registers inside the device. These values are set by loading data from the parallel or serial inputs.
(2) H = High voltage level, L = Low voltage level, X = Don't care
(3) H = Driving high, L = Driving low

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

In this application, the SN74LVC166A is used to increase the number of inputs on a microcontroller. Unlike other I/O expanders, the SN74LVC166A does not need a communication interface for control. It can be easily operated with simple GPIO pins.

At power-up, the initial states of the internal shift registers are unknown. To give them a defined state of zero, the device can be cleared by applying a low signal to the clear ($\overline{CLR}$) input. Alternatively, data can be loaded in directly by switching to load mode (SH/$\overline{LD}$ = low), then pulsing the clock (CLK) input once.

8.2 Typical Application

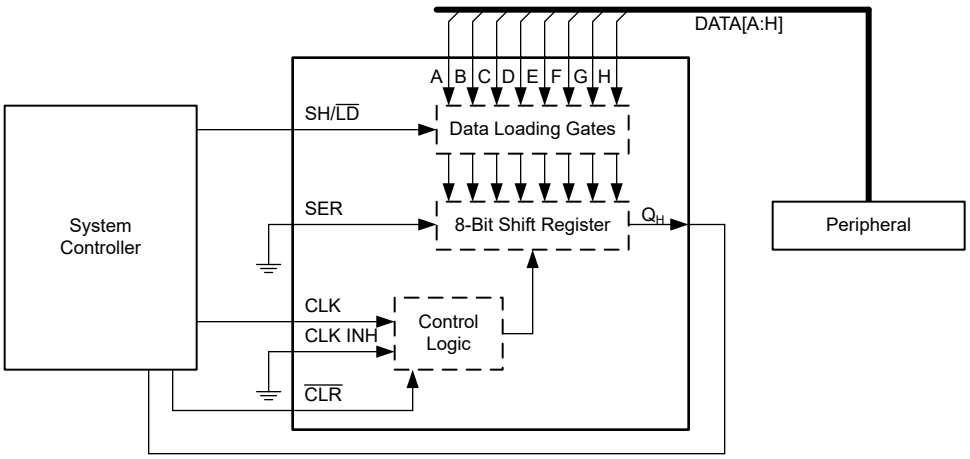


Figure 8-1. Typical Application Block Diagram

8.2.1 Design Requirements

8.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74LVC166A plus the maximum static supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Ensure the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74LVC166A plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Ensure the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SN74LVC166A can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The SN74LVC166A can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL}. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in *CMOS Power Consumption and Cpd Calculation*.

Thermal increase can be calculated using the information provided in *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices*.

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

8.2.1.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74LVC166A (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10kΩ resistor value is often used due to these factors.

The SN74LVC166A has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.

2. Ensure the capacitive load at the output is ≤ 50pF. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74LVC166A to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than (V_{CC} / $I_{O(max)}$)Ω. Doing this will prevent the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, *CMOS Power Consumption and Cpd Calculation*.

8.2.3 Application Curves

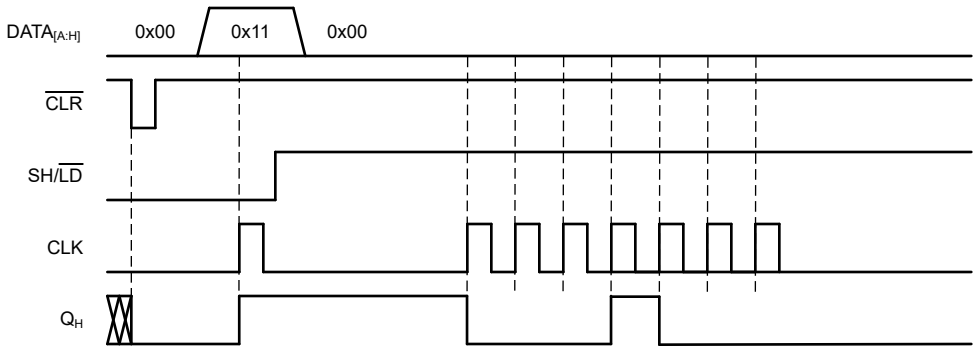


Figure 8-2. Application Timing Diagram

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the *Recommended Operating Conditions*.

During startup, the power supply should ramp within the provided power-up ramp rate range in the *Recommended Operating Conditions* table.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For the SN74LVC166A, a 0.1µF bypass capacitor is recommended. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1µF and 1µF are commonly used in parallel.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

8.4.2 Layout Example

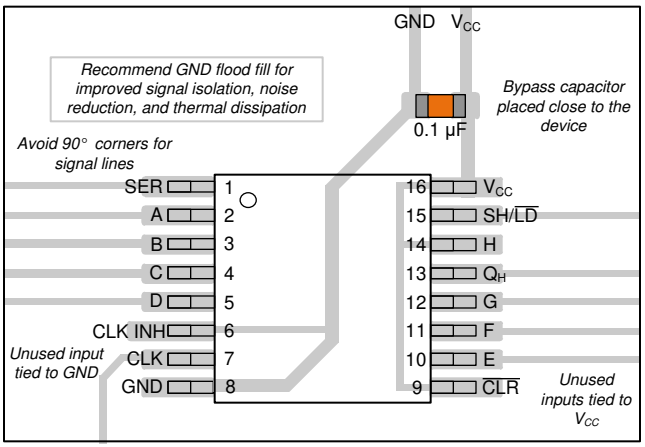


Figure 8-3. Example Layout for the SN74LVC166A

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and Cpd Calculation* application note
- Texas Instruments, *Designing With Logic* application note
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note
- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application note

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

DATE	REVISON	NOTES
May 2024	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC166ABQBR	Active	Production	WQFN (BQB) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC166A
SN74LVC166ABQBR.A	Active	Production	WQFN (BQB) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC166A
SN74LVC166ADR	Active	Production	SOIC (D) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC166A
SN74LVC166ADR.A	Active	Production	SOIC (D) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC166A
SN74LVC166APWR	Active	Production	TSSOP (PW) | 16	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LVC166
SN74LVC166APWR.A	Active	Production	TSSOP (PW) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC166

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

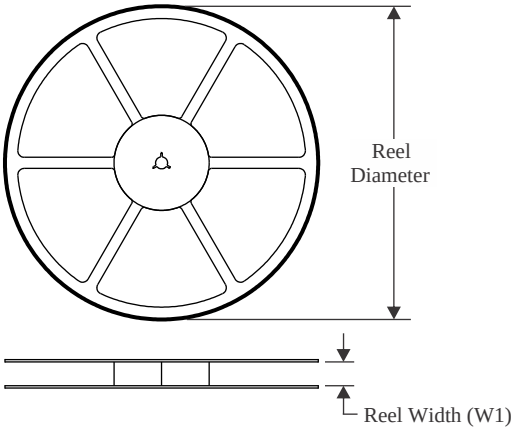
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

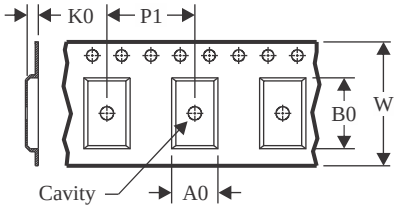
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

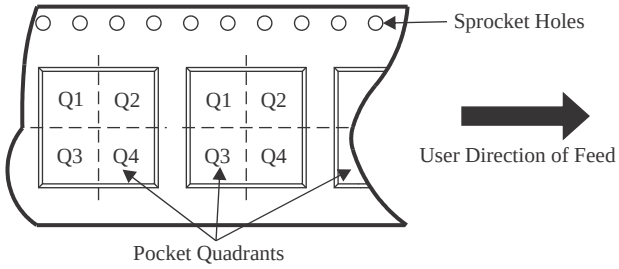


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

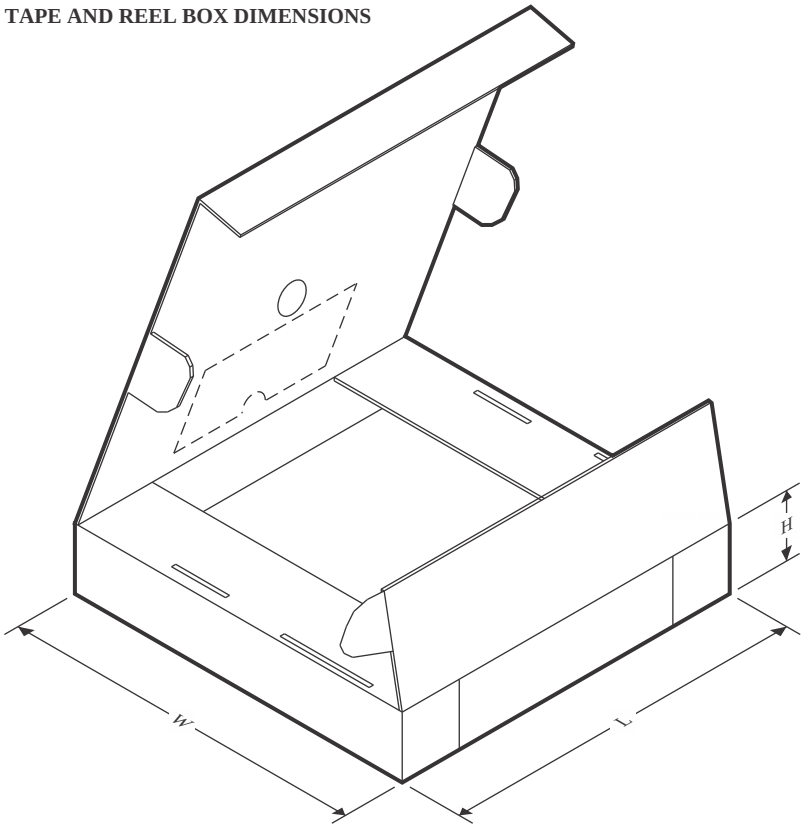
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC166ABQBR	WQFN	BQB	16	3000	180.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
SN74LVC166ADR	SOIC	D	16	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
SN74LVC166APWR	TSSOP	PW	16	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

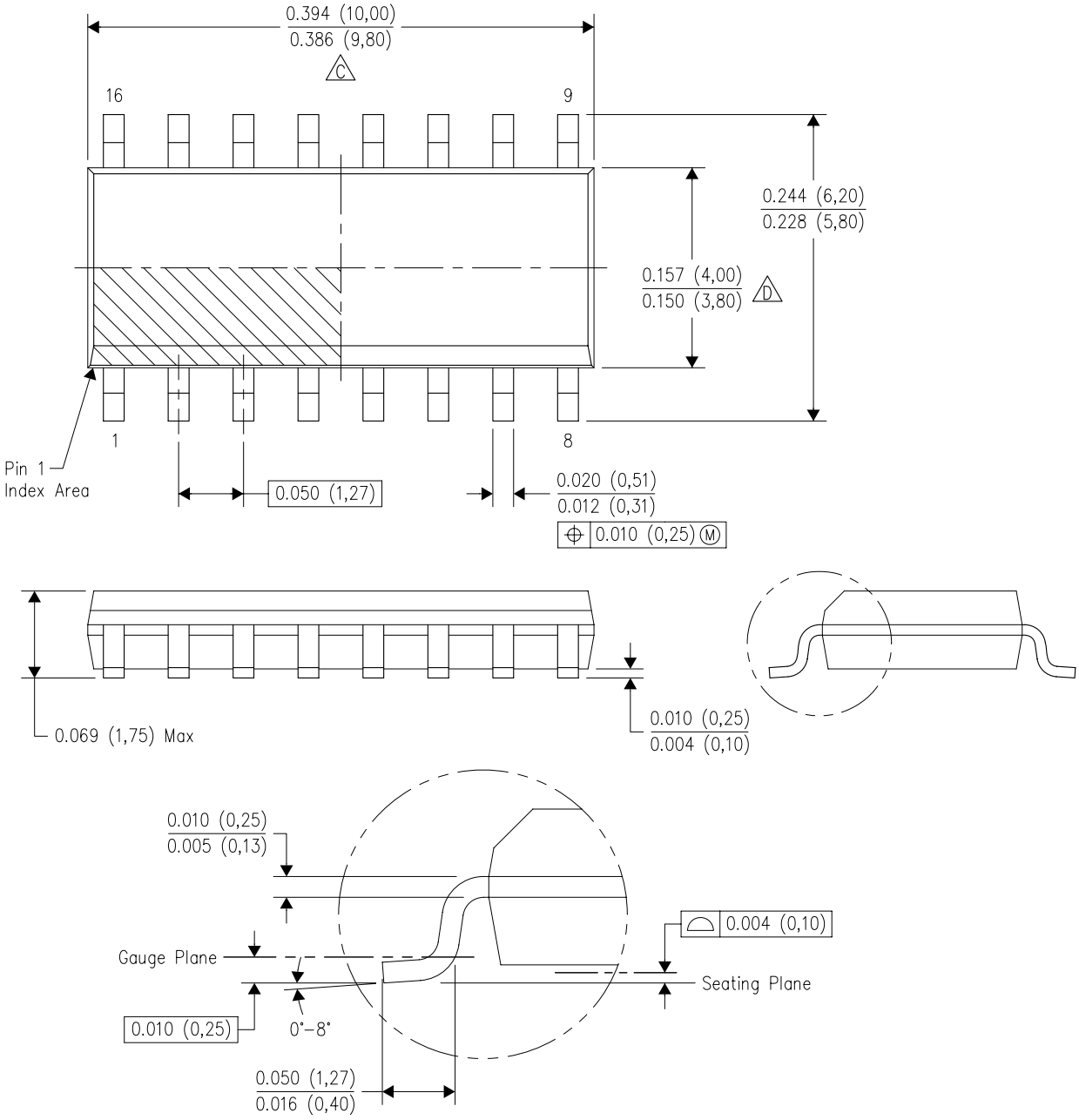
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC166ABQBR	WQFN	BQB	16	3000	210.0	185.0	35.0
SN74LVC166ADR	SOIC	D	16	3000	340.5	336.1	32.0
SN74LVC166APWR	TSSOP	PW	16	3000	353.0	353.0	32.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

GENERIC PACKAGE VIEW

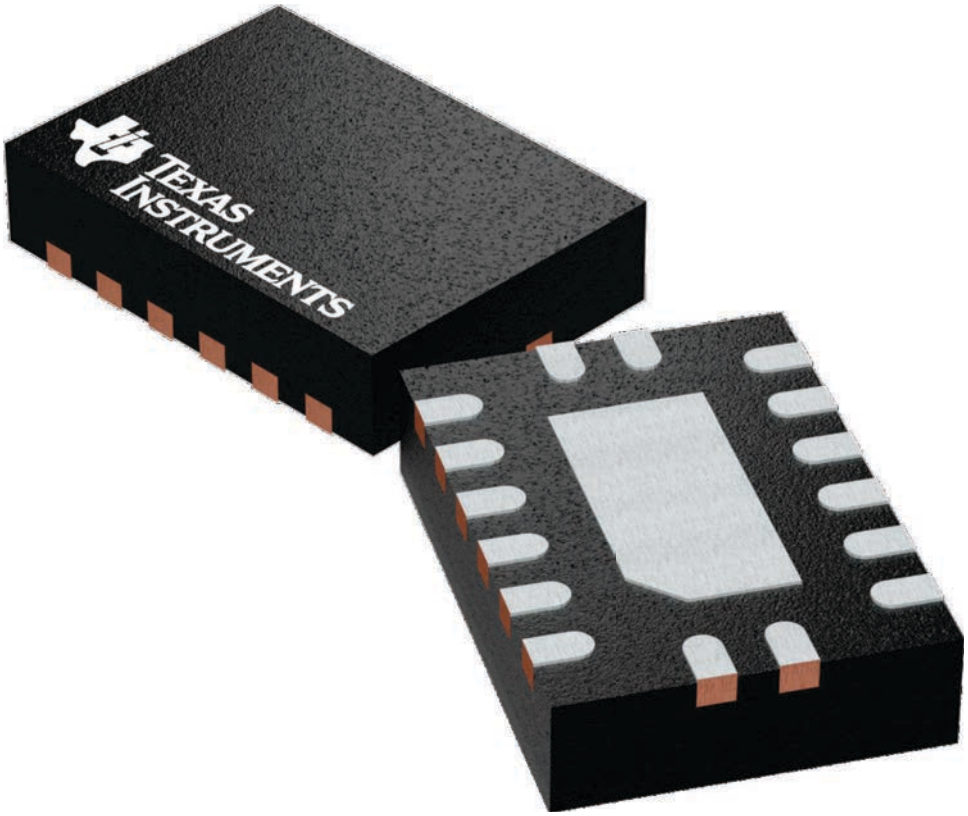
BQB 16

WQFN - 0.8 mm max height

2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



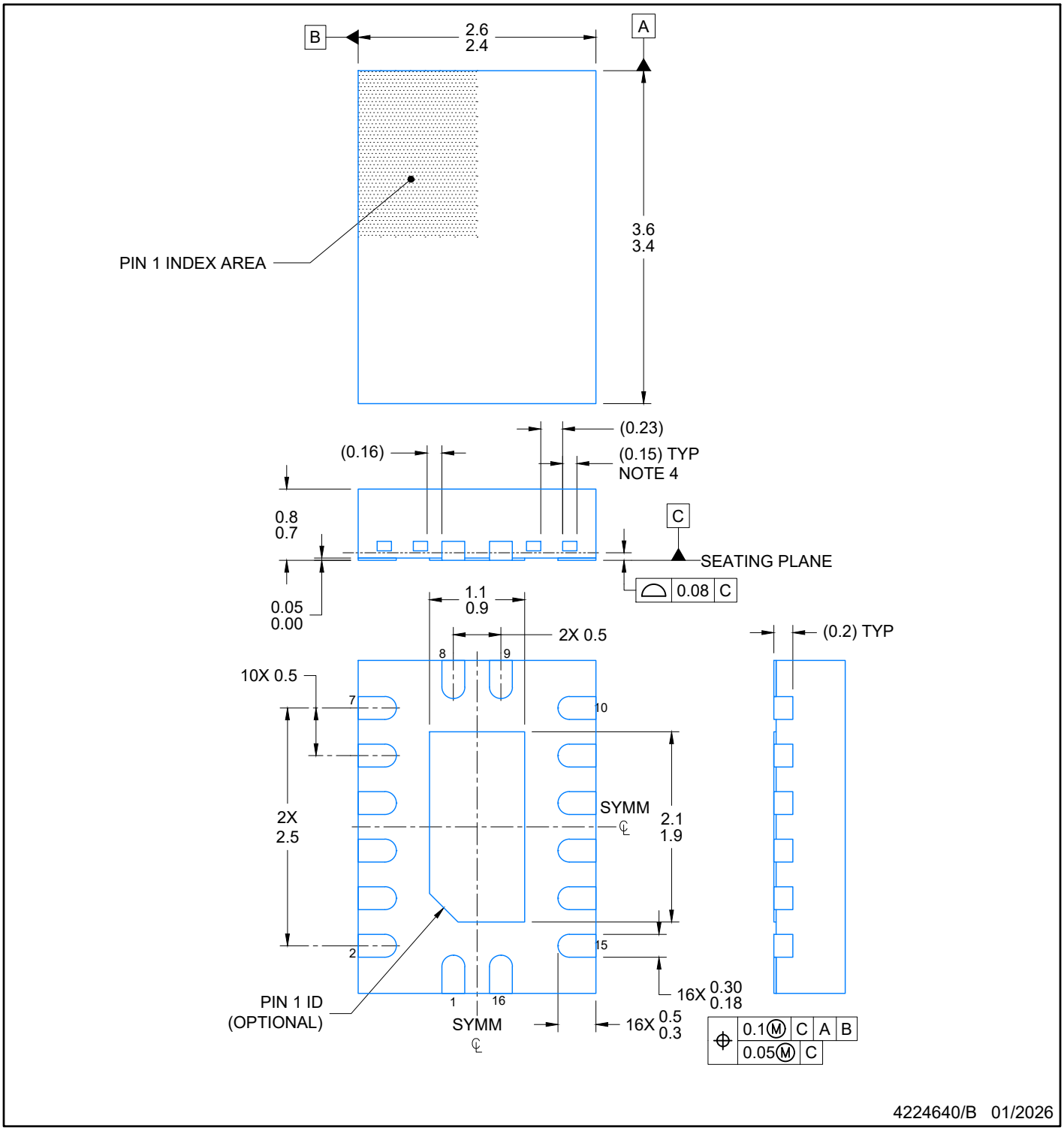
4226161/A

PACKAGE OUTLINE

BQB0016A

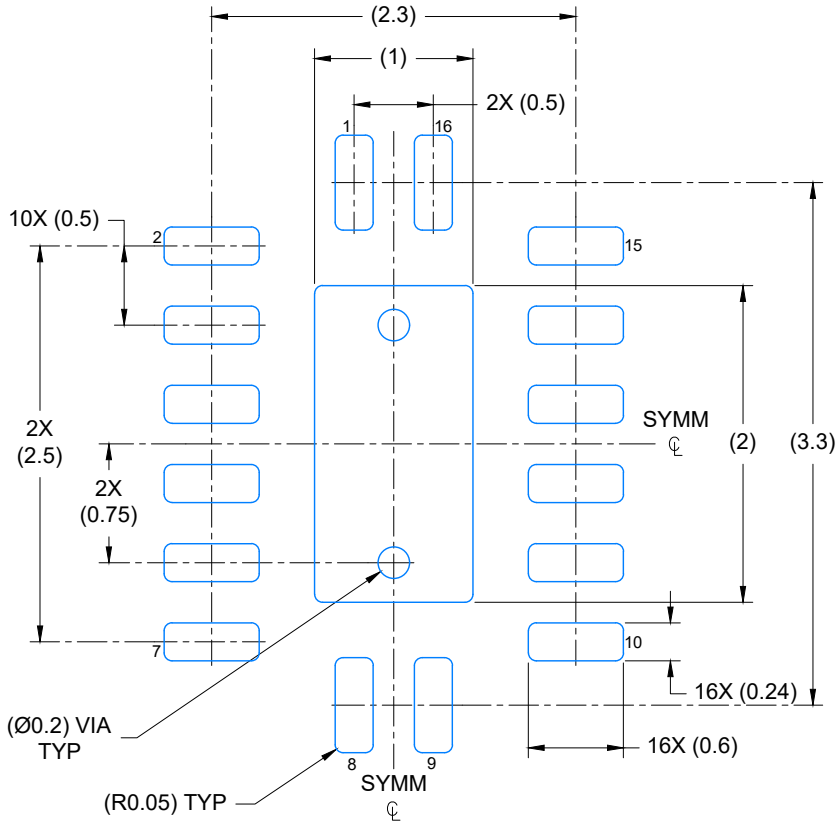
WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD

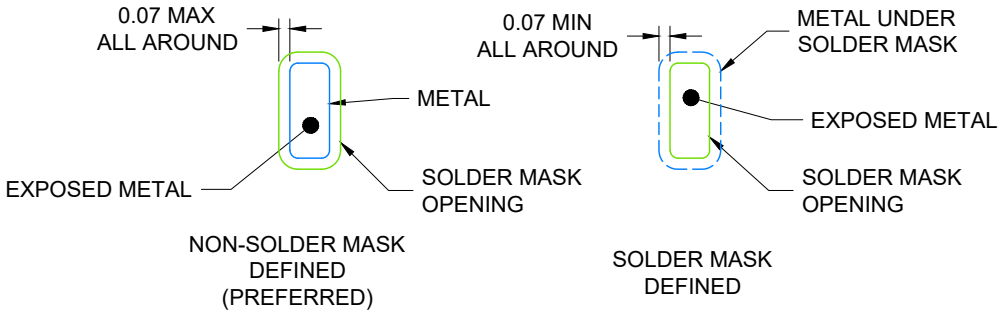


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. Features may differ or may not be present



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

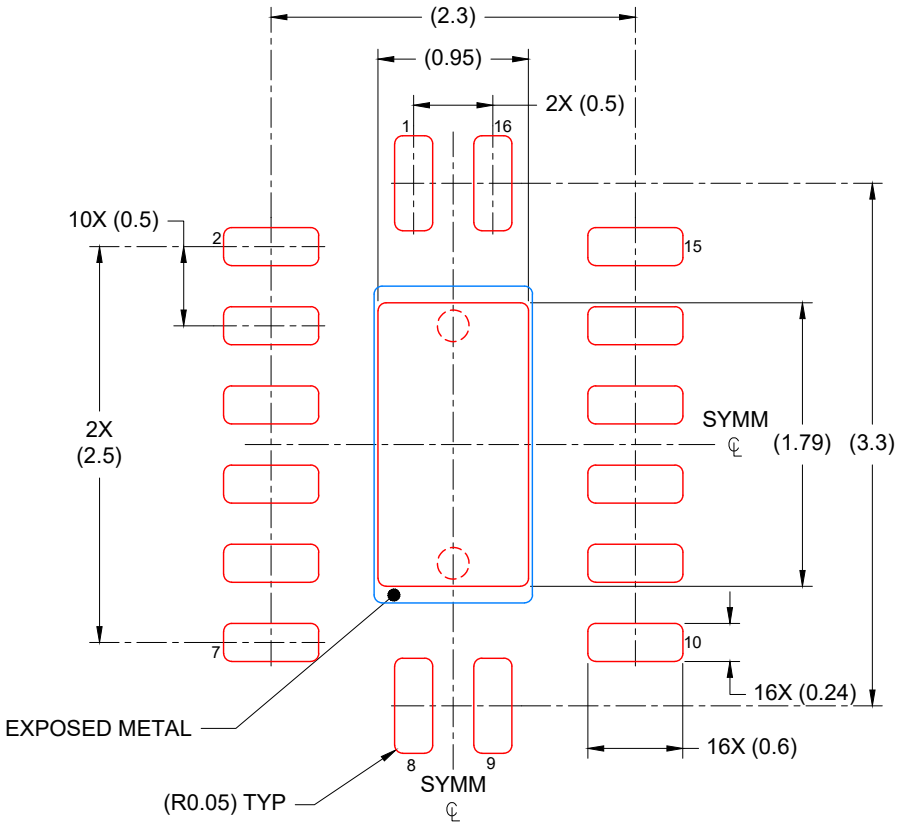


4224640/B 01/2026

1. NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
85% PRINTED COVERAGE BY AREA
SCALE: 20X

4224640/B 01/2026

NOTES: (continued)

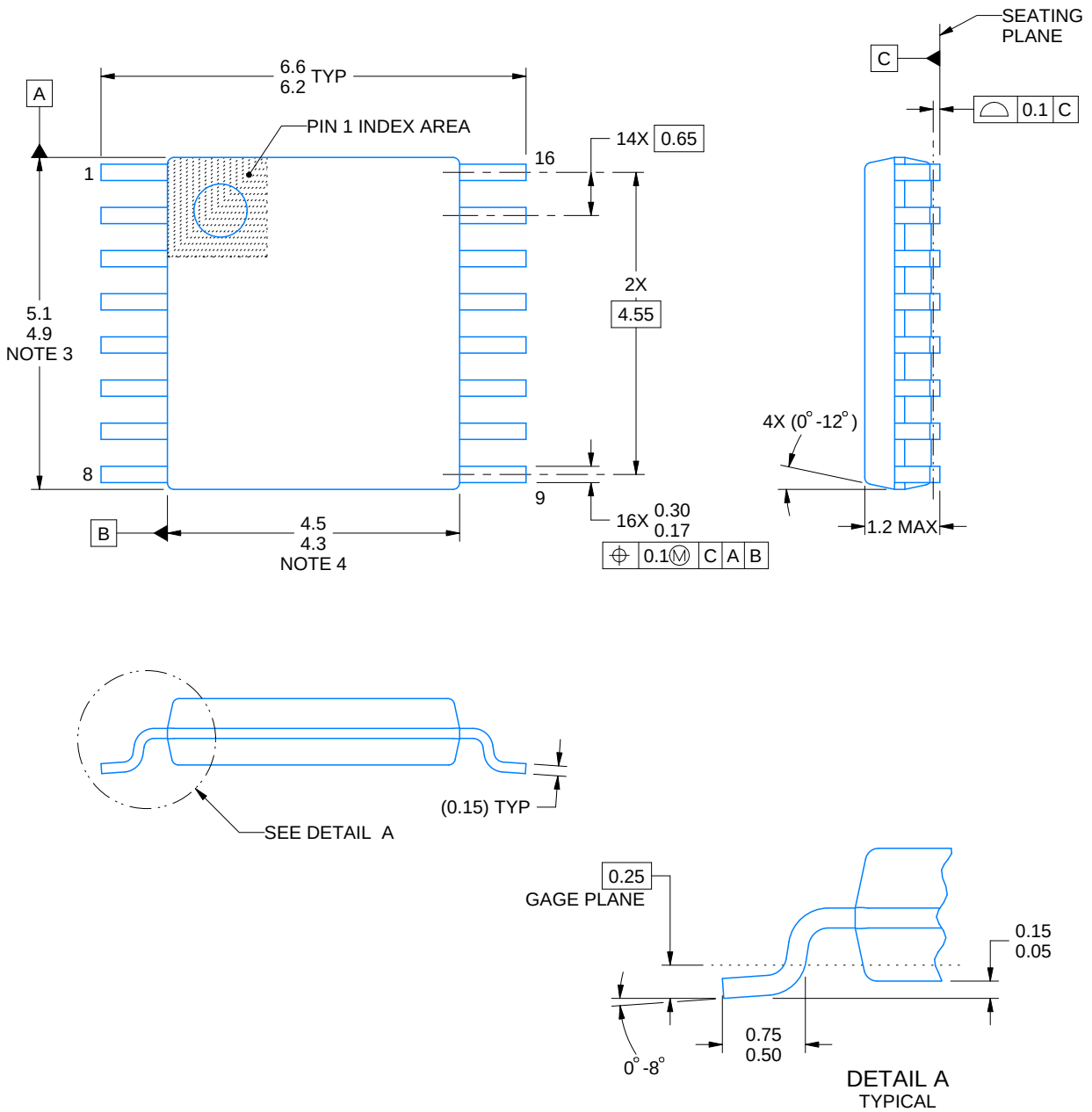
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PW0016A

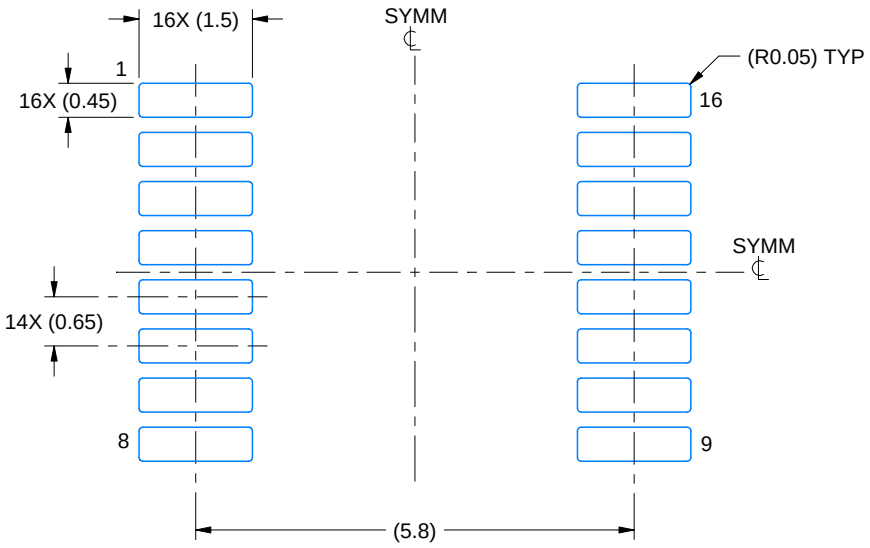
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



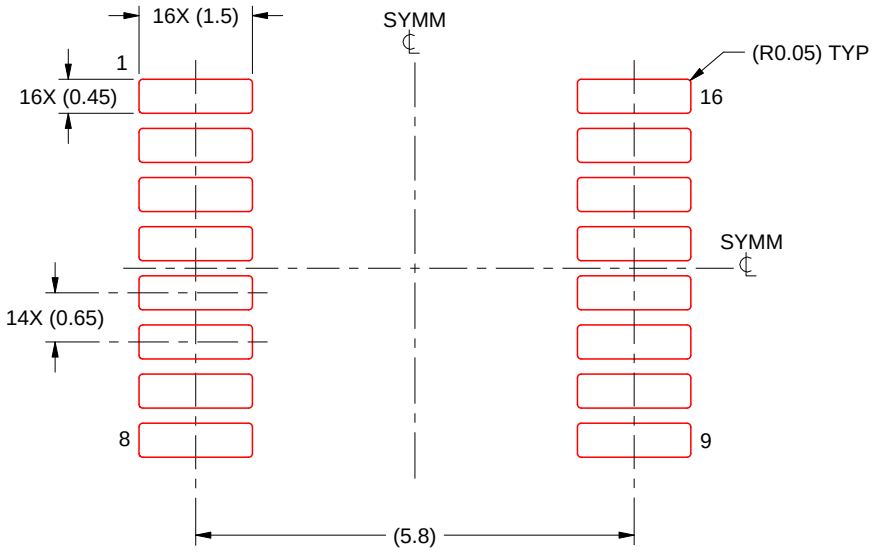
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025