SN74LVC4245A Octal Bus Transceiver and 3.3V to 5V Shifter With 3-State Outputs

1 Features

- 8-bit direction controlled translating bus transceiver
- 5.5V on A port and 2.7V to 3.6V on B port
- High drive strength for heavier loading conditions
  - 24mA at 3V supply
- Robust, glitch-free power supply sequencing
- V_{CC} isolation and V_{CC} disconnect feature
  - If either VCC input is below 100mV or left floating, all I/O outputs are disabled and become high impedance
- Control inputs V_{IH}/V_{IL} levels are referenced to V_{CCA} voltage
- I_{off} supports Partial-Power-Down node operation
- Latch-up performance exceeds 250mA per JESD 17
- Operating temperature range -40°C to 85°C
- ESD protection exceeds JESD 22
  - 2000V Human-Body Model
  - 1000V Charged-Device Model
- Compatible with SN74LVC4245

2 Applications

- Data concentrators
- Three phase UPS
- Servo drive power stage module
- Air conditioner outdoor unit
- String inverter
- Communication module
- PLC, DCS, and PAC

3 Description

This 8-bit (octal) noninverting bus transceiver contains two separate supply rails; B port has V_{CCB}, which is set at 3.3V, and A port has V_{CCA}, which is set at 5V. This allows for translation from a 3.3V to a 5V environment, and vice versa.

The SN74LVC4245A device is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated. The control circuitry (DIR, $\overline{OE}$) is powered by V_{CCA}.

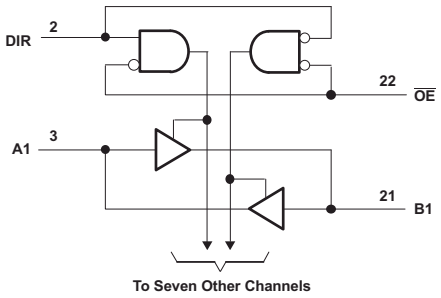
The SN74LVC4245A device terminal out allows the designer to switch to a normal all 3.3V or all 5V 20-terminal SN74LVC4245 device without board re-layout. The designer uses the data paths for pins 2–11 and 14–23 of the SN74LVC4245A device to align with the conventional '245 terminal out.

This device is fully specified for partial-power-down applications using Ioff. The Ioff circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The V_{CC} isolation feature is designed so that if either V_{CCA} or V_{CCB} is less than 100mV, both I/O ports enter a high-impedance state by disabling the outputs.

Package Information

PART NUMBER	PACKAGE(1)	PACAKGE SIZE(2)
SN74LVC4245A	DB (SSOP, 24)	8.2mm × 7.8mm
	DW (SOIC, 24)	15.5mm × 10.3mm
	PW (TSSOP, 24)	7.8mm × 6.4mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

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4 Pin Configuration and Functions

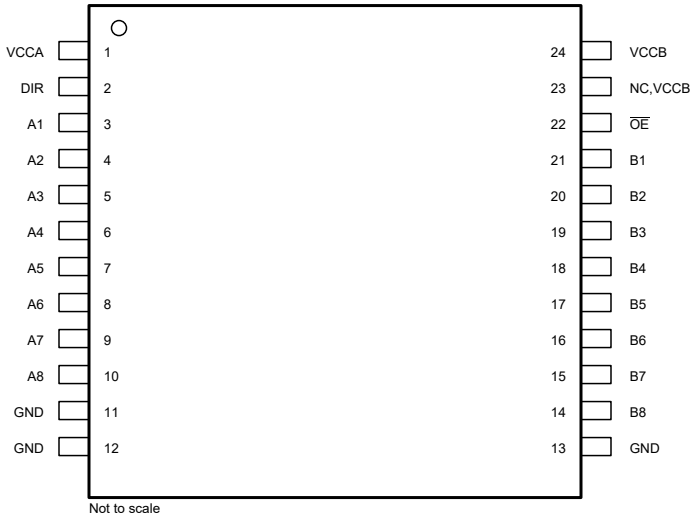


Figure 4-1. DB, DW, or PW Package, SOP, TSSOP, (Top View)

Table 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
V_{CCA}	1	—	Power supply for side A
DIR	2	I	Direction control
A1	3	I/O	Transceiver I/O pin
A2	4	I/O	Transceiver I/O pin
A3	5	I/O	Transceiver I/O pin
A4	6	I/O	Transceiver I/O pin
A5	7	I/O	Transceiver I/O pin
A6	8	I/O	Transceiver I/O pin
A7	9	I/O	Transceiver I/O pin
A8	10	I/O	Transceiver I/O pin
GND	11	—	Ground
GND	12	—	Ground
GND	13	—	Ground
B8	14	I/O	Transceiver I/O pin
B7	15	I/O	Transceiver I/O pin
B6	16	I/O	Transceiver I/O pin
B5	17	I/O	Transceiver I/O pin
B4	18	I/O	Transceiver I/O pin
B3	19	I/O	Transceiver I/O pin
B2	20	I/O	Transceiver I/O pin
B1	21	I/O	Transceiver I/O pin
$\overline{OE}$	22	I	Output Enable
V_{CCB}	23	—	Power supply for side B
V_{CCB}	24	—	Power supply for side B

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range for V_{CCA} = 4.5V to 5.5V (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage range		–0.5	6.5	V
V_I	Input voltage range	A port(2)	–0.5	V_{CCA} + 0.5	V
		Control inputs	–0.5	6	
V_O	Output voltage range	A port(2)	–0.5	V_{CCA} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through each V_{CCA} or GND			±100	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) This value is limited to 6V maximum.

5.2 Absolute Maximum Ratings

over operating free-air temperature range for V_{CCB} = 2.7V to 3.6V (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CCB}	Supply voltage range		–0.5	4.6	V
V_I	Input voltage range	B port(2)	–0.5	V_{CCB} + 0.5	V
V_O	Output voltage range	B port(2)	–0.5	V_{CCB} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCB} or GND			±100	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) This value is limited to 4.6V maximum.

5.3 ESD Ratings

PARAMETER		DEFINITION	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.4 Recommended Operating Conditions

for V_{CCA} = 4.5V to 5.5V(1)

		MIN	MAX	UNIT
V_{CCA}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_{IA}	Input voltage	0	V_{CCA}	V
V_{OA}	Output voltage	0	V_{CCA}	V
I_{OH}	High-level output current		–24	mA
I_{OL}	Low-level output current		24	mA
T_A	Operating free-air temperature	–40	85	°C

(1) All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application note, *Implications of Slow or Floating CMOS Inputs*.

5.5 Recommended Operating Conditions

for V_{CCB} = 2.7V to 3.6V(1)

			MIN	MAX	UNIT
V_{CCB}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CCB} = 2.7V to 3.6V	2		V
V_{IL}	Low-level input voltage	V_{CCB} = 2.7V to 3.6V		0.8	V
V_{IB}	Input voltage		0	V_{CCB}	V
V_{OB}	Output voltage		0	V_{CCB}	V
I_{OH}	High-level output current	V_{CCB} = 2.7V		–12	mA
		V_{CCB} = 3V		–24	
I_{OL}	Low-level output current	V_{CCB} = 2.7V		12	mA
		V_{CCB} = 3V		24	
T_A	Operating free-air temperature		–40	85	°C

(1) All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application note, *Implications of Slow or Floating CMOS Inputs*.

5.6 Thermal Information

THERMAL METRIC(1)		SN74LVC4245A		UNIT
		DB	PW	
		24 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	90.7	100.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.9	44.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.7	55.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	18.8	6.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	49.3	55.4	°C/W

(1) For more information about traditional and new thermal metrics, see the application note, *IC Package Thermal Metrics*.

5.7 Electrical Characteristics

over recommended operating free-air temperature range for V_{CCA} = 4.5V to 5.5V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS			V_{CCA}	MIN	TYP(2)	MAX	UNIT
V_{OH}		I_{OH} = –100µA			4.5V	4.3			V
					5.5V	5.3			
		I_{OH} = –24mA			4.5V	3.7			
					5.5V	4.7			
V_{OL}		I_{OL} = 100µA			4.5V			0.2	V
					5.5V			0.2	
		I_{OL} = 24mA			4.5V			0.55	
					5.5V			0.55	
I_I	Control inputs	V_I = V_{CCA} or GND			5.5V			±1	µA
I_{off}	Input and output power-off leakage current	V_I or V_O = 0 to 5.5V	V_{CCA} = 0 to 5.5V V_{CCB} = 0V	A Port			±0.5	±2	µA
			V_{CCA} = 0 to 5.5V V_{CCB}= 0V	B Port			±0.5	±2	
I_{OZ} (3)	A port	V_O = V_{CCA} or GND			5.5V			±5	µA
I_{CCA}		V_I = V_{CCA} or GND,	I_O = 0		5.5V			18	µA
ΔI_{CCA} (4)		One input at 3.4V,	Other inputs at V_{CCA} or GND		5.5V			1.5	mA
C_i	Control inputs	V_I = V_{CCA} or GND			Open		5		pF
C_{io}	A port	V_O = V_{CCA} or GND			5V		11		pF

(1) V_{CCB} = 2.7V to 3.6V.
(2) All typical values are measured at V_{CC} = 5V, T_A = 25°C.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(4) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0V or the associated V_{CC}.

5.8 Electrical Characteristics

over recommended operating free-air temperature range for V_{CCB} = 2.7V to 3.6V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		V_{CCB}	MIN	TYP(4)	MAX	UNIT
V_{OH}		I_{OH} = –100µA		2.7V to 3.6V	V_{CC} – 0.2			V
		I_{OH} = –12mA		2.7V	2.2			
				3V	2.4			
		I_{OH} = –24mA		3V	2			
V_{OL}		I_{OL} = 100µA		2.7V to 3.6V			0.2	V
		I_{OL} = 12mA		2.7V			0.4	
		I_{OL} = 24mA		3V			0.55	
I_{off}	Input and output power-off leakage current	V_I or V_O = 0 to 3.6V	V_{CCA} = 0 to 5.5V V_{CCB} = 0V			±0.5	±2	µA
			V_{CCA} = 0 to 5.5V V_{CCB}= 0V			±0.5	±2	
I_{OZ} (2)	B port	V_O = V_{CCB} or GND		3.6V			±5	
I_{CCB}		V_I = V_{CCB} or GND,	I_O = 0	3.6V			15	µA
ΔI_{CCB} (3)		One input at V_{CCB} – 0.6V,	Other inputs at V_{CCB} or GND	2.7V to 3.6V			0.5	mA
C_{io}	B port	V_O = V_{CCB} or GND		3.3V		11		pF

(1) V_{CCA} = 5 V ± 0.5 V.
(2) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(3) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0V or the associated V_{CC}.
(4) All typical values are measured at V_{CC} = 3.3V, T_A = 25°C.

5.9 Switching Characteristics

over recommended operating free-air temperature range, C_L = 50pF (unless otherwise noted) (see Figure 6-1 and Figure 6-2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCA} = 5V ± 0.5V, V_{CCB} = 2.7V to 3.6V		UNIT
			MIN	MAX	
t_{PHL}	A	B	1	6.3	ns
t_{PLH}			1	6.7	
t_{PHL}	B	A	1	6.1	ns
t_{PLH}			1	5	
t_{PZL}	$\overline{OE}$	A	1	9	ns
t_{PZH}			1	10	
t_{PZL}	$\overline{OE}$	B	1	10.3	ns
t_{PZH}			1	9.8	
t_{PLZ}	$\overline{OE}$	A	1	7	ns
t_{PHZ}			1	5.8	
t_{PLZ}	$\overline{OE}$	B	1	7.7	ns
t_{PHZ}			1	7.8	

5.10 Operating Characteristics

V_{CCA} = 4.5 V to 5.5 V, V_{CCB} = 2.7V to 3.6V, T_A = 25°C

PARAMETER			TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 0,	f = 10MHz	39.5	pF
		Outputs disabled			5	

5.11 Typical Characteristics

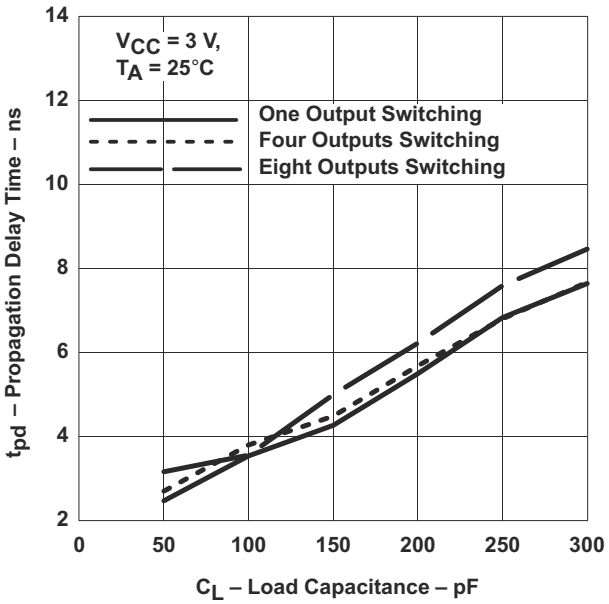


Figure 5-1. Propagation Delay (Low to High Transition) vs Load Capacitance

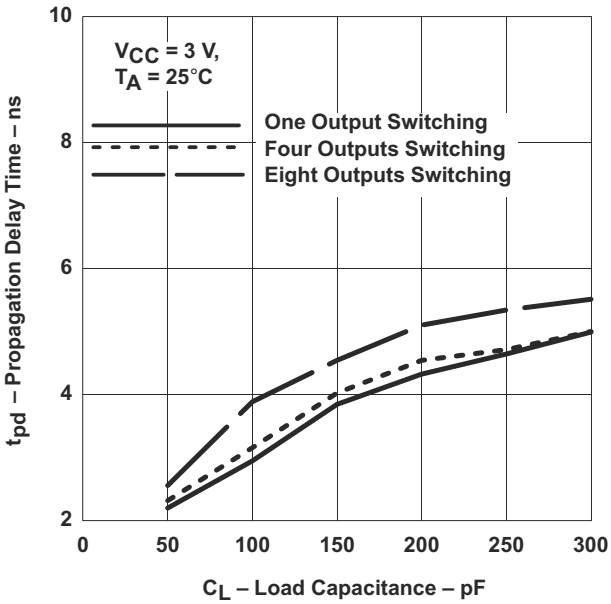
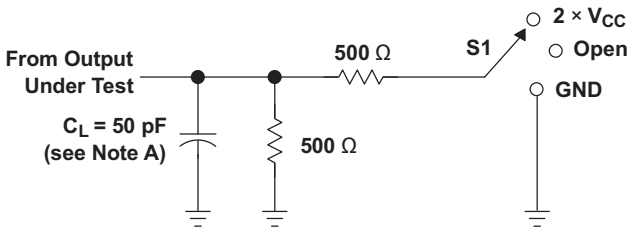


Figure 5-2. Propagation Delay (High to Low Transition) vs Load Capacitance

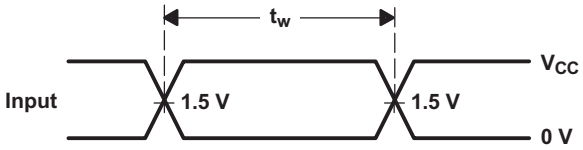
6 Parameter Measurement Information

6.1 A Port

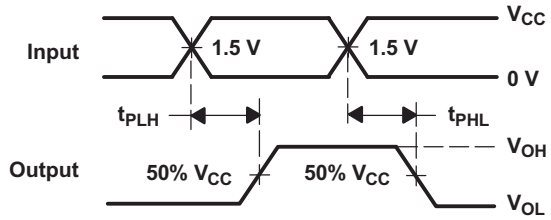


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

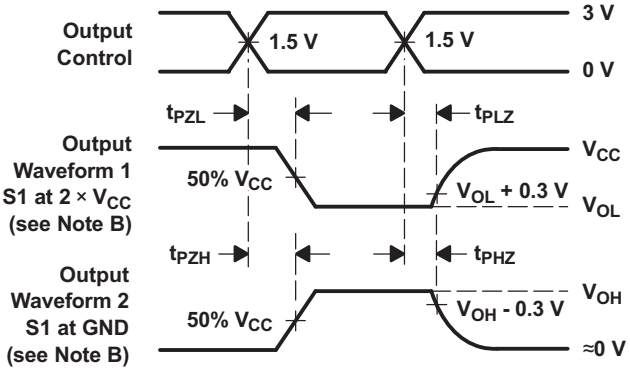
LOAD CIRCUIT



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS

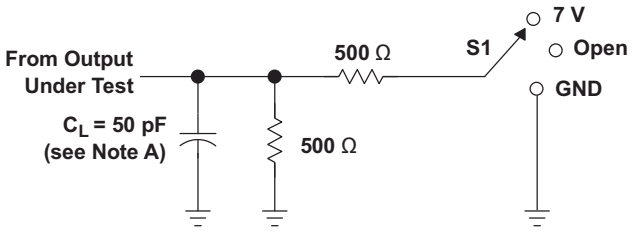


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

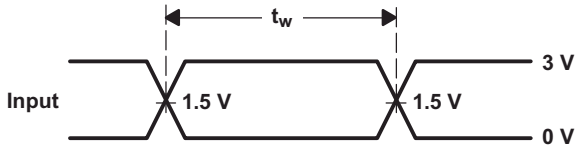
Figure 6-1. Load Circuit and Voltage Waveforms

6.2 B Port

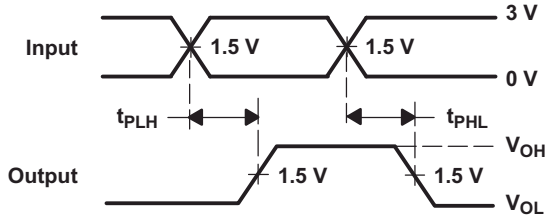


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	GND

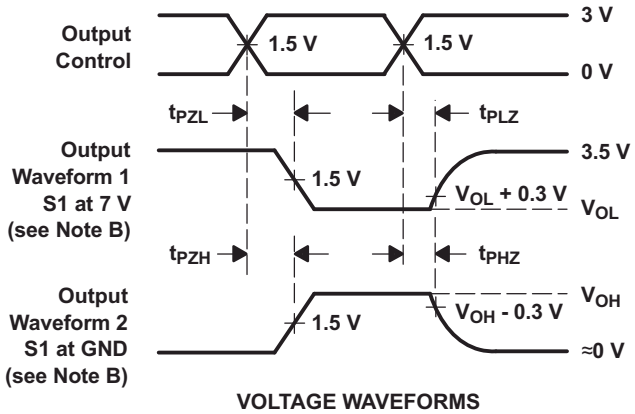
LOAD CIRCUIT



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR≤ 10 MHz, Z_O = 50 Ω, $t_r \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

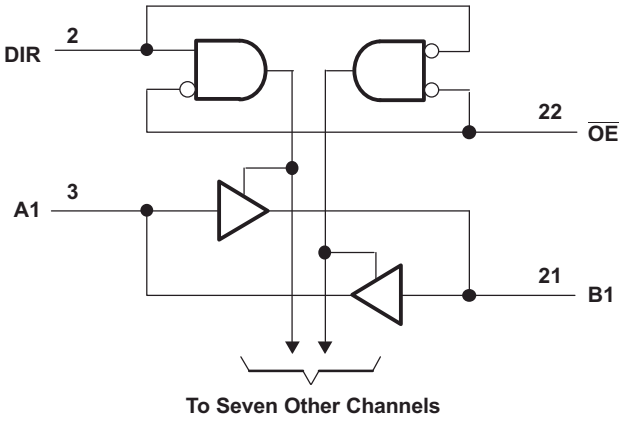
Figure 6-2. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

SN74LVC4245A is an 8-bit (octal) noninverting bus transceiver contains two separate supply rails; B port has V_{CCB}, which is set at 3.3V, and A port has V_{CCA}, which is set at 5 V. This allows for translation from a 3.3V to a 5V environment, and vice versa, designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. Glitch-free power supply sequencing allows either supply rail to be powered on or off in any order while providing robust power sequencing performance. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated. The control circuitry (DIR, $\overline{OE}$) is powered by V_{CCA}.

7.2 Functional Block Diagram



7.3 Feature Description

- 24mA drive at 3V supply
  - Good for heavier loads and longer traces
- Low V_{IH}
  - Allows 3.3V to 5V translation

7.4 Glitch-free Power Supply Sequencing

Either supply rail can be powered on or off in any order without producing a glitch on the I/Os (that is, where the output erroneously transitions to VCC when it must be held low or vice versa). Glitches of this nature can be misinterpreted by a peripheral as a valid data bit, which could trigger a false device reset of the peripheral, a false device configuration of the peripheral, or even a false data initialization by the peripheral.

7.5 V_{CC} Isolation and V_{CC} Disconnect

The I/O's enter a high-impedance state when either supply is <100mV or left floating (disconnected), while the other supply is still connected to the device. It is recommended that the I/O's for this device are not driven or kept low before floating (disconnecting) either supply. The maximum leakage into or out of any input or output pin on the device is specified by I_{off} in the *Electrical Characteristics*.

7.6 Device Functional Modes

Table 7-1. Function Table

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SN74LVC4245A device pinout allows the designer to switch to a normal all-3.3V or all-5V 20-pin '245 device without board re-layout. The designer uses the data paths for pins 2–11 and 14–23 of the SN74LVC4245A to align with the conventional SN74LVC4245 device's pinout. SN74LVC4245A is a high drive CMOS device that can be used for a multitude of bus interface type applications where output drive or PCB trace length is a concern.

8.2 Typical Application

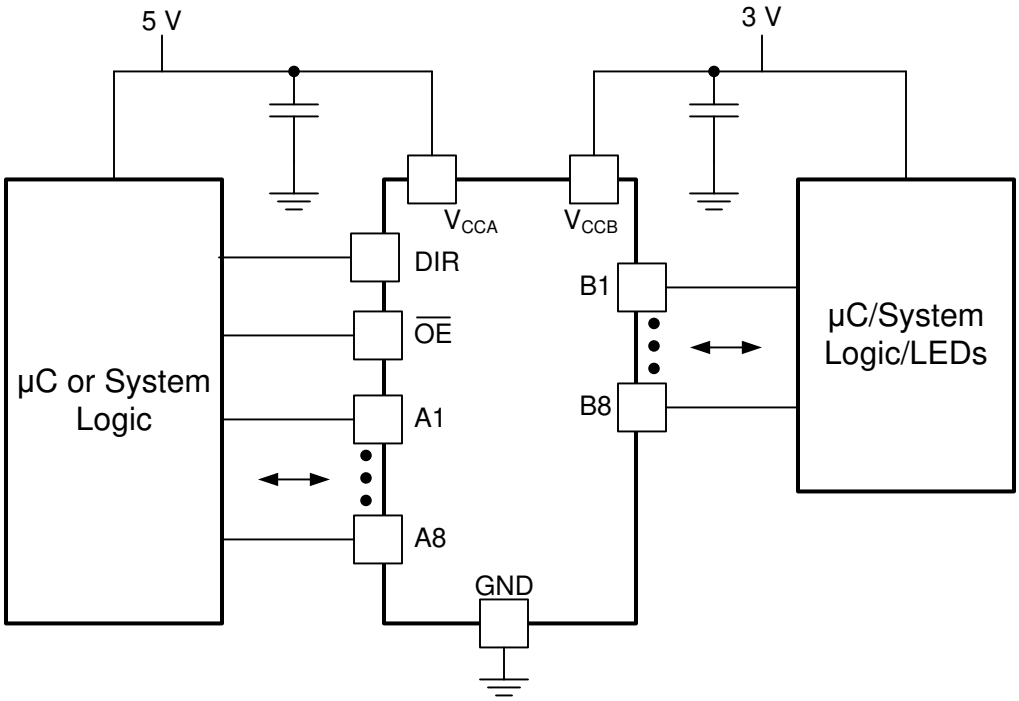


Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

8.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
   - For rise time and fall time specifications, see (Δt/ΔV) in the *Recommended Operating Conditions* table.
   - For specified high and low levels, see (V_{IH} and V_{IL}) in the *Recommended Operating Conditions* table.
2. Recommend Output Conditions:
   - Load currents should not exceed (I_O max) per output and should not exceed (Continuous current through V_{CC} or GND) total current for the part. These limits are located in the *Aboslue Maximum Ratings* table.
   - Outputs should not be pulled above V_{CC}.
   - Series resistors on the output may be used if the user desires to slow the output edge signal or limit the output current.

8.2.3 Application Curves

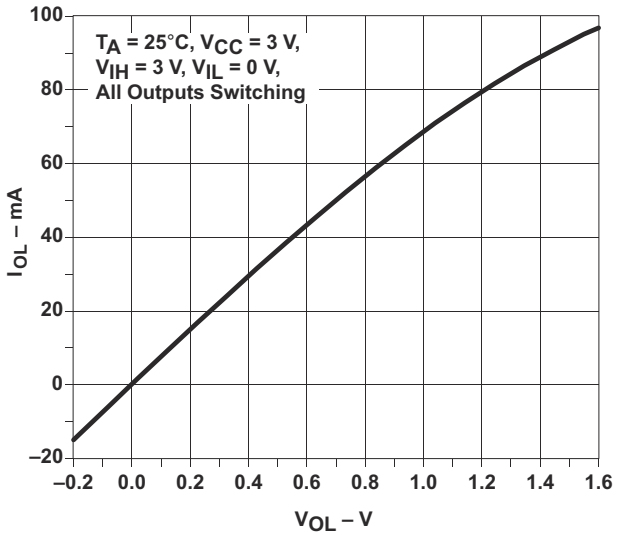


Figure 8-2. Output Drive Current (I_{OL}) vs LOW-level Output Voltage (V_{OL})

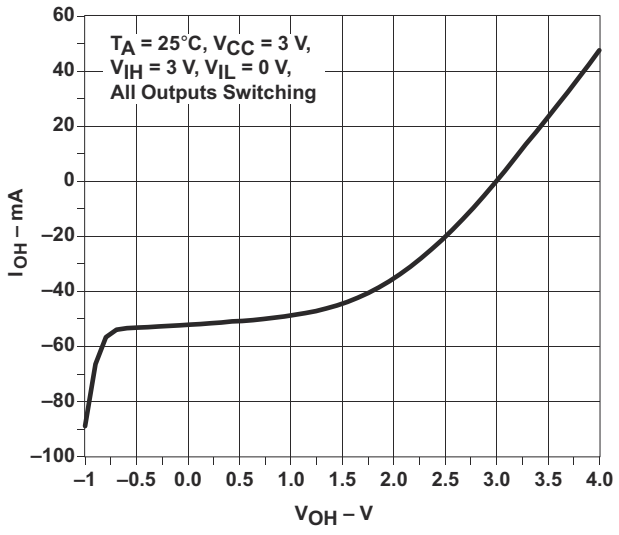


Figure 8-3. Output Drive Current (I_{OH}) vs HIGH-level Output Voltage (V_{OH})

8.3 Power Supply Recommendations

Always apply a ground reference to the GND pins first. This device is designed for glitch free power sequencing without any supply sequencing requirements, which allows to help prevent unintended triggering of downstream devices, as described in Glitch-free Power Supply Sequencing.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 8-4 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient.

8.4.2 Layout Example

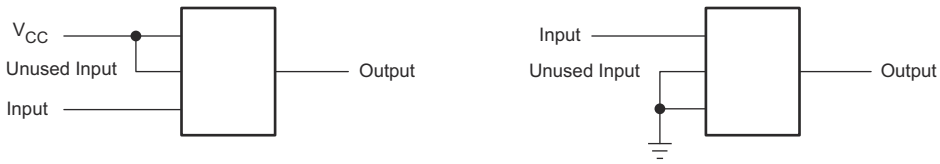


Figure 8-4. Layout Diagram

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Voltage-Level-Translation Devices* application note

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision J (December 2022) to Revision K (May 2026)	Page
• Updated Applications section	1
• Updated Description section	1
• Updated the current values in the *Electrical Characteristics* section	6
• Added the IOFF characteristics in the *Electrical Characteristics* section	6
• Added the *VCC Isolation and VCC* section	11
• Added the *Glitch-free Power Supply Sequencing* section	11
• Updated the *Power Supply Recommendations* section	13

Changes from Revision I (January 2015) to Revision J (December 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated thermals for DB and PW package	5

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC4245ADBR	Active	Production	SSOP (DB) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LJ245A
SN74LVC4245ADBR.A	Active	Production	SSOP (DB) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LJ245A
SN74LVC4245ADBR.B	Active	Production	SSOP (DB) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LJ245A
SN74LVC4245ADBRE4	Active	Production	SSOP (DB) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LJ245A
SN74LVC4245ADW	Active	Production	SOIC (DW) | 24	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC4245A
SN74LVC4245ADW.B	Active	Production	SOIC (DW) | 24	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC4245A
SN74LVC4245ADWE4	Active	Production	SOIC (DW) | 24	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC4245A
SN74LVC4245ADWG4	Active	Production	SOIC (DW) | 24	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC4245A
SN74LVC4245ADWG4.B	Active	Production	SOIC (DW) | 24	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC4245A
SN74LVC4245ADWR	Active	Production	SOIC (DW) | 24	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	LVC4245A
SN74LVC4245ADWR.B	Active	Production	SOIC (DW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC4245A
SN74LVC4245ADWRE4	Active	Production	SOIC (DW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC4245A
SN74LVC4245ADWRG4	Active	Production	SOIC (DW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC4245A
SN74LVC4245ADWRG4.B	Active	Production	SOIC (DW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC4245A
SN74LVC4245APW	Active	Production	TSSOP (PW) | 24	60 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LJ245A
SN74LVC4245APW.A	Active	Production	TSSOP (PW) | 24	60 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LJ245A
SN74LVC4245APW.B	Active	Production	TSSOP (PW) | 24	60 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LJ245A
SN74LVC4245APWG4	Active	Production	TSSOP (PW) | 24	60 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LJ245A
SN74LVC4245APWR	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LJ245A
SN74LVC4245APWR.A	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LJ245A
SN74LVC4245APWR.B	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LJ245A
SN74LVC4245APWRE4	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LJ245A
SN74LVC4245APWRG4	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LJ245A
SN74LVC4245APWT	Active	Production	TSSOP (PW) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LJ245A
SN74LVC4245APWT.B	Active	Production	TSSOP (PW) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LJ245A
SN74LVC4245APWTG4	Active	Production	TSSOP (PW) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LJ245A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC4245A :

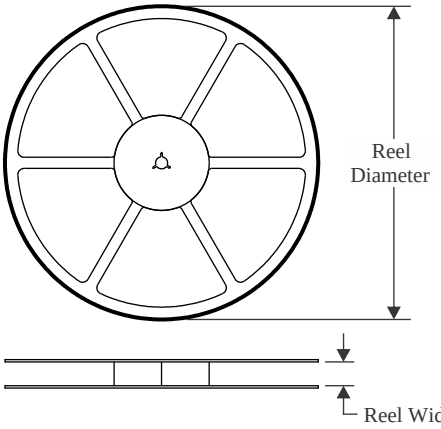
- Enhanced Product : SN74LVC4245A-EP

NOTE: Qualified Version Definitions:

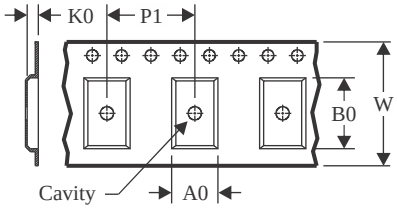
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

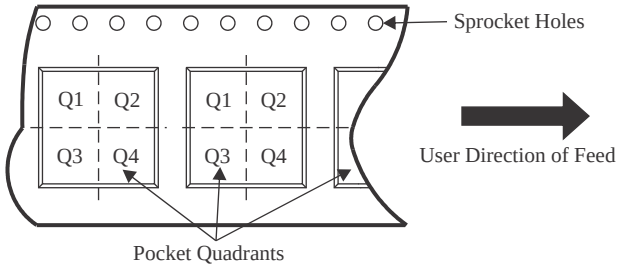


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

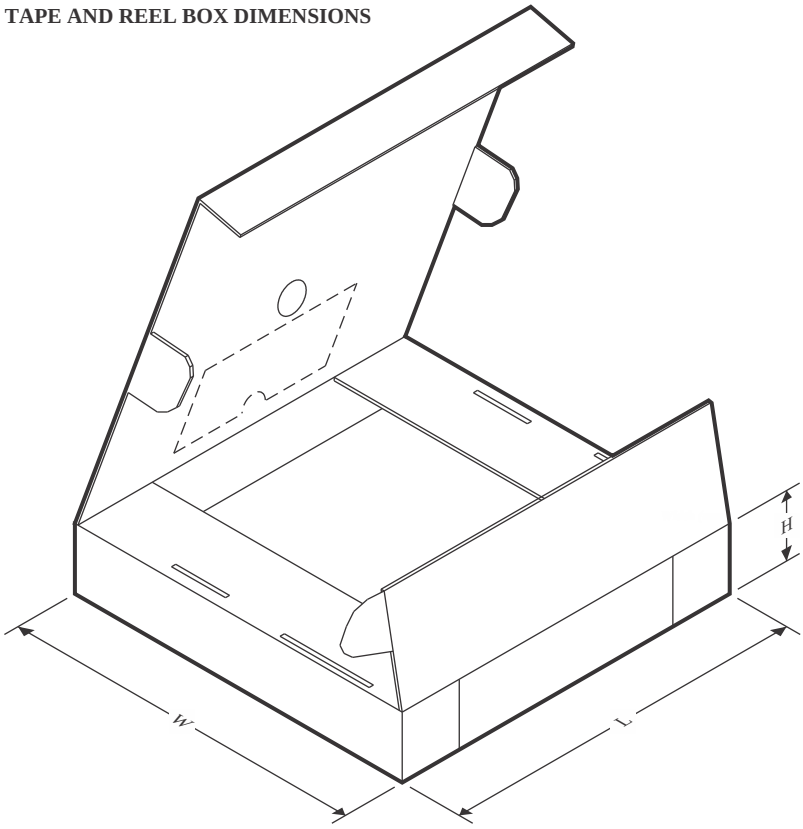
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC4245ADBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
SN74LVC4245ADWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74LVC4245ADWRG4	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74LVC4245APWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
SN74LVC4245APWT	TSSOP	PW	24	250	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

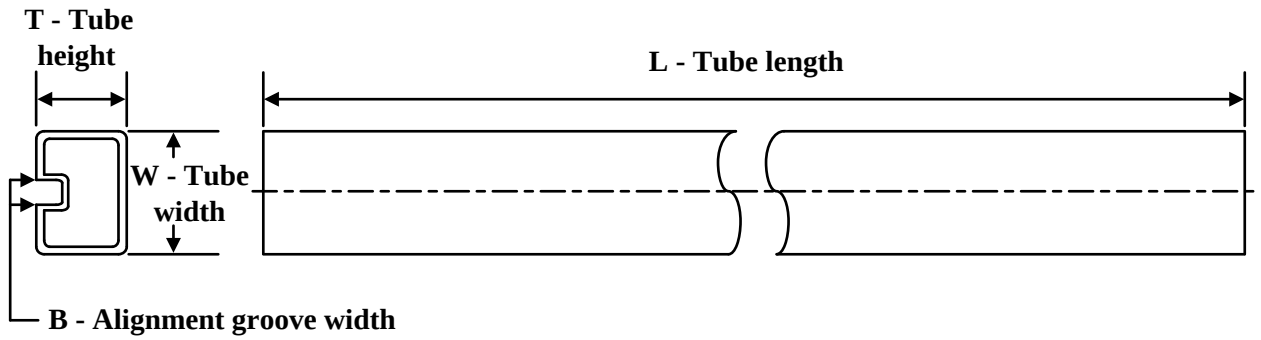
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC4245ADBR	SSOP	DB	24	2000	353.0	353.0	32.0
SN74LVC4245ADWR	SOIC	DW	24	2000	350.0	350.0	43.0
SN74LVC4245ADWRG4	SOIC	DW	24	2000	350.0	350.0	43.0
SN74LVC4245APWR	TSSOP	PW	24	2000	353.0	353.0	32.0
SN74LVC4245APWT	TSSOP	PW	24	250	353.0	353.0	32.0

TUBE



*All dimensions are nominal

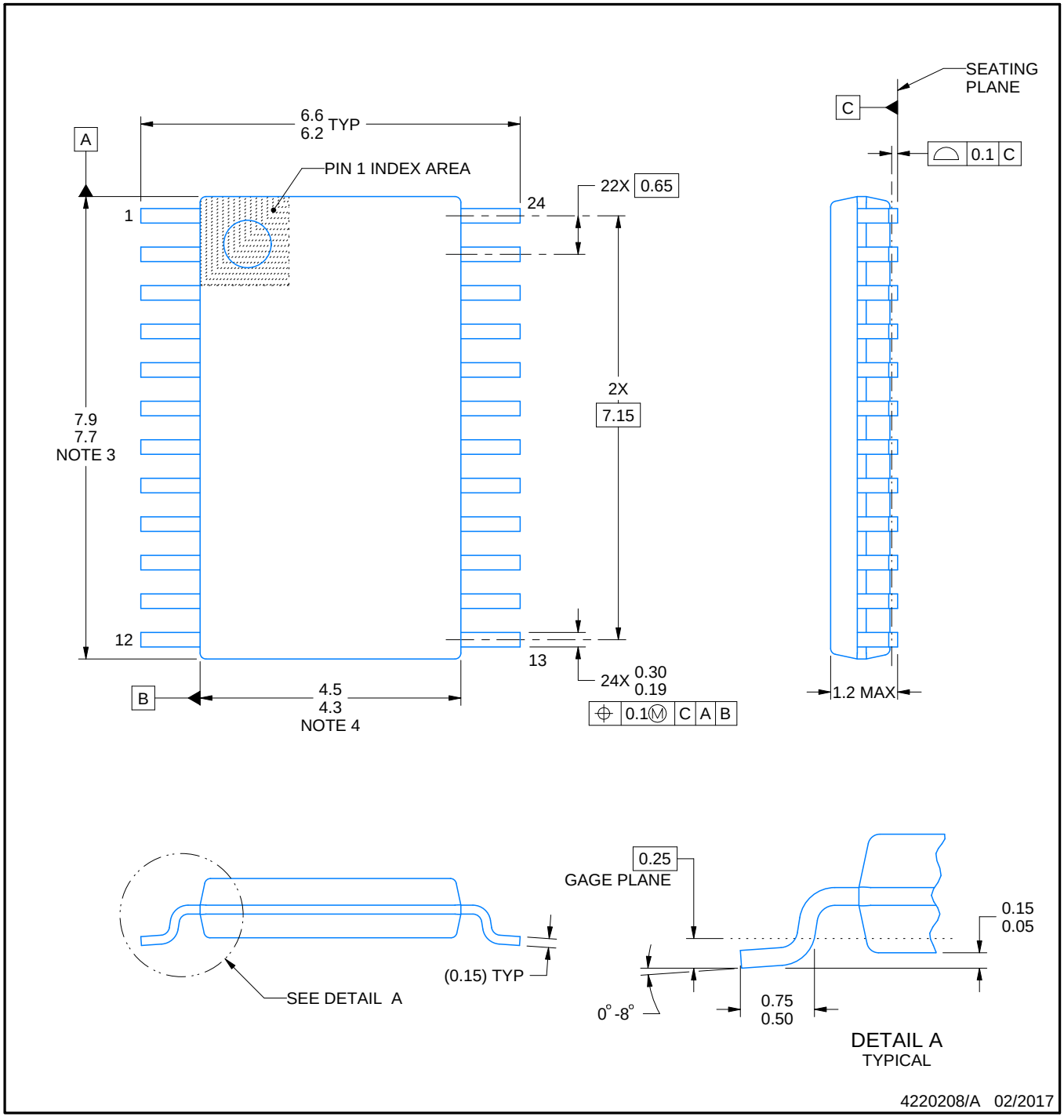
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74LVC4245ADW	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74LVC4245ADW.B	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74LVC4245ADWE4	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74LVC4245ADWG4	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74LVC4245ADWG4.B	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74LVC4245APW	PW	TSSOP	24	60	530	10.2	3600	3.5
SN74LVC4245APW.A	PW	TSSOP	24	60	530	10.2	3600	3.5
SN74LVC4245APW.B	PW	TSSOP	24	60	530	10.2	3600	3.5
SN74LVC4245APWG4	PW	TSSOP	24	60	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0024A

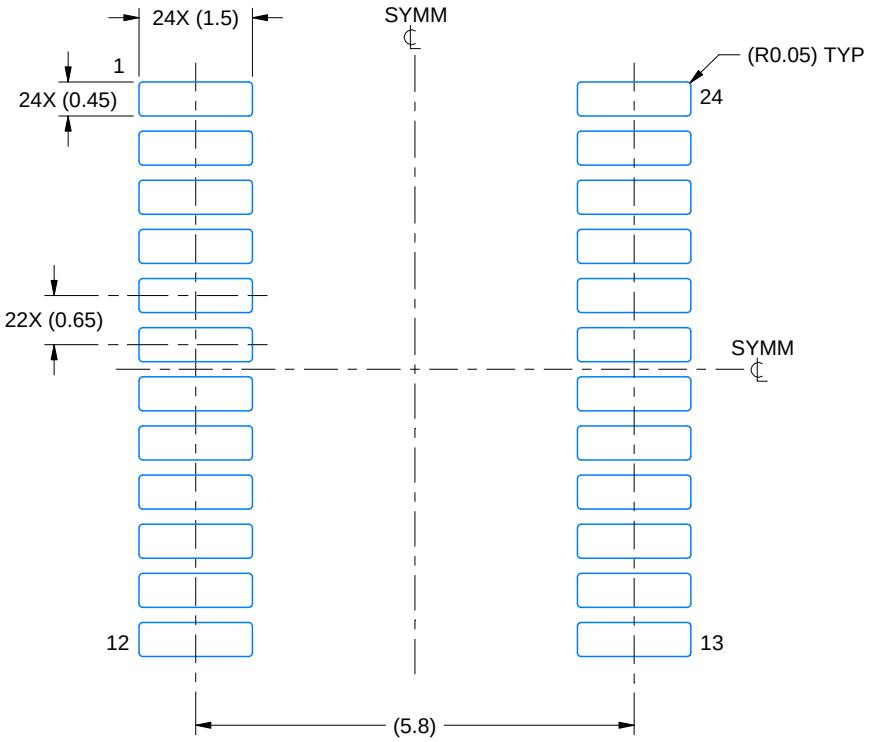
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

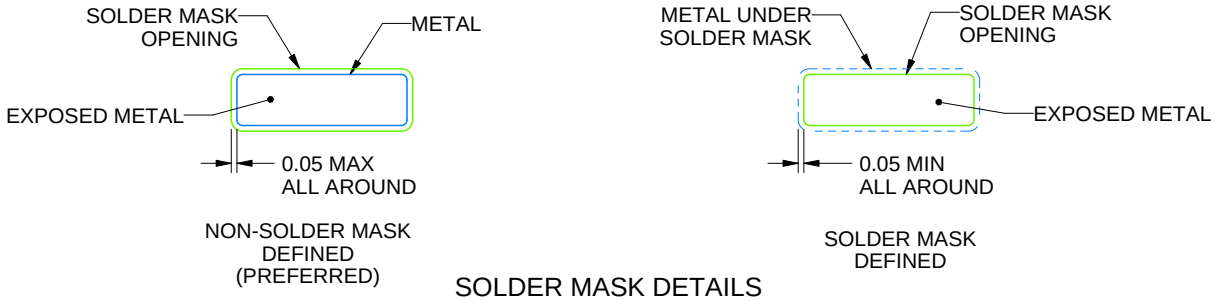


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

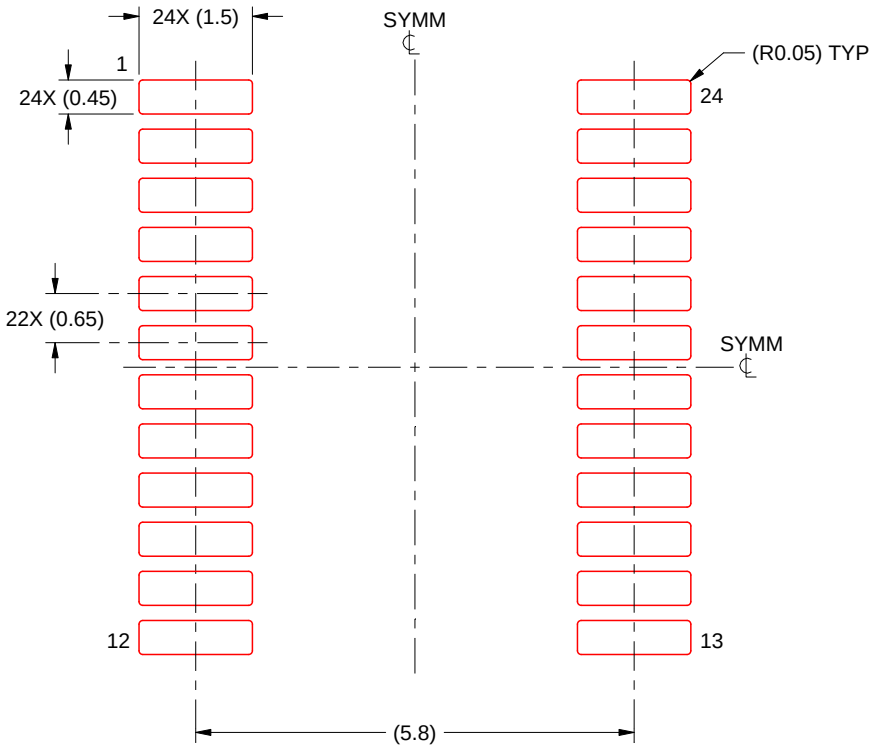


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



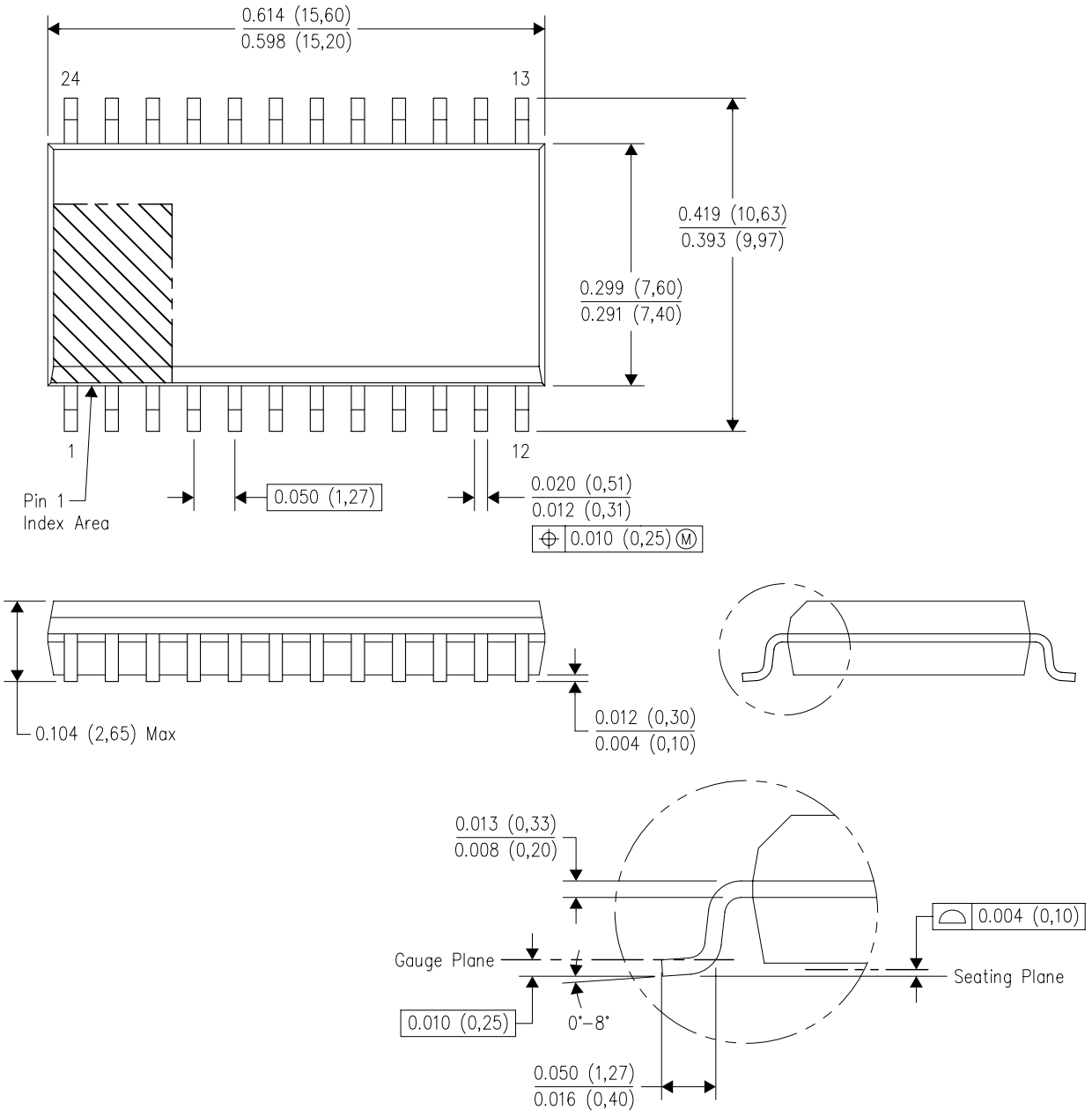
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

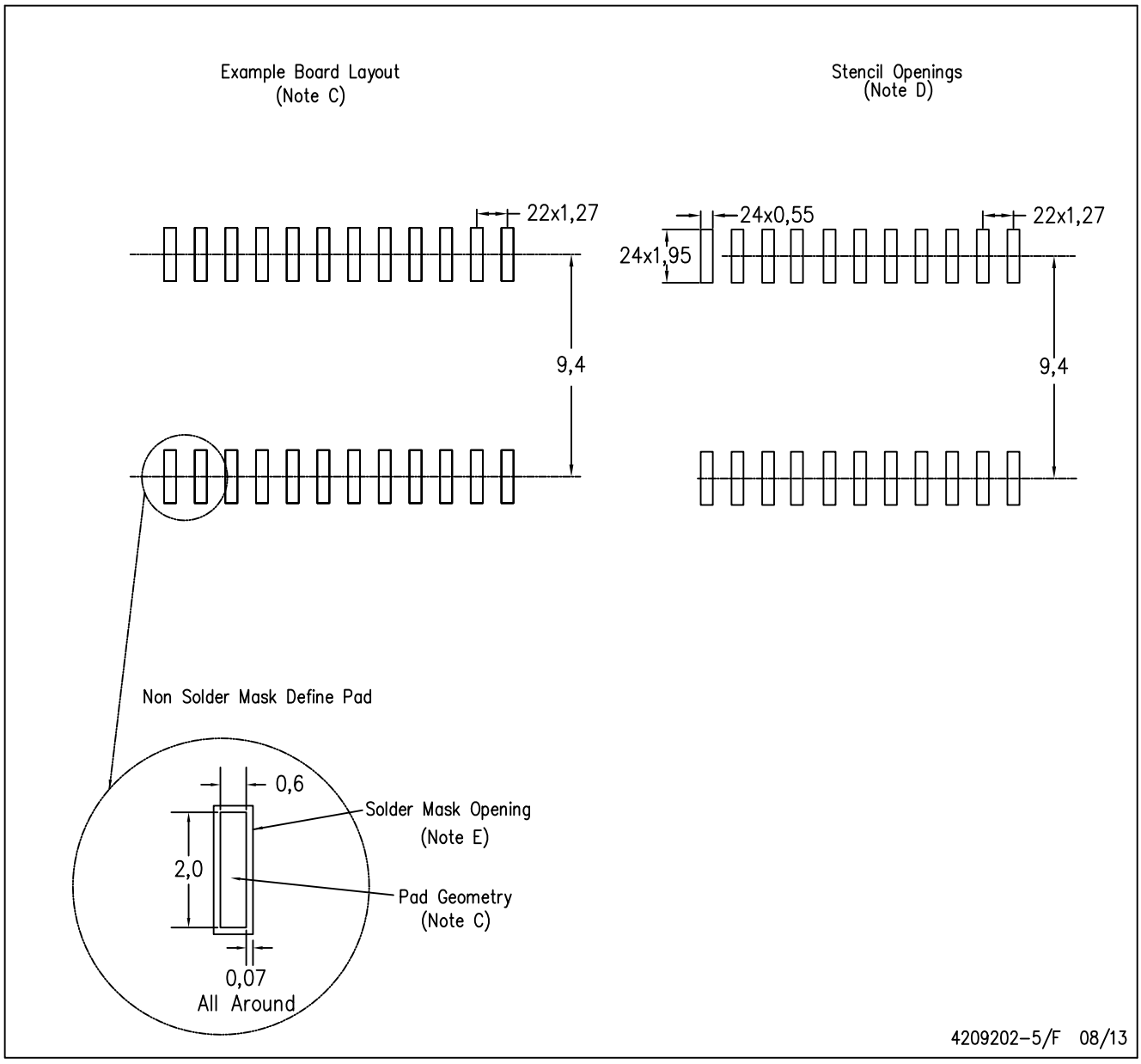
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE

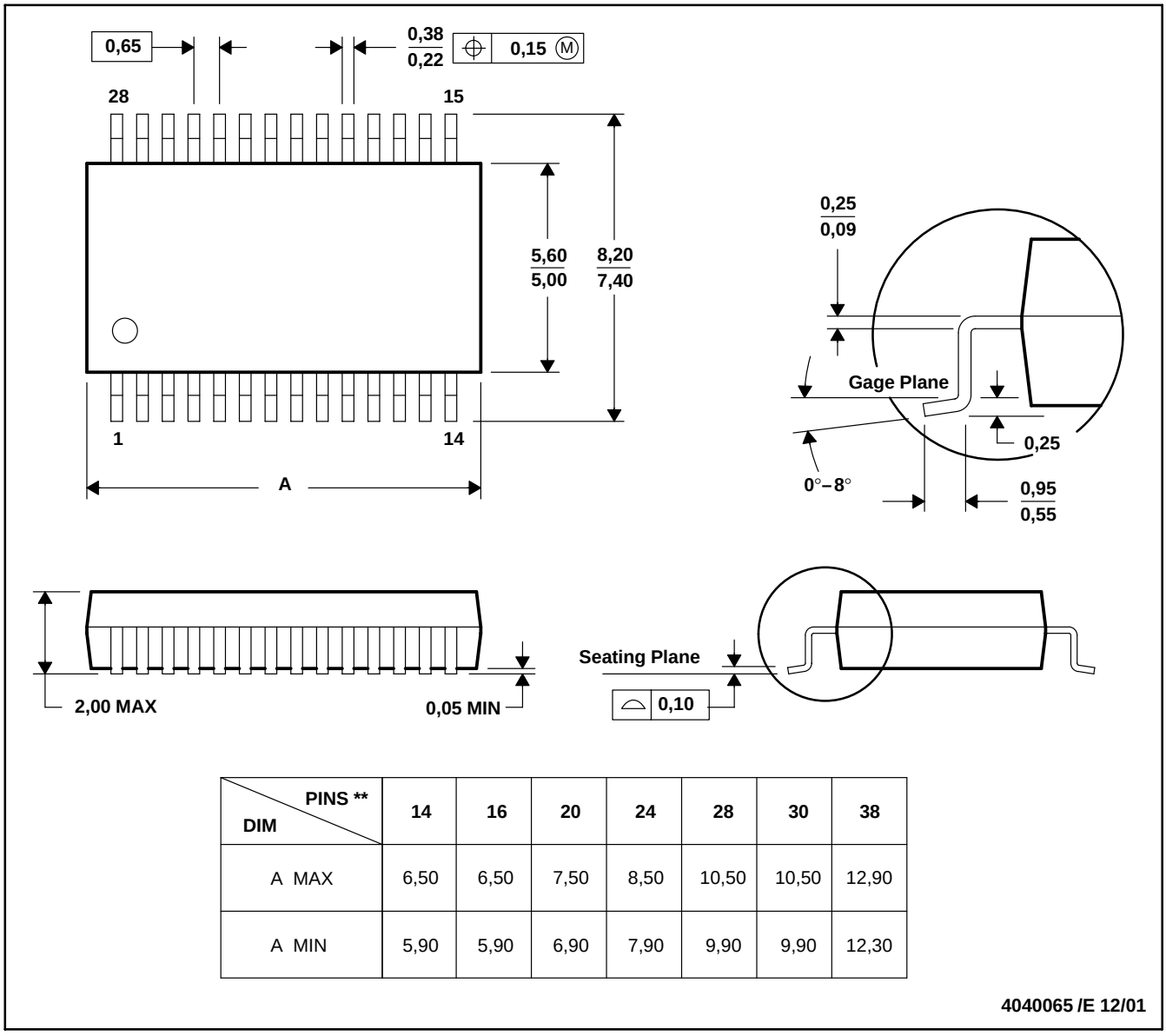


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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Last updated 10/2025