

SN74LVCZ244A Octal Buffer/Driver With 3-State Outputs

1 Features

- Operates from 2.7V to 3.6V
- Inputs accept voltages to 5.5V
- Max t_{pd} of 5.9ns at 3.3V
- Typical V_{OLP} (Output Ground Bounce) $< 0.8V$ at $V_{CC} = 3.3V$, $T_A = 25^\circ C$
- Typical V_{OHV} (Output V_{OH} Undershoot) $> 2V$ at $V_{CC} = 3.3V$, $T_A = 25^\circ C$
- I_{off} Supports live insertion, partial-power-down mode, and back-drive protection
- Supports mixed-mode signal operation on all ports (5V input/output voltage with 3.3V V_{CC})
- Latch-up performance exceeds 100mA per JESD 78, class II

2 Applications

- Servers
- Databases
- Memory systems
- Network switches
- PCs and notebooks

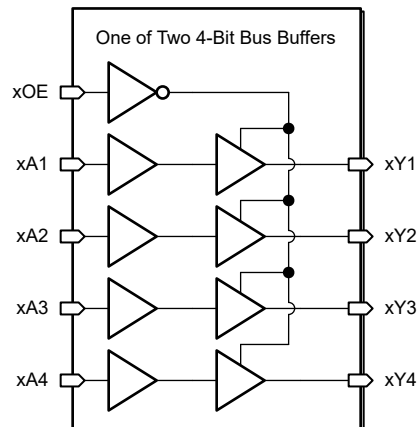
3 Description

The SN74LVCZ244A is an octal buffer with 3-state outputs. The device is configured into two banks of four drivers, each controlled by an output enable pin.

Device Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾	BODY SIZE ⁽³⁾
SN74LVCZ244A	PW (TSSOP, 20)	6.5mm × 6.4mm	6.5mm × 4.4mm
	DW (SOIC, 20)	12.80mm × 10.3mm	12.8mm × 7.5mm
	DB (SSOP, 20)	7.2mm × 7.8mm	7.50mm × 5.3mm
	NS (SOP, 20)	12.6mm × 7.8mm	12.6mm × 5.3mm
	DGS (VSSOP, 20)	5.1mm × 4.9mm	5.1mm × 3.0mm
	RKS (VQFN, 20)	4.5mm × 2.5mm	4.5mm × 2.5mm

- For more information, see [Mechanical, Packaging, and Orderable Information](#).
- The package size (length × width) is a nominal value and includes pins, where applicable.
- The body size (length × width) is a nominal value and does not include pins.



Functional Block Diagram



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4 Pin Configuration and Functions

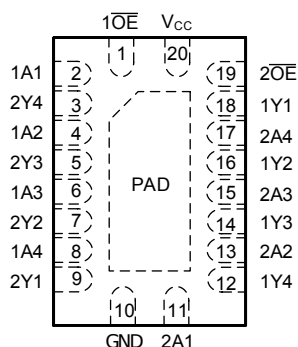


Figure 4-1. SN74LVCZ244A RKS Package (Top View)

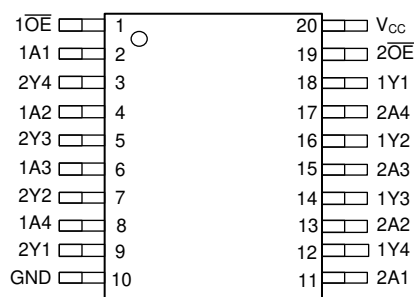


Figure 4-2. SN74LVCZ244A PW, DW, NS, DB, DGS Package (Top View)

Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
OE1	1	I	Bank 1, output enable, active low
A1	2	I	Bank 1, channel 1 input
A2	3	O	Bank 2, channel 4 output
A3	4	I	Bank 1, channel 2 input
A4	5	O	Bank 2, channel 3 output
A5	6	I	Bank 1, channel 3 input
A6	7	O	Bank 2, channel 2 output
A7	8	I	Bank 1, channel 4 input
A8	9	O	Bank 2, channel 1 output
GND	10	G	Ground
Y8	11	I	Bank 2, channel 1 input
Y7	12	O	Bank 1, channel 4 output
Y6	13	I	Bank 2, channel 2 input
Y5	14	O	Bank 1, channel 3 output
Y4	15	I	Bank 2, channel 3 input
Y3	16	O	Bank 1, channel 2 output
Y2	17	I	Bank 2, channel 4 input
Y1	18	O	Bank 1, channel 1 output
OE2	19	I	Bank 2, output enable, active low
V _{CC}	20	P	Positive supply
Thermal Pad ⁽²⁾		—	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.

(1) Signal Types: I = Input, O = Output, G = Ground, P = Power.

(2) RKS package only.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	–0.5	6.5	V
V _I	Input voltage range ⁽²⁾	–0.5	6.5	V
V _O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	–0.5	6.5	V
V _O	Voltage range applied to any output in the high or low state ^{(2) (3)}	–0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0	–50	mA
I _{OK}	Output clamp current	V _O < 0	–50	mA
I _O	Continuous output current		±50	mA
	Continuous current through V _{CC} or GND		±100	mA
T _{stg}	Storage temperature range	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

5.2 ESD Ratings

			MIN	MAX	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	0	2500	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	0	4000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		2.7	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 2.7V to 3.6V	2		V
V _{IL}	Low-level input voltage	V _{CC} = 2.7V to 3.6V		0.8	V
V _I	Input voltage		0	5.5	V
V _O	Output voltage	High or low state	0	V _{CC}	V
		3-state	0	5.5	
I _{OH}	High-level output current	V _{CC} = 2.7V		–12	mA
		V _{CC} = 3V		–24	
I _{OL}	Low-level output current	V _{CC} = 2.7V		12	mA
		V _{CC} = 3V		24	
Δt/Δv	Input transition rise or fall rate			6	ns/V
Δt/ΔV _{CC}	Power-up ramp rate		150		μs/V
T _A	Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, (SCBA004).

5.4 Thermal Information

PACKAGE	PINS	THERMAL METRIC ⁽¹⁾						UNIT
		R _{θJA}	R _{θJC(top)}	R _{θJB}	Ψ _{JT}	Ψ _{JB}	R _{θJC(bot)}	
PW (TSSOP)	20	120.3	62.5	82.4	16.0	81.5	N/A	°C/W
DGS (VSSOP)	20	129.9	72.4	86.1	18.6	85.8	N/A	°C/W
RKS (VQFN)	20	87.2	93.4	59.8	24.9	59.6	44.3	°C/W
DB (SSOP)	20	97.7	59.4	52.9	21.4	52.5	-	°C/W
DW (SOIC)	20	78.7	45.0	46.2	18.3	45.8	-	°C/W
NS (SOP)	20	77.9	44.5	45.5	18.3	45.1	-	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application note](#).

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	–40°C TO 85°C			–40°C TO 125°C			UNIT
			MIN	TYP ⁽¹⁾	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = –100μA	2.7V to 3.6V	V _{CC} – 0.2			V _{CC} – 0.2			V
	I _{OH} = –12mA	2.7V	2.2			2.2			
		3V	2.4			2.4			
	I _{OH} = –24mA	3V	2.2			2.2			
V _{OL}	I _{OL} = 100μA	2.7V to 3.6V	0.2			0.2			V
	I _{OL} = 12mA	2.7V	0.4			0.4			
	I _{OL} = 24mA	3V	0.55			0.55			
I _I	V _I = 0 to 5.5V	3.6V	±5			±5			μA
I _{off}	V _I or V _O = 5.5V	0	±5			±5			μA
I _{OZ}	V _O = 0 to 5.5V	3.6V	±5			±5			μA
I _{OZPU}	V _O = 0.5 to 2.5V, $\overline{\text{OE}}$ = don't care	0 to 1.5V	±5			±5			μA
I _{OZPD}	V _O = 0.5 to 2.5V, $\overline{\text{OE}}$ = don't care	1.5V to 0	±5			±5			μA
I _{CC}	V _I = V _{CC} or GND	3.6V	100			100			μA
	3.6V ≤ V _I ≤ 5.5V ⁽²⁾		100			100			
ΔI _{CC}	One input at V _{CC} – 0.6V, Other inputs at V _{CC} or GND	2.7V to 3.6V	100			100			μA
C _i	V _I = V _{CC} or GND	3.3V	3.5			—			pF
C _o	V _O = V _{CC} or GND	3.3V	5.5			—			pF

(1) All typical values are at V_{CC} = 3.3V, T_A = 25°C.

(2) This applies in the disabled state only.

5.6 Switching Characteristics, –40°C to 85°C

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 6-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 2.7V		V _{CC} = 3.3V ± 0.3V		UNIT
			MIN	MAX	MIN	MAX	
t _{pd}	A or B	B or A		6.9	1.5	5.9	ns
t _{en}	$\overline{\text{OE}}$	A or B		8.6	1.5	7.6	ns
t _{dis}	$\overline{\text{OE}}$	A or B		6.8	1.5	6.5	ns

5.7 Switching Characteristics, –40°C to 125°C

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.7V$		$V_{CC} = 3.3V \pm 0.3V$		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A		7.4	1.5	6.4	ns
t_{en}	$\overline{OE}$	A or B		9.1	1.5	8.1	ns
t_{dis}	$\overline{OE}$	A or B		7.3	1.5	7.1	ns

5.8 Operating Characteristics

$T_A = 25^\circ C$

PARAMETER			TEST CONDITIONS	V _{CC} = 3.3V	UNIT
				TYP	
C _{pd}	Power dissipation capacitance per buffer/driver	Outputs enabled	f = 10MHz	40	pF
		Outputs disabled		3	

5.9 Typical Characteristics

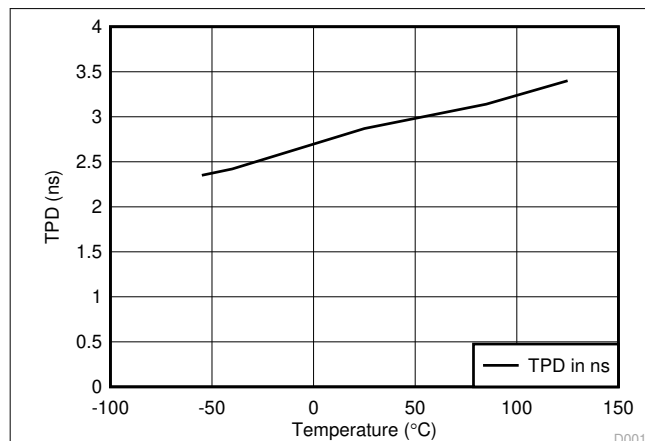


Figure 5-1. TPD Across Temperature at 3.3V

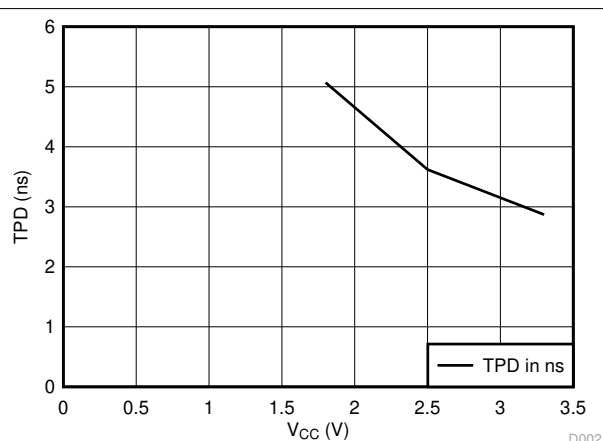
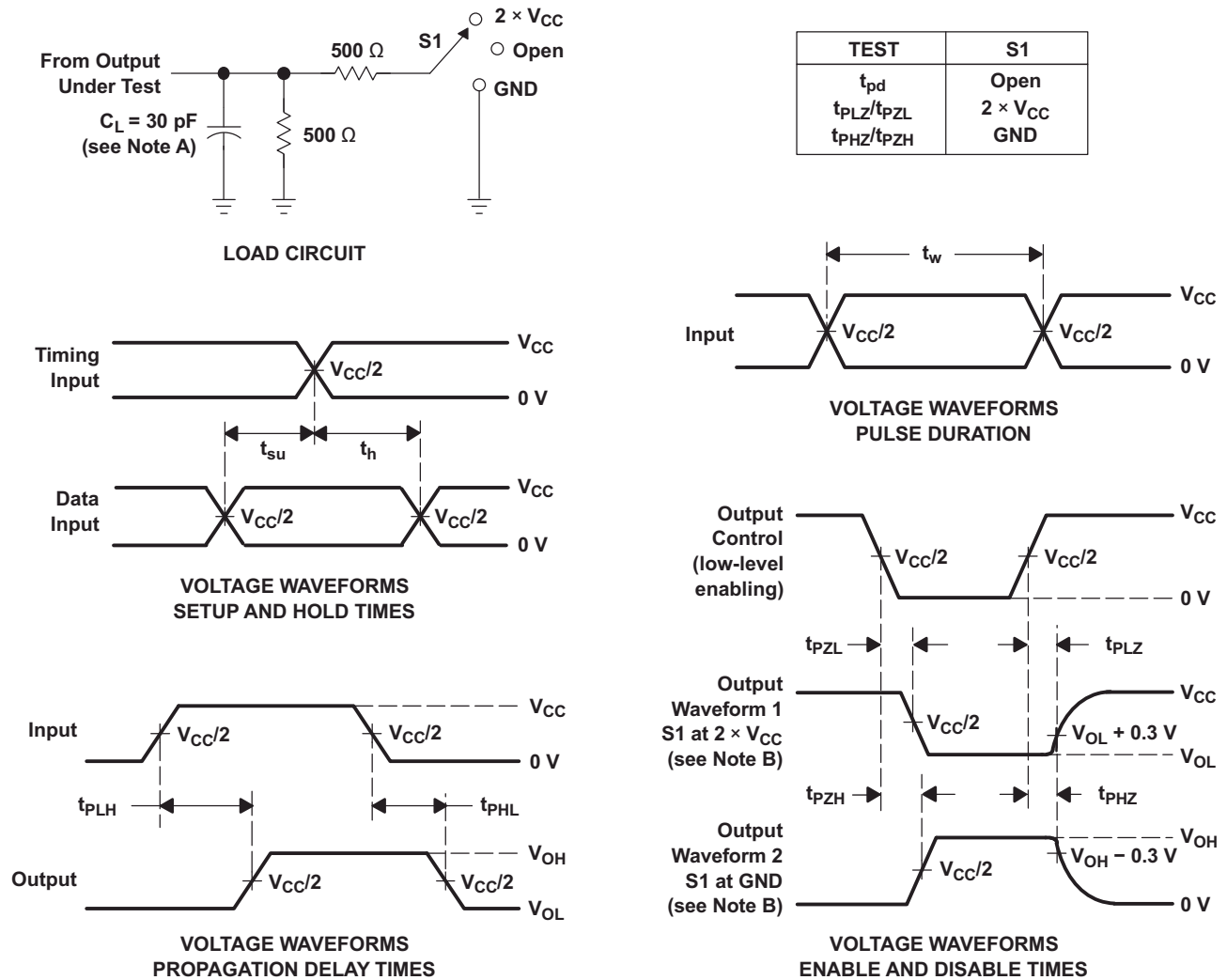


Figure 5-2. TPD Across V_{CC} at 25°C

6 Parameter Measurement Information

6.1 $V_{CC} = 2.7V$ and $3.3V \pm 0.3V$



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 6-1. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

The SN74LVCZ244A contains 8 individual high speed CMOS buffers organized as two 4-bit buffers/line drives with 3-state outputs.

Each buffer performs the boolean logic function $xY_n = xA_n$, with x being the bank number and n being the channel number.

Each output enable ($x\overline{OE}$) controls four buffers. When the $x\overline{OE}$ pin is in the low state, the outputs of all buffers in the bank x are enabled. When the $x\overline{OE}$ pin is in the high state, the outputs of all buffers in the bank x are disabled. All disabled output are placed into the high-impedance state.

To put the device in the high-impedance state during power up or power down, tie both $\overline{OE}$ pins to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current sinking capability of the driver and the leakage of the pin as defined in the *Electrical Characteristics* table.

7.2 Functional Block Diagram

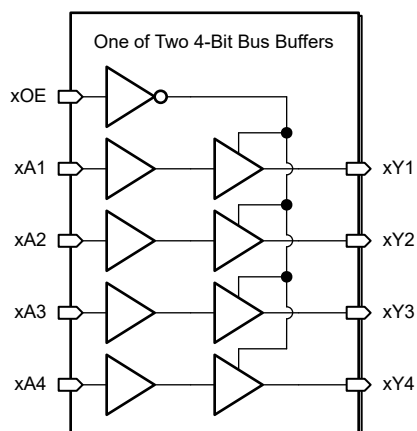


Figure 7-1. Logic Diagram (Positive Logic)

7.3 Feature Description

7.3.1 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-state outputs: driving high, driving low, and high impedance. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device can create fast edges into light loads, so consider routing and load conditions to prevent ringing. Additionally, the outputs of this device can drive larger currents than the device can sustain without damage. Limit the output power of the device to avoid damage from overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance state, the output does not source or sink current except minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the device does not control the output voltage. The output current is dependent on external factors. A floating node is a node that has no other drivers connected, and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while the device is in the high-impedance state. The value of the resistor depends on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10kΩ resistor meets these requirements.

Leave unused 3-state CMOS outputs disconnected.

7.3.2 Partial Power Down (I_{off})

This device includes circuitry to disable all outputs when the supply pin is held at 0V. When disabled, the outputs neither source nor sink current, regardless of the input voltages. The amount of leakage current at each output is defined by the I_{off} specification in the *Electrical Characteristics* table.

7.3.3 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law ($R = V \div I$).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification results in excessive power consumption and can cause oscillations. See more details in *Implications of Slow or Floating CMOS Inputs*.

Do not leave standard CMOS inputs floating at any time during operation. Terminate unused inputs at V_{CC} or GND. If a system does not always drive an input, consider adding a pull-up or pull-down resistor to provide a valid input voltage. The resistor value depends on multiple factors; a 10k Ω resistor, however, is recommended and typically meets all requirements.

7.3.4 Clamp Diode Structure

Figure 7-2 shows the inputs and outputs to this device have negative clamping diodes only.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

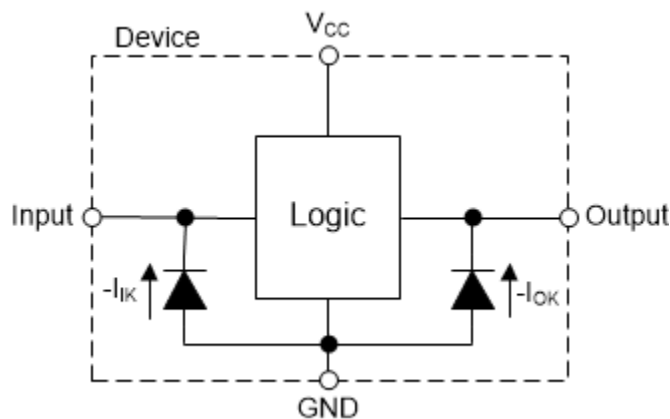


Figure 7-2. Electrical Placement of Clamping Diodes for Each Input and Output

7.4 Device Functional Modes

Table 7-1 lists the functional modes of the SN74LVCZ244A.

Table 7-1. Function Table

INPUTS ⁽¹⁾		OUTPUTS
$\overline{OE}$	A	Y
L	L	L
L	H	H
H	X	Z

(1) H = High Voltage Level, L = Low Voltage Level, X = Do Not Care, Z = High-Impedance State

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

SN74LVCZ244A is a high drive CMOS device that can be used for a multitude of bus interface type applications where output drive or PCB trace length is a concern.

8.2 Typical Application

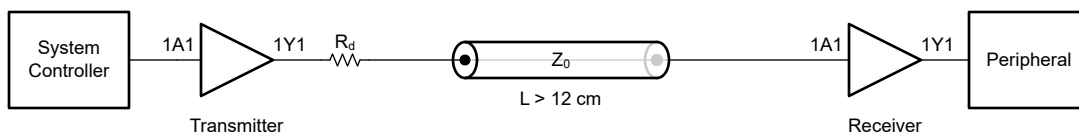


Figure 8-1. Application Schematic

8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Avoid bus contention because it can drive currents in excess of maximum limits. The high drive also creates fast edges into light loads, so consider routing and load conditions to prevent ringing.

8.2.2 Detailed Design Procedure

- Recommended Input Conditions:
 - For rise time and fall time specification, see $(\Delta t/\Delta V)$ in the *Recommended Operating Conditions* table.
 - For specified high and low levels, see $(V_{IH}$ and $V_{IL})$ in the *Recommended Operating Conditions* table.
 - Inputs are overvoltage tolerant allowing them to go as high as $(V_I \text{ max})$ in the *Recommended Operating Conditions* table at any valid V_{CC} .
- Recommended maximum Output Conditions:
 - Load currents must not exceed $(I_O \text{ max})$ per output and must not exceed (Continuous current through V_{CC} or GND) total current for the part. These limits are located in the *Absolute Maximum Ratings* table.
 - Outputs must not be pulled above V_{CC} .

8.2.3 Application Curves

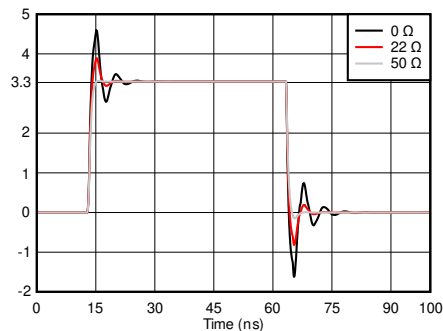


Figure 8-2. Simulated Signal Integrity at the Receiver With Different Damping Resistor (R_d) Values

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance.

A $0.1\mu\text{F}$ capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The $0.1\mu\text{F}$ and $1\mu\text{F}$ capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power terminal as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

- Bypass capacitor placement
 - Place near the positive supply terminal of the device
 - Provide an electrically short ground return path
 - Use wide traces to minimize impedance
 - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
 - 8mil to 12mil trace width
 - Lengths less than 12cm to minimize transmission line effects
 - Avoid 90° corners for signal traces
 - Use an unbroken ground plane below signal traces
 - Flood fill areas around signal traces with ground
 - Parallel traces must be separated by at least 3x dielectric thickness
 - For traces longer than 12cm
 - Use impedance controlled traces
 - Source-terminate using a series damping resistor near the output
 - Avoid branches; buffer each signal that must branch separately

8.4.2 Layout Example

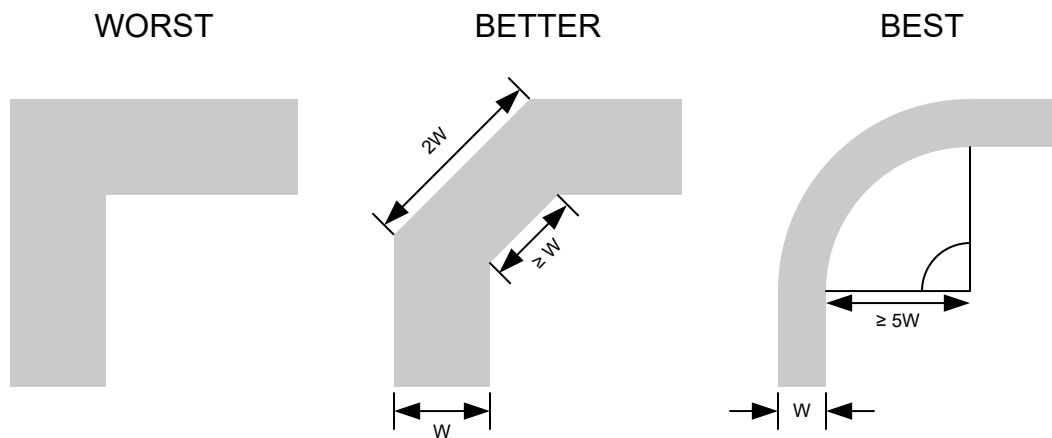


Figure 8-3. Example Trace Corners for Improved Signal Integrity

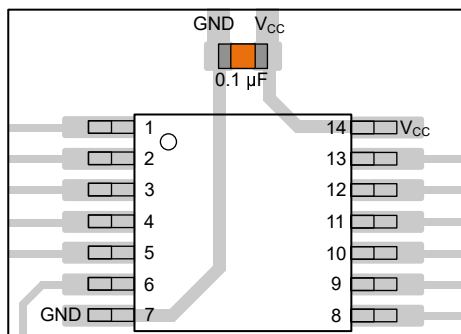


Figure 8-4. Example Bypass Capacitor Placement for TSSOP and Similar Packages

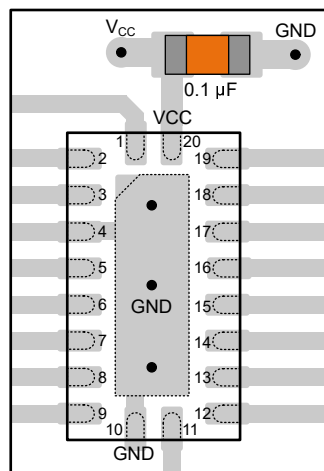


Figure 8-5. Example Bypass Capacitor Placement for WQFN and Similar Packages

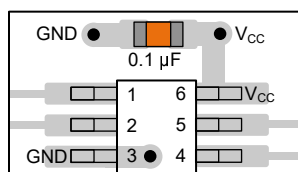


Figure 8-6. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages

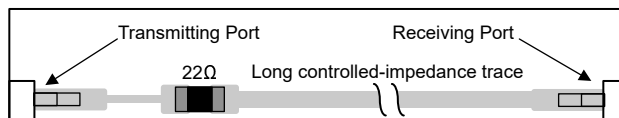


Figure 8-7. Example Damping Resistor Placement for Improved Signal Integrity

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [CMOS Power Consumption and \$C_{pd}\$ Calculation application note](#)
- Texas Instruments, [Designing With Logic application note](#)
- Texas Instruments, [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices application note](#)

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from October 1, 2014 to June 1, 2026 (from Revision I (October 2014) to Revision J (June 2026))

	Page
• Add RKS package options.....	1
• Moved T_{stg} to <i>Absolute Maximum Ratings</i> table.....	4
• Change <i>Handling Ratings</i> to <i>ESD Ratings</i>	4
• Changed Junction-to-ambient thermal resistance value for PW package from: 103.5°C/W to: 120.3°C/W.....	5
• Changed Junction-to-case (top) thermal resistance value for PW package from: 37.9°C/W to: 62.5°C/W.....	5
• Changed Junction-to-board characterization value for PW package from: 54.5°C/W to: 82.4°C/W.....	5
• Changed Junction-to-top characterization value for PW package from: 3.3°C/W to: 16°C/W.....	5
• Changed Junction-to-board characterization value for PW package from: 53.9°C/W to: 81.5°C/W.....	5
• Updated <i>Overview</i> , <i>Application and Implementation</i> , <i>Device and Documentation Support</i> sections to extend detailed feature descriptions and more detailed information.	7
• Added parallel trace spacing recommendation to layout guidelines. Changed wording of "Avoid branches; buffer signals that must branch separately" to "Avoid branches; buffer each signal that must branch separately"	12

Changes from Revision H (August 2003) to Revision I (October 2014)

	Page
• Updated document to new TI data sheet standards.....	1
• Deleted Ordering Information table.....	1
• Changed I_{off} bullet in Features.	1
• Added Applications.....	1
• Added Handling Ratings table.....	4
• Changed Max operating temperature to 125°C in Recommended Operating Conditions table.	4
• Added Thermal Information table.....	5
• Added –40°C TO 125°C temperature range to Electrical Characteristics table.....	5
• Added Switching Characteristics table for –40°C TO 125°C temperature range.....	6
• Added Typical Characteristics section.....	6
• Added Power Supply Recommendations and Layout sections.....	7

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVCZ244ADBR	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CV244A
SN74LVCZ244ADBR.B	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CV244A
SN74LVCZ244ADGSR	Active	Production	VSSOP (DGS) 20	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CZ244A
SN74LVCZ244ADWR	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVCZ244A
SN74LVCZ244ADWR.B	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVCZ244A
SN74LVCZ244ANSR	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVCZ244A
SN74LVCZ244ANSR.B	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVCZ244A
SN74LVCZ244APW	Active	Production	TSSOP (PW) 20	70 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CV244A
SN74LVCZ244APW.B	Active	Production	TSSOP (PW) 20	70 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CV244A
SN74LVCZ244APWR	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CV244A
SN74LVCZ244APWR.A	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CV244A
SN74LVCZ244APWR.B	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CV244A
SN74LVCZ244APWRG4	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CV244A
SN74LVCZ244APWRG4.A	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CV244A
SN74LVCZ244APWRG4.B	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CV244A
SN74LVCZ244APWT	Active	Production	TSSOP (PW) 20	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CV244A
SN74LVCZ244APWT.B	Active	Production	TSSOP (PW) 20	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CV244A

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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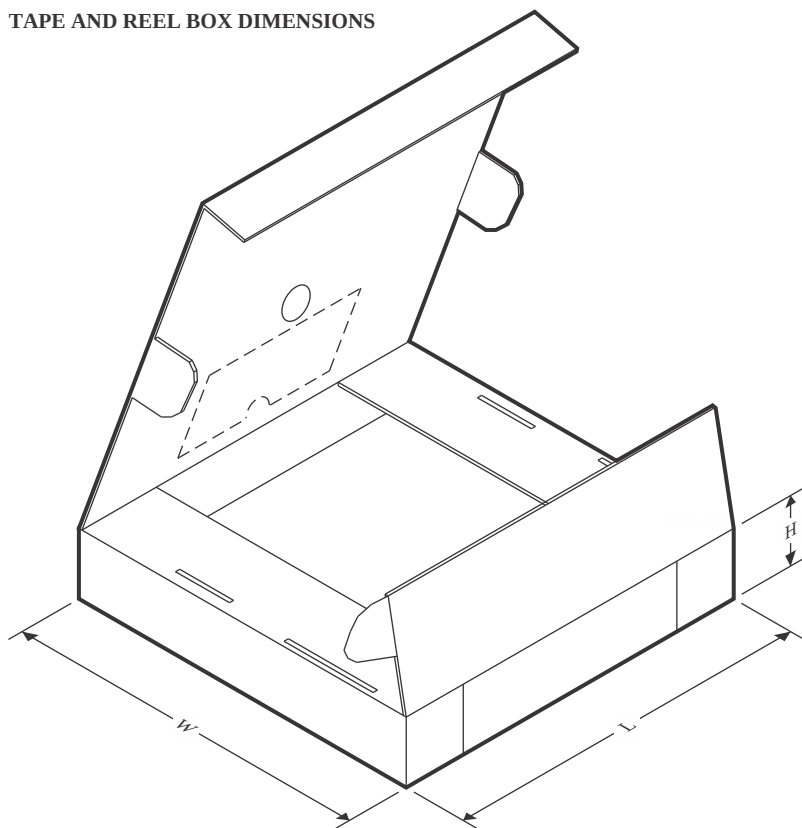
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVCZ244ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LVCZ244ADGSR	VSSOP	DGS	20	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1
SN74LVCZ244ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LVCZ244ANSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LVCZ244APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LVCZ244APWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LVCZ244APWT	TSSOP	PW	20	250	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

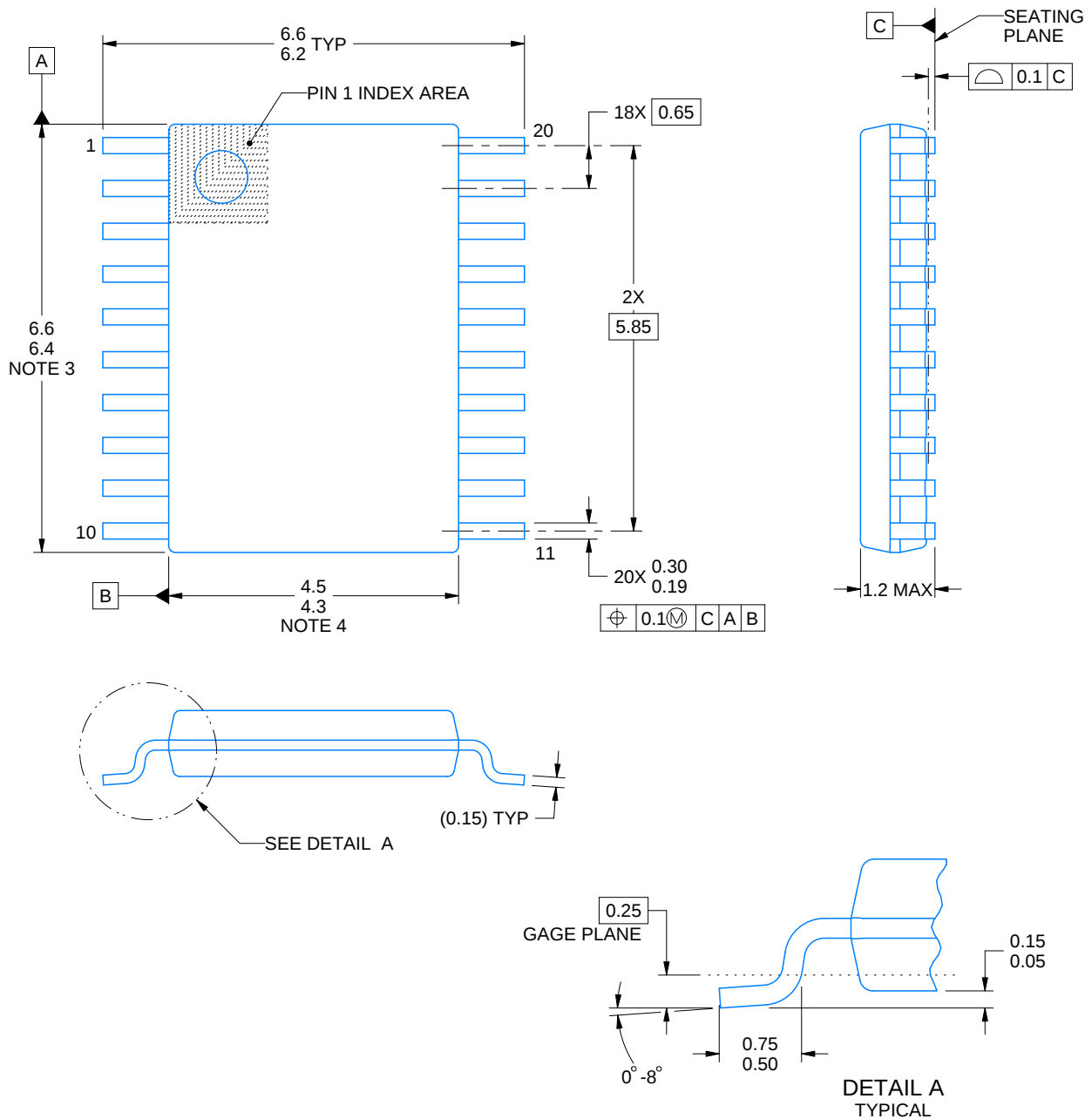
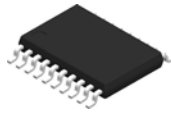
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVCZ244ADBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74LVCZ244ADGSR	VSSOP	DGS	20	5000	353.0	353.0	32.0
SN74LVCZ244ADWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74LVCZ244ANSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74LVCZ244APWR	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74LVCZ244APWRG4	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74LVCZ244APWT	TSSOP	PW	20	250	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74LVCZ244APW	PW	TSSOP	20	70	530	10.2	3600	3.5
SN74LVCZ244APW.B	PW	TSSOP	20	70	530	10.2	3600	3.5



4220206/A 02/2017

NOTES:

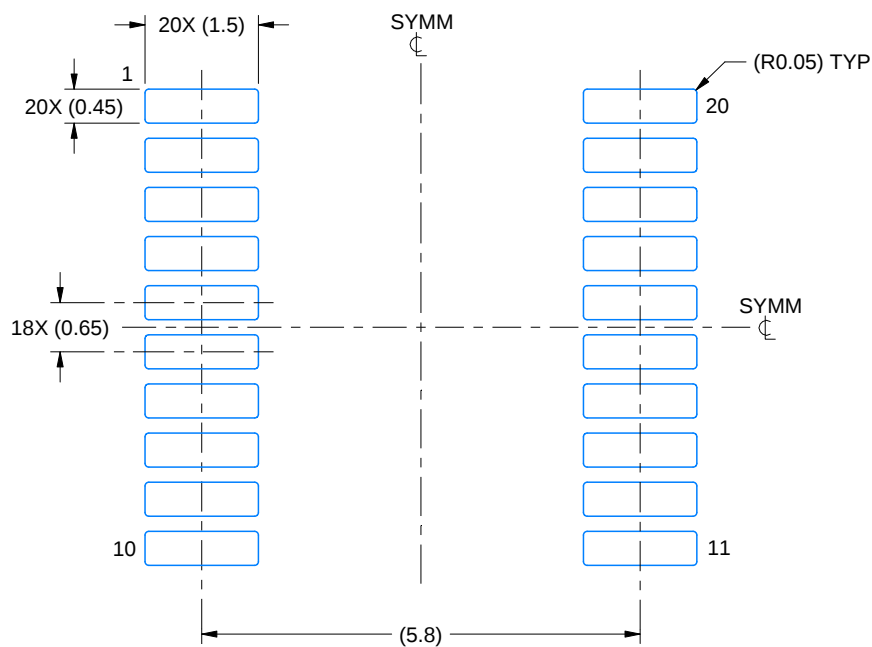
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

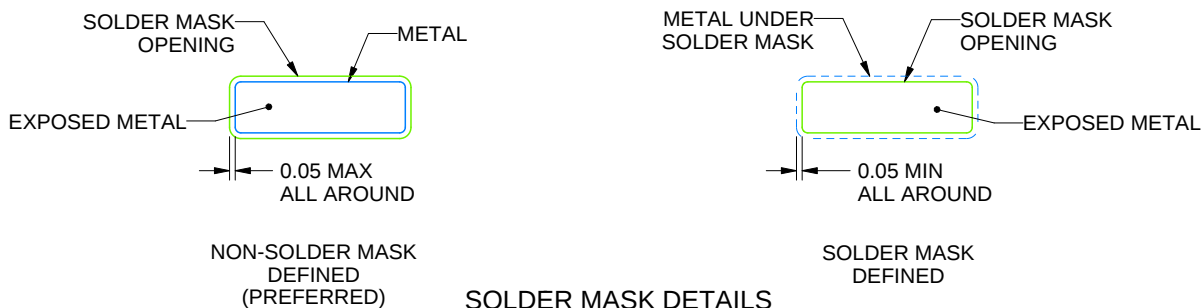
PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

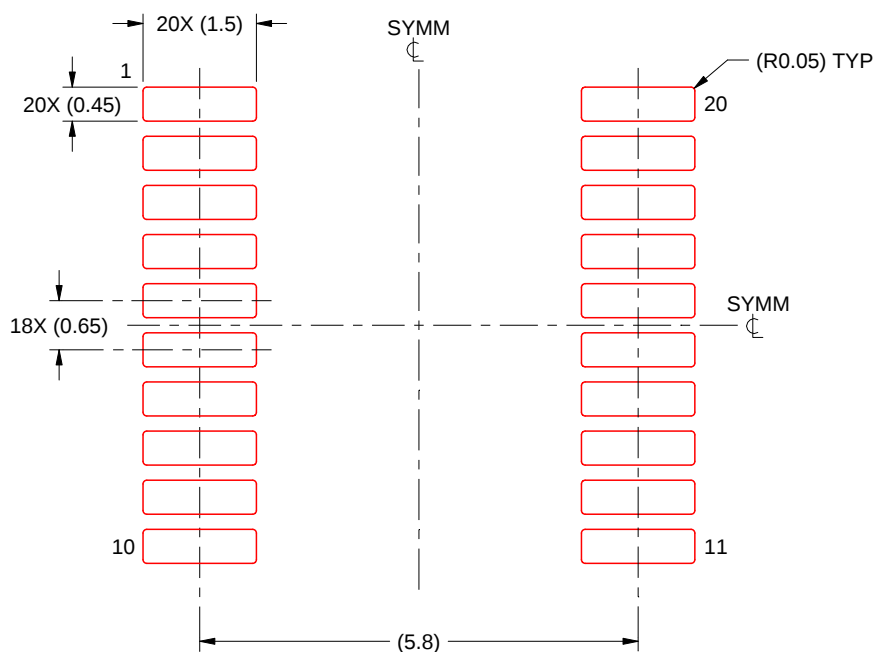
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

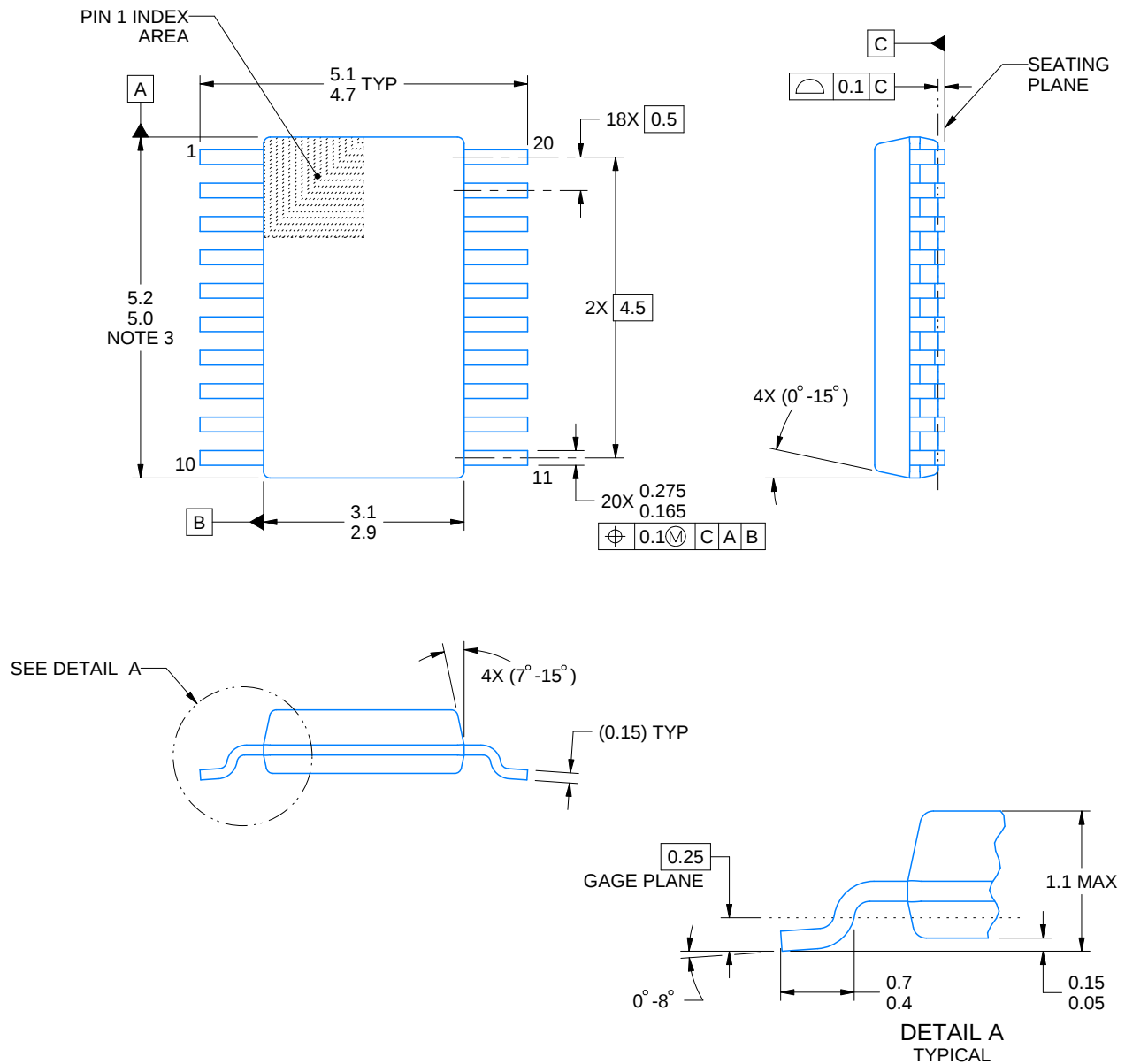


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4226367/A 10/2020

NOTES:

PowerPAD is a trademark of Texas Instruments.

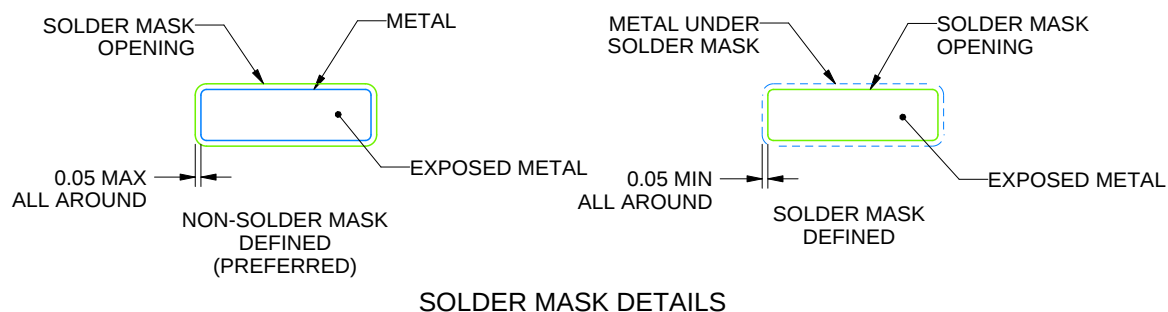
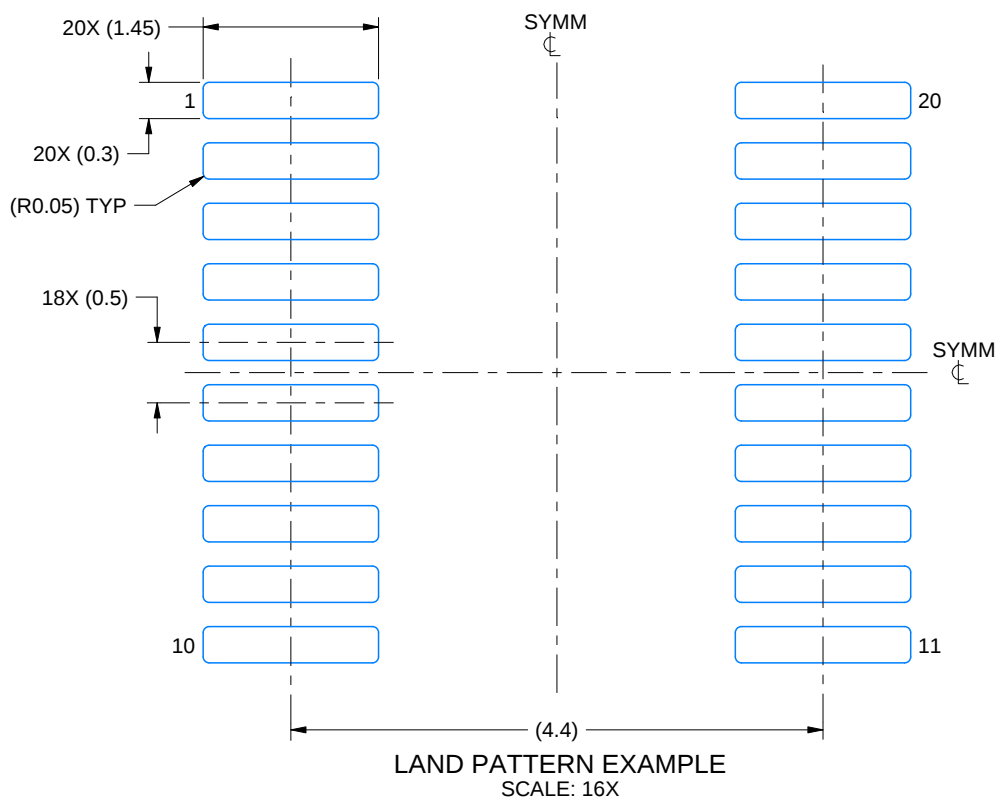
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.

EXAMPLE BOARD LAYOUT

DGS0020A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4226367/A 10/2020

NOTES: (continued)

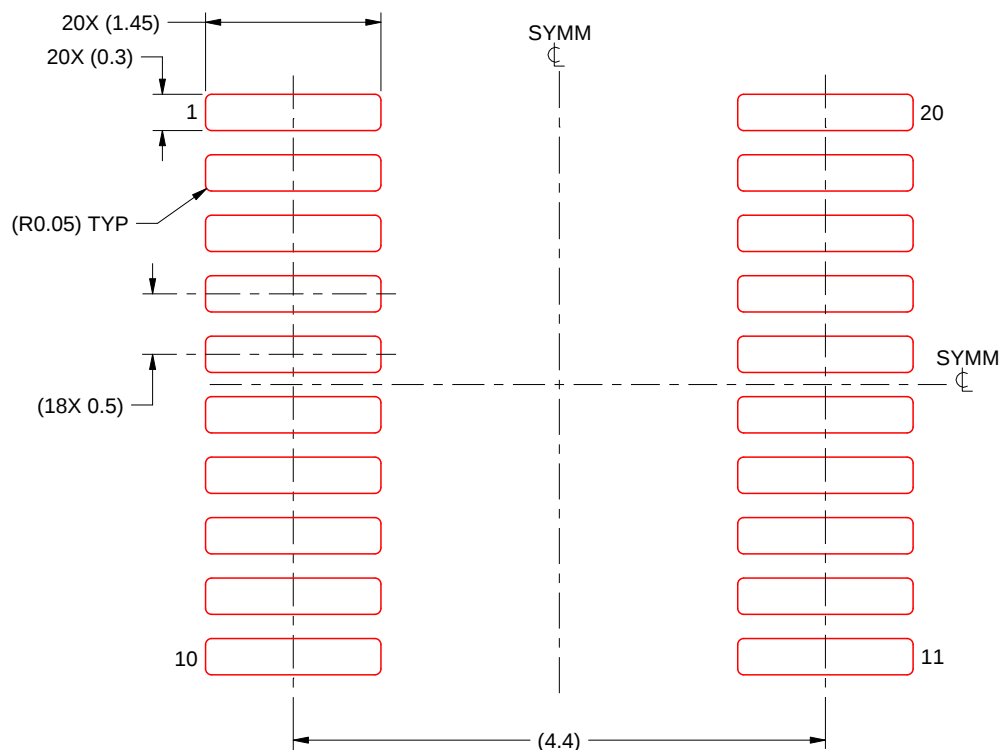
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DGS0020A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

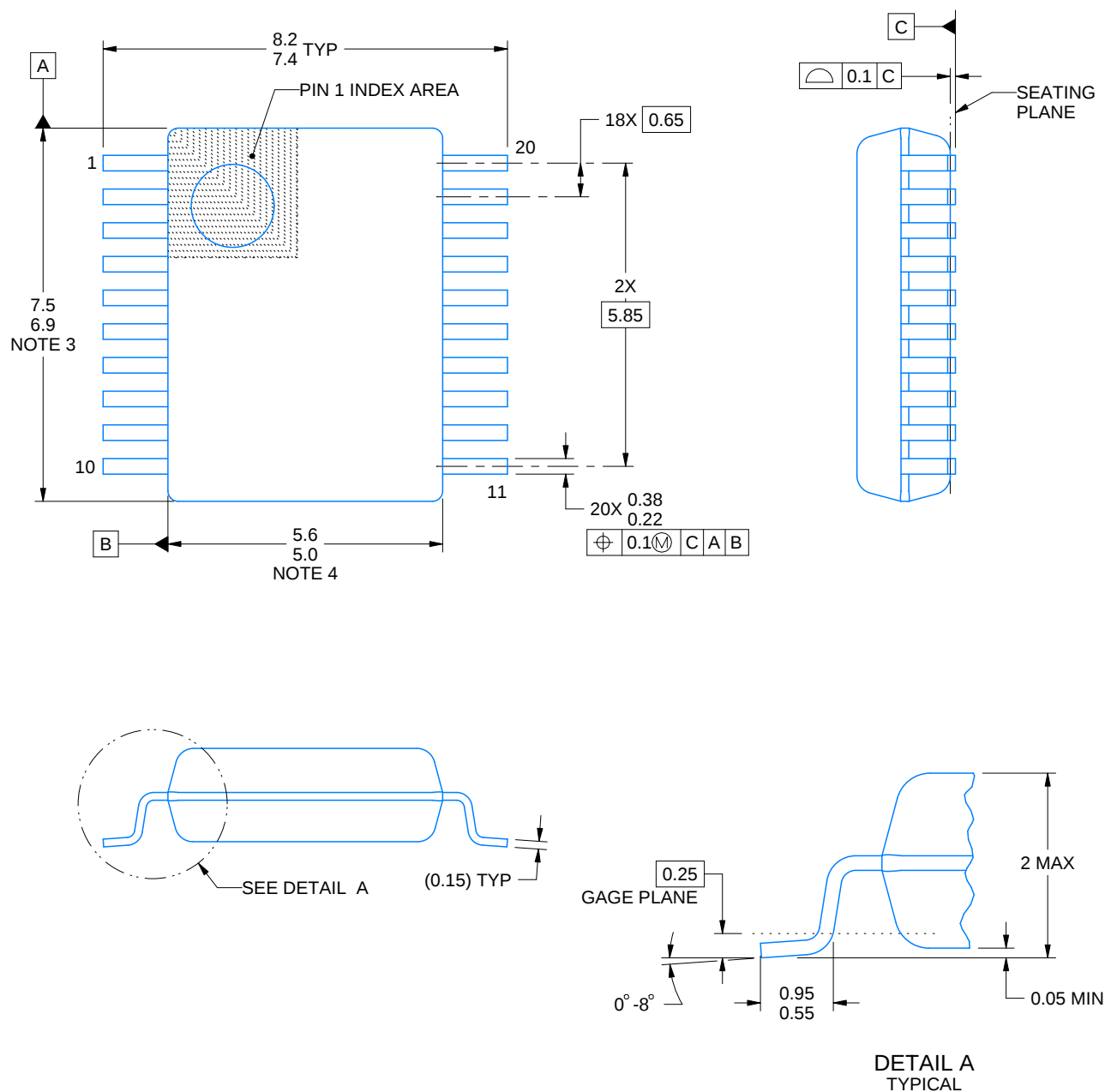


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 16X

4226367/A 10/2020

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.



4214851/B 08/2019

NOTES:

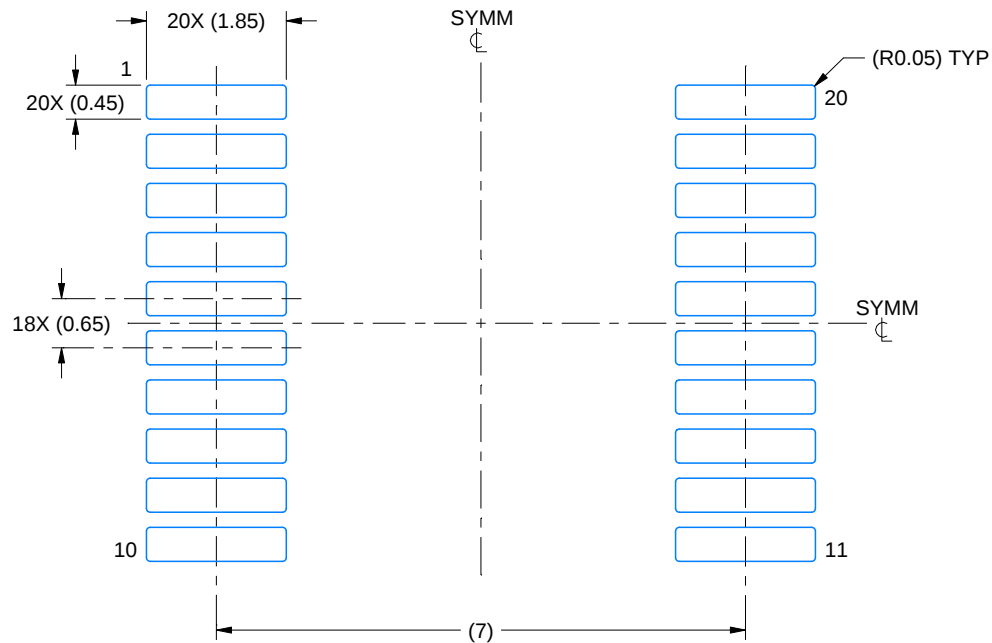
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

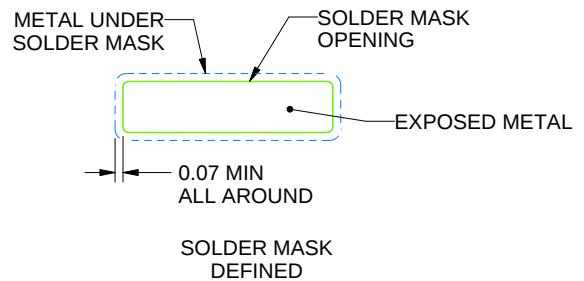
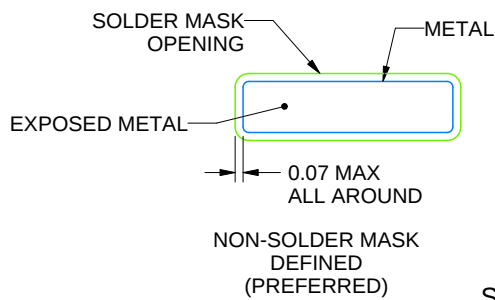
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

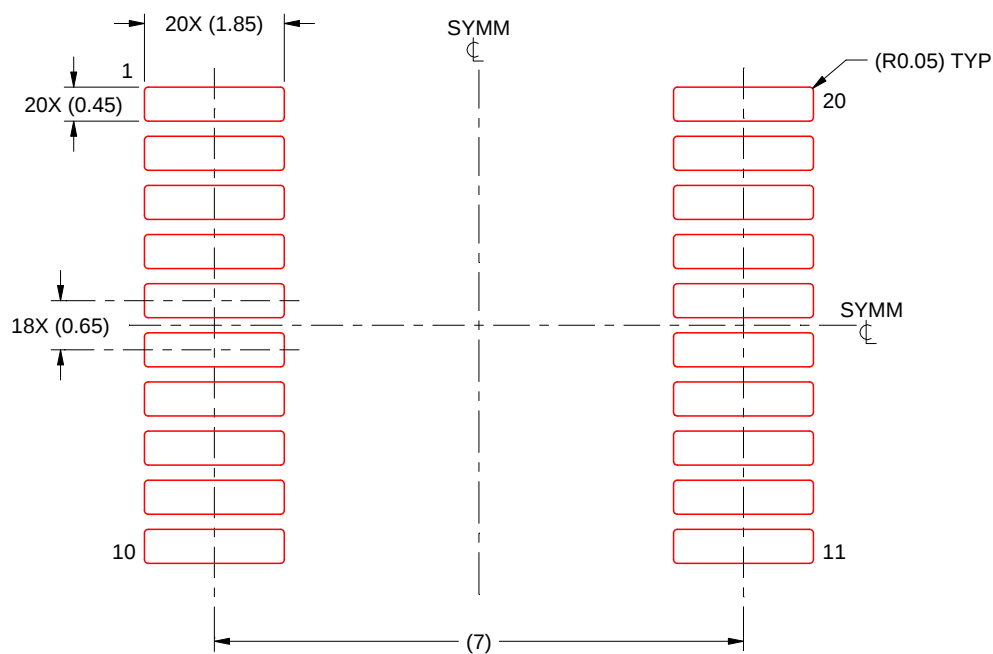
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

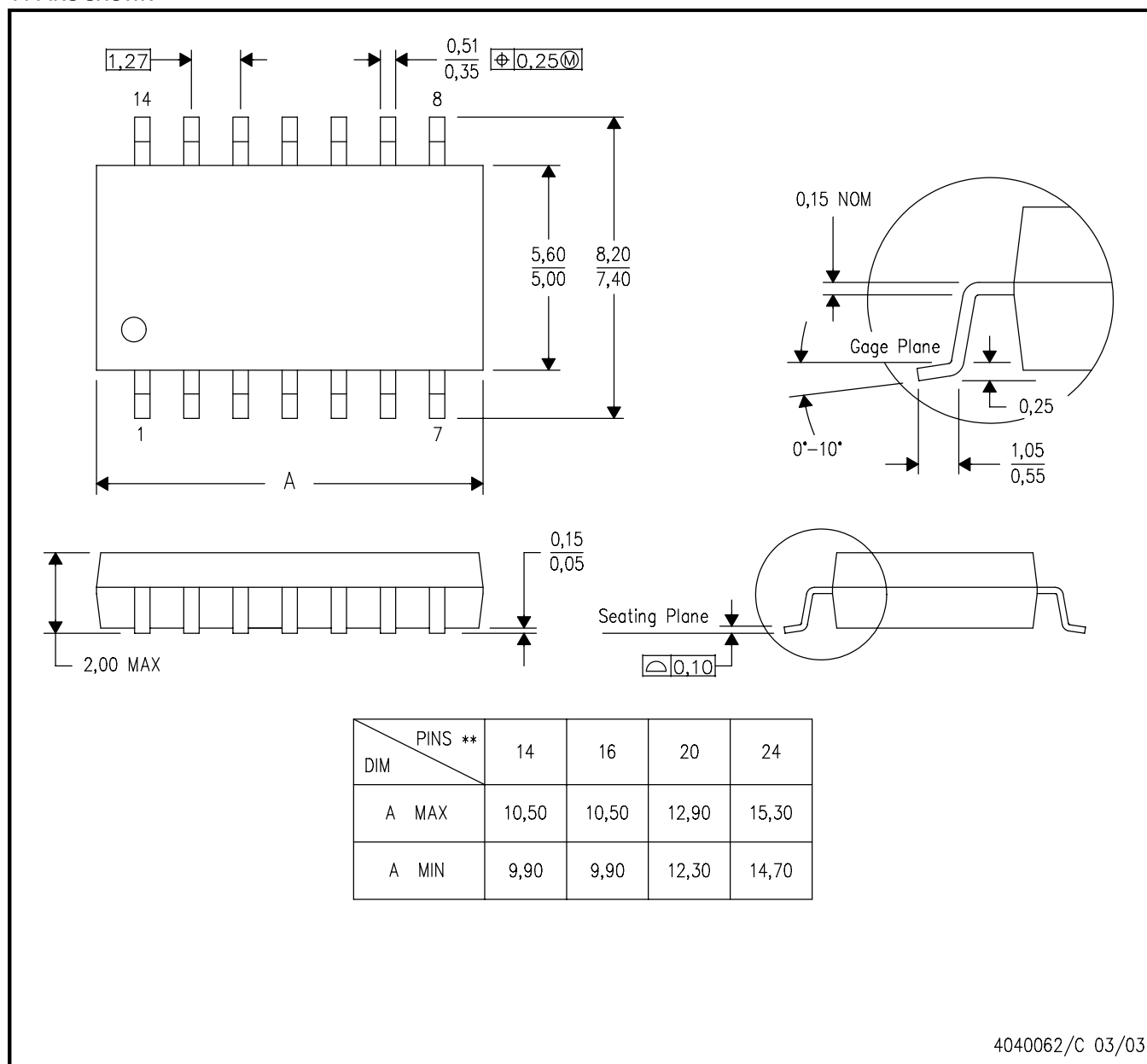
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

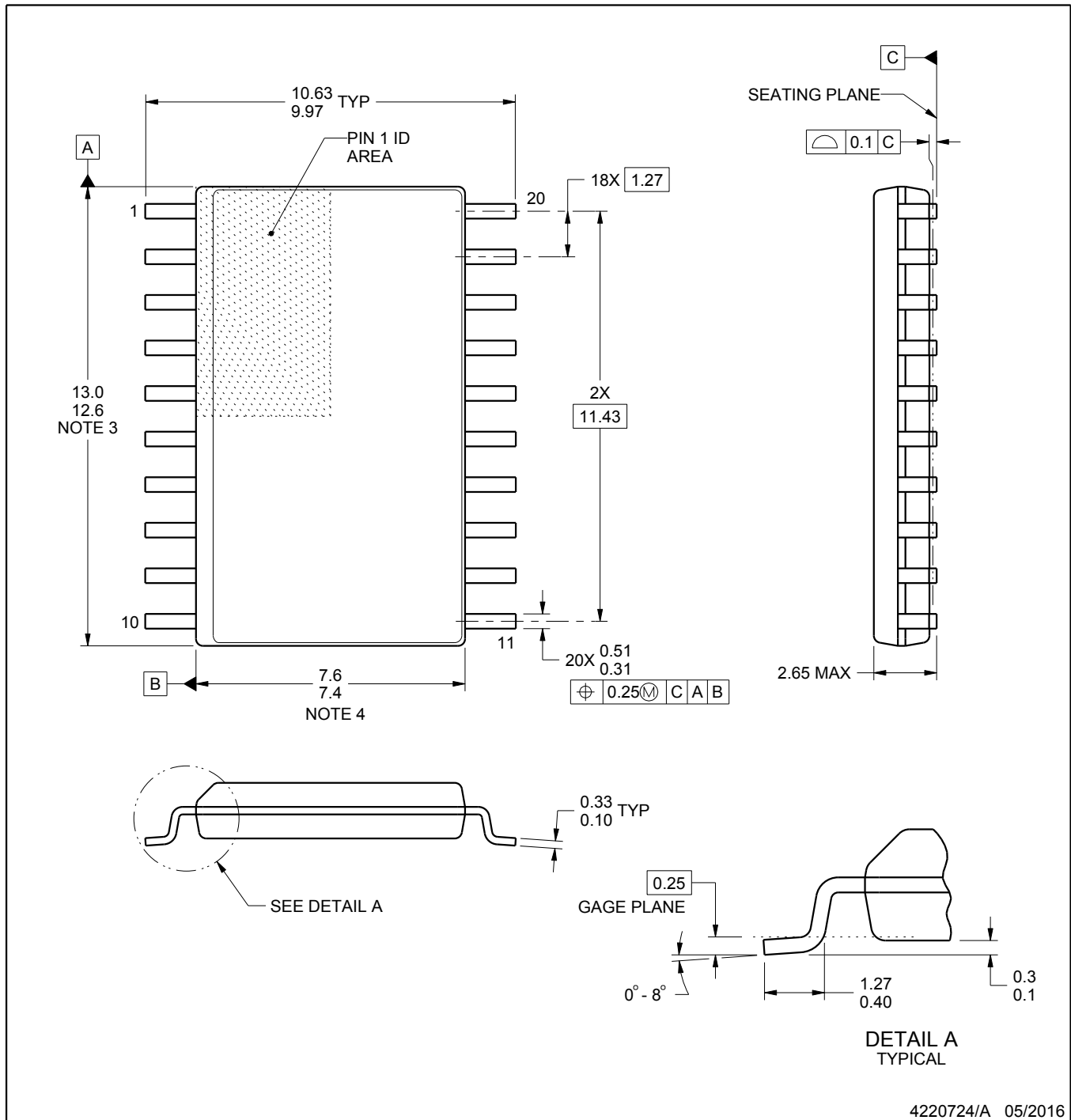
NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



NOTES:

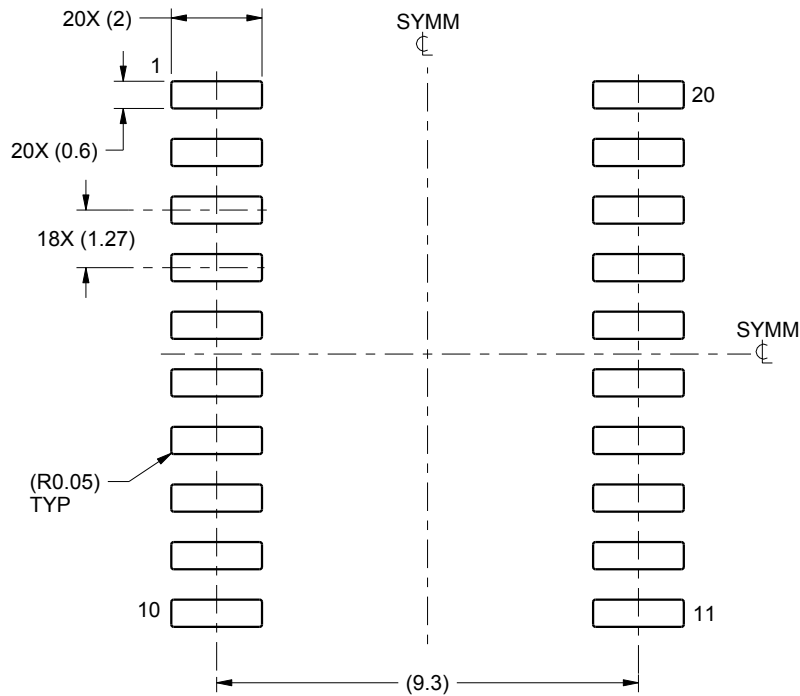
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

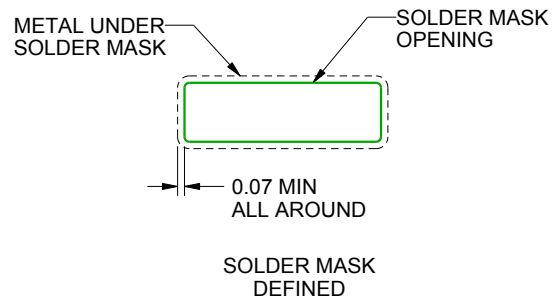
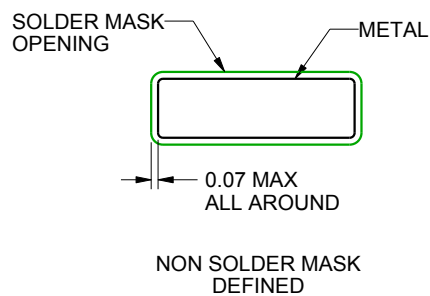
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

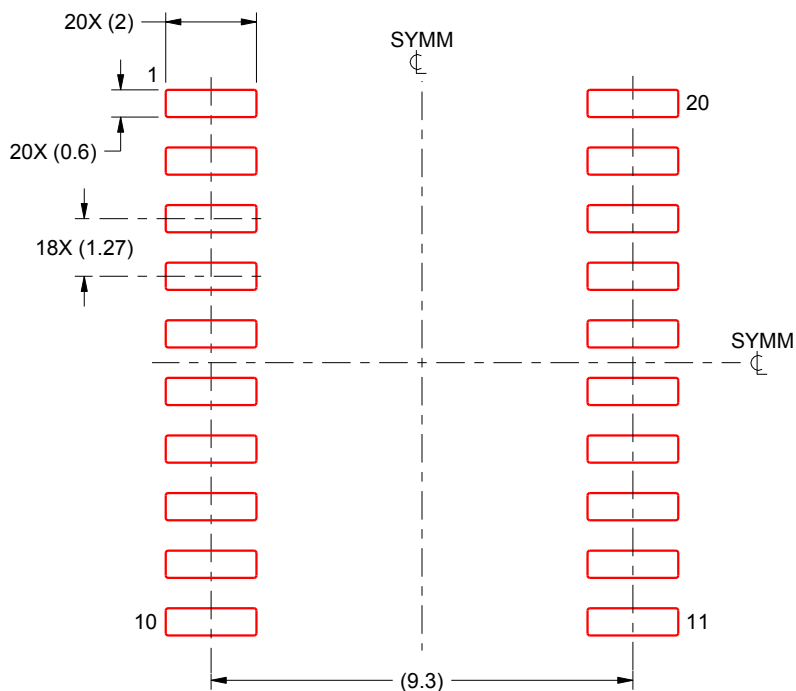
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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