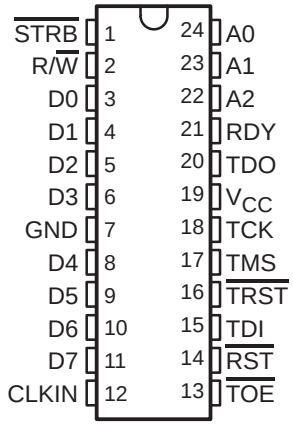
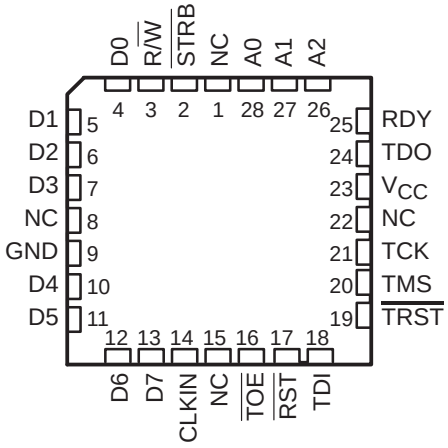
- **Members of Texas Instruments Broad Family of Testability Products Supporting IEEE Std 1149.1-1990 (JTAG) Test Access Port (TAP) and Boundary-Scan Architecture**
- **Provide Built-In Access to IEEE Std 1149.1 Scan-Accessible Test/Maintenance Facilities at Board and System Levels**
- **While Powered at 3.3 V, the TAP Interface Is Fully 5-V Tolerant for Mastering Both 5-V and/or 3.3-V IEEE Std 1149.1 Targets**
- **Simple Interface to Low-Cost 3.3-V Microprocessors/Microcontrollers Via 8-Bit Asynchronous Read/Write Data Bus**
- **Easy Programming Via Scan-Level Command Set and Smart TAP Control**
- **Transparently Generate Protocols to Support Multidrop TAP Configurations Using TI's Addressable Scan Port**
- **Flexible TCK Generator Provides Programmable Division, Gated-TCK, and Free-Running-TCK Modes**
- **Discrete TAP Control Mode Supports Arbitrary TMS/TDI Sequences for Noncompliant Targets**
- **Programmable 32-Bit Test Cycle Counter Allows Virtually Unlimited Scan/Test Length**
- **Accommodate Target Retiming (Pipeline) Delays of up to 15 TCK Cycles**
- **Test Output Enable ($\overline{TOE}$) Allows for External Control of TAP Signals**
- **High-Drive Outputs (−32-mA I_{OH}, 64-mA I_{OL}) at TAP Support Backplane Interface and/or High Fanout**

SN54LVT8980A . . . JT PACKAGE
SN74LVT8980A . . . DW PACKAGE
(TOP VIEW)



SN54LVT8980A . . . FK PACKAGE
(TOP VIEW)



NC − No internal connection

description

The 'LVT8980A embedded test-bus controllers (eTBCs) are members of the TI broad family of testability integrated circuits. This family of devices supports IEEE Std 1149.1-1990 boundary scan to facilitate testing of complex circuit assemblies. Unlike most other devices of this family, the eTBCs are not boundary-scannable devices; rather, their function is to master an IEEE Std 1149.1 (JTAG) test access port (TAP) under the command of an embedded host microprocessor/microcontroller. Thus, the eTBCs enable the practical and effective use of the IEEE Std 1149.1 test-access infrastructure to support embedded/built-in test, emulation, and configuration/maintenance facilities at board and system levels.

description (continued)

The eTBCs master all TAP signals required to support one 4- or 5-wire IEEE Std 1149.1 serial test bus: test clock (TCK), test mode select (TMS), test data input (TDI), test data output (TDO), and test reset ($\overline{\text{TRST}}$). All such signals can be connected directly to the associated target IEEE Std 1149.1 devices without need for additional logic or buffering. However, as well as being directly connected, the TMS, TDI, and TDO signals can be connected to distant target IEEE Std 1149.1 devices via a pipeline, with a retiming delay of up to 15 TCK cycles; the eTBCs automatically handle all associated serial-data justification.

Conceptually, the eTBCs operate as simple 8-bit memory- or I/O-mapped peripherals to a microprocessor/microcontroller (host). High-level commands and parallel data are passed to/from the eTBCs via their generic host interface, which includes an 8-bit data bus (D7−D0) and a 3-bit address bus (A2−A0). Read/write select (R/$\overline{\text{W}}$) and strobe ($\overline{\text{STRB}}$) signals are implemented so that the critical host-interface timing is independent of the CLKIN period. An asynchronous ready (RDY) indicator is provided to hold off, or insert wait states into, a host read/write cycle when the eTBCs cannot respond immediately to the requested read/write operation.

High-level commands are issued by the host to cause the eTBCs to generate the TMS sequences necessary to move the test bus from any stable TAP-controller state to any other such stable state, to scan instruction or data through test registers in target devices, and/or to execute instructions in the Run-Test/Idle TAP state. A 32-bit counter can be programmed to allow a predetermined number of scan or execute cycles.

During scan operations, serial data that appears at the TDI input is transferred into a serial to 4×8-bit-parallel first-in/first-out (FIFO) read buffer, which then can be read by the host to obtain the return serial-data stream up to eight bits at a time. Serial data that is to be transmitted from the TDO output is written by the host, up to eight bits at a time, to a 4×8-bit parallel-to-serial FIFO write buffer.

In addition to such simple state-movement, scan, and run-test operations, the eTBCs support several additional commands that provide for input-only scans, output-only scans, recirculate scans (in which TDI is mirrored back to TDO), and a scan mode that generates the protocols used to support multidrop TAP configurations using TI's addressable scan port. Two loopback modes also are supported that allow the microprocessor/microcontroller host to monitor the TDO or TMS data streams output by the eTBCs.

The eTBCs' flexible clocking architecture allows the user to choose between free-running (in which the TCK always follows CLKIN) and gated modes (in which the TCK output is held static except during state-move, run-test, or scan cycles) as well as to divide down TCK from CLKIN. A discrete mode also is available in which the TAP is driven strictly by read/write cycles under full control of the microprocessor/microcontroller host. These features ensure that virtually any IEEE Std 1149.1 target device or device chain can be serviced by the eTBCs, even where such may not fully comply to IEEE Std 1149.1.

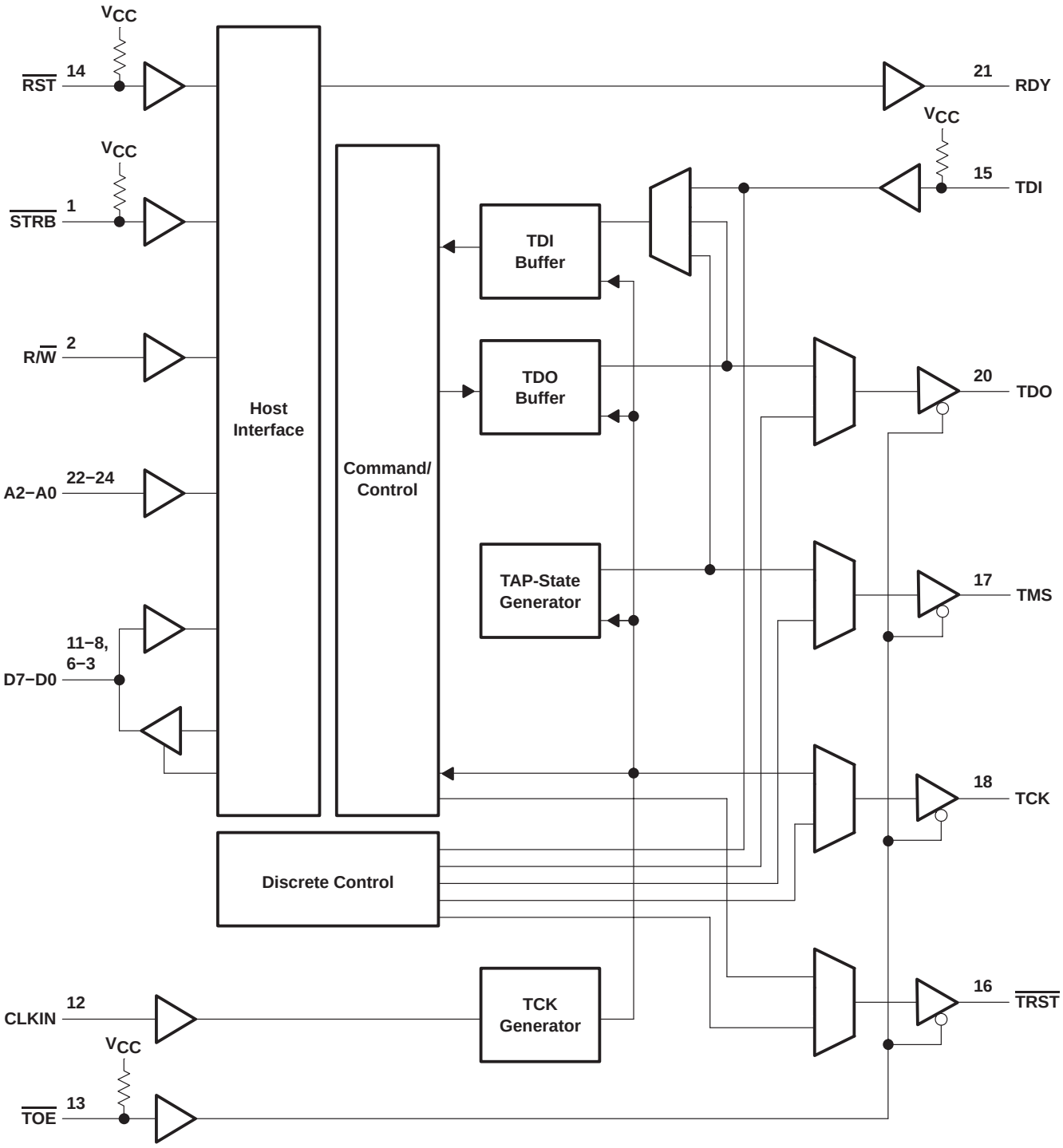
While most operations of the eTBCs are synchronous to CLKIN, a test-output enable ($\overline{\text{TOE}}$) is provided for output control of the TAP outputs, and a reset ($\overline{\text{RST}}$) input is provided for hardware reset of the eTBCs. The former can be used to disable the eTBCs so that an external controller can master the associated IEEE Std 1149.1 test bus.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SOIC − DW	Tube	SN74LVT8980ADW	LVT8980A
	SOIC − DWR	Tape and reel	SN74LVT8980ADWR	LVT8980A
−55°C to 125°C	CDIP − JT	Tube	SNJ54LVT8980AJT	SNJ54LVT8980AJT
	CFP − W	Tube	SNJ54LVT8980AW	SNJ54LVT8980AW
	LCCC − FK	Tube	SNJ54LVT8980AFK	SNJ54LVT8980AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

functional block diagram



Pin numbers shown are for the DW and JT packages.

Terminal Functions

TERMINAL NAME	DESCRIPTION
A2−A0	Address inputs. A2−A0 form the 3-bit address bus that interfaces the eTBC to its microprocessor/microcontroller host. These inputs directly index the eTBC register to be accessed (read from or written to).
CLKIN	Clock input. CLKIN is the system clock input for the eTBC. Most operations of the eTBC are synchronous to CLKIN. Internally, the CLKIN signal is divided by a programmable divisor to generate TCK.
D7−D0	Data inputs/outputs. D7−D0 form the 8-bit bidirectional data bus that interfaces the eTBC to its microprocessor/microcontroller host. Data in the eTBC registers is accessed (read or written) using this data bus. D7 is considered the most-significant bit (MSB), while D0 is considered the least-significant bit (LSB).
GND	Ground
RDY	Ready output. RDY is used to indicate to the microprocessor/microcontroller host whether or not the eTBC is ready to service the access (read or write) operation that currently is being requested. If RDY remains high following the initiation of an access cycle ($\overline{\text{STRB}}$ negative edge) the eTBC is ready. Otherwise, if RDY goes low following the initiation of an access cycle ($\overline{\text{STRB}}$ negative edge), the eTBC is not ready. In cases where the eTBC is not ready, subsequent processing in the eTBC may clear the not-ready state, which allows RDY to return high before the end of the access cycle. In any event, the RDY output returns high, upon the termination of any access cycle ($\overline{\text{STRB}}$ positive edge).
$\overline{\text{RST}}$	Reset input. $\overline{\text{RST}}$ is used to initiate asynchronous reset of the eTBC. Assertion (low) of $\overline{\text{RST}}$ places the eTBC in a reset state, from which it does not exit until $\overline{\text{RST}}$ is released (high). While $\overline{\text{RST}}$ is low, the eTBC ignores host writes, the RDY, TDO, TMS, and $\overline{\text{TRST}}$ outputs that are high, while TCK outputs CLKIN/16. An internal pullup forces $\overline{\text{RST}}$ to a high level if it has no external connection.
R/$\overline{\text{W}}$	Read/write select. R/$\overline{\text{W}}$ is used by the microprocessor/microcontroller host to instruct the eTBC as to whether it is to perform read access (R/$\overline{\text{W}}$ high) or write access (R/$\overline{\text{W}}$ low). While R/$\overline{\text{W}}$ is high and $\overline{\text{STRB}}$ is low, the D7−D0 outputs are enabled to drive low and/or high logic levels onto the host data bus. Otherwise, while R/$\overline{\text{W}}$ is low, the D7−D0 outputs are disabled to the high-impedance state so that the host data bus can drive to the eTBC.
$\overline{\text{STRB}}$	Read/write strobe. $\overline{\text{STRB}}$ is used by the microprocessor/microcontroller host to instruct the eTBC to initiate ($\overline{\text{STRB}}$ negative edge) or terminate/conclude ($\overline{\text{STRB}}$ positive edge) an access (read or write) operation. An internal pullup forces $\overline{\text{STRB}}$ to a high level if it has no external connection.
TCK	Test clock. TCK transmits the TCK signal required by the eTBC IEEE Std 1149.1 target(s). All operations of the TAP are synchronous to TCK. Generally, the TCK signal is generated internally by the eTBC by division of CLKIN by a programmable divisor. Alternatively, when the eTBC is in its discrete-control mode, a rising edge of TCK is generated on a read to the discrete-control register, while a falling edge is generated on a write to the discrete-control register.
TDI	Test data input. TDI receives the TDI signal output by the eTBC IEEE Std 1149.1 target(s). It is the serial input for shifting test data from the target(s); it is sampled on the rising edge of TCK and is expected to be transferred from the target(s) on the falling edge of TCK. An internal pullup forces TDI to a high level if it has no external connection.
TDO	Test data output. TDO transmits the TDO signal required by the eTBC IEEE Std 1149.1 target(s). It is the serial output for shifting test data to the target(s); it is transferred on the falling edge of TCK and is sampled in the target on the rising edge of TCK.
TMS	Test mode select. TMS transmits the TMS signal required by the eTBC IEEE Std 1149.1 target(s). It is the one control signal that directs the next TAP-controller state of the target(s). It is transferred from the eTBC on the falling edge of TCK and is sampled in the target(s) on the rising edge of TCK.
$\overline{\text{TOE}}$	Test-output enable. $\overline{\text{TOE}}$ is the active-low output enable for the eTBC TAP outputs (TCK, TDO, TMS, $\overline{\text{TRST}}$). When $\overline{\text{TOE}}$ is inactive (high) the TAP outputs are disabled to a high-impedance state. Otherwise, when $\overline{\text{TOE}}$ is active (low), the TAP outputs are enabled to drive low and/or high logic levels according to other eTBC functions. An internal pullup forces $\overline{\text{TOE}}$ to a high level if it has no external connection.
$\overline{\text{TRST}}$	Test reset. $\overline{\text{TRST}}$ transmits the $\overline{\text{TRST}}$ signal that may be required by some of the eTBC IEEE Std 1149.1 target(s). A low signal at $\overline{\text{TRST}}$ is intended to initiate asynchronous test reset of the connected target(s). Such a low signal at $\overline{\text{TRST}}$ is generated only when the microprocessor/microcontroller host writes an appropriate value into the eTBC command register or, while the eTBC is in discrete-control mode, into the discrete-control register.
V_{CC}	Supply voltage

application information

In application, the eTBC is used to master a single IEEE Std 1149.1 TAP under the control of a microprocessor/microcontroller host. A typical implementation is shown in Figure 1.

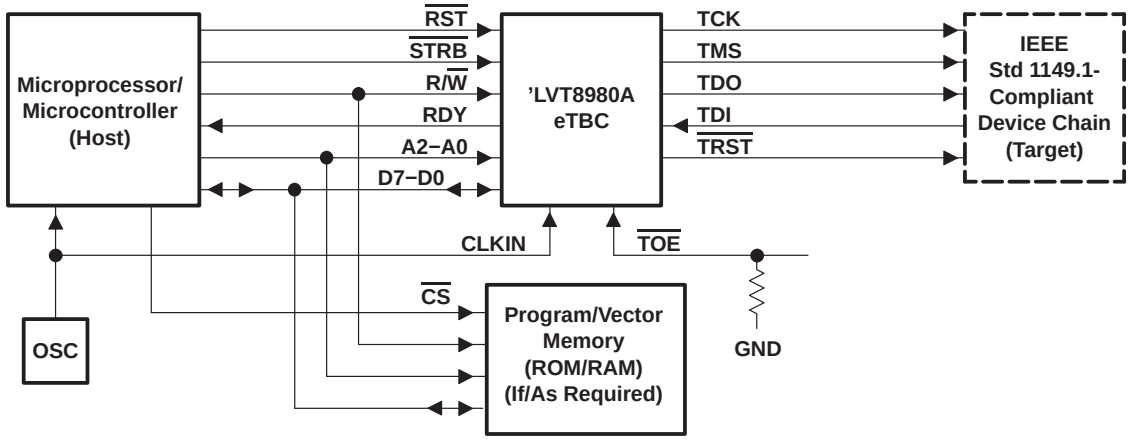


Figure 1. eTBC Application

All signals required to master IEEE Std 1149.1-compliant devices—TCK, TMS, TDO, TDI—are sourced/received by the eTBC. The eTBC also can source the optional $\overline{\text{TRST}}$ signal. Additionally, the eTBC implements high-drive output buffers, allowing it to interface directly to on- or off-board targets without need for buffering or other additional logic.

The eTBC generic host interface allows it to act as a simple 8-bit memory- or I/O-mapped peripheral. As shown in Figure 1, for many choices of host microprocessor/microcontroller, this interface can be accomplished without additional logic. While the eTBC requires a clock input (CLKIN), in many cases it can be driven from the same source that provides a clock signal to the host.

Thus, in combination with the host microprocessor/microcontroller, the eTBC can be used to implement a two-chip embedded test control function supporting board- and system-level built-in test based on structured IEEE Std 1149.1 test access. In some cases, for additional program and/or test vector storage, an external ROM/RAM may be required.

By use of the eTBC in such an embedded test control function, the host microprocessor/microcontroller is freed from the burden of generating the TAP-state sequences, serializing the outgoing bit stream, and deserializing the incoming bit stream. All such tasks are implemented in the eTBC, allowing the host to operate at full 8-bit parallel efficiency, host software to operate at the level of discrete scan operations versus the level of TAP manipulation, and test throughput to be maximized. The eTBC's full suite of data-scan and instruction-scan commands ensure that the host software operates efficiently.

Host efficiency and flexibility also is maximized through the eTBC's fully visible status and implementation of the ready (RDY) output. RDY goes inactive during a read or write access if the host-requested access cannot be performed immediately. Thus, it can be used to insert hold or wait states back to the host. When the condition blocking the access clears, the requested access completes. Additionally, all conditions that can cause such a blocking condition are updated continuously in the eTBC status and command registers. Thus, the host software can poll the eTBC status, rather than implement RDY in hardware.

application information (continued)

The eTBC also provides several capabilities that support special target application requirements. The eTBC $\overline{\text{TOE}}$ allows its master function to be disabled so that another device (an external tester, for example) can control the target TAP. Where required, due to target noncompliance or sensitivity to state sequencing, discrete-control mode provides the host software with arbitrary control of TMS and TDO sequences. Also, where targets may be sensitive to leaving Shift-DR state during scan operation, gated-TCK mode allows the TCK output to be stopped, rather than cycling the target TAP state to Pause-DR state, when service to TDI buffer or TDO buffer is required.

Where target devices are extremely distant (due to cabling, etc.), pipelining can be implemented at intervals along the incoming or outgoing paths to retime (deskew) the TDI, TDO, and TMS signals. An example is shown in Figure 2. In such applications, the eTBC automatically can adjust the incoming test-data bit stream to account for cycle delays introduced by the pipeline.

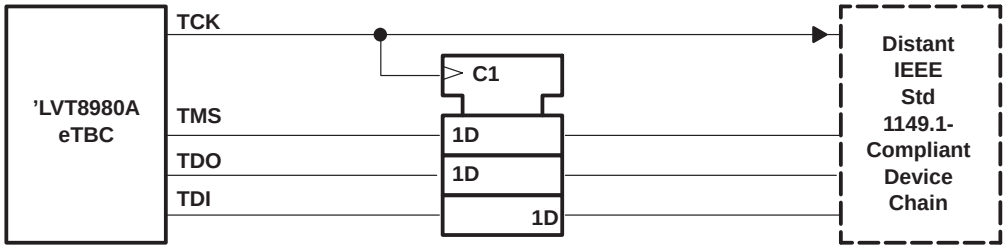


Figure 2. Retimed Interface to Target

Also, in gated-TCK mode, special scan commands provide transparent support for addressable shadow protocols. Thus, in conjunction with its high-drive outputs, the eTBC can fully support multidrop backplane TAP configurations implemented with TI addressable scan ports (ASPs). Figure 3 shows a multidrop TAP configuration in a passive-backplane application implemented with a centralized (one eTBC per chassis/rack) test-control architecture, while Figure 4 shows a passive-backplane application implemented with a distributed (eTBC per module) test-control architecture. Figure 5 shows a multidrop TAP configuration in an active-backplane (motherboard) application.

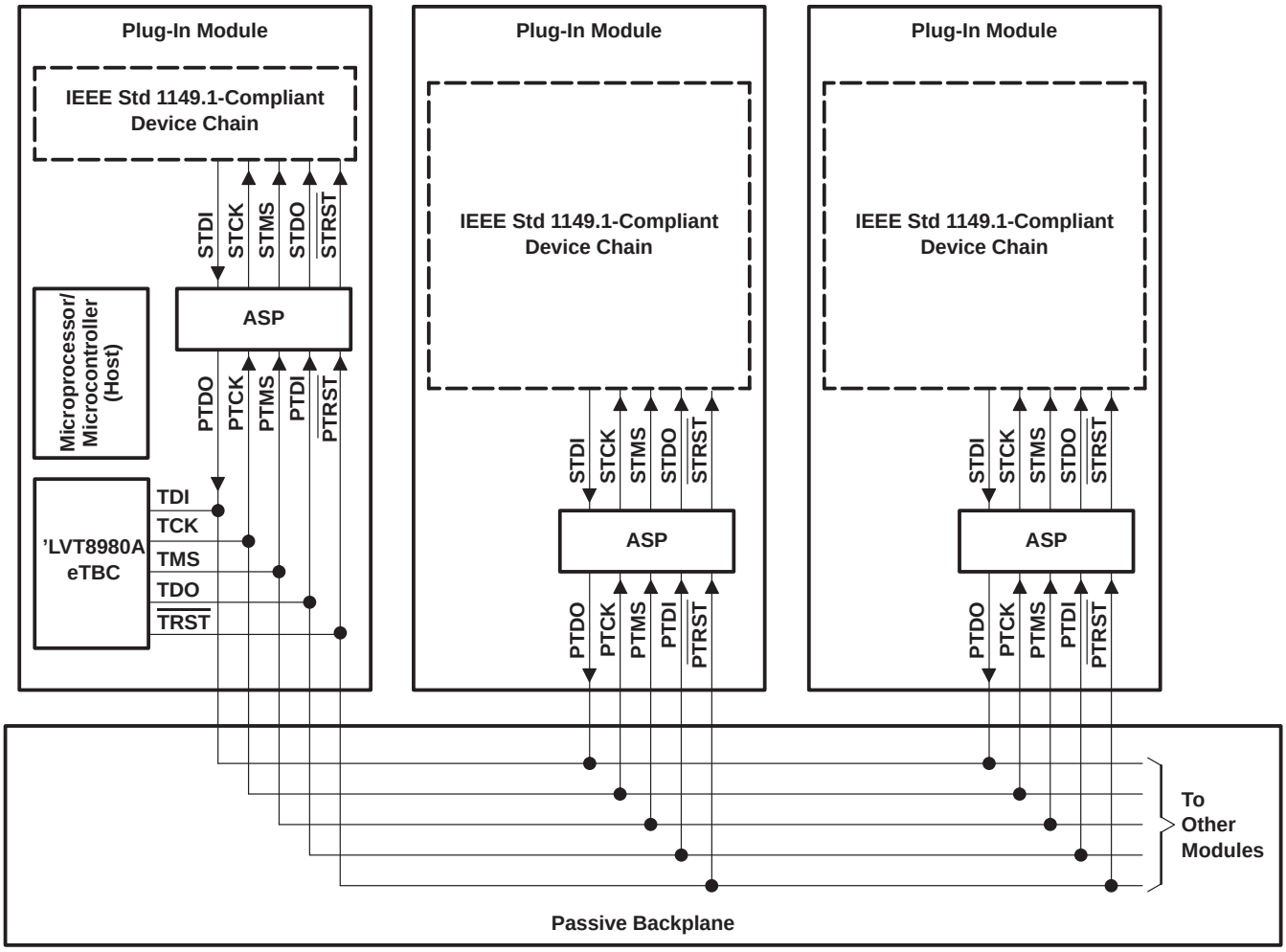


Figure 3. Passive-Backplane Application With Centralized (eTBC Per Chassis) Test-Control Architecture

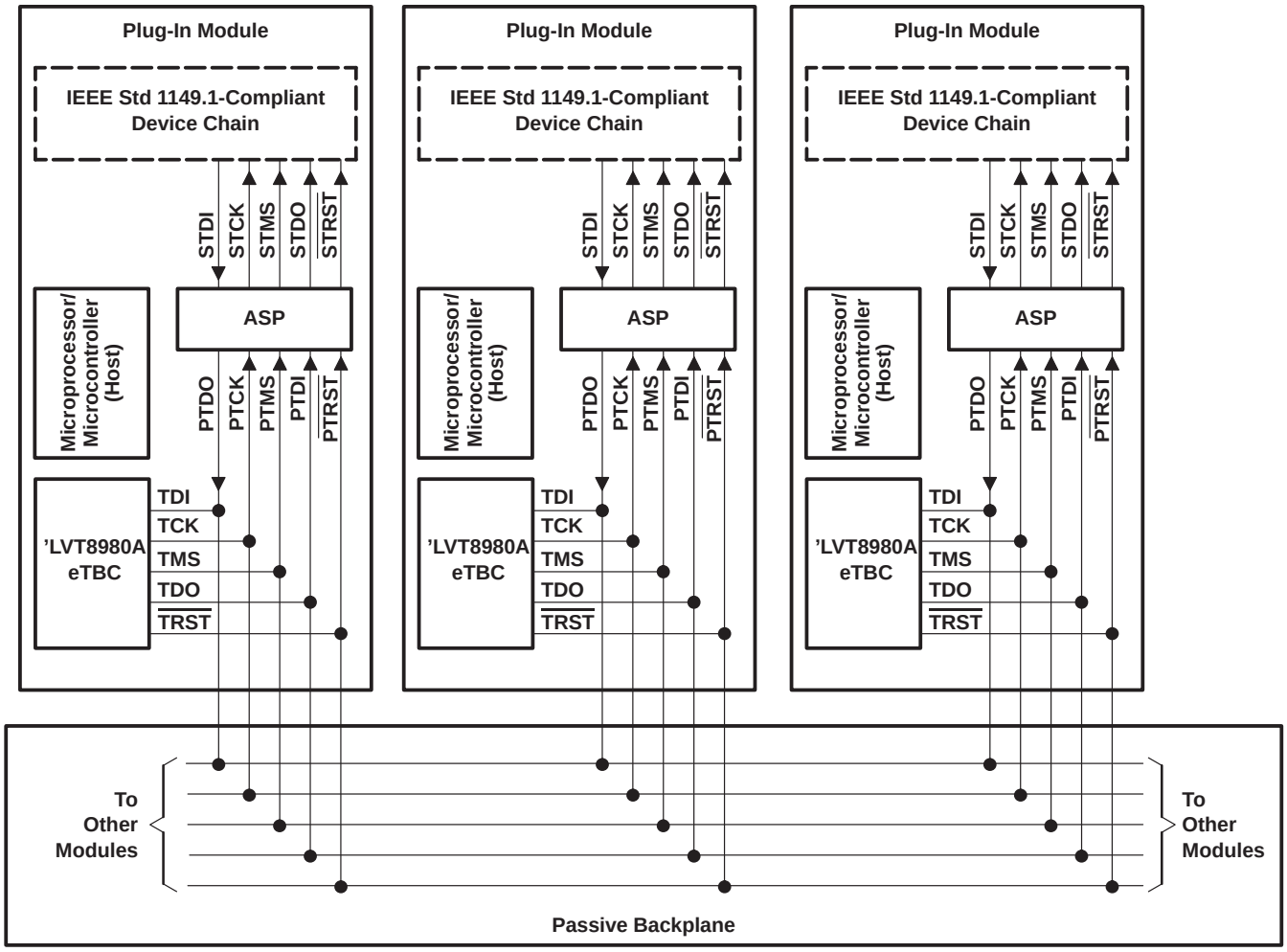


Figure 4. Passive-Backplane Application With Distributed Test-Control (eTBC Per Card) Architecture

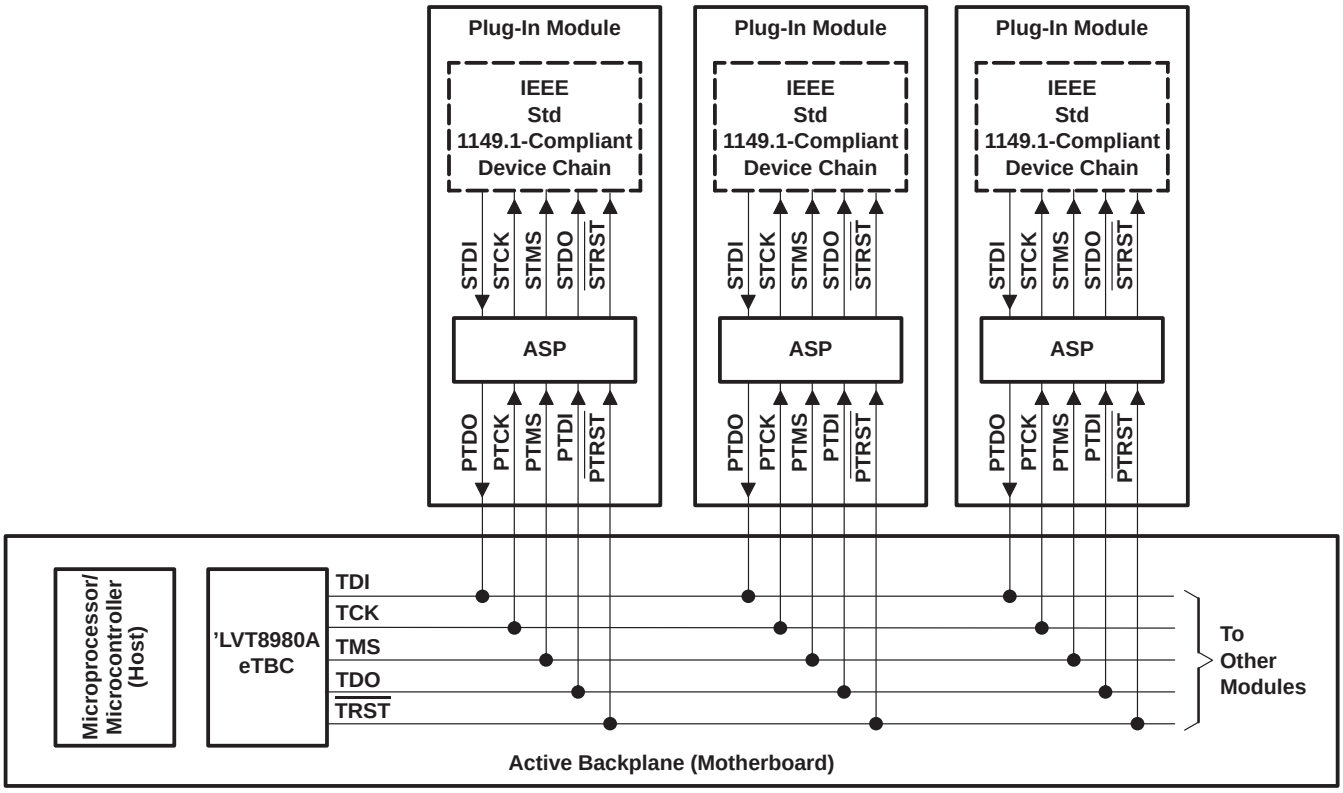


Figure 5. Active-Backplane (Motherboard) Application

architecture

Conceptually, the eTBC can be viewed as an IEEE Std 1149.1 coprocessor/accelerator that operates in conjunction with (and under the control of) a host microprocessor/microcontroller. The eTBC implements this function using an 8-bit generic host interface and a scan-test-based command/control architecture. As shown in the functional block diagram, beyond these fundamental elements and another central block supporting discrete-control mode, the eTBC functions are accomplished in four additional blocks—one for each of the required TAP signals—a TCK generator, a TAP-state (TMS) generator, a TDO buffer, and a TDI buffer.

host interface

The eTBC host interface is implemented generically on an 8-bit read/write data bus (D7−D0). Three address (A2−A0) pins directly index the eTBC's eight read/write registers: configurationA, configurationB, status, command, TDO buffer, TDI buffer, counter, and discrete control. The register address map is given in Table 1.

host access timing

Host access timing is asynchronous to the clock input (CLKIN) and is fully controlled by the read/write strobe ($\overline{\text{STRB}}$). The read/write select (R/$\overline{\text{W}}$) serves to control the direction of data flow on the bidirectional data bus. Figure 6 shows the read access timing, while Figure 7 shows the write access timing. As shown, for either read or write access, R/$\overline{\text{W}}$ and address signals should be held constant while $\overline{\text{STRB}}$ is low.

For read access (R/$\overline{\text{W}}$ high), the eTBC data bus outputs are made active, on the falling edge of $\overline{\text{STRB}}$, to drive the data contained in the eTBC register selected by address (A2−A0). Otherwise, when $\overline{\text{STRB}}$ is high, the eTBC data outputs are at high impedance. Therefore, in many applications, the R/$\overline{\text{W}}$ signal can be shared with other host peripherals (ROM or RAM, for example), while the $\overline{\text{STRB}}$ signal is generated separately (by discrete chip-select signals available from the host or a decode logic) for each required peripheral.

host access timing (continued)

For write access (R/$\overline{W}$ low), the eTBC data outputs remain at high impedance, independent of $\overline{STRB}$. During write access, the register selected by the address (A2−A0) inputs latches the values from the data bus on the rising edge of $\overline{STRB}$.

RDY from the host interface can be used, where the selected microprocessor/microcontroller supports it, to insert wait or hold states back to the host. If a host-requested access cannot be performed immediately, RDY goes inactive (low) during that given access. When the condition blocking the access clears, RDY goes active (high) and the eTBC grants the requested access. Alternatively, where such hardware-generated hold or wait states are not supported in the selected microprocessor/microcontroller host, the eTBC status and/or command registers can be polled to determine its readiness to grant a given read or write access.

Conditions that cause a host access to be blocked (and RDY to become inactive) are limited to the following:

- While the TDI buffer is empty, as indicated in status register (bit 7, TDIS), a requested read to TDI-buffer register generates RDY inactive; this condition clears, RDY goes active, and the requested access completes when the TDI buffer no longer is empty. Data on the data bus (D7−D0) is invalid while RDY is inactive. The correct data value will be latched onto the bus when RDY becomes active.
- While the TDO buffer is full or is being reset upon initiation of a scan command, as indicated in status register (bit 6, TDOS), a requested write to TDO-buffer register generates RDY inactive; this condition clears, RDY goes active, and the requested access completes when the TDO buffer no longer is full or the TDO-buffer reset completes, as applicable.
- While a command is in progress, as indicated by a nonzero value in the opcode field (bits 3−0, OPCOD) of the command register, a requested write to command, configurationA, configurationB, or counter registers generate RDY inactive. This condition clears, RDY goes active, and the requested access is complete when the previously specified command finishes. The sole exception is the writing of a logic 1 into the software reset (bit 7, SWRST) bit of the command register, which is never blocked.
- While a full-duplex scan command is in progress and the number of retiming-delay bits is other than zero, the number of writes to the TDO-buffer register may not exceed, by more than 4, the number of reads to the TDI-buffer register. A write to the TDO-buffer register that does exceed this limit is blocked and generates RDY inactive indefinitely; the TDI-buffer register must be read before another write to the TDO-buffer register.
- There also may be cases when the condition blocking the access does not clear. This might occur when trying to read the TDI buffer when empty and no bits are shifted into the TDI buffer before the host wait state times out. In this case, the host may abort the read or write access by taking $\overline{STRB}$ high while RDY is low. If the read/write access is terminated, the user should verify that a read/write did not occur. This verification should be performed to ensure that the eTBC did not begin to transition RDY active (high) just as the host wait state times out.

host access timing (continued)

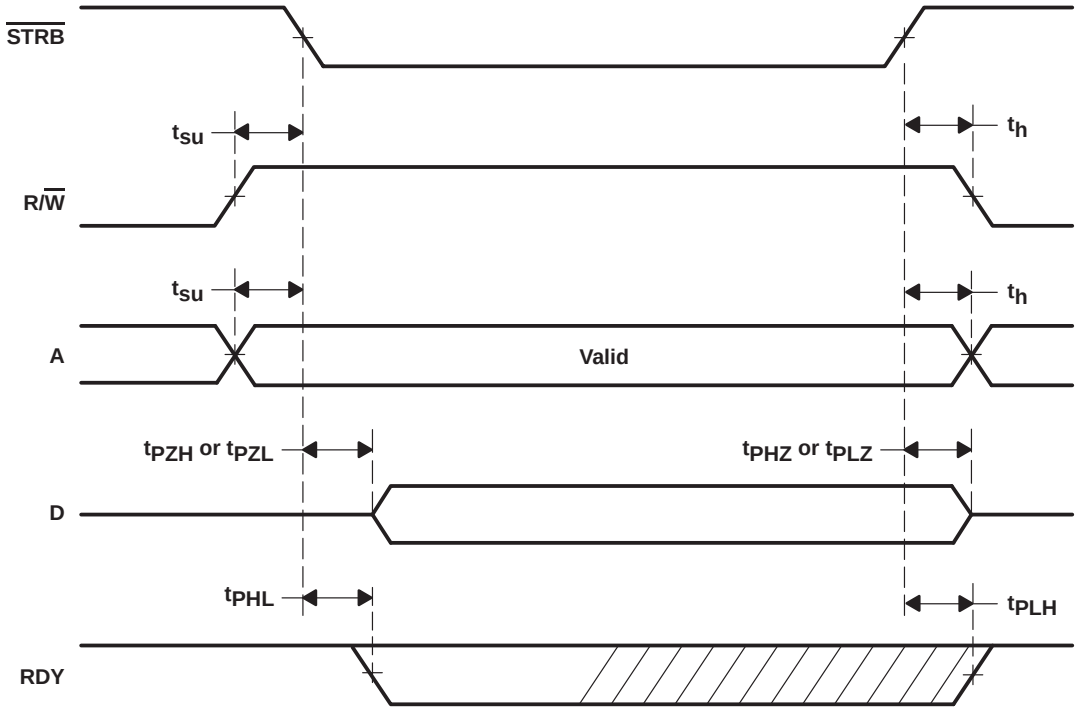


Figure 6. Read Access Timing

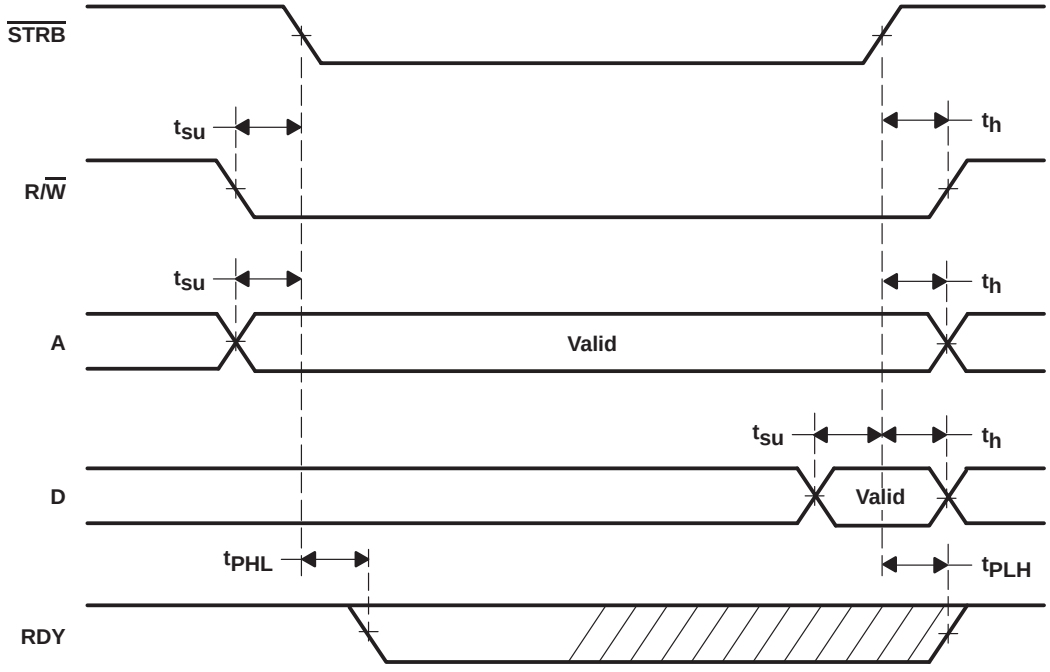


Figure 7. Write Access Timing

register descriptions

A summary of the eTBC registers, their address mappings, bit assignments, reset values, and host accessibility (read/write or read-only) is provided in Table 1. All registers are fully readable by the host. All registers are fully writeable by the host, with the exception of the status and TDI-buffer registers. Also, with the exception of TDO-buffer and command registers, writes to any register while a command is in progress are held off (RDY inactive) or ignored. Bits designated as reserved should be written to logic 0; read-only bits designated as reserved always read logic 0.

Table 1. Register Summary

ADDRESS A2−A0	REGISTER	REGISTER DETAIL (BIT ASSIGNMENTS)								RESET VALUE	HOST ACCESS
		BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)		
000	ConfigurationA	Reserved		NTOE	LPBK		MODE			0x00	R/W
001	ConfigurationB	CDIV			Reserved	RDLY				0x80	R/W
010	Status	TDIS	TDOS	CTRS	Reserved	TAPST				0x00	R
011	Command	SWRST	NTRST	ENDST		OPCOD				0x00	R/W
100	TDO buffer									0x00	R/W
101	TDI buffer									0x00	R
110	Counter									0x00	R/W
111	Discrete control	Reserved				DNTR	DTMS	DTDI	DTDO	0x00	R/W

configuration registers

All eTBC test commands operate under the influence of the configurationA and configurationB registers. The decodes of the various bit groups assigned to these registers are given in Table 2 and Table 3, respectively. These registers are fully readable at all times and are fully writeable except when an eTBC command is in progress. Bit group values designated as reserved should not be written.

Table 2. ConfigurationA Register Decode

CONFIGURATIONA		VALUE	RESULT
BIT GROUP	BIT NO.		
NTOE	5	0	TAP outputs (TCK, TDO, TMS, $\overline{\text{TRST}}$) are enabled.
		1	TAP outputs (TCK, TDO, TMS, $\overline{\text{TRST}}$) are disabled (high impedance).
LPBK	4−3	00	No loopback − TDI pin inputs to TDI buffer.
		01	TMS loopback − TAP-state generator inputs to TDI buffer. TMS and TDO pins are fixed high.
		10	TDO loopback − TDO buffer inputs to TDI buffer. TMS and TDO pins are fixed high.
		11	Reserved
MODE	2−0	000	Automatic/free-running-TCK mode − all TAP outputs are generated autonomously in the eTBC according to the active command. The TCK output runs continuously. While operating a scan command, if the TDI buffer becomes full and/or the TDO buffer becomes empty, the TAP state is cycled to Pause-DR or Pause-IR, as appropriate, until the host performs the required buffer service.
		001	Automatic/gated-TCK mode − all TAP outputs are generated autonomously in the eTBC according to the active command. The TCK output is run only when required to move TAP state or to progress run-test or scan operations, otherwise, it is gated off (low). While operating a scan command, if the TDI buffer becomes full and/or the TDO buffer becomes empty, the TAP state remains in Shift-IR or Shift-DR, as appropriate, but the TCK output is gated off until the host performs the required buffer service.
		010	Discrete-control mode − all TAP outputs are determined by contents of the discrete-control register under control of host software.
		011−111	Reserved

Table 3. ConfigurationB Register Decode

CONFIGURATIONB		VALUE	RESULT
BIT GROUP	BIT NO.		
CDIV	7−5	000−111	TCK = (CLKIN)/(2^{CDIV}); reset value TCK = (CLKIN)/(2^4) = CLKIN/16
RDLY	3−0	0000−1111	Number of retiming delays to accommodate = RDLY. While operating a scan command, TDI sampling is delayed by a number of TCK cycles, equal to RDLY, following the generation of Shift-DR or Shift-IR state, as appropriate.

The negated test-output-enable ($\overline{\text{TOE}}$) bit allows the host to disable the TAP outputs via software in a manner analogous to the hardware $\overline{\text{TOE}}$. The loopback (LPBK) bit group allows the selection of the source of data to be input to the TDI buffer, from the TDI pin for normal eTBC operations or, for eTBC verification purposes, from TAP-state (TMS) generator or TDO buffer. The test mode (MODE) bit group provides a choice of automatic/free-running-TCK, automatic/gated-TCK, or discrete-control modes.

The clock-divisor (CDIV) bit group allows software control of the TCK output frequency based on a division of the CLKIN input. Divisors from 2^0 (1) to 2^7 (128) are provided. The clock divisor defaults to 2^4 (16) on eTBC reset (power up, hardware initiated, or software initiated). The retiming-delay (RDLY) bit group provides for the automatic accommodation of retiming (pipeline) delays, which can be used to deskew the TAP signals to target scan chains that are electrically distant (due to cabling delays, etc).

status register

The status of the eTBC is reported fully and updated continuously in the status register. The decode of the various bit groups assigned to the status register is given in Table 4.

Table 4. Status Register Decode

STATUS		VALUE	RESULT
BIT GROUP	BIT NO.		
TDIS	7	0	The TDI buffer is empty − no TDI data is available for host read.
		1	The TDI buffer is not empty − at least one byte of TDI data is available for host read.
TDOS	6	0	The TDO buffer is not full − at least one byte in TDO buffer is available for host write.
		1	The TDO buffer is full − no bytes in TDO buffer are available for host write.
CTRS	5	0	The counter is not loaded with a complete 32-bit value − command operation cannot begin until counter load completes.
		1	The counter is loaded with a complete 32-bit value − command operation can begin.
TAPST	3−0	0000	The current target TAP state (as sent by the eTBC) is Test-Logic-Reset.
		0001	The current target TAP state (as sent by the eTBC) is Select-DR-Scan.
		0010	The current target TAP state (as sent by the eTBC) is Capture-DR.
		0011	The current target TAP state (as sent by the eTBC) is Shift-DR.
		0100	The current target TAP state (as sent by the eTBC) is Exit1-DR.
		0101	The current target TAP state (as sent by the eTBC) is Pause-DR.
		0110	The current target TAP state (as sent by the eTBC) is Exit2-DR.
		0111	The current target TAP state (as sent by the eTBC) is Update-DR.
		1000	The current target TAP state (as sent by the eTBC) is Run-Test/Idle.
		1001	The current target TAP state (as sent by the eTBC) is Select-IR-Scan.
		1010	The current target TAP state (as sent by the eTBC) is Capture-IR.
		1011	The current target TAP state (as sent by the eTBC) is Shift-IR
		1100	The current target TAP state (as sent by the eTBC) is Exit1-IR.
		1101	The current target TAP state (as sent by the eTBC) is Pause-IR.
		1110	The current target TAP state (as sent by the eTBC) is Exit2-IR.
		1111	The current target TAP state (as sent by the eTBC) is Update-IR.

The TDI-buffer-status (TDIS) bit reports the readiness of the TDI buffer to respond to a host read. The TDO-buffer-status (TDOS) bit reports the readiness of the TDO buffer to respond to a host write. The counter-status (CTRS) bit reports the readiness of the counter to support a command that uses the counter. The current-TAP-state (TAPST) bit group continuously reports the target TAP state as monitored by the eTBC.

command register

The command register is used to perform software reset of the eTBC, to discretely control the state of the TRST output when not in discrete-control mode, and to initiate test operations in the target(s).The decode of the various bits assigned to the command register is given in Table 5.

Any read to the command register while a command is in progress returns the value written to the command register upon initiation of the command. Once a command finishes, the operation-code (OPCOD) bit group in the command register is reset to null. In this way, the status of a requested command can be monitored/polled by the host.

With the exception of the software-reset (SWRST) bit, which can be written at any time, writes to the command register while a command is in progress causes RDY to go inactive and is ignored if the write cycle is terminated before the previously requested command finishes.

command register (continued)

Table 5. Command Register Decode

COMMAND		VALUE	RESULT	TEST OPERATION COMMENTS			
BIT GROUP	BIT NO.			WORKING TAP STATE	USES COUNTER	USES TDI BUFFER	USES TDO BUFFER
SWRST	7	0	Normal operation				
		1	Full reset				
TRST	6	0	If not in discrete-control mode, output high to $\overline{\text{TRST}}$ pin				
		1	If not in discrete-control mode, output low to $\overline{\text{TRST}}$ pin				
ENDST	5−4	00	Finish command in TAP state Test-Logic-Reset				
		01	Finish command in TAP state Run-Test/Idle				
		10	Finish command in TAP state Pause-DR				
		11	Finish command in TAP state Pause-IR				
OPCOD	3−0	0000	Null				
		0001	Reserved				
		0010	Execute run test	Run-Test/Idle	Yes	No	No
		0011	Execute input-only ASP scan	N/A	Yes	Yes	No
		0100	Execute ASP scan	N/A	Yes	Yes	Yes
		0101	Execute output-only ASP scan	N/A	Yes	No	Yes
		0110	Execute state move	N/A	No	No	No
		0111	Execute state jump	N/A	No	No	No
		1000	Execute instruction-register scan	Shift-IR	Yes	Yes	Yes
		1001	Execute data-register scan	Shift-DR	Yes	Yes	Yes
		1010	Execute input-only instruction-register scan	Shift-IR	Yes	Yes	No
		1011	Execute input-only data-register scan	Shift-DR	Yes	Yes	No
		1100	Execute output-only instruction-register scan	Shift-IR	Yes	No	Yes
		1101	Execute output-only data-register scan	Shift-DR	Yes	No	Yes
		1110	Execute recirculate instruction-register scan	Shift-IR	Yes	Yes	No
		1111	Execute recirculate data-register scan	Shift-DR	Yes	Yes	No

The software-reset (SWRST) bit is provided to allow software initiation of full eTBC reset. This bit of the command register can be written at any time, regardless of the configuration or command in progress. The test-reset (TRST) bit allows direct software control of the state of $\overline{\text{TRST}}$ output in modes other than discrete control.

The end-TAP-state (ENDST) bit group determines the TAP state in which the target scan chain is left when the requested command finishes. The operation-code (OPCOD) bit group determines the test operation to be executed in the target.

counter register

The counter register, while only 8 bits wide like any other eTBC register, provides read/write access to the full 32-bit eTBC counter. Writes to the counter register are accomplished by four complete host access cycles; otherwise, the counter is considered unloaded (CTRS = 0). Reads to the counter register likewise are accomplished by four complete host access cycles. However, reads do not affect the CTRS. The counter access (both read and write) is in least-significant-byte-first order. Any writes to the counter register while a command is in progress are ignored. The 32-bit value present in the counter at initiation of a command is used to determine the number of TCK cycles or scan bits for which the command is operated.

TDO-buffer register

The TDO-buffer register, while only 8 bits wide like any other eTBC register, provides write access to the full 4×8 (32-bit) FIFO that comprises the TDO buffer. The TDO-buffer register can be written to as long as the TDO buffer does not become full. When the TDO buffer becomes full, further writes to the TDO-buffer register cause RDY to go inactive (and consequent hold or wait states to be sent back to the host, if supported) and cause the write to be ignored if the write cycle is terminated before the TDO-buffer-full status is cleared.

TDI-buffer register

The TDI-buffer register, while only 8 bits wide like any other eTBC register, provides read access to the full 4×8 (32-bit) FIFO that comprises the TDI buffer. The TDI-buffer register can be read as long as the TDI buffer does not become empty. When the TDI buffer becomes empty, further reads to the TDI-buffer register cause RDY to go inactive (and consequent hold or wait states to be sent back to the host, if supported) and cause the read data to be invalid if the read cycle is terminated before the TDI-buffer-empty status is cleared.

discrete-control register

The discrete-control register is used to program the state of the TAP outputs (TCK, TDO, TMS, $\overline{\text{TRST}}$) and to poll the state of the TAP input (TDI) when the eTBC is in its discrete-control mode. The contents of the discrete-control register determine values output to TDO, TMS, and $\overline{\text{TRST}}$ according to the decode in Table 6. The TCK output is generated on each read and write to the discrete-control register; writes generate TCK falling edge, while reads generate TCK rising edge. In modes other than the discrete-control mode, this register is fully writeable and readable, but writes and reads have no effect on the eTBC or target operation.

Table 6. Discrete-Control Register Decode

DISCRETE CONTROL		VALUE	RESULT
BIT GROUP	BIT NO.		
DNTR	3	0	If in discrete-control mode, output low to $\overline{\text{TRST}}$ pin, otherwise nothing
		1	If in discrete-control mode, output high to $\overline{\text{TRST}}$ pin, otherwise nothing
DTMS	2	0	If in discrete-control mode, output low to TMS pin, otherwise nothing
		1	If in discrete-control mode, output high to TMS pin, otherwise nothing
DTDI	1	0	The TDI data received is a logic 0.
		1	The TDI data received is a logic 1.
DTDO	0	0	If in discrete-control mode, output low to TDO pin, otherwise nothing
		1	If in discrete-control mode, output high to TDO pin, otherwise nothing

command/control

The eTBC command-based architecture is structured around a set of comprehensive IEEE Std 1149.1 (JTAG) test objectives, which include TAP state movement, scan operations, and run test (operation of test logic in Run-Test/Idle state). The set of test operations, as decoded from the command register (bits 3−0, OPCOD) is given in Table 5. Commands are initiated by writing the eTBC command register; upon command initiation, the test-control logic is initialized and the TDO and TDI buffers are cleared. Command completion is indicated when the operation code (OPCOD) field of the command register returns to the value of the null command.

The eTBC command operation is modified by the configurationA and configurationB registers, which should be written prior to writing the command register, as the values in these registers cannot be modified while a command is in progress. Also, commands are operated only in automatic test modes, as specified in the configurationA register (bits 2−0, MODE); while in the discrete-control mode, commands are ignored.

All eTBC commands operate similarly to accomplish IEEE Std 1149.1 test objectives. First, the eTBC generates a TMS sequence to move the target scan chain from its current TAP state to a working state that depends on the test objective. Second, the command is operated (test run, bits scanned) in the working state for a number of TCK cycles (or scan bits) determined by the value of the counter upon command initiation. Third, the eTBC generates a TMS sequence to move the target scan chain from the working state to the end state specified in the command register (bits 5−4, ENDST). For some commands, one or more of these steps are omitted.

TAP-state-movement commands

Two eTBC commands are provided to accomplish TAP state movement. The state-move command operates to generate a TMS sequence to move the target scan chain directly from its current TAP state to the end state specified in the command register. The state-jump command moves the eTBC's stored value of the target TAP state without generating any changes to the TMS output. The state-jump command can, therefore, be used to switch between targets that share the same test bus, such as those in a multidrop backplane configuration implemented with TI addressable scan ports, but that may be left in different TAP states.

run-test command

The run-test command allows the test logic of the target scan chain to execute autonomously in the Run-Test/Idle TAP state. Such test logic is commonly used to implement chip- or board-level built-in self test. The run-test command generates TMS sequences to move the target scan chain from its current TAP state to the Run-Test/Idle TAP state where it remains for a number of TCK cycles determined by the value of the counter upon command initiation. Upon the countdown of the counter to zero, the eTBC generates TMS sequences to move the target scan chain to the end state specified in the command register.

scan commands

Eleven eTBC commands are provided to perform scan operations to target scan chains. These can be classified by the destination of scan data in the target-addressable scan port (ASP), IEEE Std 1149.1 instruction register, or IEEE Std 1149.1 data register—and by the nature/direction of the data transfer—full duplex (default), input only, output only, or recirculate. The only combination of these two factors that is not implemented is recirculate ASP scan.

addressable scan-port (ASP) scan commands

The ASP scan commands scan data to and/or from an addressable scan-port target. Since ASP devices require that TMS remain fixed throughout their select and acknowledge protocols, the eTBC does not generate TMS sequences or change its stored value of the target's TAP state. Also, for the same reason, ASP scan commands that target ASP devices should be operated in gated-TCK mode. The ASP scan commands do allow data written to the TDO buffer to be driven serially onto the TDO pin and bits received serially at the TDI pin to be stored into the TDI buffer for reading by the host. However, the ASP scan commands do not perform any bit-pair encoding of ASP select protocols or decoding of ASP acknowledge protocols. Such encoding/decoding must be performed in the host. The number of data bits transferred in and/or out is determined by the value of the counter upon command initiation.

instruction-register scan commands

The instruction-register scan commands scan bits to and/or from the concatenation of instruction registers in a target scan chain. The eTBC generates a TMS sequence to move the target scan chain from its current TAP state to the Shift-IR TAP state. Data written to the TDO buffer can be driven serially onto the TDO pin and bits received serially at the TDI pin can be stored into the TDI buffer for reading by the host. The number of data bits transferred in and/or out is determined by the value of the counter upon command initiation. If, during the operation of an instruction register scan command, the TDO buffer becomes empty or the TDI buffer becomes full, the TAP state is sequenced to Pause-IR (if in free-running-TCK mode) or the TCK output is gated off (if in gated-TCK mode) until the required buffer service is performed. Upon the countdown of the counter to zero, the eTBC generates TMS sequences to move the target scan chain to the end state specified in the command register.

data-register scan commands

The data-register scan commands operate to scan bits to and/or from the concatenation of data registers in a target scan chain. The eTBC generates a TMS sequence to move the target scan chain from its current TAP state to the Shift-DR TAP state. Data written to the TDO buffer can be driven serially onto the TDO pin and bits received serially at the TDI pin can be stored in the TDI buffer for reading by the host. The number of data bits transferred in and/or out is determined by the value of the counter upon command initiation. If, during the operation of a data-register scan command, the TDO buffer becomes empty or the TDI buffer becomes full, the TAP state is sequenced to Pause-DR (if in free-running-TCK mode) or the TCK output is gated off (if in gated-TCK mode) until the required buffer service is performed. Upon the countdown of the counter to zero, the eTBC generates TMS sequences to move the target scan chain to the end state specified in the command register.

other scan-command variations

As noted before, the nature/direction of the data transfer for any scan command can vary along with the destination of scan data in the target:

- For scan commands of the full-duplex class, both TDO buffer and TDI buffer are used to scan data to and from the target scan chain, respectively.
- For scan commands of the input-only class, only the TDI buffer is used to scan data from the target scan chain; outgoing TDO data is fixed at a high level throughout the scan operation. When using link delays and input-only commands, the counter must be loaded with no more than 32 bits to avoid TDI buffer overflow errors.
- For scan commands of the output-only class, only the TDO buffer is used to scan data to the target scan chain; incoming TDI data is simply ignored.
- For scan commands of the recirculate class, only the TDI buffer is used to scan data from the target scan chain; outgoing TDO data is generated by recirculating the incoming TDI data back into the target scan chain. When using link delays and recirculate commands, the counter must be loaded with no more than 32 bits to avoid TDI buffer overflow errors.

counter

As previously described, the value loaded in the eTBC 32-bit counter at initiation of a command is used to specify the number of TCK cycles or scan bits to remain in the command's working state. As each TCK cycle or scan bit is processed for a run-test or scan command, respectively, the counter value is decremented. When the counter value reaches zero, the command leaves its working state to finish in the end state specified in the command register.

Before a command that uses the counter can be initiated, a full 32-bit value should be loaded by four consecutive writes to the counter register. Also, the full 32-bit current value of the counter can be observed by four consecutive reads to the counter register. The counter status (unloaded/loaded) is maintained and observable in the status register (bit 5, CTRS).

Upon eTBC reset (power up, hardware initiated, or software initiated), the counter is cleared and assumes its unloaded state.

TCK generator

The TCK generator sources the TCK signal required by the IEEE Std 1149.1 target(s) and the eTBC internal test-control logic. The fundamental TCK frequency is produced by division of CLKIN. The divisor is programmable within a range of 1 to 128 in the configurationB register (bits 7−5, CDIV). The TCK output to the target(s) operate in free-running or gated modes. The free-running mode toggles TCK continuously, based on CLKIN, while the gated mode operates the TCK only when required to move the target TAP state or to perform a run-test or scan operation.

While the eTBC is in discrete-control mode, the TCK generator is not used; instead, the state of TCK is toggled on each alternating read and write to the discrete-control register. A falling edge of TCK is produced by write, while a rising edge of TCK is produced by read.

Upon eTBC reset (power up, hardware initiated, or software initiated), the TCK generator assumes its free-running mode with a clock divisor of 16 (TCK = CLKIN/16).

TAP-state generator

The TAP-state generator sources the TMS signal, which sequences the TAP controllers of connected IEEE Std 1149.1-compliant target devices. The TAP controller specified by IEEE Std 1149.1 is a synchronous finite-state machine that provides test control signals throughout each target device; its state diagram is shown in Figure 8. This diagram and the TAP-controller states are discussed subsequently.

The TAP-state generator operates under the control of an executing command to generate the TMS sequences required to move connected target devices from one stable state to another, to capture and scan test data into/out of target devices, and to operate built-in test modes of target devices in the Run-Test/Idle state.

The TAP state currently being generated always is maintained by the TAP-state generator and always is available in the eTBC status register (bits 3−0, TAPST) for host read. Based on the TAP state that is current upon command initiation, the TAP-state generator sources a defined sequence of TMS values to reach the TAP state in which the command is progressed (e.g., Shift-IR, Shift-DR, Run-Test/Idle) and, ultimately, to reach the specified end TAP state. These sequences are detailed in Tables 7−12.

While the eTBC is in free-running-TCK mode, if a currently operating scan command empties or fills a required test data buffer, then the TAP-state generator sources the TMS sequences required to move the connected target devices to their Pause-IR or Pause-DR states. In such case, the TAP-state generator maintains target devices in their Pause-IR or Pause-DR states until the required test-data buffer is serviced appropriately. However, if such a buffer condition occurs while the eTBC is in gated-TCK mode, the TAP-state generator maintains the target devices in their Shift-IR or Shift-DR states while the TCK is gated off.

TAP-state generator (continued)

While the eTBC is in discrete-control mode, the TAP-state generator is not used; instead, the state of the TMS pin is determined by the contents of the discrete-control register. Thus, TMS sequences that cannot be generated automatically still can be applied through the eTBC to targets that require such (e.g., near-compliant devices).

The TAP-state generator also is not used during the operation of the special addressable shadow protocol (ASP) scan commands. Since, by definition, ASPs operate only while the TAP is idling (maintaining one of the TAP states Test-Logic-Reset, Run-Test/Idle, Pause-IR, or Pause-DR), the TMS pin must be maintained at the value it held upon initiation of the ASP scan command.

For eTBC verification/debugging, in addition to continuous update of the current target TAP state in the eTBC status register, the output of the TAP-state (TMS) generator can be selected for loopback into the TDI buffer. When this TMS-loopback mode is selected, although a host-requested command executes in the eTBC, the target is not affected, as both TMS and TDI are fixed at a high level.

Upon eTBC reset (power up, hardware initiated, or software initiated), the TAP-state generator assumes the Test-Logic-Reset TAP state.

Table 7. TMS Sequencing From TAP State Test-Logic-Reset

FROM TEST-LOGIC-RESET (TMS = H) TO:											
TEST-LOGIC-RESET		RUN-TEST/IDLE		SHIFT-DR		PAUSE-DR		SHIFT-IR		PAUSE-IR	
NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE
H	T-L-R	L	R-T/I	L	R-T/I	L	R-T/I	L	R-T/I	L	R-T/I
				H	S-DR-S	H	S-DR-S	H	S-DR-S	H	S-DR-S
				L	Capture-DR	L	Capture-DR	H	S-IR-S	H	S-IR-S
				L	Shift-DR	H	Exit1-DR	L	Capture-IR	L	Capture-IR
						L	Pause-DR	L	Shift-IR	H	Exit1-IR
										L	Pause-IR

Table 8. TMS Sequencing From TAP State Run-Test/Idle

FROM RUN-TEST/IDLE (TMS = L) TO:											
TEST-LOGIC-RESET		RUN-TEST/IDLE		SHIFT-DR		PAUSE-DR		SHIFT-IR		PAUSE-IR	
NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE
H	S-DR-S	L	R-T/I	H	S-DR-S	H	S-DR-S	H	S-DR-S	H	S-DR-S
H	S-IR-S			L	Capture-DR	L	Capture-DR	H	S-IR-S	H	S-IR-S
H	T-L-R			L	Shift-DR	H	Exit1-DR	L	Capture-IR	L	Capture-IR
						L	Pause-DR	L	Shift-IR	H	Exit1-IR
										L	Pause-IR

Table 9. TMS Sequencing From TAP State Pause-DR

FROM PAUSE-DR (TMS = L) TO:											
TEST-LOGIC-RESET		RUN-TEST/IDLE		SHIFT-DR		PAUSE-DR		SHIFT-IR		PAUSE-IR	
NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE
H	Exit2-DR	H	Exit2-DR	H	Exit2-DR	H	Exit2-DR	H	Exit2-DR	H	Exit2-DR
H	Update-DR	H	Update-DR	L	Shift-DR	H	Update-DR	H	Update-DR	H	Update-DR
H	S-DR-S	L	R-T/I			H	S-DR-S	H	S-DR-S	H	S-DR-S
H	S-IR-S					L	Capture-DR	H	S-IR-S	H	S-IR-S
H	T-L-R					H	Exit1-DR	L	Capture-IR	L	Capture-IR
						L	Pause-DR	L	Shift-IR	H	Exit1-IR
										L	Pause-IR

Table 10. TMS Sequencing From TAP State Pause-IR

FROM PAUSE-IR (TMS = L) TO:											
TEST-LOGIC-RESET		RUN-TEST/IDLE		SHIFT-DR		PAUSE-DR		SHIFT-IR		PAUSE-IR	
NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE
H	Exit2-IR	H	Exit2-IR	H	Exit2-IR	H	Exit2-IR	H	Exit2-IR	H	Exit2-IR
H	Update-IR	H	Update-IR	H	Update-IR	H	Update-IR	L	Shift-IR	H	Update-IR
H	S-DR-S	L	R-T/I	H	S-DR-S	H	S-DR-S			H	S-DR-S
H	S-IR-S			L	Capture-DR	L	Capture-DR			H	S-IR-S
H	T-L-R			L	Shift-DR	H	Exit1-DR			L	Capture-IR
						L	Pause-DR			H	Exit1-IR
										L	Pause-IR

Table 11. TMS Sequencing From TAP State Shift-DR

FROM SHIFT-DR (TMS = L) TO:							
TEST-LOGIC-RESET		RUN-TEST/IDLE		PAUSE-DR		PAUSE-IR	
NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE
H	Exit1-DR	H	Exit1-DR	H	Exit1-DR	H	Exit1-DR
H	Update-DR	H	Update-DR	L	Pause-DR	H	Update-DR
H	S-DR-S	L	R-T/I			H	S-DR-S
H	S-IR-S					H	S-IR-S
H	T-L-R					L	Capture-IR
						H	Exit1-IR
						L	Pause-IR

Table 12. TMS Sequencing From TAP State Shift-IR

FROM SHIFT-IR (TMS = L) TO:							
TEST-LOGIC-RESET		RUN-TEST/IDLE		PAUSE-DR		PAUSE-IR	
NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE
H	Exit1-IR	H	Exit1-IR	H	Exit1-IR	H	Exit1-IR
H	Update-IR	H	Update-IR	H	Update-IR	L	Pause-IR
H	S-DR-S	L	R-T/I	H	S-DR-S		
H	S-IR-S			L	Capture-DR		
H	T-L-R			H	Exit1-DR		
				L	Pause-DR		

state diagram description

The state diagram shown in Figure 8 is in accordance with IEEE Std 1149.1-1990. The TAP controller proceeds through its states, based on the level of TMS at the rising edge of TCK.

As shown, the TAP controller consists of 16 states. There are six stable states (indicated by a looping arrow in the state diagram) and ten unstable states. A stable state is a state the TAP controller can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths though the state diagram: one to access and control the selected data register and one to access and control the instruction register. Only one register can be accessed at any given time.

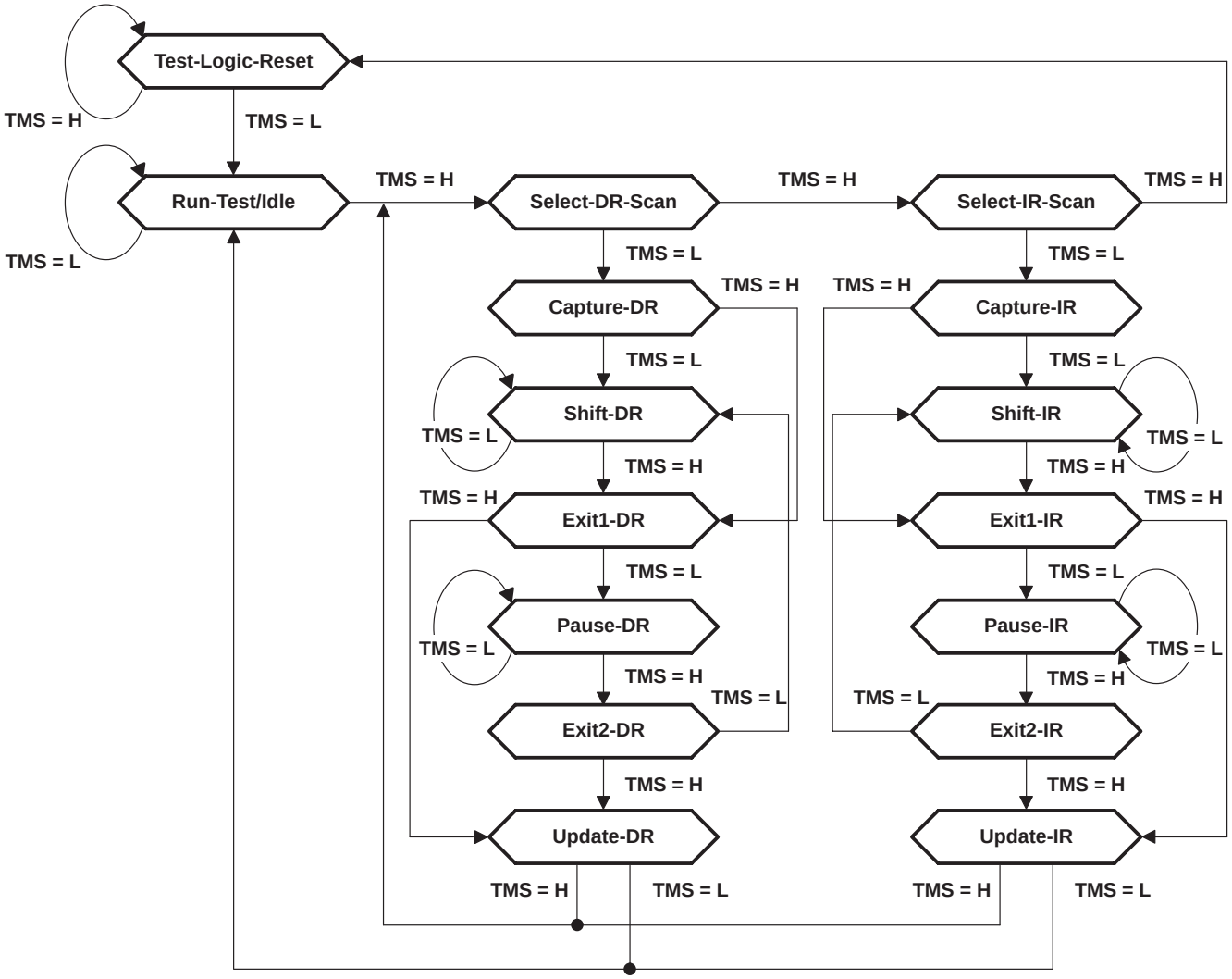


Figure 8. TAP-Controller State Diagram

Test-Logic-Reset

The eTBC TAP-state generator powers up in the Test-Logic-Reset state. Alternatively, the eTBC can be forced to this state asynchronously by assertion of its $\overline{\text{RST}}$ input or synchronously by writing the eTBC command register (bit 7, SWRST).

For a target device in the stable Test-Logic-Reset state, the test logic is reset and is disabled so that the normal logic function of the device is performed. The instruction register is reset to an opcode that selects the optional IDCODE instruction, if supported, or the BYPASS instruction. Certain data registers also can be reset to their power-up values.

Run-Test/Idle

For a target device, Run-Test/Idle is a stable state in which the test logic can be actively running a test or can be idle.

Select-DR-Scan, Select-IR-Scan

For a target device, no specific function is performed in the Select-DR-Scan and Select-IR-Scan states, and the TAP controller exits either of these states on the next TCK cycle. These states allow the selection of either data-register scan or instruction-register scan.

Capture-DR

For a target device in the Capture-DR state, the selected data register can capture a data value as specified by the current instruction. Such capture operations occur on the rising edge of TCK, upon which the Capture-DR state is exited.

Shift-DR

For a target device, upon entry to the Shift-DR state, the selected data register is placed in the scan path between TDI and TDO, and on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO outputs the logic level present in the least-significant bit of the selected data register. While in the stable Shift-DR state, data is shifted serially through the selected data register on each TCK cycle.

Exit1-DR, Exit2-DR

For a target device, the Exit1-DR and Exit2-DR states are temporary states that end a data-register scan. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register. On the first falling edge of TCK after entry to Exit1-DR, TDO goes from the active state to the high-impedance state.

Pause-DR

For a target device, no specific function is performed in the stable Pause-DR state. The Pause-DR state suspends and resumes data-register scan operations without loss of data.

Update-DR

For a target device, if the current instruction calls for the selected data register to be updated with current data, such update occurs on the falling edge of TCK, following entry to the Update-DR state.

Capture-IR

For a target device in the Capture-IR state, the instruction register captures its current status value. This capture operation occurs on the rising edge of TCK, upon which the Capture-IR state is exited.

Shift-IR

For a target device, upon entry to the Shift-IR state, the instruction register is placed in the scan path between TDI and TDO, and on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO outputs the logic level present in the least-significant bit of the instruction register. While in the stable Shift-IR state, instruction data is shifted serially through the instruction register on each TCK cycle.

Exit1-IR, Exit2-IR

For a target device, the Exit1-IR and Exit2-IR states are temporary states that end an instruction-register scan. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register. On the first falling edge of TCK after entry to Exit1-IR, TDO goes from the active state to the high-impedance state.

Pause-IR

For a target device, no specific function is performed in the stable Pause-IR state, in which the TAP controller can remain indefinitely. The Pause-IR state suspends and resumes instruction-register scan operations without loss of data.

Update-IR

For a target device, the current instruction is updated and takes effect on the falling edge of TCK, following entry to the Update-IR state.

TDO buffer

The TDO buffer is the 4×8-bit-parallel-to-serial FIFO that accepts scan data from the host in 8-bit-parallel format and serializes it onto the TDO pin during scan operations. Scan data is expected to be transferred from the host in least-significant-byte-first order to meet IEEE Std 1149.1 requirements for LSB-first scan order. Any partial byte to be written should be justified to D0. The TDO buffer is cleared upon command initiation, so no scan data should be written to the TDO buffer before writing a scan command to the command register.

The TDO-buffer status (not full/full) is maintained in the status register (bit 6, TDOS). When the TDO-buffer status is full, writes to the TDO buffer is held off by RDY inactive and, if the write cycle is aborted prior to RDY active, the write data is ignored.

For the convenience and efficiency of operating scans to the target for which outgoing data is not required, the eTBC supports special classes of input-only and recirculate scan commands that do not require nor operate the TDO buffer, so the host need not perform any write access to it. While the input-only scan commands are operating, the TDO pin outputs a fixed high level. While the recirculate scan commands are operating, the TDO pin recirculates to the target the data that is received at TDI.

While the eTBC is in discrete-control mode, the TDO buffer is not used; instead, the state of the TDO pin is determined by the contents of the discrete-control register. Thus, TMS/TDO sequences that cannot be generated automatically still can be applied through the eTBC to targets that require such (e.g., near-compliant devices).

For eTBC verification/debugging, the TDO-buffer output can be selected for loopback into the TDI buffer. When this TDO-loopback mode is selected, although a host-requested command executes in the eTBC, the target is not affected, as both TMS and TDI are fixed at a high level.

Upon eTBC reset (power up, hardware initiated, or software initiated), the TDO buffer is cleared and assumes its not-full state.

TDI buffer

The TDI buffer is the serial to 4 × 8-bit-parallel FIFO that serially receives data at the TDI pin and makes it available in 8-bit-parallel format for reading by the host. Scan data is expected to be transferred from the IEEE Std 1149.1 targets in LSB-first order and is made available for host read in least-significant-byte-first order. The last data available for host read during a scan command may be a partial byte, in which case it is justified to D0.

The TDI-buffer status (empty/not empty) is maintained in the status register (bit 7, TDIS). When the TDI-buffer status is empty, reads to the TDI buffer are held off by RDY inactive and, if the read cycle is aborted prior to RDY active, the read data is invalid.

The TDI buffer automatically is able to accommodate retiming (pipeline) delays to the target. While operating a scan command, TDI sampling is delayed by a number of TCK cycles, equal to a value given in the configurationB register (bits 3−0, RDLY), following the generation of Shift-DR or Shift-IR state, as appropriate.

For the convenience and efficiency of operating scans to the target, for which incoming data is not required, the eTBC supports a special class of output-only scan commands that neither require nor operate the TDI buffer. While the output-only scan commands are operating, the data received at TDI is ignored and the host need not perform any read access to the TDI buffer.

While the eTBC is in discrete-control mode, the TDI buffer is not used; instead, the state of the TDO pin is observed in the discrete-control register. Thus, TMS/TDO sequences that cannot be generated automatically still can be applied through the eTBC to targets that require such (e.g., near-compliant devices).

For eTBC verification/debugging, the input to the TDI buffer can be selected for loopback from either TDO buffer or TAP-state (TMS) generator. When either of these loopback modes is selected, although a host-requested command executes in the eTBC, the target is not affected, as both TMS and TDI are fixed at a high level.

Upon eTBC reset (power up, hardware initiated, or software initiated), the TDI buffer is cleared and assumes its empty state.

discrete control

The discrete-control block provides the multiplexing and control logic required to support the eTBC discrete-control mode in addition to its automatic modes. While the eTBC is in discrete-control mode, the TAP signals are fully controllable/accessible to the host via reads/writes to the discrete-control register. No commands can be initiated/operated while the eTBC is in the discrete-control mode.

Upon eTBC reset (power up, hardware initiated, or software initiated), the discrete-control mode is inactive.

reset

The eTBC provides three mechanisms for comprehensive and equivalent reset: power-up reset, hardware-initiated reset ($\overline{RST}$), and software-initiated reset (SWRST, bit 7 of command register) to the following effect:

- All eTBC registers are reset to default values as given in Table 1.
- The command/control logic is fully reset.
- The counter is cleared/unloaded. The TDO buffer and TDI buffer are cleared/emptied.
- The TAP-state generator is reset to the Test-Logic-Reset TAP state.
- TDO, TMS, and $\overline{TRST}$ output high levels; TCK outputs CLKIN/16.

As a consequence, the IEEE Std 1149.1 targets can be expected to be driven synchronously to the Test-Logic-Reset state no later than the fifth rising edge of TCK (72 CLKIN cycles).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) . . . . . −0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O
(see Note 1): D, RDY . . . . . −0.5 V to V_{CC} + 0.5 V
TCK, TDO, TMS, $\overline{TRST}$ . . . . . −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT8980A (D, RDY) . . . . . 12 mA
SN54LVT8980A (TCK, TDO, TMS, $\overline{TRST}$) . . . . . 96 mA
SN74LVT8980A (D, RDY) . . . . . 12 mA
SN74LVT8980A (TCK, TDO, TMS, $\overline{TRST}$) . . . . . 128 mA
Current into any output in the high state, I_O
(see Note 2): SN54LVT8980A (D, RDY) . . . . . 16 mA
SN54LVT8980A (TCK, TDO, TMS, $\overline{TRST}$) . . . . . 48 mA
SN74LVT8980A (D, RDY) . . . . . 16 mA
SN74LVT8980A (TCK, TDO, TMS, $\overline{TRST}$) . . . . . 64 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . −50 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . −50 mA
Output clamp current, I_{OK} (V_O > V_{CC}): D, RDY . . . . . 50 mA
Package thermal impedance, θ_{JA} (see Note 3) DW package (low K): . . . . . 81°C/W
(high K): . . . . . 46°C/W
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This current flows only when the output is in the high state and V_O > V_{CC}.
3. The package thermal impedance is calculated in accordance with JESD 51 for low K, and JESD 51-7 for high K.

recommended operating conditions (see Note 4)

			SN54LVT8980A		SN74LVT8980A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current	D, RDY		−8		−8	mA
		TCK, TDO, TMS, $\overline{TRST}$		−24		−32	
I_{OL}	Low-level output current	D, RDY		6		6	mA
		TCK, TDO, TMS, $\overline{TRST}$		48		64	
$\Delta t/\Delta v$	Input transition rise or fall rate			10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200		μs/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: Unused control inputs (A, CLKIN, R/$\overline{W}$) must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54LVT8980A			SN74LVT8980A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 2.7 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	D, RDY	V_{CC} = MIN to MAX‡,	I_{OH} = −100 µA	V_{CC}−0.2			V_{CC}−0.2			V
		V_{CC} = 2.7 V,	I_{OH} = −4 mA	2.3			2.3			
		V_{CC} = 3 V	I_{OH} = −4 mA	2.6			2.6			
			I_{OH} = − 8 mA	2.4			2.4			
	TCK, TDO, TMS, TRST	V_{CC} = MIN to MAX‡,	I_{OH} = −100 µA	V_{CC}−0.2			V_{CC}−0.2			
		V_{CC} = 2.7 V,	I_{OH} = −8 mA	2.4			2.4			
		V_{CC} = 3 V	I_{OH} = −24 mA	2						
			I_{OH} = −32 mA				2			
V_{OL}	D, RDY	V_{CC} = MIN to MAX‡,	I_{OL} = 100 µA			0.2			0.2	V
		V_{CC} = 2.7 V	I_{OL} = 4 mA			0.55			0.55	
			I_{OL} = 6 mA			0.8			0.8	
		V_{CC} = 3 V	I_{OL} = 4 mA			0.55			0.55	
			I_{OL} = 6 mA			0.8			0.8	
	TCK, TDO, TMS, TRST	V_{CC} = MIN to MAX‡,	I_{OL} = 100 µA			0.2			0.2	
		V_{CC} = 2.7 V,	I_{OL} = 24 mA			0.5			0.5	
		V_{CC} = 3 V	I_{OL} = 16 mA			0.4			0.4	
			I_{OL} = 32 mA			0.5			0.5	
			I_{OL} = 48 mA			0.55				
			I_{OL} = 64 mA						0.55	
I_I	A, CLKIN, RST, R/W, STRB, TDI, TOE	V_{CC} = 0 or MAX‡,	V_I = 5.5 V			10			10	µA
	A, CLKIN, R/W, D, RDY	V_{CC} = 3.6 V,	V_I = V_{CC} or GND			±1			±1	
	RST, STRB, TDI, TOE	V_{CC} = 3.6 V	V_I = V_{CC}			1			1	
			V_I = 0			−100			−100	
I_{off}	TCK, TDO, TMS, TRST	V_{CC} = 0, V_I or V_O = 0 to 4.5 V				±100			±100	µA
I_{OZH}	D, TCK, TDO, TMS, TRST	V_{CC} = 3.6 V,	V_O = 3 V			5			5	µA
I_{OZL}	D, TCK, TDO, TMS, TRST	V_{CC} = 3.6 V,	V_O = 0.5 V			−5			−5	µA
I_{OZPU}§	TCK, TDO, TMS, TRST	V_{CC} = 0 to 1.5 V, V_O = 0.5 V to 3 V, TOE = 0				±100			±100	µA
I_{OZPD}§	TCK, TDO, TMS, TRST	V_{CC} = 1.5 V to 0, V_O = 0.5 V to 3 V, TOE = 0				±100			±100	µA

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ This parameter is characterized, but not tested.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	SN54LVT8980A			SN74LVT8980A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
I_{CC}	Outputs high	V_{CC} = 3.6 V, I_O = 0, V_I = V_{CC} or GND			0.5			0.5	mA
	Outputs low				7			7	
	Outputs disabled				0.5			0.5	
ΔI_{CC}¶		V_{CC} = 3 V to 3.6 V, One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND			0.2			0.2	mA
C_i		V_I = 3 V or 0		4			4		pF
C_{io}		V_O = 3 V or 0		5			5		pF
C_o		V_O = 3 V or 0		7			7		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 9 and 10)

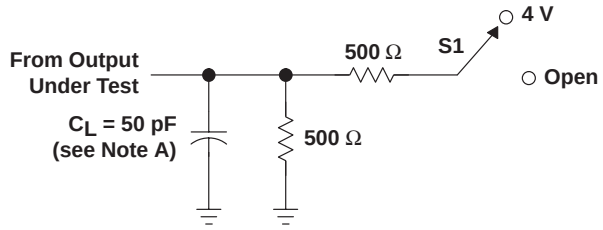
				SN54LVT8980A				SN74LVT8980A				UNIT
				V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 ± 0.3 V		V_{CC} = 2.7 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency, CLKIN		TCK = CLKIN (CDIV = 0)	0	20	0	16	0	20	0	16	MHz
			TCK = CLKIN/2 (CDIV = 1)	0	40	0	32	0	40	0	32	
			TCK ≤ CLKIN/4 (CDIV ≥ 2)	0	70	0	64	0	70	0	64	
t_w	Pulse duration	CLKIN high or low	TCK = CLKIN (CDIV = 0)	25		31		25		31		ns
			TCK = CLKIN/2 (CDIV = 1)	12.5		15.6		12.5		15.6		
			TCK ≤ CLKIN/4 (CDIV ≥ 2)	7.1		7.8		7.1		7.8		
		$\overline{RST}$ low		10		10		10		10		
		$\overline{STRB}$ low		8		8		8		8		
t_{su}	Setup time	A before $\overline{STRB}$↓	Read or write (R/$\overline{W}$ high or low)	10		10		10		10		ns
		D before $\overline{STRB}$↑	Write (R/$\overline{W}$ low)	5		5		5		5		
		R/$\overline{W}$ before $\overline{STRB}$↓		5		5		5		5		
		TDI before CLKIN↑		5		5		5		5		
t_h	Hold time	A after $\overline{STRB}$↑	Read or write (R/$\overline{W}$ high or low)	5		5		5		5		ns
		D after $\overline{STRB}$↑	Write (R/$\overline{W}$ low)	15		15		15		15		
		R/$\overline{W}$ after $\overline{STRB}$↑		6		6		6		6		
		TDI after CLKIN↑		10		10		10		10		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 9 and 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT8980A				SN74LVT8980A					UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN	MAX	
t_{PLH}	CLKIN	TCK	6	20		25	6	10	17		20	ns
t_{PHL}			6	20		25	6	10	17		20	
t_{PLH}	CLKIN	TDO, TMS	8	35		40	8	18	30		35	ns
t_{PHL}			8	35		40	8	18	30		35	
t_{PLH}	$\overline{RST}$↓	D	3	35		40	3	17	30		35	ns
t_{PHL}			3	35		40	3	17	30		35	
t_{PLH}	$\overline{RST}$↓	RDY	3	35		40	3	17	30		35	ns
t_{PHL}			3	35		40	3	17	30		35	
t_{PLH}	$\overline{RST}$↓	TDO, TMS, $\overline{TRST}$	5	30		35	5	15	25		30	ns
t_{PHL}		TCK	5	30		35	5	15	25		30	
t_{PLH}	$\overline{STRB}$↑	RDY	3	22		28	3	10	18		22	ns
t_{PHL}	$\overline{STRB}$↓		3	22		28	3	10	18		22	
t_{PLH}	$\overline{STRB}$↑	TCK, TDO, TMS, $\overline{TRST}$ discrete mode	3	28		35	3	14	22		28	ns
t_{PHL}			3	28		35	3	14	22		28	
t_{PLH}	$\overline{STRB}$↑	TCK, TDO, TMS, $\overline{TRST}$ other modes	6	40		45	6	20	35		40	ns
t_{PHL}			6	40		45	6	20	35		40	
t_{PZH}	$\overline{STRB}$↓	D	3	20		25	3	8	15		18	ns
t_{PZL}			3	20		25	3	8	15		18	
t_{PZH}	$\overline{STRB}$↑	TCK, TDO, TMS, $\overline{TRST}$	5	30		35	5	15	25		30	ns
t_{PZL}			5	30		35	5	15	25		30	
t_{PZH}	$\overline{TOE}$↓	TCK, TDO, TMS, $\overline{TRST}$	2	15		18	2	6	12		15	ns
t_{PZL}			2	15		18	2	6	12		15	
t_{PHZ}	$\overline{STRB}$↑	D	3	20		25	3	8	15		18	ns
t_{PLZ}			3	20		25	3	8	15		18	
t_{PHZ}	$\overline{STRB}$↑	TCK, TDO, TMS, $\overline{TRST}$	5	30		35	5	15	25		30	ns
t_{PLZ}			5	30		35	5	15	25		30	
t_{PHZ}	$\overline{TOE}$↑	TCK, TDO, TMS, $\overline{TRST}$	2	15		18	2	6	12		15	ns
t_{PLZ}			2	15		18	2	6	12		15	

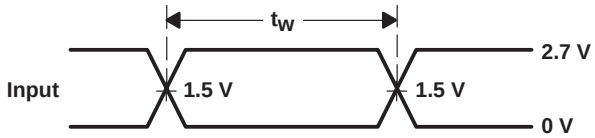
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

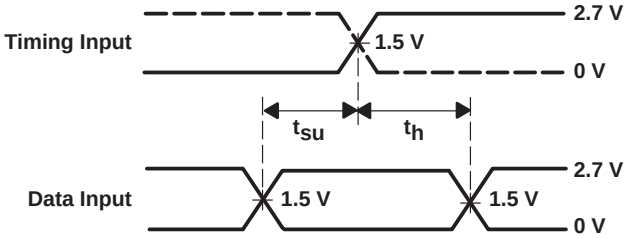


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	4 V
t_{PHZ}/t_{PZH}	GND

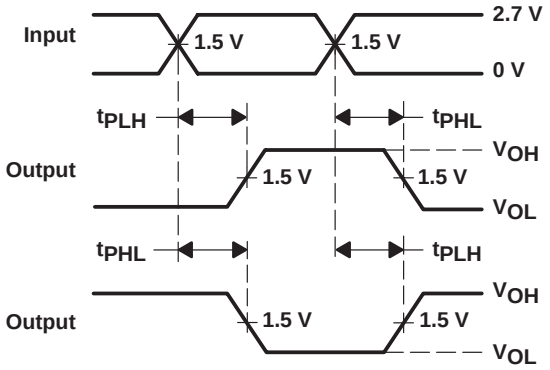
LOAD CIRCUIT



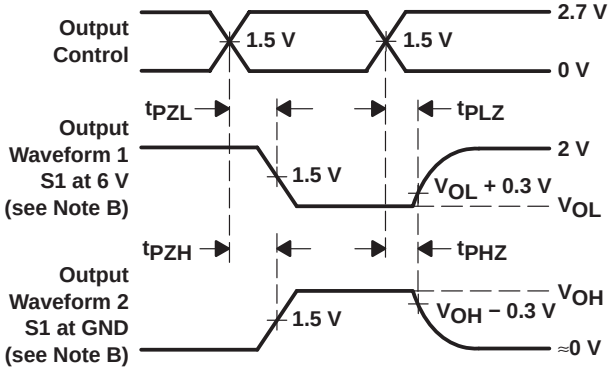
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

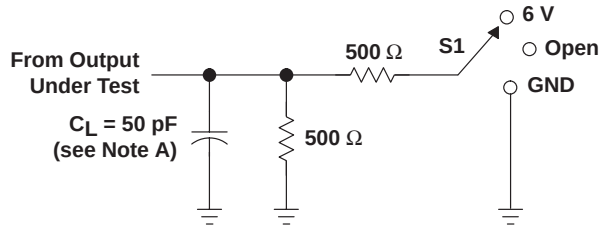


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.

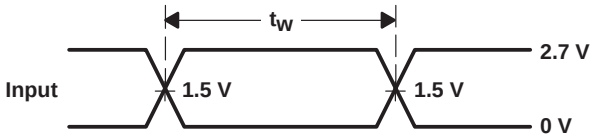
Figure 9. Load Circuit and Voltage Waveforms (D and RDY Outputs)

PARAMETER MEASUREMENT INFORMATION

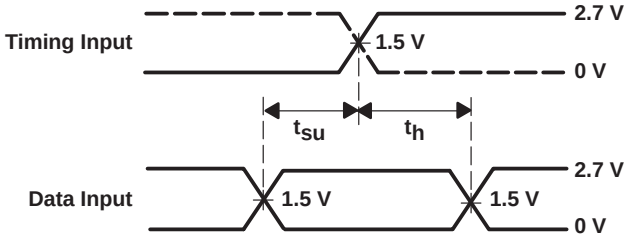


LOAD CIRCUIT

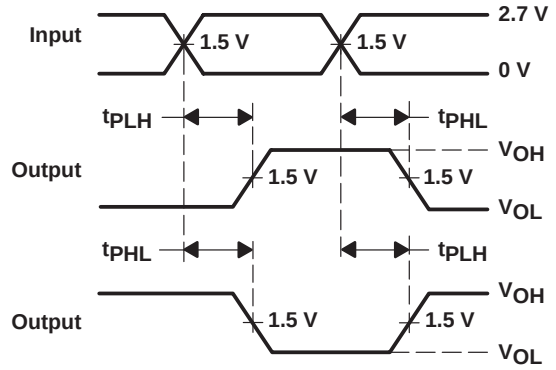
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



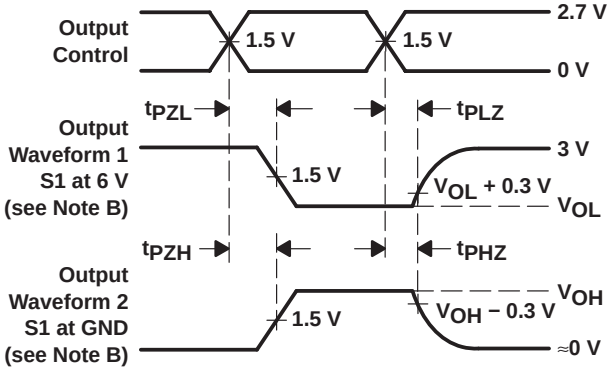
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.

Figure 10. Load Circuit and Voltage Waveforms (TCK, TDO, TMS, $\overline{\text{TRST}}$ Outputs)

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVT8980ADW	Active	Production	SOIC (DW) | 24	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT8980A
SN74LVT8980ADWR	Active	Production	SOIC (DW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT8980A
SN74LVT8980ADWRG4	Active	Production	SOIC (DW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT8980A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF SN74LVT8980A :

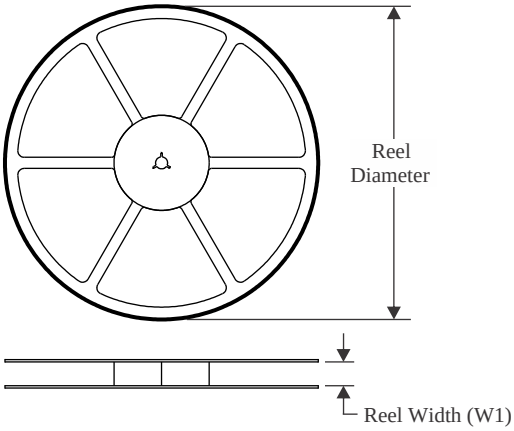
- Enhanced Product : SN74LVT8980A-EP

NOTE: Qualified Version Definitions:

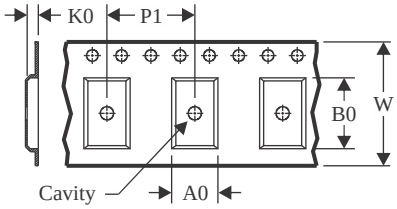
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

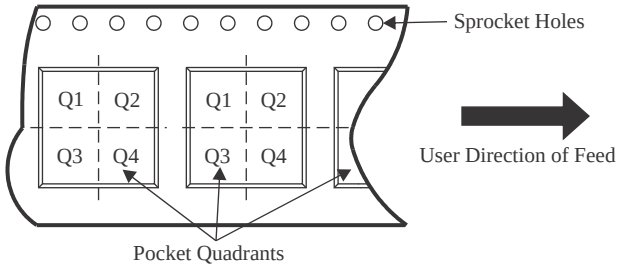


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

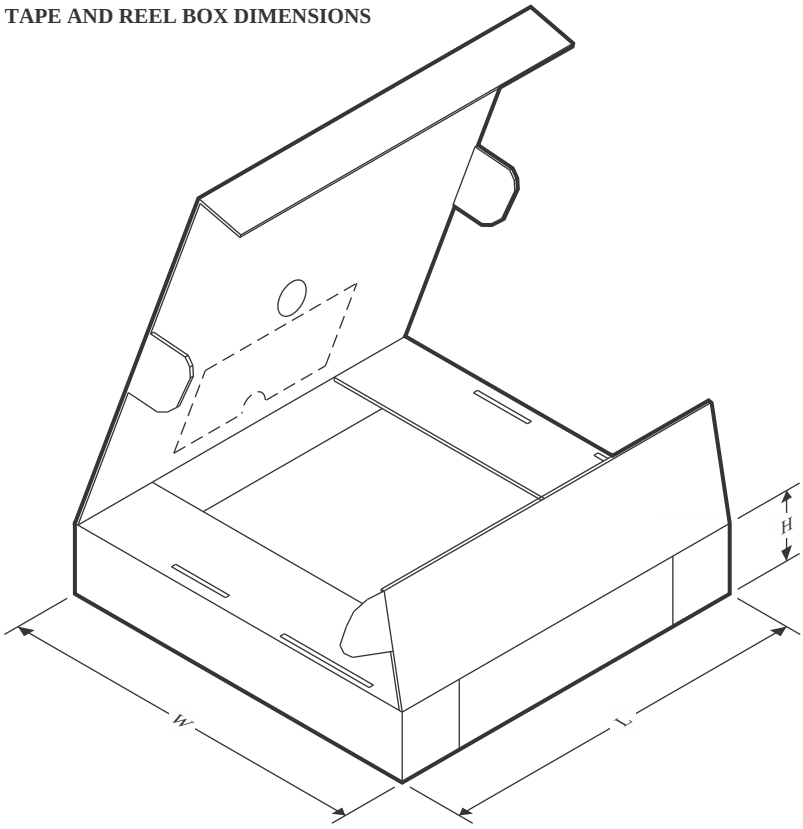
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVT8980ADWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74LVT8980ADWRG4	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

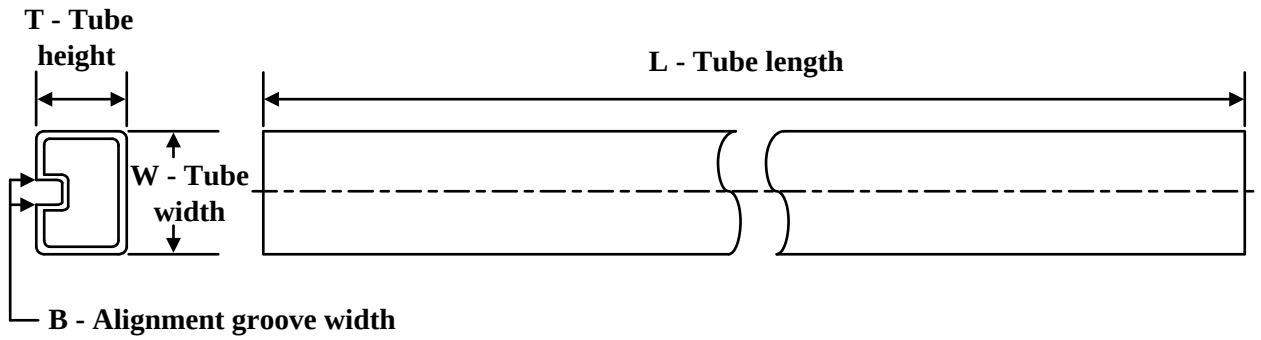
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVT8980ADWR	SOIC	DW	24	2000	350.0	350.0	43.0
SN74LVT8980ADWRG4	SOIC	DW	24	2000	350.0	350.0	43.0

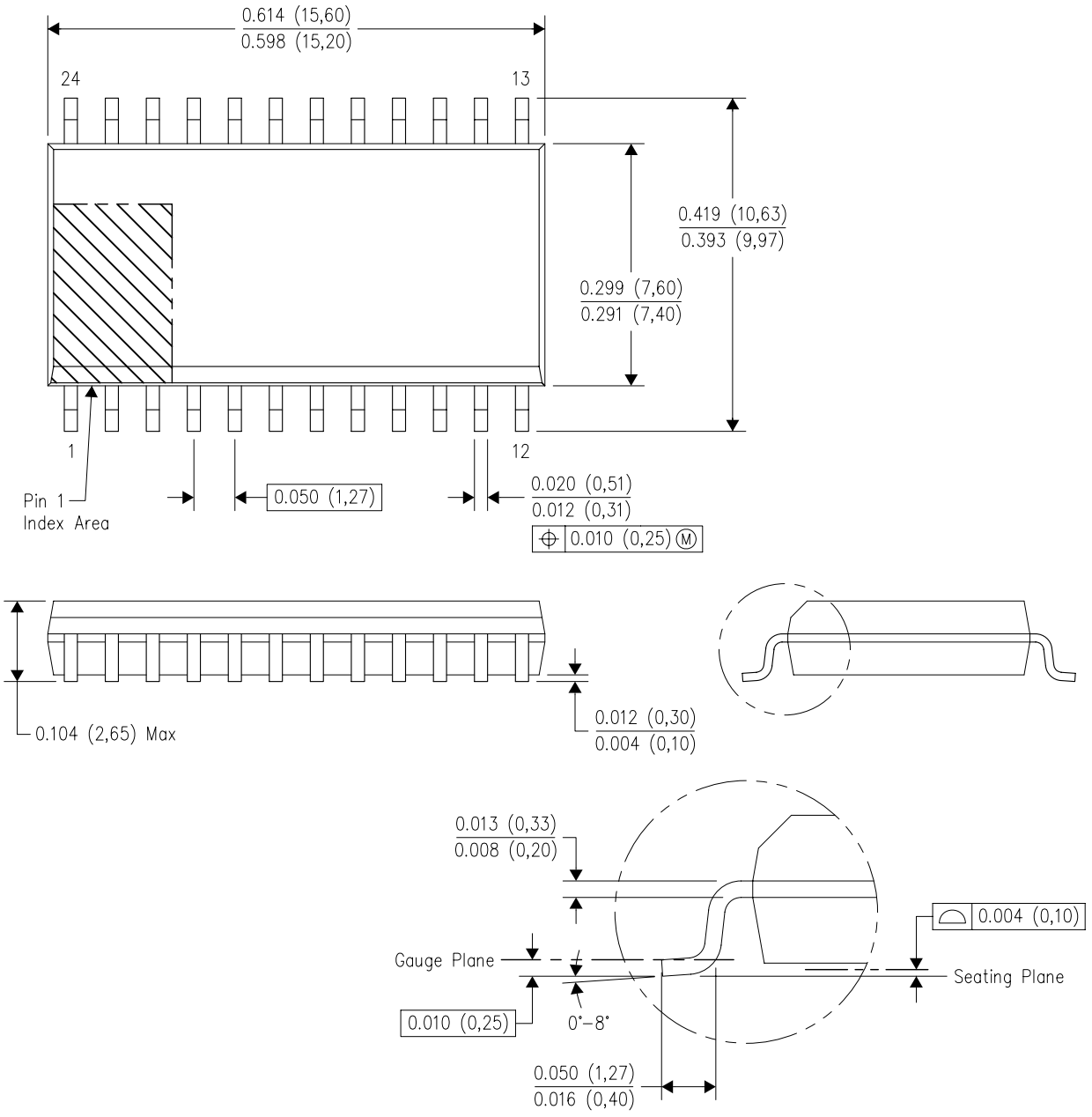
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74LVT8980ADW	DW	SOIC	24	25	506.98	12.7	4826	6.6

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

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Last updated 10/2025