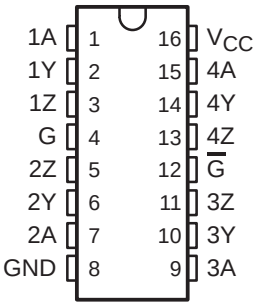
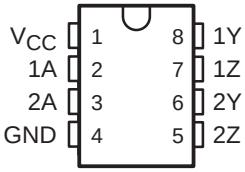
- **Meets or Exceeds the Requirements of ANSI TIA/EIA-644 Standard**
- **Low-Voltage Differential Signaling With Typical Output Voltage of 350 mV and a 100-Ω Load**
- **Signaling Rates up to 155 Mbps**
- **Operates From a Single 3.3-V Supply**
- **Driver at High Impedance When Disabled or With V_{CC} = 0**
- **Low-Voltage TTL (LVTTL) Logic Input Levels**
- **Characterized For Operation From 0°C to 70°C**

SN75LVDS31D (Marked as **75LVDS31**)
SN75LVDS31PW (Marked as **DS31**)
(TOP VIEW)



SN75LVDS9638D (Marked as **DF638** or **7L9638**)
SN75LVDS9638DGK (Marked as **AXK)**
(TOP VIEW)



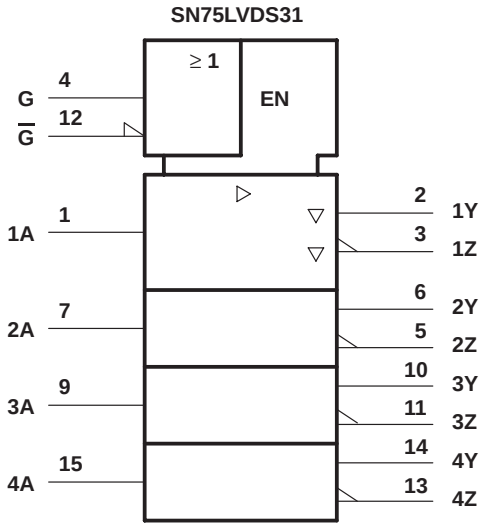
description

The SN75LVDS31 and SN75LVDS9638 are differential line drivers that implement the electrical characteristics of low-voltage differential signaling (LVDS). This signaling technique lowers the output voltage levels of 5-V differential standard levels (such as TIA/EIA-422B) to reduce the power, increase the switching speeds, and allow operation with a 3.3-V supply rail. Any of the four current-mode drivers will deliver a minimum differential output voltage magnitude of 247 mV into a 100-Ω load when enabled.

The intended application of these devices and signaling technique is for point-to-point baseband data transmission over controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

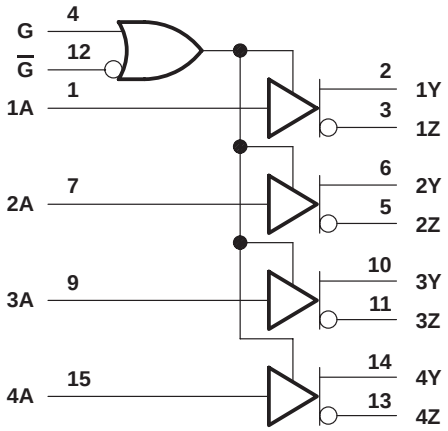
The SN75LVDS31 and SN75LVDS9638 are characterized for operation from 0°C to 70°C.

logic symbol†

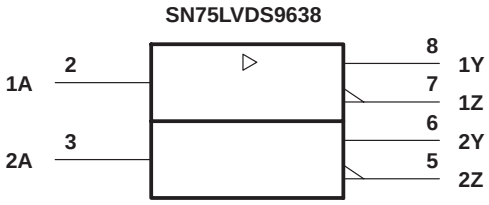


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

’LVDS31 logic diagram (positive logic)

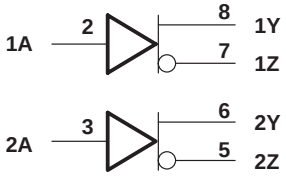


logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

’LVDS9638 logic diagram (positive logic)



Function Tables

SN75LVDS31

INPUT A	ENABLES		OUTPUTS	
	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z
Open	H	X	L	H
Open	X	L	L	H

H = high level, L = low level, X = irrelevant,
Z = high impedance (off)

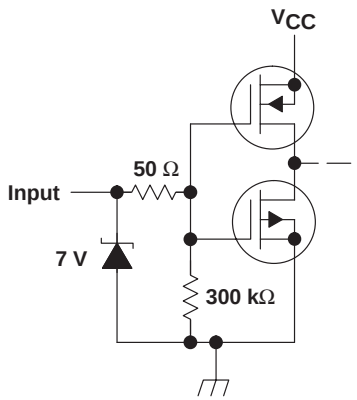
SN75LVDS9638

INPUT A	OUTPUTS	
	Y	Z
H	H	L
L	L	H
OPEN	L	H

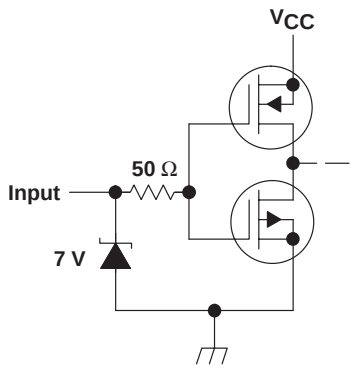
H = high level, L = low level

equivalent input and output schematic diagrams

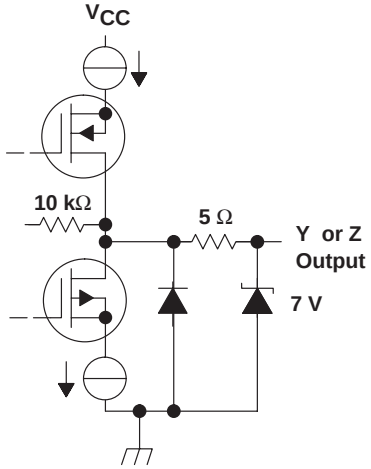
EQUIVALENT OF EACH A INPUT



EQUIVALENT OF G, $\overline{G}$ INPUTS



TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.5 V to 4 V
Input voltage range: Inputs . . . . . –0.5 V to V_{CC} + 0.5 V
Y or Z . . . . . –0.5 V to 4 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages, except differential I/O bus voltages, are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR‡ ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D (8)	725 mW	5.8 mW/°C	464 mW
D (16)	950 mW	7.6 mW/°C	608 mW
PW	774 mW	6.2 mW/°C	496 mW
DGK	425 mW	3.4 mW/°C	272 mW

‡ This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	3	3.3	3.6	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		SN75LVDS31, SN75LVDS9638			UNIT
					MIN	TYP†	MAX	
V_{OD}	Differential output voltage magnitude		R_L = 100 Ω,	See Figure 2	247	340	454	mV
ΔV_{OD}	Change in differential output voltage magnitude between logic states		R_L = 100 Ω,	See Figure 2	–50		50	mV
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states		See Figure 3		1.125	1.2	1.375	V
$V_{OC(SS)}$	Steady-state common-mode output voltage		See Figure 3		–50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage		See Figure 3			50	150	mV
I_{CC}	Supply current	SN75LVDS31	V_I = 0.8 V or 2 V, No load	Enabled,		9	20	mA
			V_I = 0.8 or 2 V, Enabled	R_L = 100 Ω,		25	35	mA
			V_I = 0 or V_{CC},	Disabled		0.25	1	mA
		SN75LVDS9638	V_I = 0.8 V or 2 V	No load		4.7	8	mA
				R_L = 100 Ω		9	13	mA
I_{IH}	High-level input current		V_{IH} = 2			4	20	μA
I_{IL}	Low-level input current		V_{IL} = 0.8 V			0.1	10	μA
I_{OS}	Short-circuit output current		$V_{O(Y)}$ or $V_{O(Z)}$ = 0			–4	–24	mA
			V_{OD} = 0				±12	mA
I_{OZ}	High-impedance output current		V_O = 0 or 2.4 V				±1	μA
$I_{O(OFF)}$	Power-off output current		V_{CC} = 0,	V_O = 2.4 V			±1	μA
C_I	Input capacitance					3		pF

† All typical values are at T_A = 25°C and with V_{CC} = 3.3 V.

switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN75LVDS31, SN75LVDS9638			UNIT
				MIN	TYP†	MAX	
t_{pLH}	Propagation delay time, low-to-high-level output	R_L = 100 Ω, See Figure 2	C_L = 10 pF,			6	ns
t_{pHL}	Propagation delay time, high-to-low-level output	R_L = 100 Ω, See Figure 2	C_L = 10 pF,			6	ns
t_r	Differential output signal rise time (20% to 80%)	R_L = 100 Ω, See Figure 2	C_L = 10 pF,		0.5	1.2	ns
t_f	Differential output signal fall time (80% to 20%)	R_L = 100 Ω, See Figure 2	C_L = 10 pF,		0.5	1.2	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)‡	R_L = 100 Ω, See Figure 2	C_L = 10 pF,			0.6	ns
$t_{sk(o)}$	Channel-to-channel output skew§	R_L = 100 Ω, See Figure 2	C_L = 10 pF,			0.6	ns
$t_{sk(pp)}$	Part-to-part skew¶	R_L = 100 Ω, See Figure 2	C_L = 10 pF,			1	ps
t_{pZH}	Propagation delay time, high-impedance-to-high-level output	See Figure 4				25	ns
t_{pZL}	Propagation delay time, high-impedance-to-low-level output	See Figure 4				25	ns
t_{pHZ}	Propagation delay time, high-level-to-high-impedance output	See Figure 4				25	ns
t_{pLZ}	Propagation delay time, low-level-to-high-impedance output	See Figure 4				25	ns

† All typical values are at T_A = 25°C and with V_{CC} = 3.3 V.
‡ $t_{sk(p)}$ is the magnitude of the time difference between the high-to-low and low-to-high propagation delay times at an output.
§ $t_{sk(o)}$ is the magnitude of the time difference between the outputs of a single device with all of their inputs connected together.
¶ $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, same temperature, and have identical packages and test circuits.

PARAMETER MEASUREMENT INFORMATION

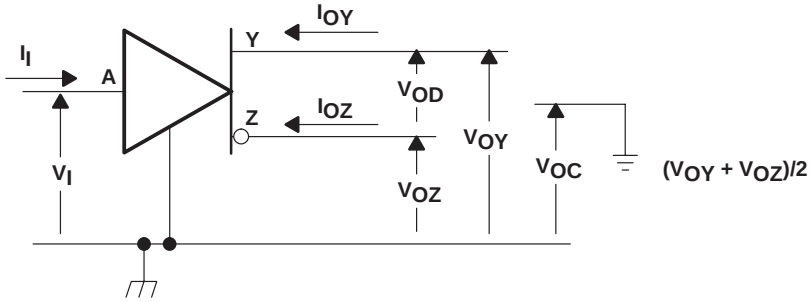
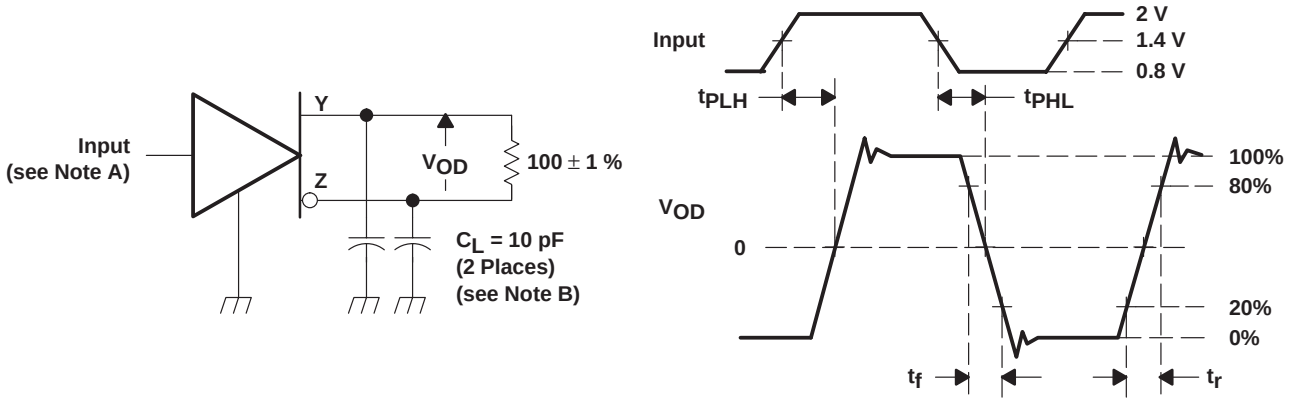
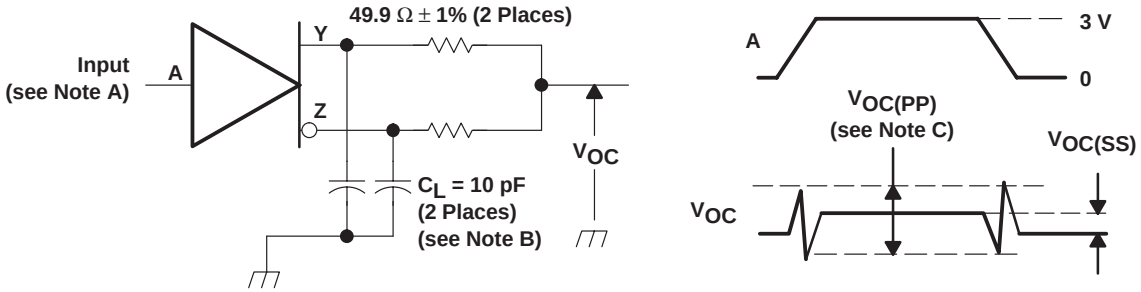


Figure 1. Voltage and Current Definitions



NOTES: A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns.
B. C_L includes instrumentation and fixture capacitance within 6 mm of the D.U.T.

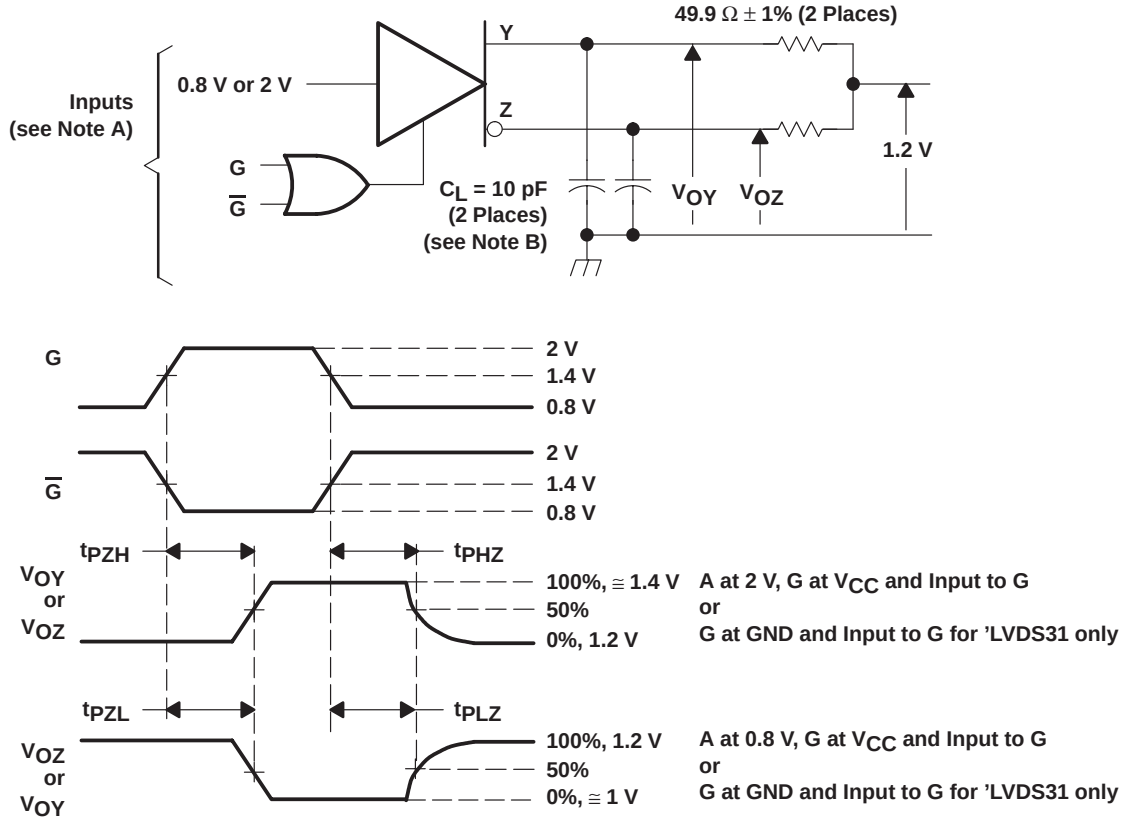
Figure 2. Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal



NOTES: A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns.
B. C_L includes instrumentation and fixture capacitance within 6 mm of the D.U.T.
C. The measurement of $V_{OC(PP)}$ is made on test equipment with a –3 dB bandwidth of at least 300 MHz.

Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

PARAMETER MEASUREMENT INFORMATION

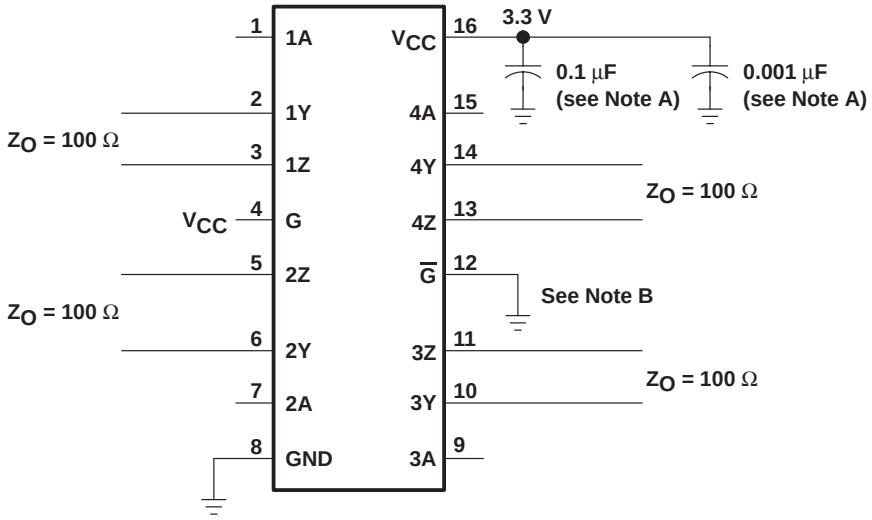


NOTES: A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f < 1 ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns.

B. C_L includes instrumentation and fixture capacitance within 6 mm of the D.U.T.

Figure 4. Enable and Disable Time Circuit and Definitions

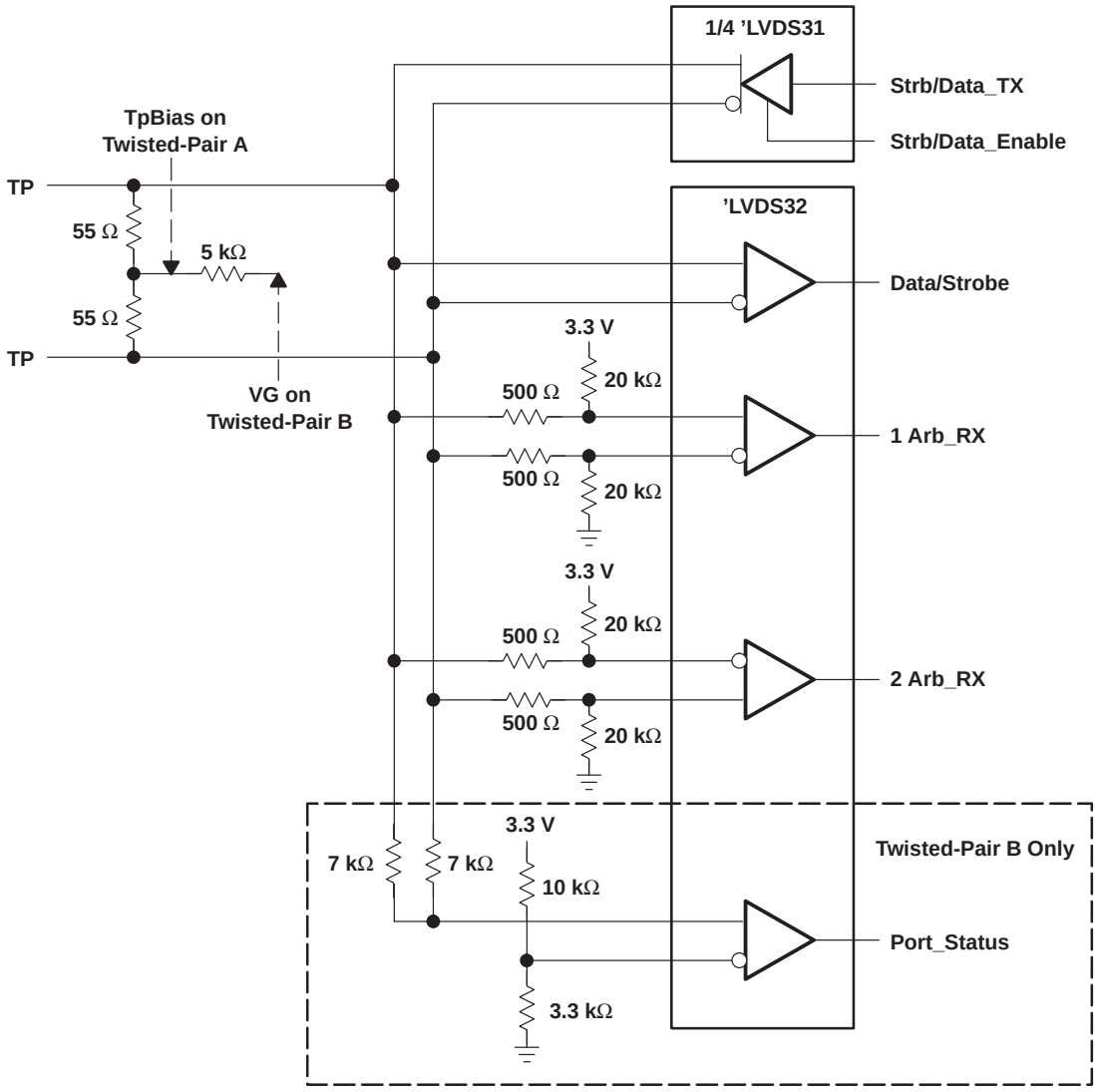
APPLICATIONS INFORMATION



NOTES: A. Place a 0.1 μF and a 0.001 μF Z5U ceramic, mica or polystyrene dielectric, 0805 size, chip capacitor between V_{CC} and the ground plane. The capacitors should be located as close as possible to the device terminals.
B. Unused enable inputs should be tied to V_{CC} or GND as appropriate.

Figure 5. Typical Application Circuit Schematic

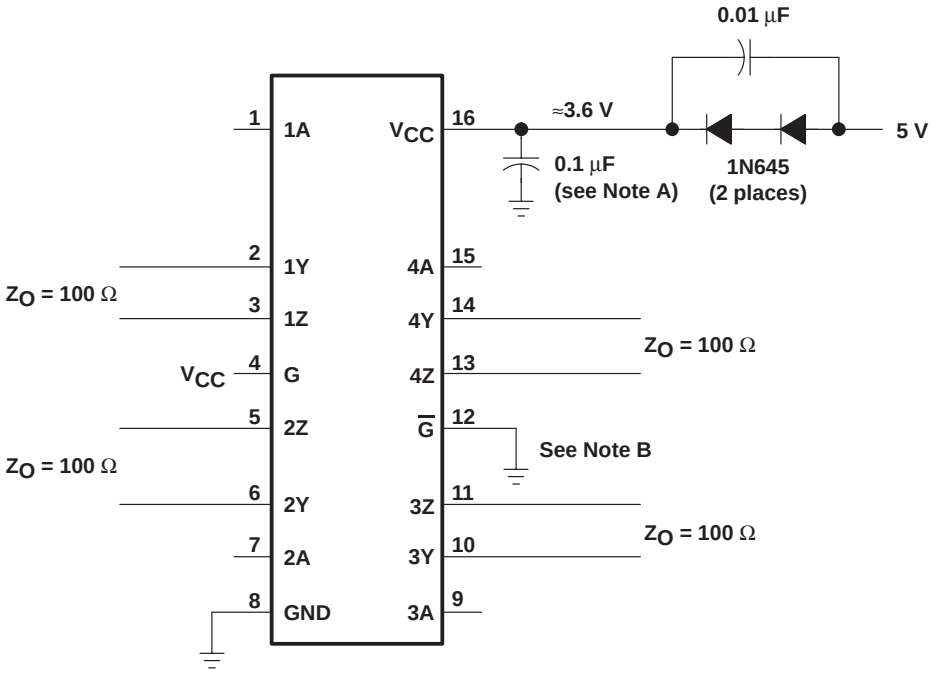
APPLICATIONS INFORMATION



NOTES: A. Resistors are leadless thick-film (0603) 5% tolerance.
B. Decoupling capacitance is not shown but recommended.
C. V_{CC} is 3 V to 3.6 V.
D. The differential output voltage of the 'LVDS31 can exceed that specified by IEEE1394.

Figure 6. 100 Mbps IEEE1394 Transceiver

APPLICATIONS INFORMATION



NOTE A: Place a 0.1 μF Z5U ceramic, mica or polystyrene dielectric, 0805 size, chip capacitor between V_{CC} and the ground plane. The capacitor should be located as close as possible to the device terminals.

Figure 7. Operation With a 5-V Supply

related information

IBIS modeling is available for this device. Please contact the local TI sales office or the TI Web site at *www.ti.com* for more information.

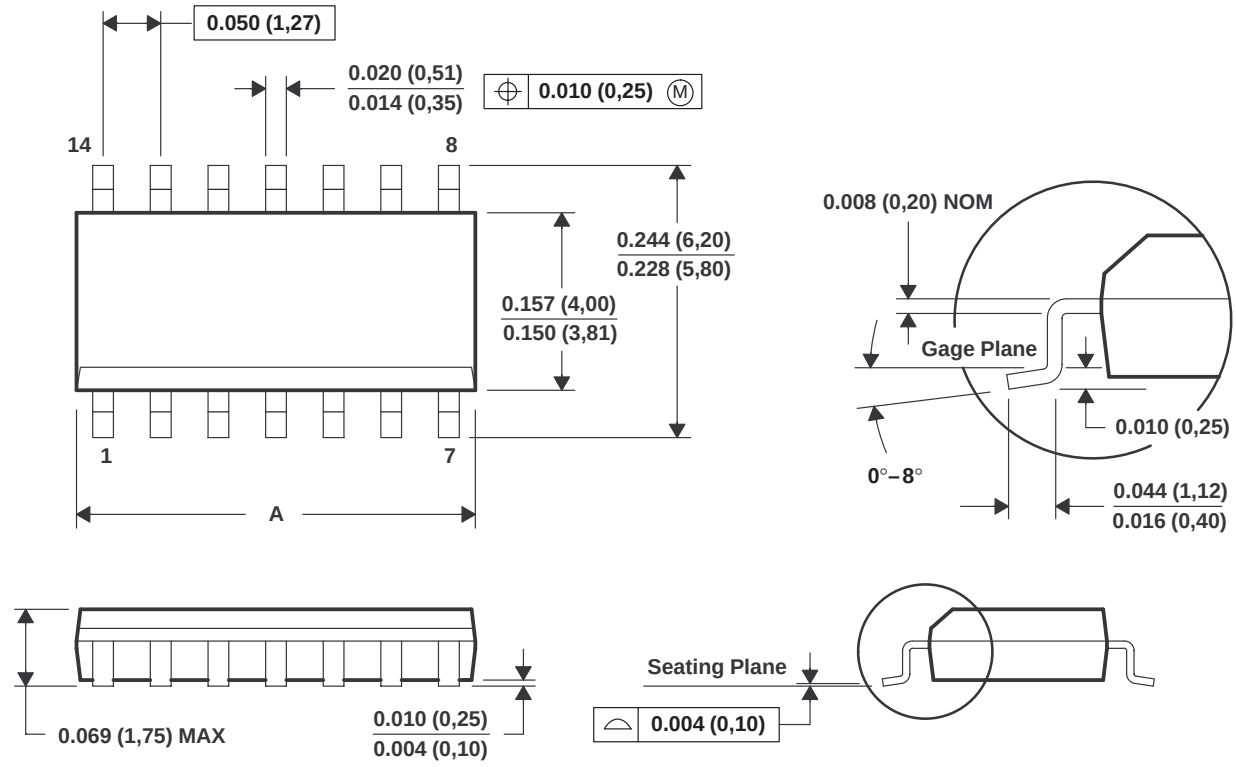
For more application guidelines, please see the following documents:

- *Low-Voltage Differential Signalling Design Notes* (TI literature number SLLA014)
- *Interface Circuits for TIA/EIA-644* (LVDS) (TI literature number SLLA038)
- *Reducing EMI With LVDS* (TI literature number SLLA030)
- *Slew Rate Control of LVDS Circuits* (TI literature number SLLA034)
- *Using an LVDS Receiver With RS-422 Data* (TI literature number SLLA031)
- *Evaluating the LVDS EVM* (TI literature number SLLA033)

MECHANICAL INFORMATION

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



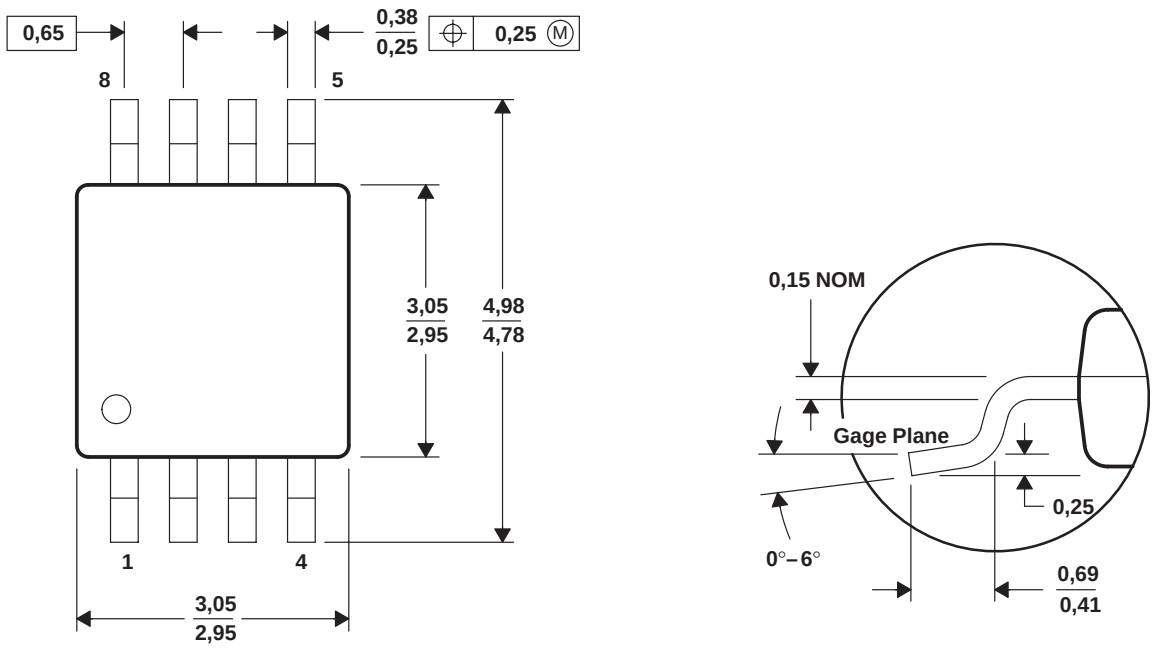
DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

MECHANICAL INFORMATION

DGK (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**

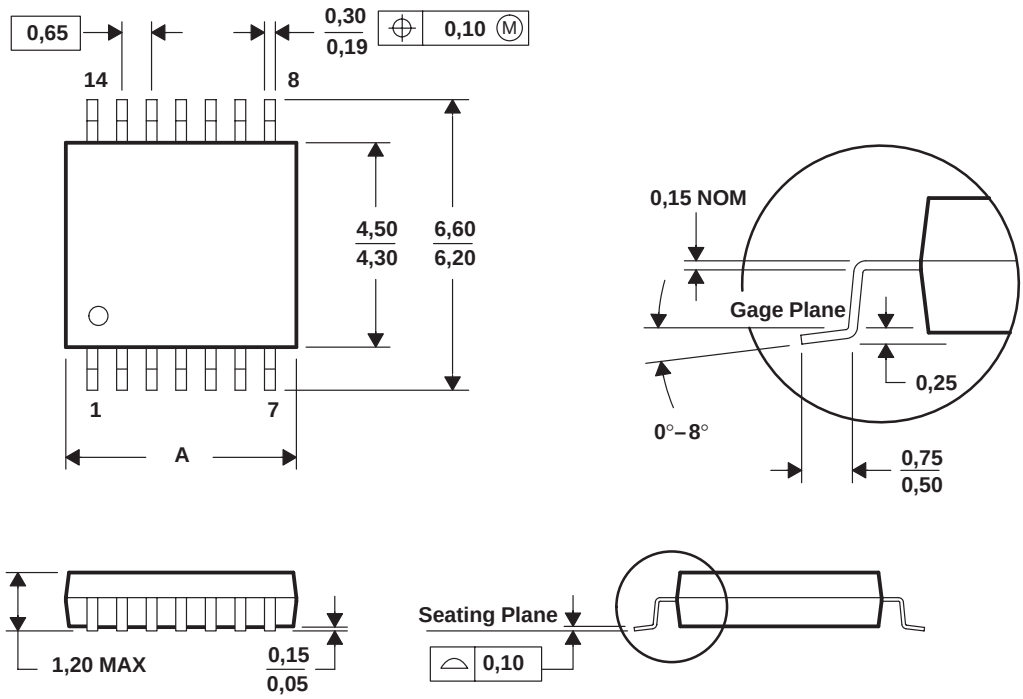


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-187

MECHANICAL INFORMATION

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN75LVDS31D	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75LVDS31
SN75LVDS31D.B	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75LVDS31
SN75LVDS31DR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75LVDS31
SN75LVDS31DR.B	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75LVDS31
SN75LVDS31PW	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	DS31
SN75LVDS31PW.B	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	DS31
SN75LVDS9638D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	DF638
SN75LVDS9638D.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	DF638
SN75LVDS9638DGK	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	AXK
SN75LVDS9638DGK.B	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	AXK

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN75LVDS31 :

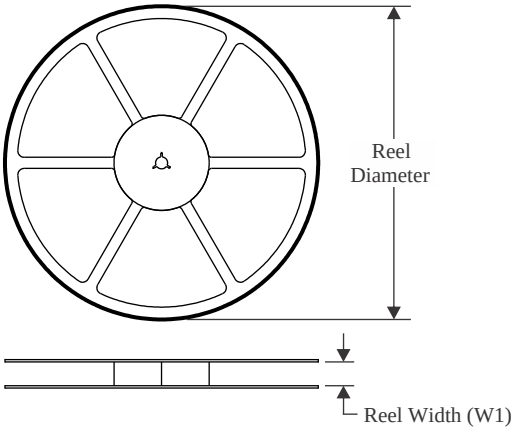
- Military : SN55LVDS31

NOTE: Qualified Version Definitions:

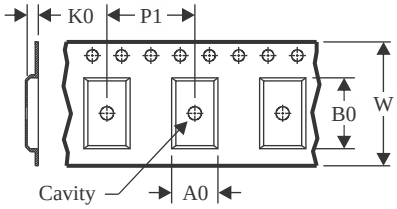
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

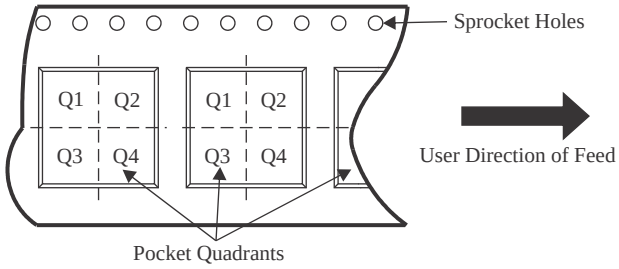


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

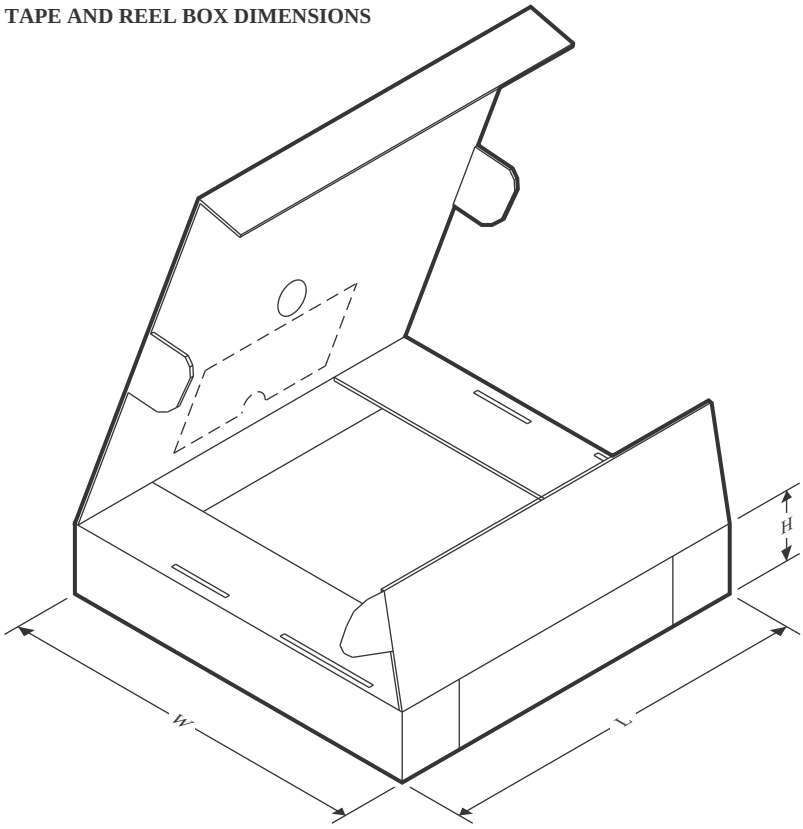
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75LVDS31DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

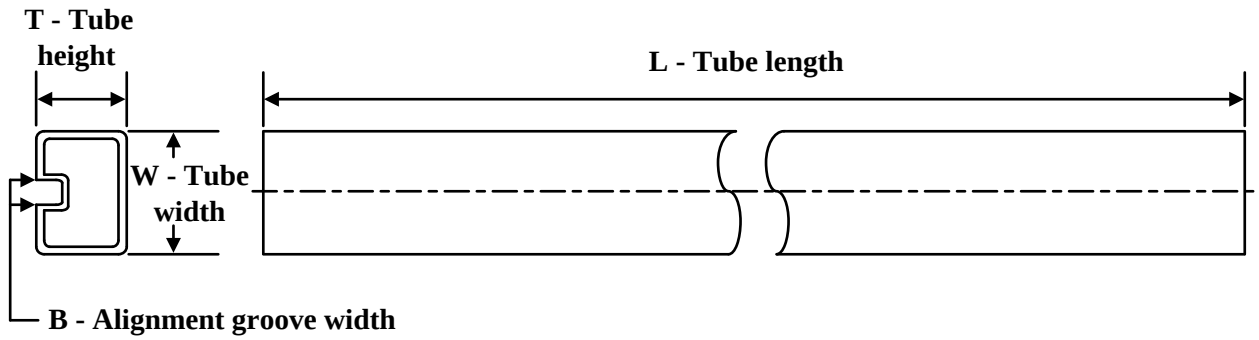
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75LVDS31DR	SOIC	D	16	2500	340.5	336.1	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN75LVDS31D	D	SOIC	16	40	507	8	3940	4.32
SN75LVDS31D.B	D	SOIC	16	40	507	8	3940	4.32
SN75LVDS31PW	PW	TSSOP	16	90	530	10.2	3600	3.5
SN75LVDS31PW.B	PW	TSSOP	16	90	530	10.2	3600	3.5
SN75LVDS9638D	D	SOIC	8	75	505.46	6.76	3810	4
SN75LVDS9638D.B	D	SOIC	8	75	505.46	6.76	3810	4

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