

# TAS6511-Q1 - 50W, 2MHz Digital Input 1-Channel Automotive Heatsink-Free Class-D Audio Amplifier with Current Sense and Real-time Load Diagnostics

## 1 Features

- AEC-Q100 qualified for automotive applications
  - Temperature grade 1:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ,  $T_A$
- General operation
  - 4.5V to 19V supply voltage, 40V load dump
  - Support for 1.8V and 3.3V I/O's
  - I<sup>2</sup>C control with 8 address options
  - $<0.5\text{W}$  idle power loss at 14.4V,  $<5\text{uA}$  max PVDD shutdown loss
- Output current sensing via I<sup>2</sup>S or TDM
  - No need for external circuitry
- Real-time load diagnostics
  - Monitor output conditions while playing audio
  - Open load, Shorted load, Short-to-power, Short-to-ground detection
- Integrated DSP processing
  - Thermal monitoring and foldback
  - PVDD monitoring and foldback
  - Clip detection
  - Low Latency Path, >70% reduced signal delay at 48kHz
- DC and AC Standby load diagnostics
- Audio inputs
  - I<sup>2</sup>S and TDM support up to TDM16
  - Input sample rates: 16, 32, 44.1, 48, 96, 192kHz
- Audio outputs
  - 384kHz to 2MHz configurable output switching frequency
  - Up to 7A channel output current
  - 30W (14.4V, 4Ω, 10% THD+N)
  - 50W (14.4V, 2Ω, 10% THD+N)
- Audio Performance
  - THD+N  $<0.02\%$  (4Ω, 1W, 1kHz)
  - 108dB SNR
  - Output noise:  $41\mu\text{V}_{\text{RMS}}$  at 14.4V, A-weighting
- Protection
  - Output short protection
  - Speaker Guard™ Pro power limiter
  - Configurable overtemperature warning and shutdown
  - I<sup>2</sup>C temperature and supply voltage readout
  - DC offset, undervoltage and overvoltage
- Easily meet CISPR25-L5 EMC specification
  - Advanced spread-spectrum

## 2 Applications

- Acoustic vehicle alerting system (AVAS)
- Emergency call (eCall)

- Automotive head unit
- Telematics control unit
- Automotive cluster display

## 3 Description

The TAS6511-Q1 is a mono-channel, digital-input, Class-D audio amplifier that supports 2MHz switching frequency enabling a cost and size-optimized single-channel audio amplifier design. The device operates from 4.5V to 19V and delivers up to 30W (14.4V, 4Ω, 10% THD+N) and up to 50W (14.4V, 2Ω, 10% THD+N). The device integrates DC and AC load diagnostics to determine the status of the connected load before enabling the output stage. Additionally, the device can monitor the output load condition while in PLAY mode with or without audio using real-time load diagnostics which operates independently from the host and audio input.

TAS6511-Q1 can monitor the output current, PVDD voltage, and temperature of the device and can report this data through TDM or I<sup>2</sup>S. The integrated DSP of the TAS6511-Q1 enables advanced protection features such as PVDD foldback, thermal foldback, and Speaker Guard™ Pro power limiter. The DSP also enables an additional low-latency signal path, providing up to 70% faster signal processing at 48kHz for time-sensitive Active Noise Cancellation (ANC) and Road Noise Cancellation (RNC) applications.

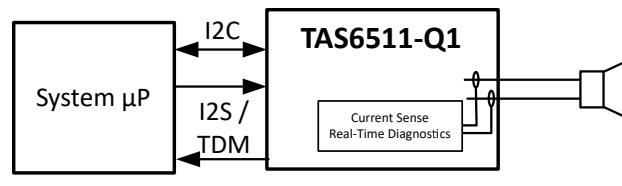
The device is available in a small pad-down TSSOP package, enabling a heatsink-free audio amplifier design.

### Packaging Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>
TAS6511-Q1	HTSSOP (28)	6.4mm × 9.7mm

(1) For more information, see Mechanical, Packaging, and Orderable Information.

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop designs are listed below.

### 4.1 Device Support

### 4.2 Documentation Support

#### 4.2.1 Related Documentation

### 4.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 4.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 4.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 4.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 4.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision A (December 2024) to Revision B (April 2025)</b>	<b>Page</b>
• Updated 14.4V, 4Ω, 10% THD+N output power to 30W.....	1
• Added Mechanical, Packaging, and Orderable Information section.....	4

<b>Changes from Revision * (December 2023) to Revision A (December 2024)</b>	<b>Page</b>
• Updated device status to production data.....	1

## 6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## 6.1 Package Option Addendum

### Packaging Information

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish <sup>(6)</sup>	MSL Peak Temp <sup>(3)</sup>	Op Temp (°C)	Device Marking <sup>(4) (5)</sup>
TAS6511QPWPRQ1	ACTIVE	HTSSOP	PWP	28	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125C	TAS6511

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PRE\_PROD** Unannounced device, not in production, not available for mass market, nor on the web, samples not available.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

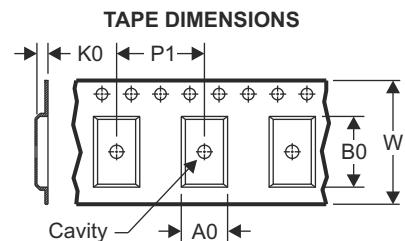
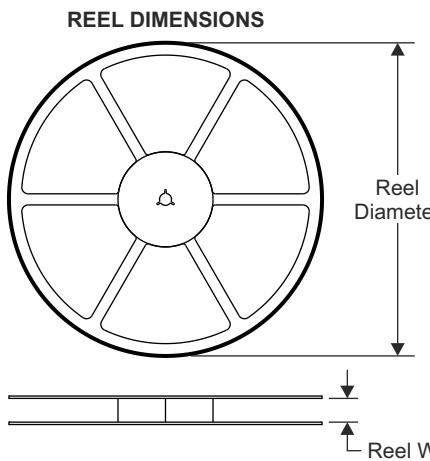
(5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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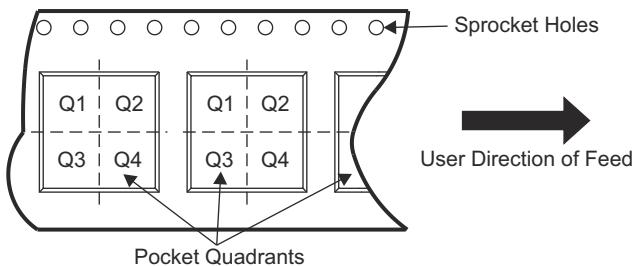
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## 6.2 Tape and Reel Information



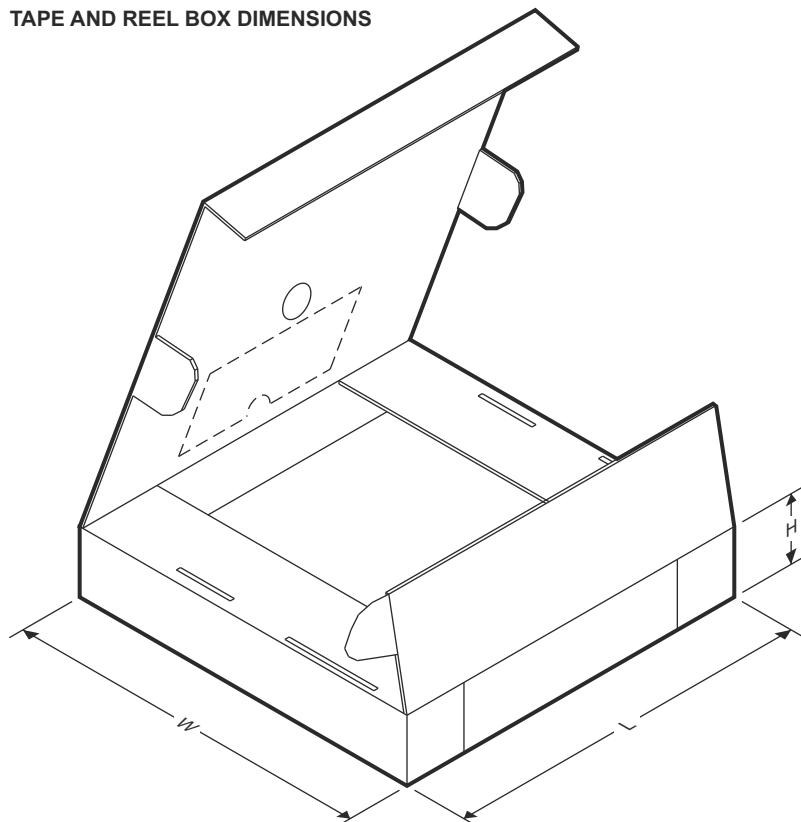
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS6511QPWPRQ1	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

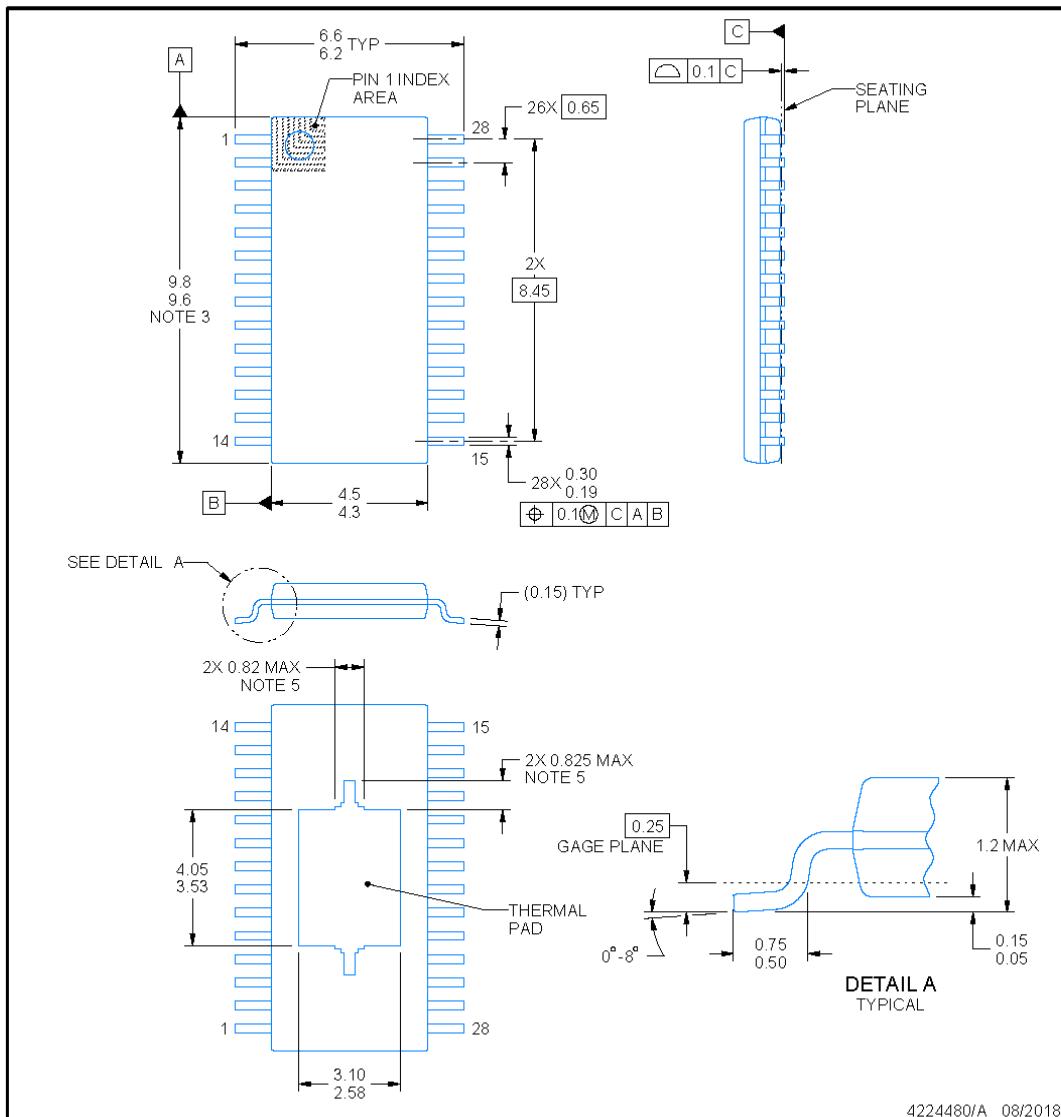
**TAPE AND REEL BOX DIMENSIONS**



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS6511QPWPRQ1	HTSSOP	PWP	28	2000	356.0	356.0	35.0

**PWP0028M****PACKAGE OUTLINE****PowerPAD™ TSSOP - 1.2 mm max height**

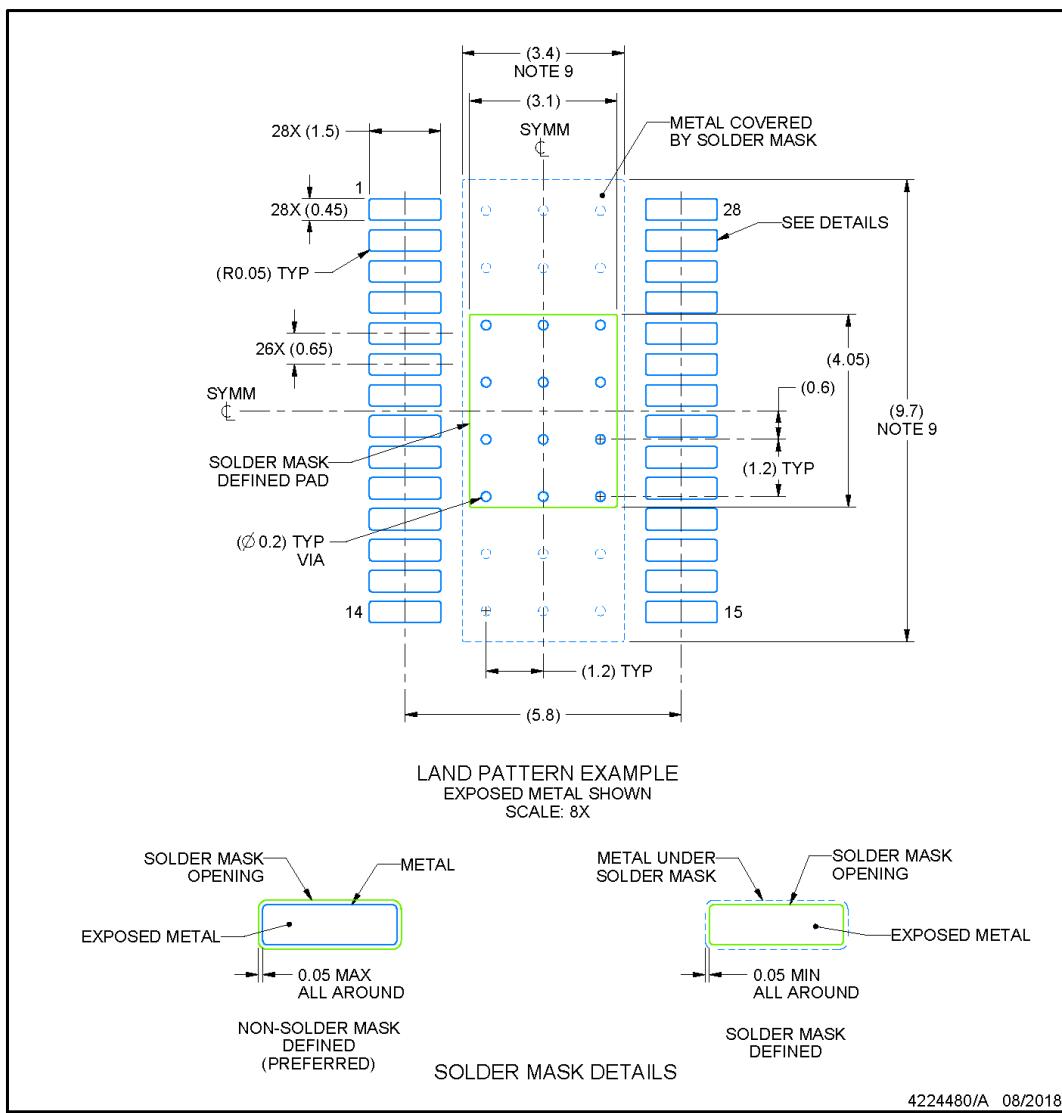
SMALL OUTLINE PACKAGE



PowerPAD is a trademark of Texas Instruments.

**EXAMPLE BOARD LAYOUT**  
**PWP0028M** **PowerPAD™ TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



NOTES: (continued)

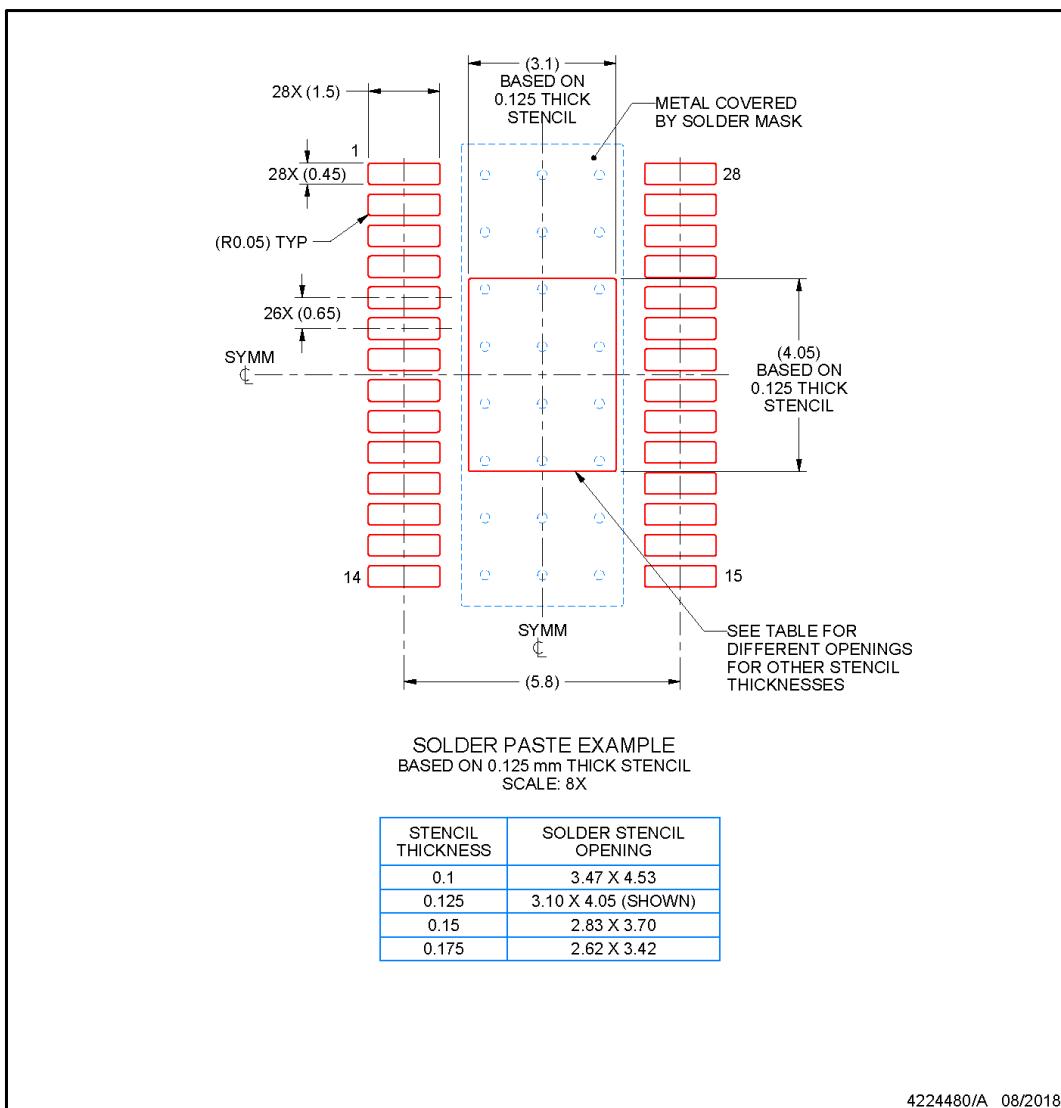
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/itslma002](http://www.ti.com/itslma002)) and SLMA004 ([www.ti.com/itslma004](http://www.ti.com/itslma004)).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

## PWP0028M

### EXAMPLE STENCIL DESIGN

#### PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TAS6511QPWPRQ1	Active	Production	HTSSOP (PWP)   28	2000   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TAS6511
TAS6511QPWPRQ1.A	Active	Production	HTSSOP (PWP)   28	2000   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TAS6511

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

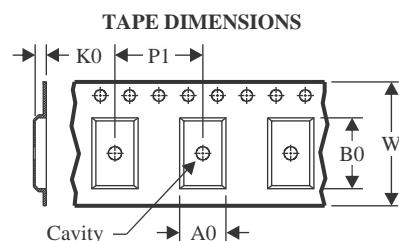
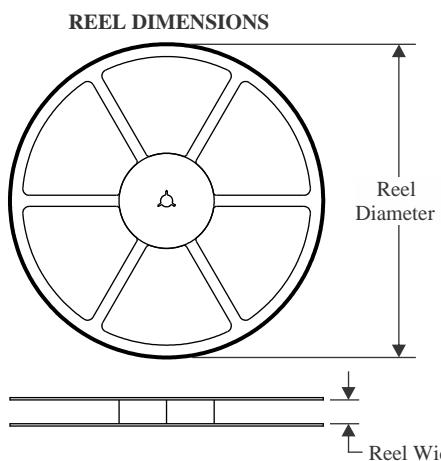
<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

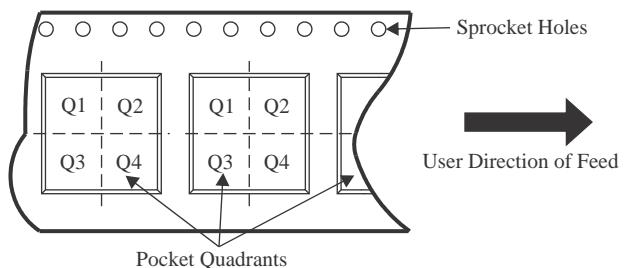
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

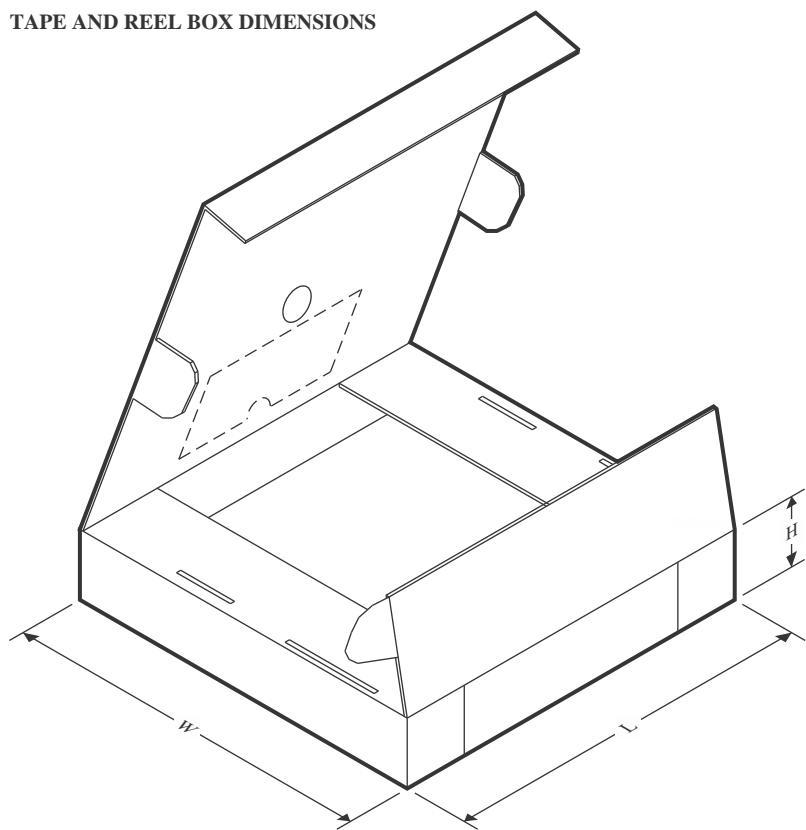
**TAPE AND REEL INFORMATION**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS6511QPWPRQ1	HTSSOP	PWP	28	2000	330.0	16.4	6.75	10.1	1.8	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

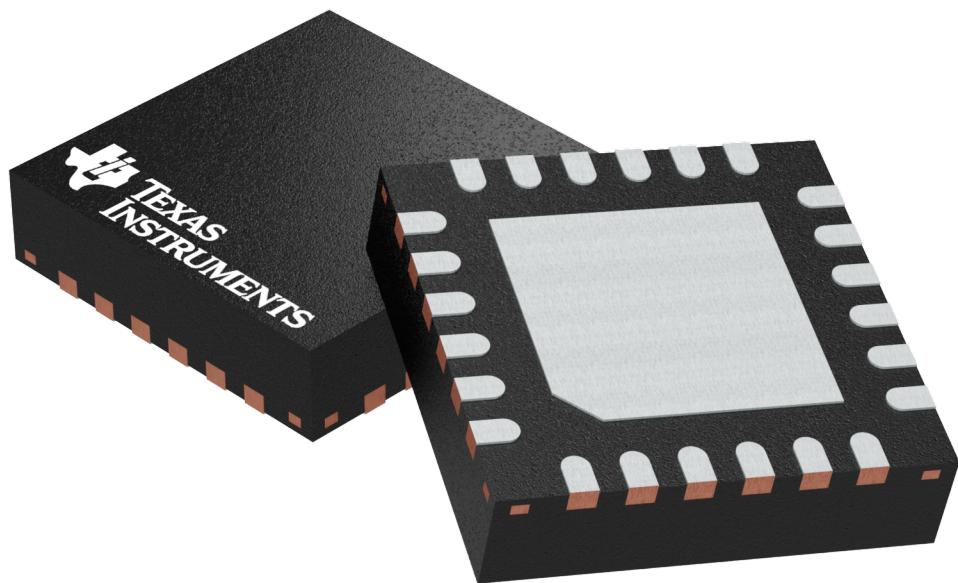
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS6511QPWPRQ1	HTSSOP	PWP	28	2000	353.0	353.0	32.0

## GENERIC PACKAGE VIEW

RGE 24

**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

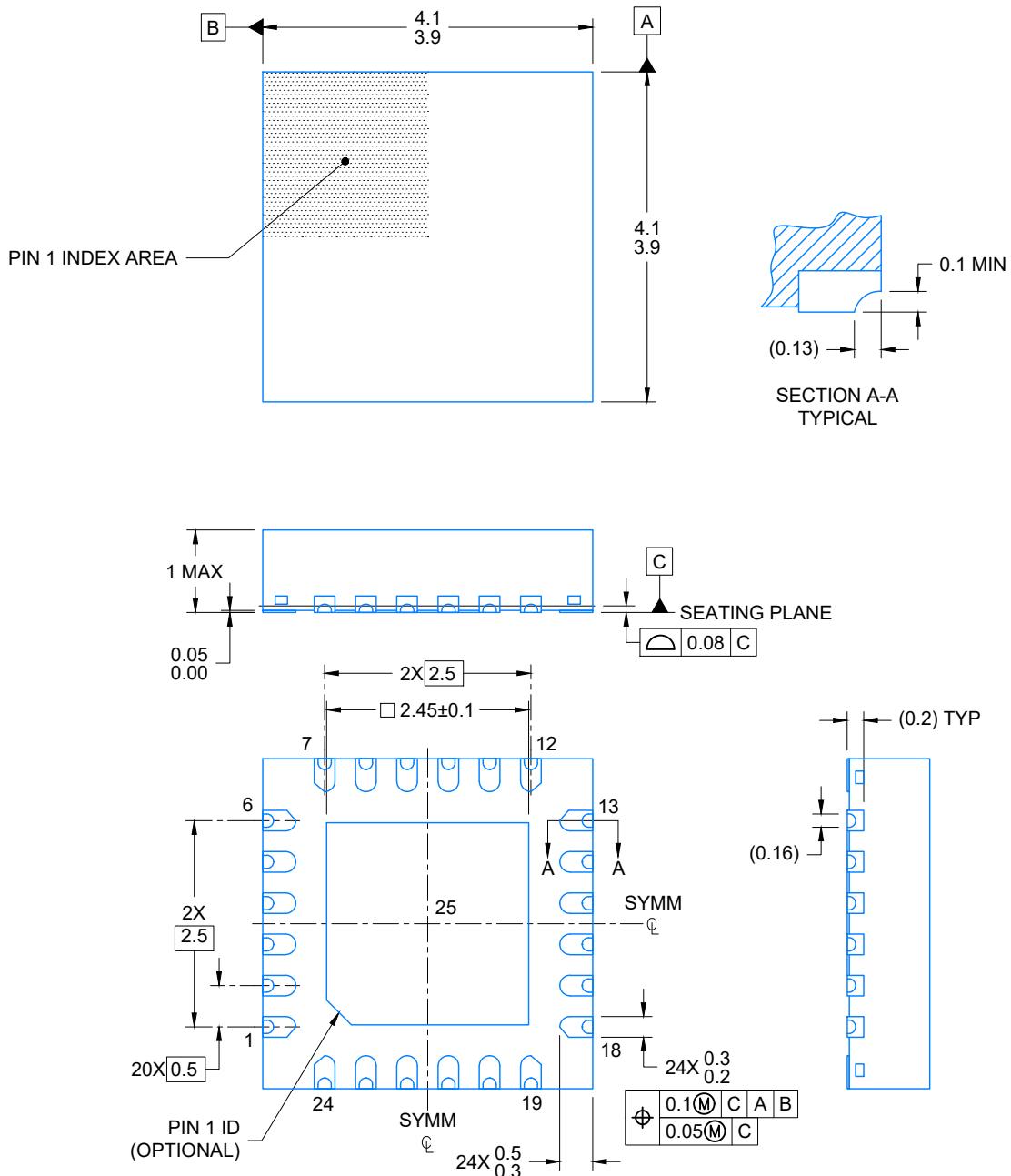
4204104/H

## PACKAGE OUTLINE

## **VQFN - 1 mm max height**

## PLASTIC QUAD FLATPACK-NO LEAD

RGE0024N



4224736/A 12/2018

## NOTES:

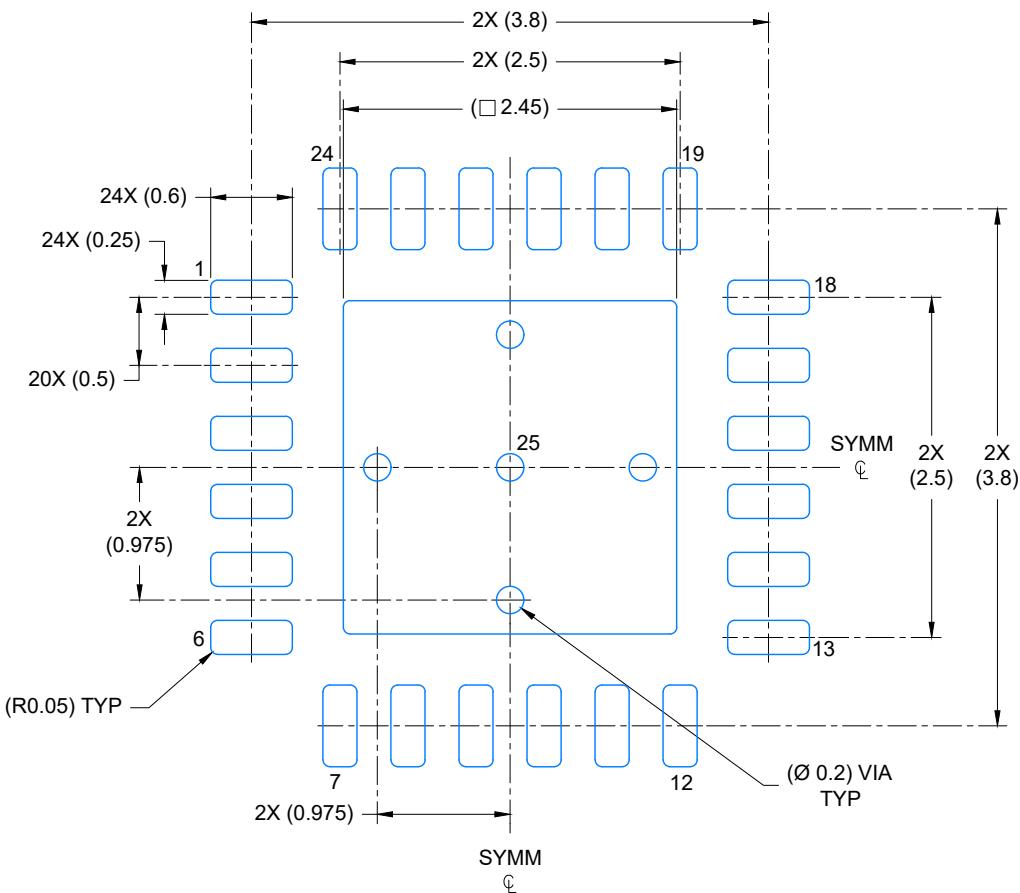
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

RGE0024N

VQFN - 1 mm max height

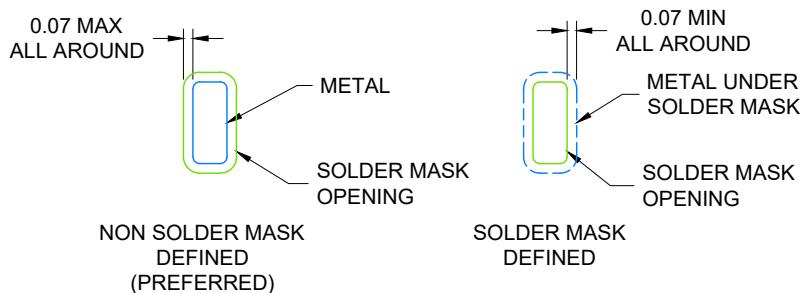
PLASTIC QUAD FLATPACK-NO LEAD



## LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

SCALE: 18X



## SOLDER MASK DETAILS

4224736/A 12/2018

NOTES: (continued)

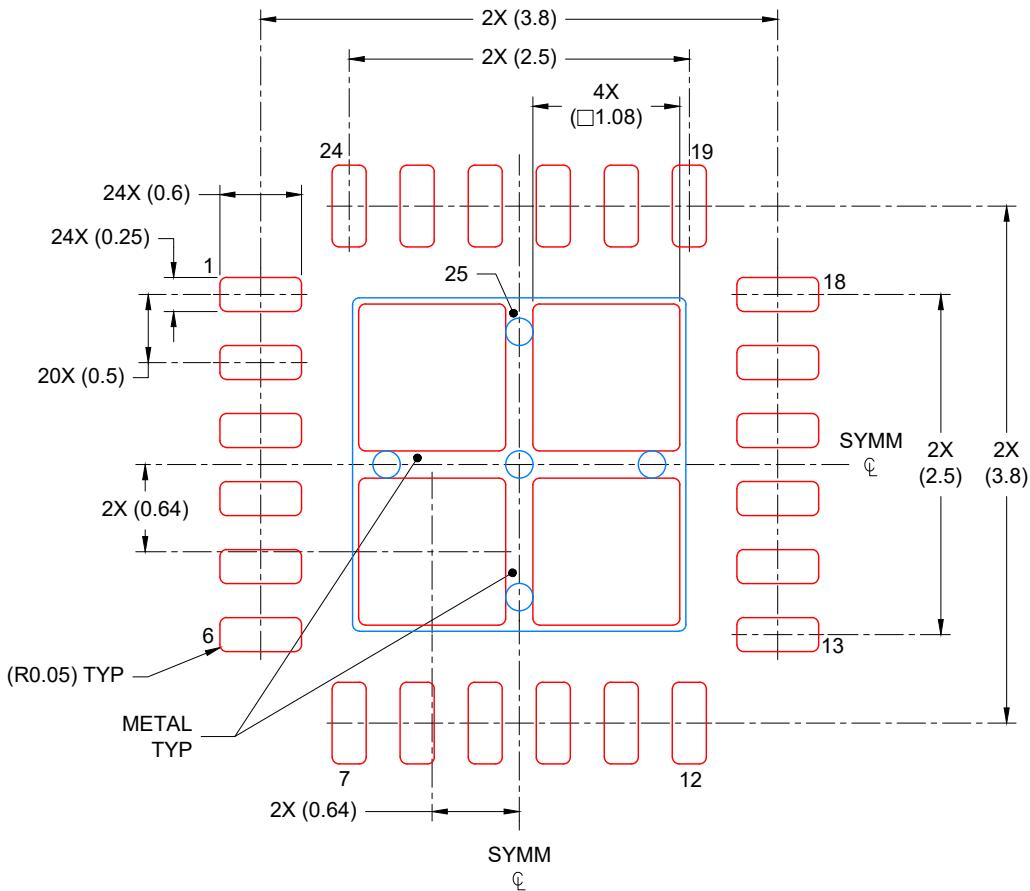
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RGE0024N

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



4224736/A 12/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## GENERIC PACKAGE VIEW

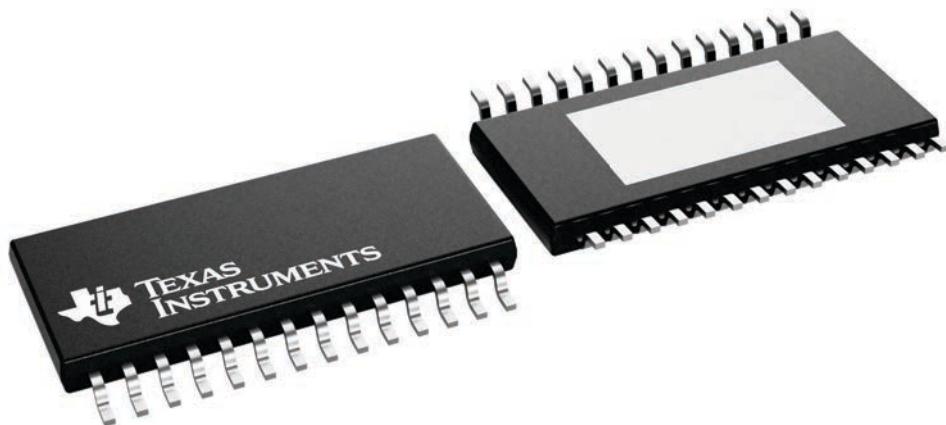
### PWP 28

4.4 x 9.7, 0.65 mm pitch

### PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

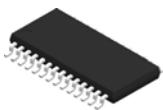
This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224765/B

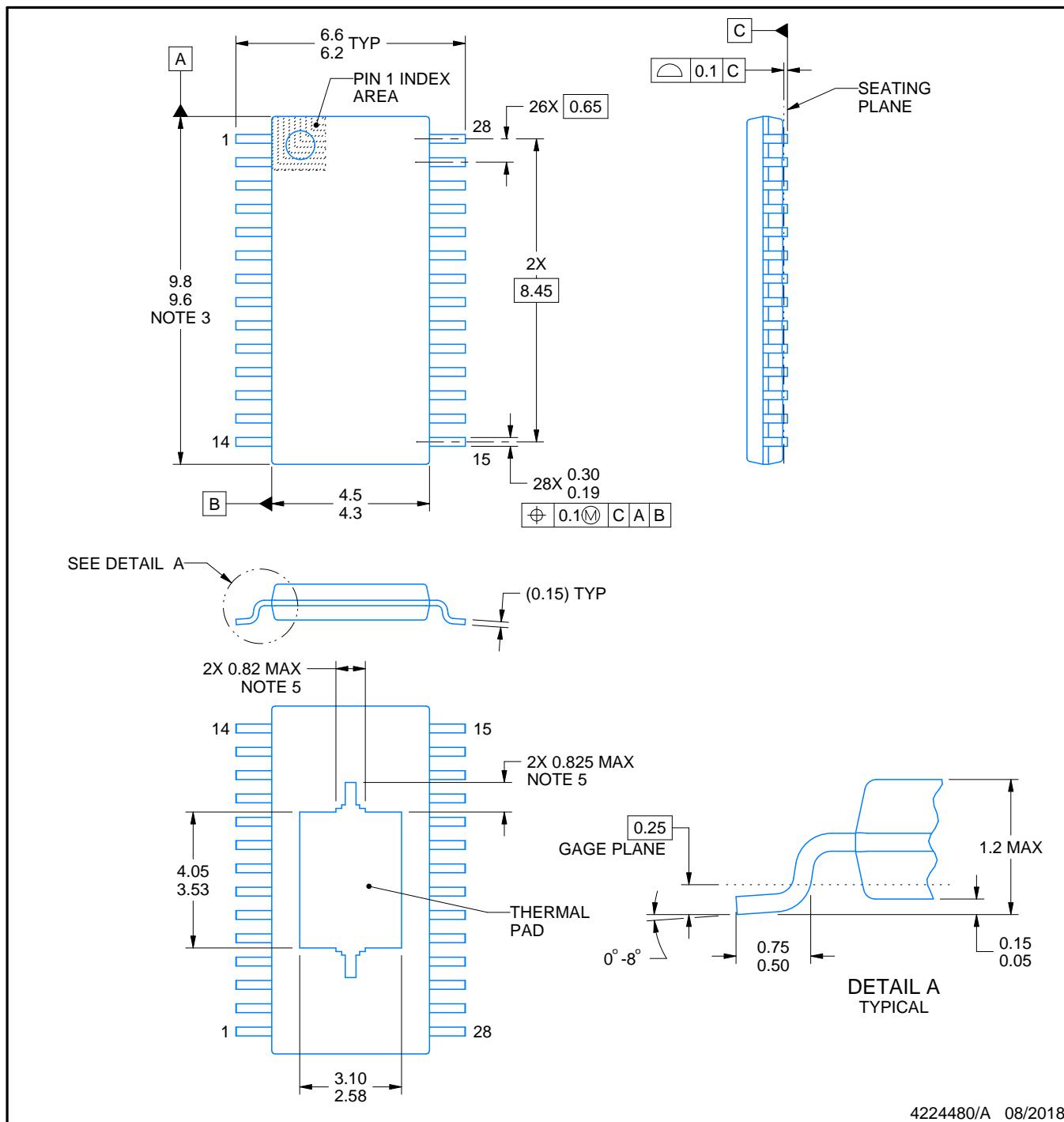
## PACKAGE OUTLINE

PWP0028M



## PowerPAD™ TSSOP - 1.2 mm max height

## SMALL OUTLINE PACKAGE



## NOTES:

PowerPAD is a trademark of Texas Instruments.

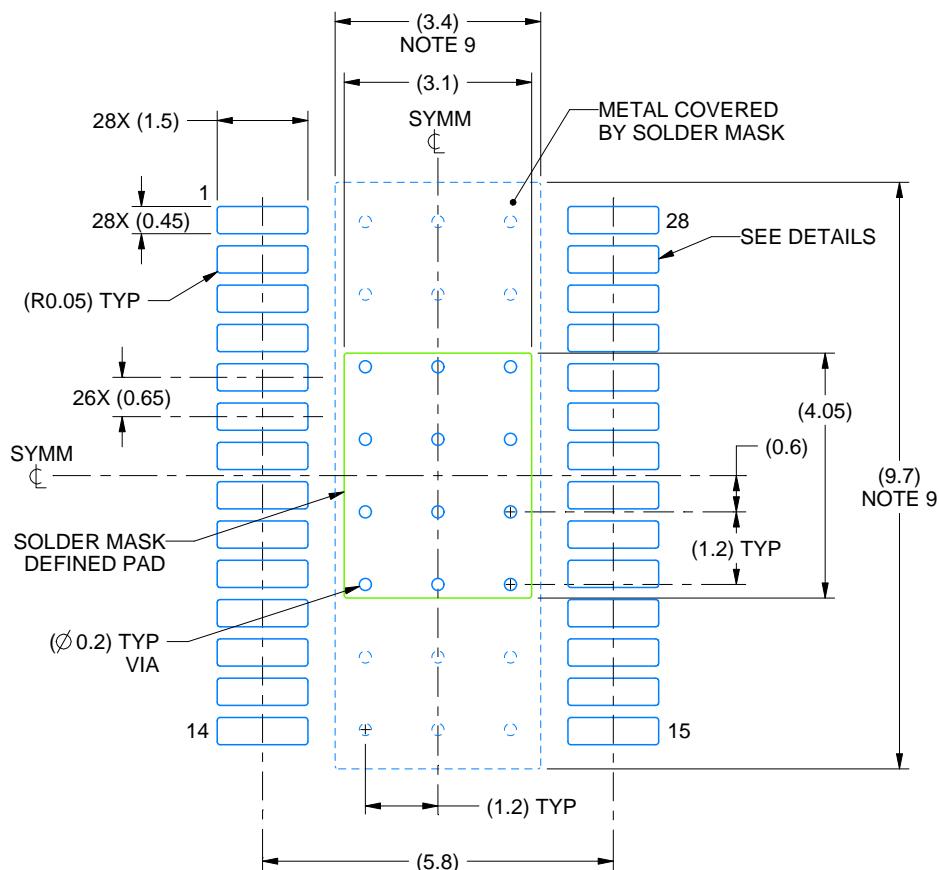
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

# EXAMPLE BOARD LAYOUT

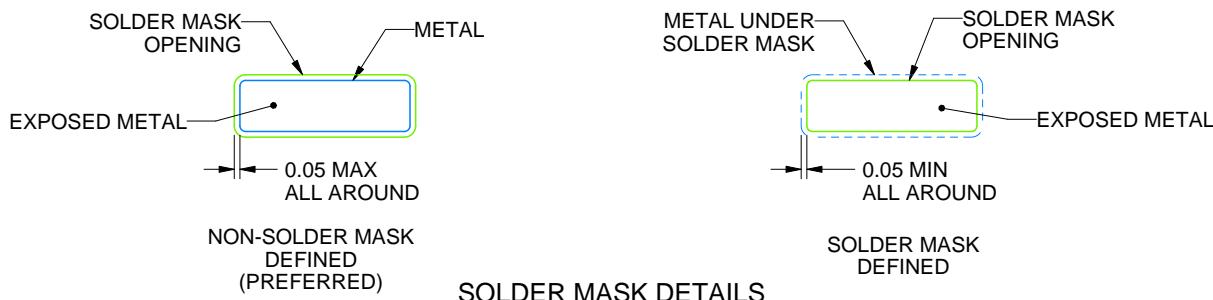
PWP0028M

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 8X



SOLDER MASK DETAILS

4224480/A 08/2018

NOTES: (continued)

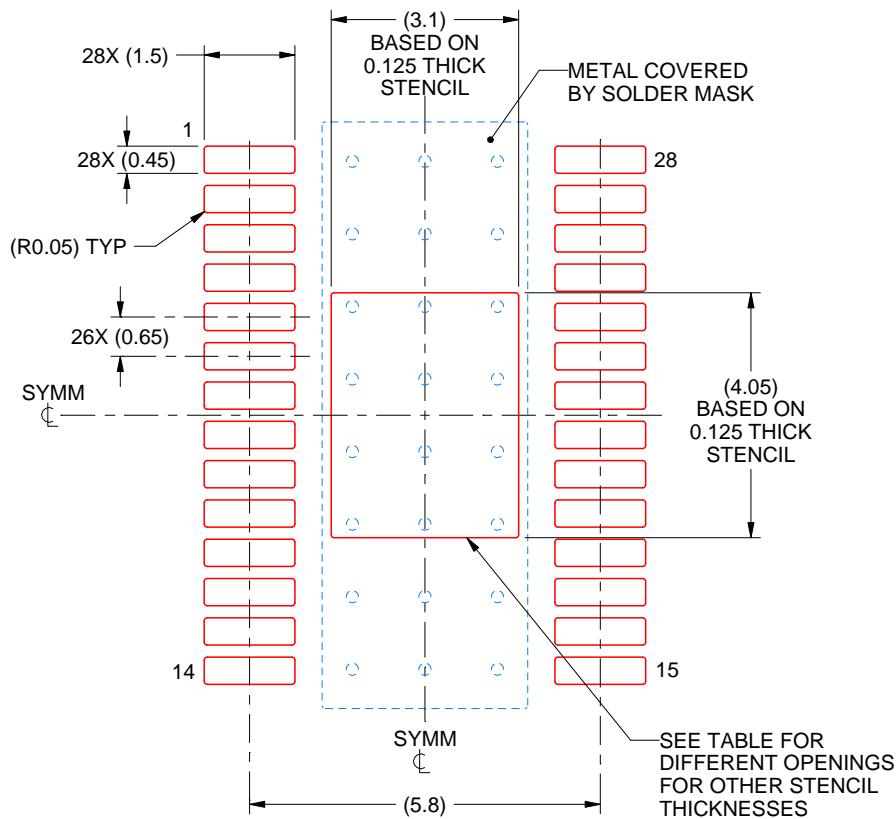
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

PWP0028M

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.47 X 4.53
0.125	3.10 X 4.05 (SHOWN)
0.15	2.83 X 3.70
0.175	2.62 X 3.42

4224480/A 08/2018

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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