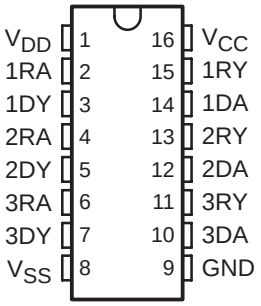
SLLS185D − DECEMBER 1994 − REVISED JULY 2001

- **Meets or Exceeds the Requirements of ANSI TIA/EIA-232-F and ITU V.28**
- **Designed to Support Data Rates up to 120 kbit/s Over 3-m Cable**
- **ESD Protection Exceeds 5 kV on All Pins**
- **Flow-Through Design**
- **Wide-Driver Supply Voltage . . . ±7.5 V to ±15 V**
- **Functionally Interchangeable With Motorola MC145406 and Texas Instruments SN75C1406**

DW OR N PACKAGE
(TOP VIEW)



description

The TL145406 is a bipolar device containing three independent drivers and receivers that are used to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE). The drivers and receivers of the TL145406 are similar to those of the SN75188 quadruple driver and SN75189A quadruple receiver, respectively. The pinout matches the flow-through design of the SN75C1406 to reduce the board space required and to allow easy interconnection. The bipolar circuits and processing of the TL145406 provide a rugged low-cost solution for this function at the expense of quiescent power and external passive components relative to the SN75C1406.

The TL145406 complies with the requirements of TIA/EIA-232-F and ITU (formerly CCITT) V.28 standards. These standards are for data interchange between a host computer and peripheral at signaling rates up to 20 kbit/s. The switching speeds of the TL145406 are fast enough to support rates up to 120 kbit/s with lower capacitive loads (shorter cables). Interoperability at the higher signaling rates cannot be assured unless the designer has design control of the cable and of the interface circuits at both ends. For interoperability at signaling rates to 120 kbit/s, use of TIA/EIA-423-B (ITU V.10) and TIA/EIA-422-B (ITU V.11) standards is recommended.

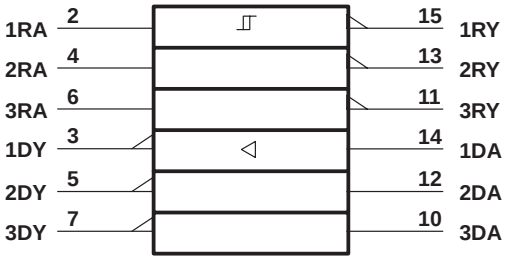
The TL145406 is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES	
	PLASTIC DIP (N)	PLASTIC SMALL OUTLINE (DW)
0°C to 70°C	TL145406N	TL145406DW

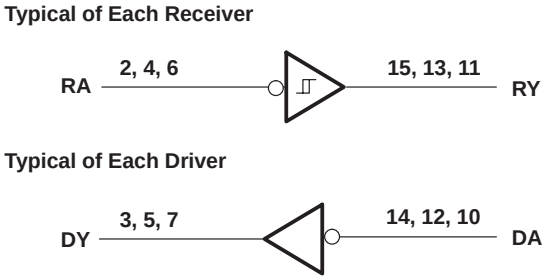
The DW package also is available taped and reeled. Add the suffix R to the device type (e.g., TL145406DWR).

logic symbol†

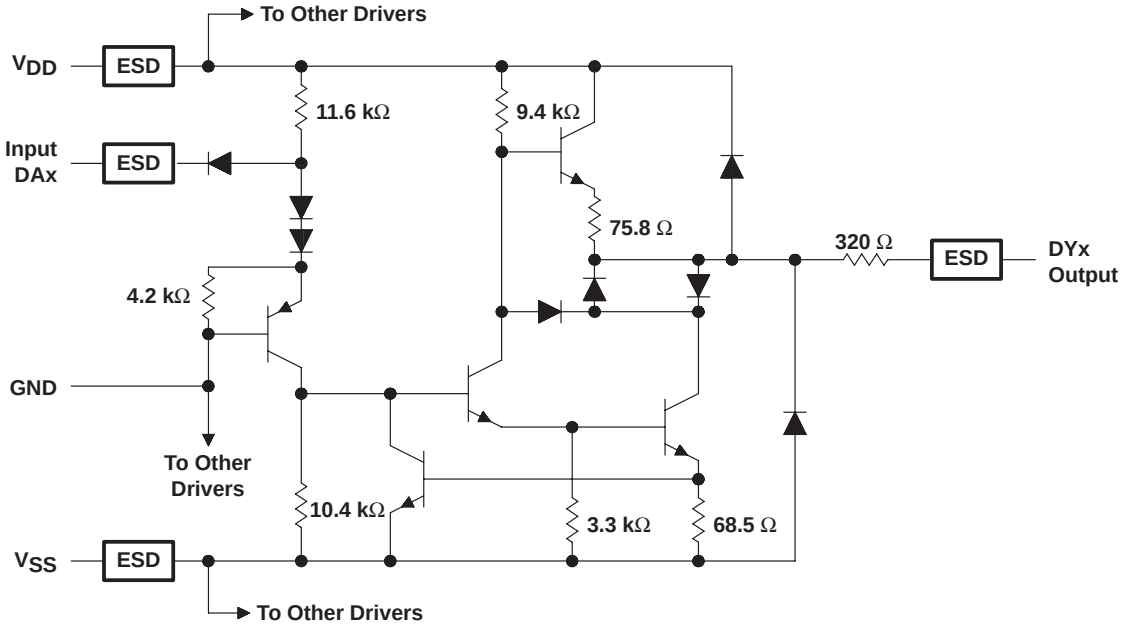


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

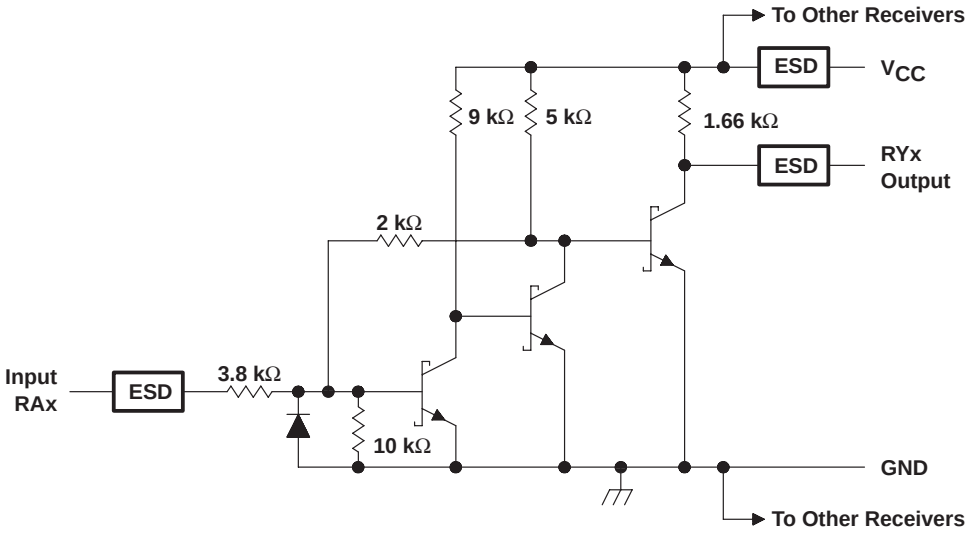


schematic (each driver)



Resistor values shown are nominal.

schematic (each receiver)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (see Note 1): V_{CC}	10 V
V_{DD}	15 V
V_{SS}	−15 V
Input voltage range: Driver	−15 V to 7 V
Receiver	−30 V to 30 V
Driver output voltage range	−15 V to 15 V
Receiver low-level output current	20 mA
Package thermal impedance, θ_{JA} (see Note 2): DW package	57°C/W
N package	67°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to the network ground terminal.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		7.5	9	15	V
V_{SS}	Supply voltage		−7.5	−9	−15	V
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage (driver only)		1.9			V
V_{IL}	Low-level input voltage (driver only)				0.8	V
I_{OH}	High-level output current	Driver			−6	mA
		Receiver			−0.5	
I_{OL}	Low-level output current	Driver			6	mA
		Receiver			16	
T_A	Operating free-air temperature		0		70	°C

supply currents

PARAMETER		TEST CONDITIONS				MIN	TYP	MAX	UNIT
I_{DD}	Supply current from V_{DD}	All inputs at 1.9 V,	No load	V_{DD} = 9 V,	V_{SS} = −9 V			15	mA
				V_{DD} = 12 V,	V_{SS} = −12 V			19	
				V_{DD} = 15 V,	V_{SS} = −15 V			25	
		All inputs at 0.8 V,	No load	V_{DD} = 9 V,	V_{SS} = −9 V			4.5	
				V_{DD} = 12 V,	V_{SS} = −12 V			5.5	
				V_{DD} = 15 V,	V_{SS} = −15 V			9	
I_{SS}	Supply current from V_{SS}	All inputs at 1.9 V,	No load	V_{DD} = 9 V,	V_{SS} = −9 V			−15	mA
				V_{DD} = 12 V,	V_{SS} = −12 V			−19	
				V_{DD} = 15 V,	V_{SS} = −15 V			−25	
		All inputs at 0.8 V,	No load	V_{DD} = 9 V,	V_{SS} = −9 V			−3.2	
				V_{DD} = 12 V,	V_{SS} = −12 V			−3.2	
				V_{DD} = 15 V,	V_{SS} = −15 V			−3.2	
I_{CC}	Supply current from V_{CC}	All inputs at 5 V,	No load,	V_{CC} = 5 V			13.2	20	mA

DRIVER SECTION

electrical characteristics over recommended operating free-air temperture range, V_{DD} = 9 V, V_{SS} = −9 V, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	V_{IL} = 0.8 V,	R_L = 3 kΩ,	See Figure 1	6	7.5		V
V_{OL}	Low-level output voltage (see Note 3)	V_{IH} = 1.9 V,	R_L = 3 kΩ,	See Figure 1		−7.5	−6	V
I_{IH}	High-level input current	V_I = 5 V,	See Figure 2				10	μA
I_{IL}	Low-level input current	V_I = 0,	See Figure 2				−1.6	mA
$I_{OS(H)}$	High-level short-circuit output current (see Note 4)	V_{IL} = 0.8 V,	V_O = 0 or V_{SS},	See Figure 1	−4.5	−10	−19.5	mA
$I_{OS(L)}$	Low-level short-circuit output current	V_{IH} = 2 V,	V_O = 0 or V_{DD},	See Figure 1	4.5	10	19.5	mA
r_O	Output resistance (see Note 5)	V_{CC} = V_{DD} = V_{SS} = 0, V_O = −2 V to 2 V			300			Ω

NOTES: 3. The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only (e.g., if −10 V is maximum, the typical value is a more negative voltage).
4. Output short-circuit conditions must maintain the total power dissipation below absolute maximum ratings.
5. Test conditions are those specified by TIA/EIA-232-F and as listed above.

switching characteristics, V_{CC} = 5 V, V_{DD} = 12 V, V_{SS} = −12 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF, See Figure 3		315	500	ns
t_{PHL}	Propagation delay time, high- to low-level output	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF, See Figure 3		75	175	ns
t_{TLH}	Transition time, low- to high-level output	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF, See Figure 3		60	100	ns
		R_L = 3 kΩ to 7 kΩ, C_L = 2500 pF, See Figure 3 and Note 6		1.7	2.5	μs
t_{THL}	Transition time, high- to low-level output	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF, See Figure 3		40	75	ns
		R_L = 3 kΩ to 7 kΩ, C_L = 2500 pF, See Figure 3 and Note 7		1.5	2.5	μs

NOTES: 6. Measured between −3-V and 3-V points of the output waveform (TIA/EIA-232-F conditions). All unused inputs are tied.
7. Measured between 3-V and −3-V points of the output waveform (TIA/EIA-232-F conditions). All unused inputs are tied.

RECEIVER SECTION

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going threshold voltage	See Figure 5	T_A = 25°C	1.75	1.9	2.3	V
			T_A = 0°C to 70°C	1.55		2.3	
V_{IT-}	Negative-going threshold voltage			0.75	0.97	1.25	V
V_{hys}	Input hysteresis ($V_{IT+} - V_{IT-}$)			0.5			V
V_{OH}	High-level output voltage	I_{OH} = −0.5 mA	V_{IH} = 0.75 V	2.6	4	5	V
			Inputs open	2.6			
V_{OL}	Low-level output voltage	I_{OL} = 10 mA,	V_I = 3 V		0.2	0.45	V
I_{IH}	High-level input current	V_I = 25 V,	See Figure 5	3.6		8.3	mA
		V_I = 3 V,	See Figure 5	0.43			
I_{IL}	Low-level input current	V_I = −25 V,	See Figure 5	−3.6		−8.3	mA
		V_I = −3 V,	See Figure 5	−0.43			
I_{OS}	Short-circuit output current				−3.4	−12	mA

† All typical values are at T_A = 25°C, V_{CC} = 5, V_{DD} = 9 V, and V_{SS} = −9 V.

switching characteristics, V_{CC} = 5 V, V_{DD} = 12 V, V_{SS} = −12 V, T_A = 25°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 50 pF,	R_L = 5 kΩ,	See Figure 6		107	425	ns
t_{PHL}	Propagation delay time, high- to low-level output	C_L = 50 pF,	R_L = 5 kΩ,	See Figure 6		42	150	ns
t_{TLH}	Transition time, low- to high-level output	C_L = 50 pF,	R_L = 5 kΩ,	See Figure 6		175	400	ns
t_{THL}	Transition time, high- to low-level output	C_L = 50 pF,	R_L = 5 kΩ,	See Figure 6		16	60	ns

PARAMETER MEASUREMENT INFORMATION

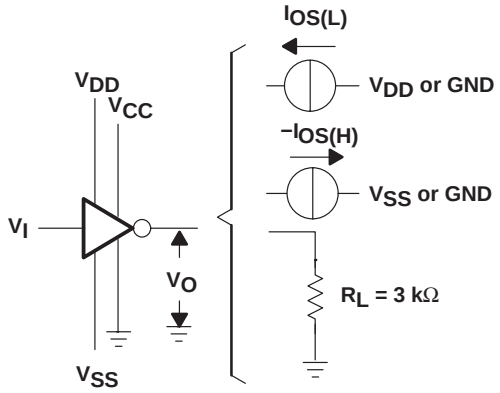


Figure 1. Driver Test Circuit for V_{OH}, V_{OL}, $I_{OS(H)}$, and $I_{OS(L)}$

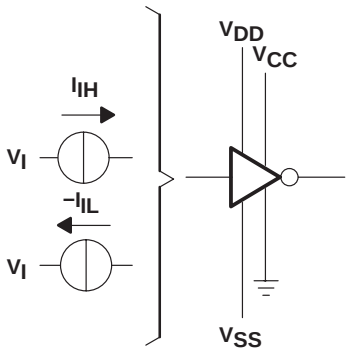
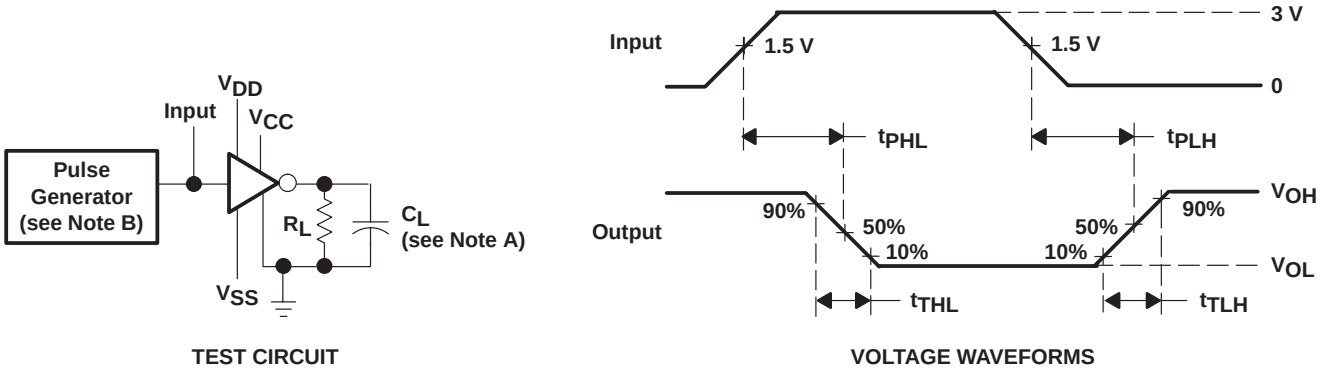


Figure 2. Driver Test Circuit for I_{IH} and I_{IL}

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: t_w = 25 µs, PRR = 20 kHz, Z_O = 50 Ω, $t_r = t_f$ < 50 ns.

Figure 3. Driver Test Circuit and Voltage Waveforms

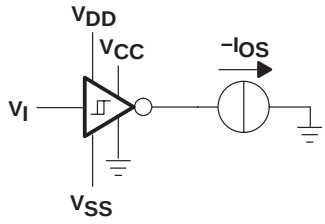


Figure 4. Receiver Test Circuit for I_{OS}

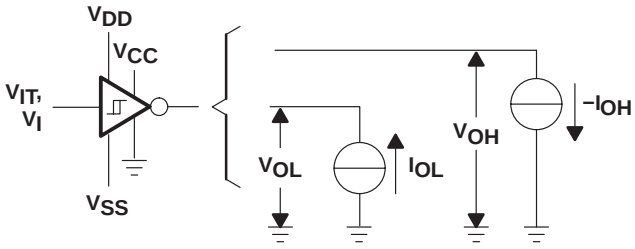
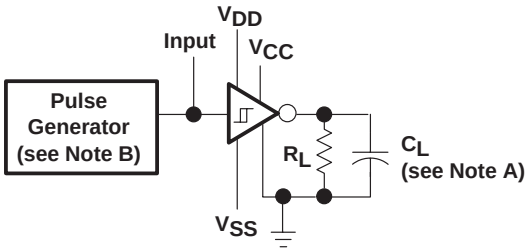


Figure 5. Receiver Test Circuit for V_{IT}, V_{OH}, and V_{OL}



NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: t_w = 25 µs, PRR = 20 kHz, Z_O = 50 Ω, $t_r = t_f$ < 50 ns.

Figure 6. Receiver Propagation and Transition Times

TYPICAL CHARACTERISTICS

DRIVER
VOLTAGE TRANSFER CHARACTERISTICS

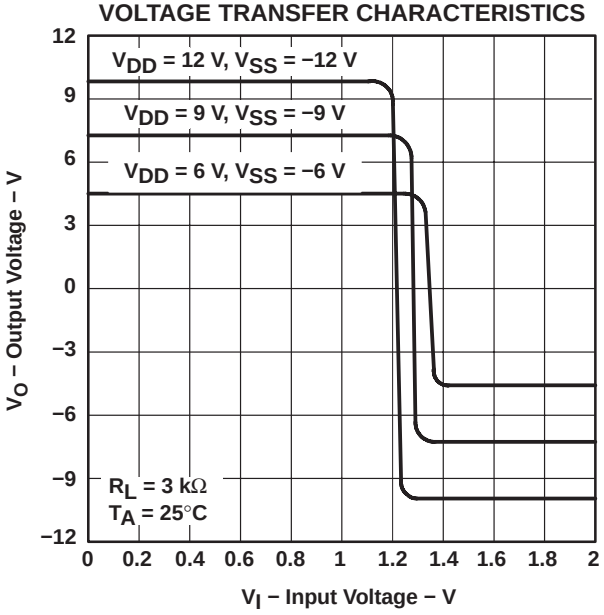


Figure 7

DRIVER
OUTPUT CURRENT
vs
OUTPUT VOLTAGE

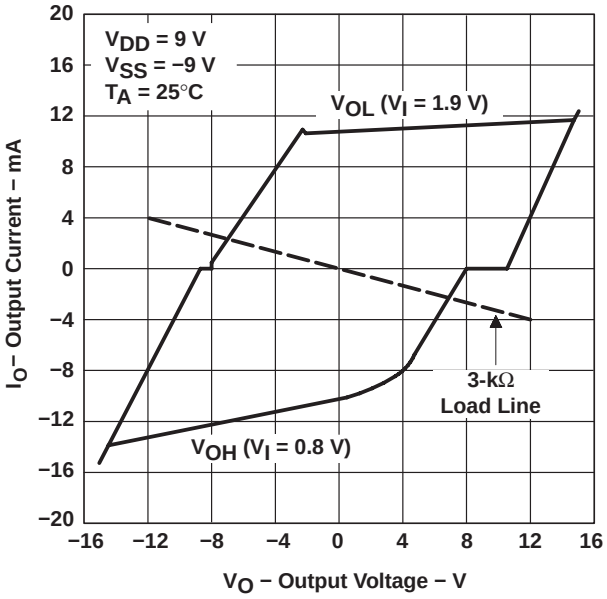


Figure 8

DRIVER
SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

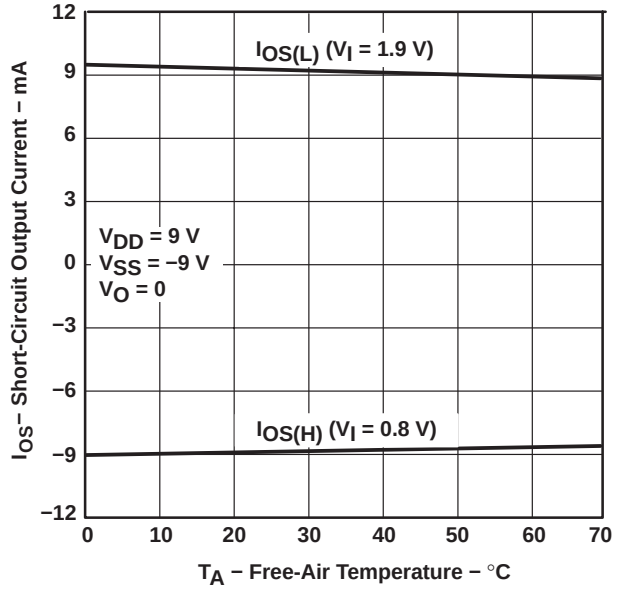


Figure 9

DRIVER
SLEW RATE
vs
LOAD CAPACITANCE

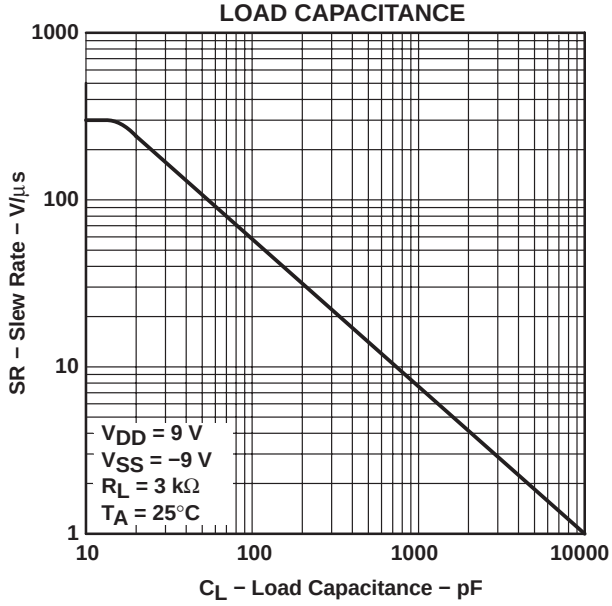


Figure 10

TYPICAL CHARACTERISTICS

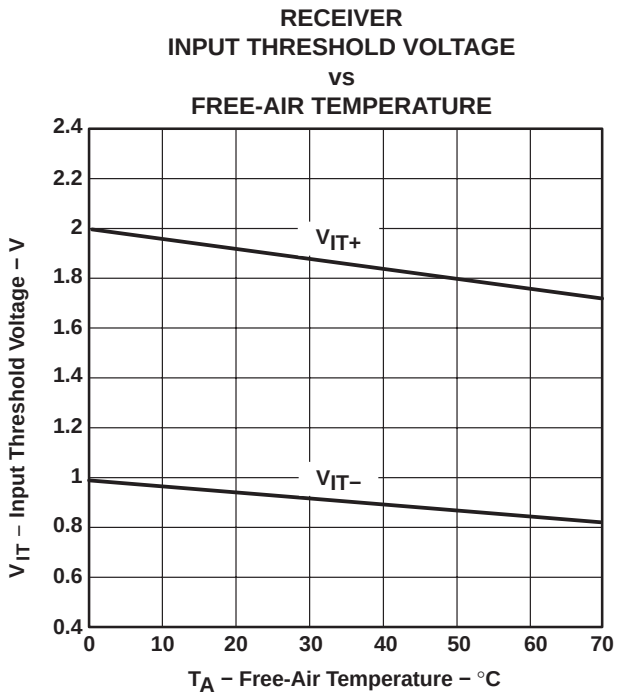


Figure 11

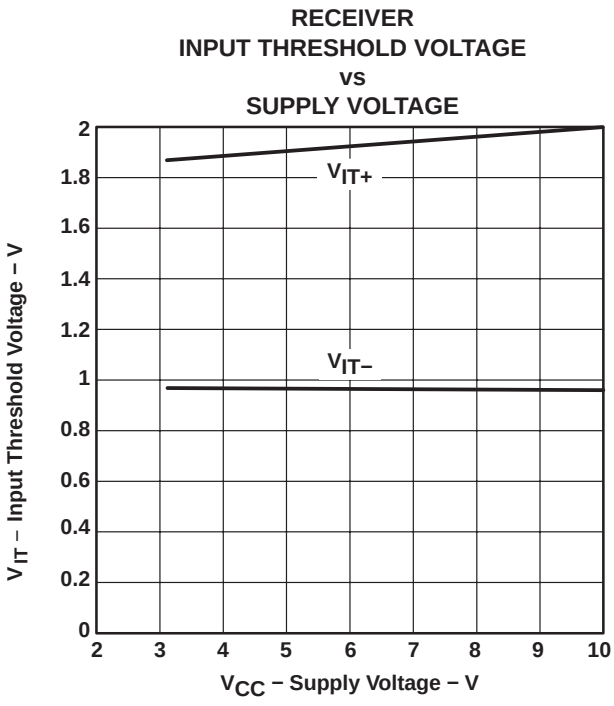
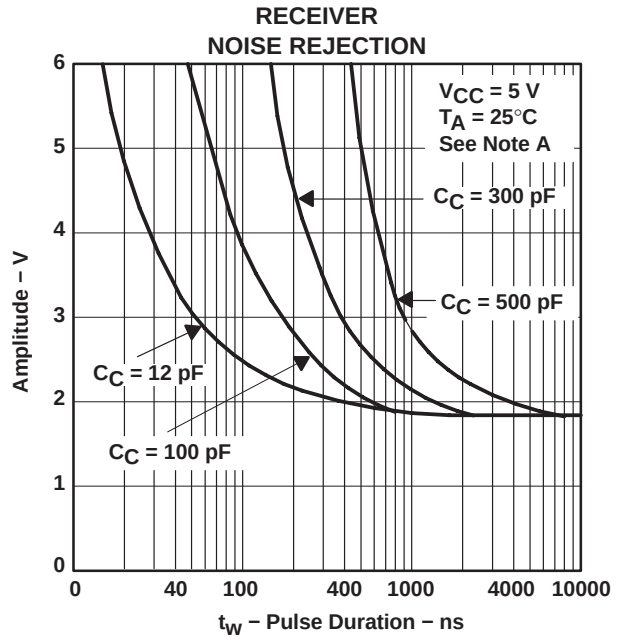


Figure 12



NOTE A: This figure shows the maximum amplitude of a positive-going pulse that, starting from 0, does not cause a change of the output level.

Figure 13

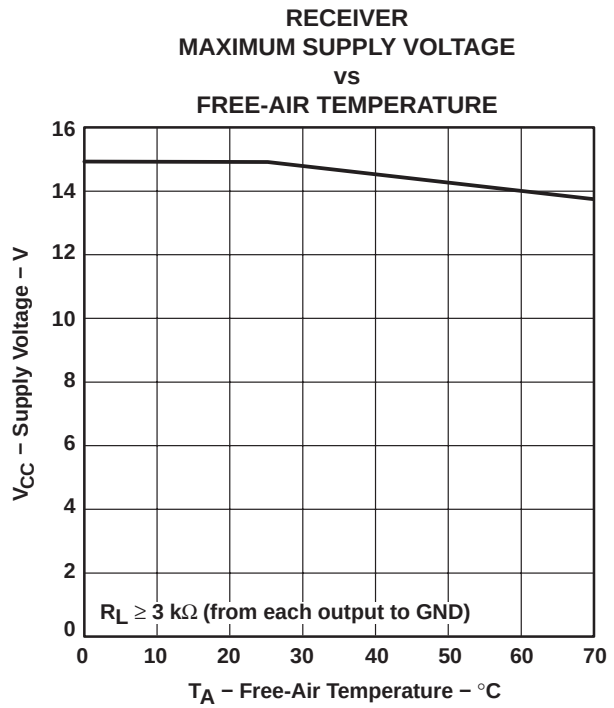


Figure 14

APPLICATION INFORMATION

Diodes placed in series with the V_{DD} and V_{SS} leads protect the TL145406 during the fault condition in which the device outputs are shorted to ±15 V and the power supplies are at low. Diodes also provide low-impedance paths to ground (see Figure 15).

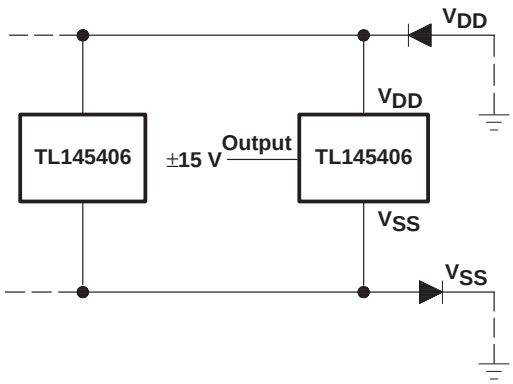


Figure 15. Power-Supply Protection to Meet Power-Off Fault Conditions of ANSI TIA/EIA-232-F

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL145406DW	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL145406
TL145406DW.A	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL145406
TL145406DWR	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL145406
TL145406DWR.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL145406
TL145406N	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL145406N
TL145406N.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL145406N

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

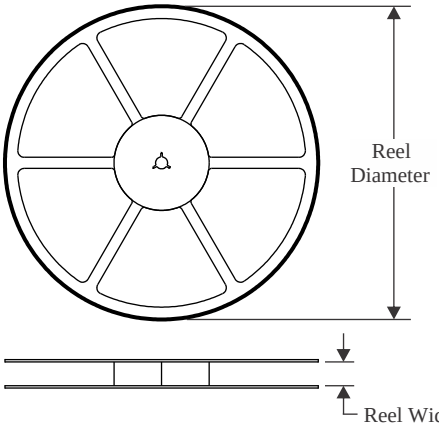
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

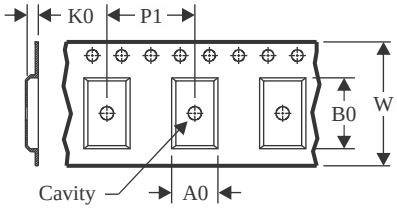
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

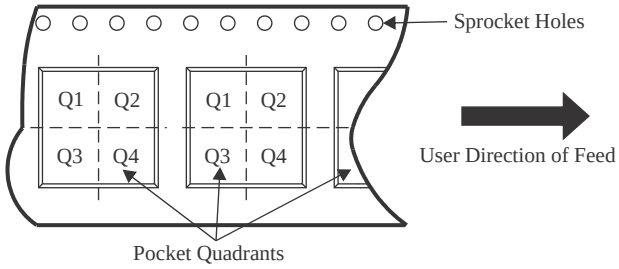


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

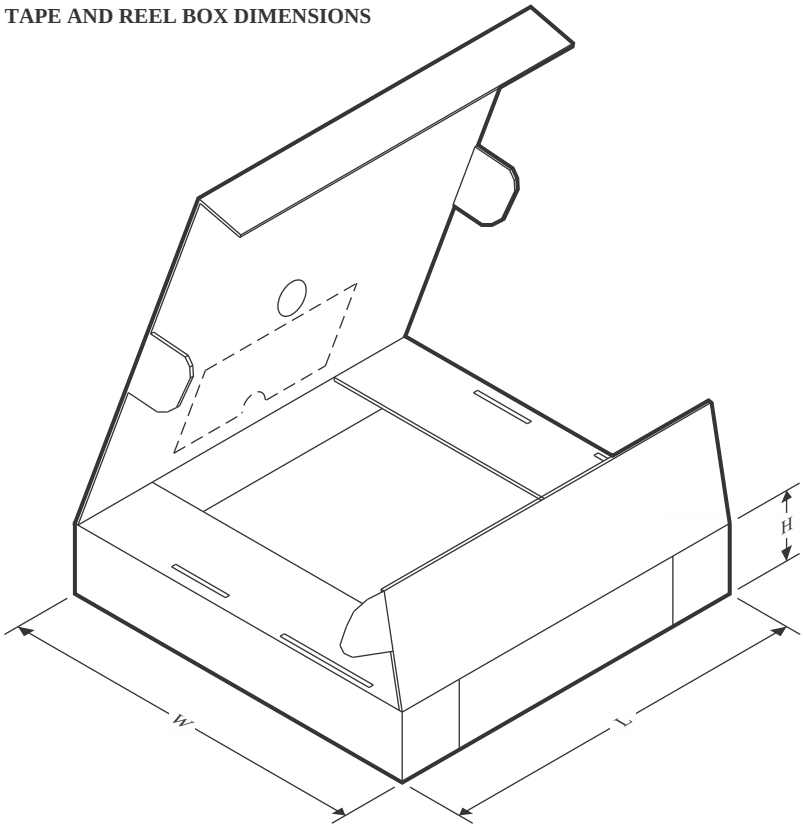
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL145406DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

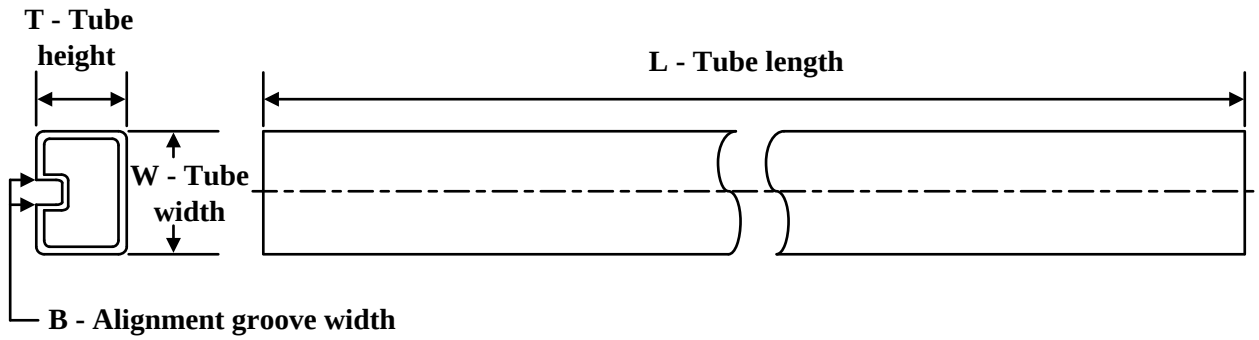
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL145406DWR	SOIC	DW	16	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TL145406DW	DW	SOIC	16	40	506.98	12.7	4826	6.6
TL145406DW.A	DW	SOIC	16	40	506.98	12.7	4826	6.6
TL145406N	N	PDIP	16	25	506	13.97	11230	4.32
TL145406N.A	N	PDIP	16	25	506	13.97	11230	4.32

GENERIC PACKAGE VIEW

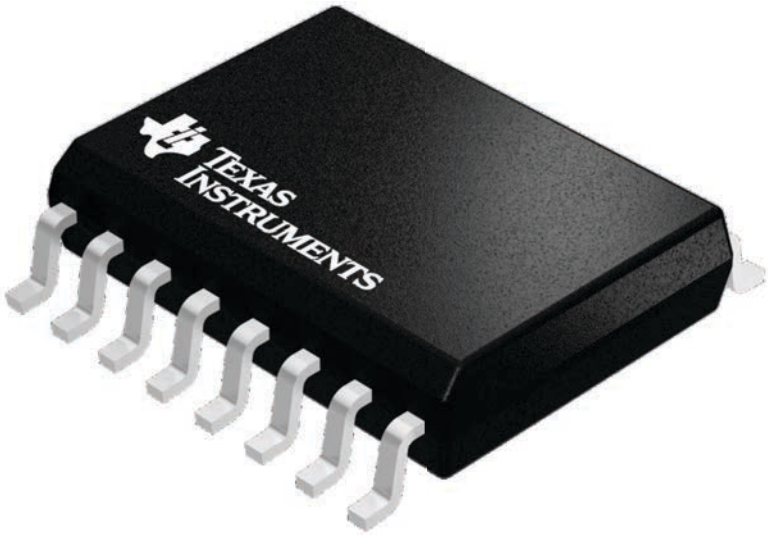
DW 16

SOIC - 2.65 mm max height

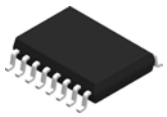
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

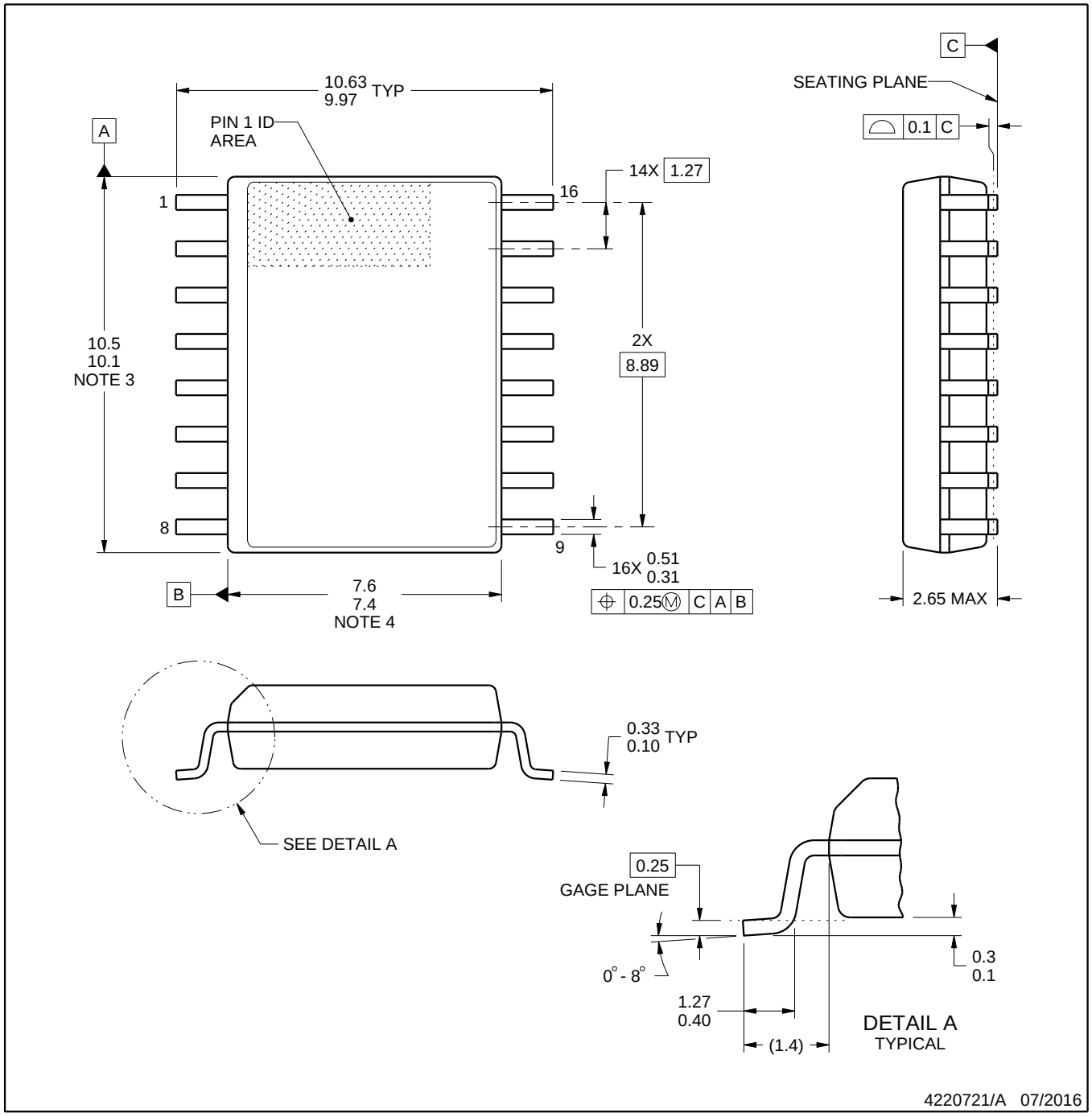


PACKAGE OUTLINE

DW0016A

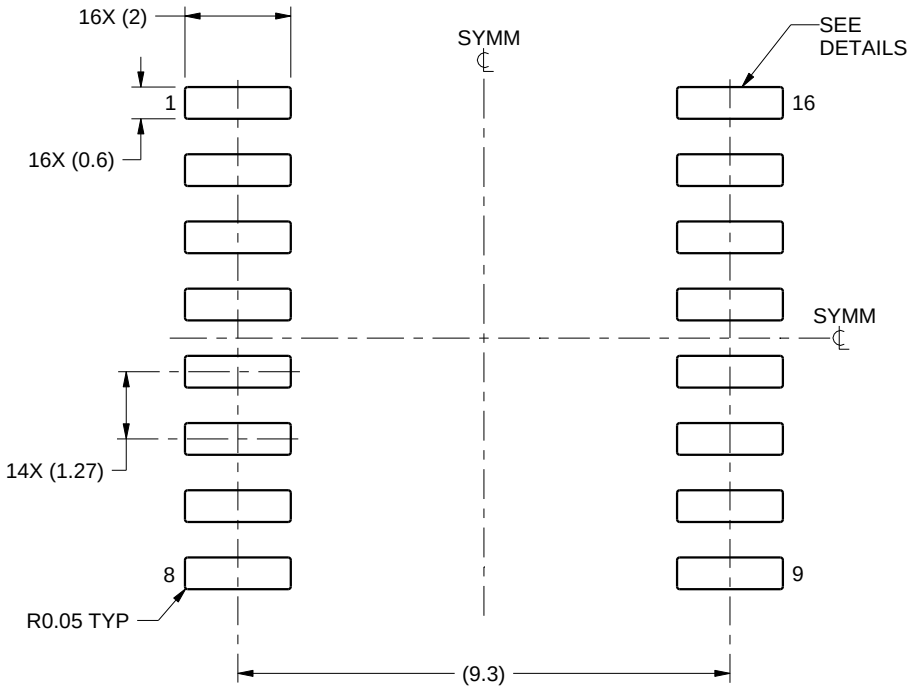
SOIC - 2.65 mm max height

SOIC

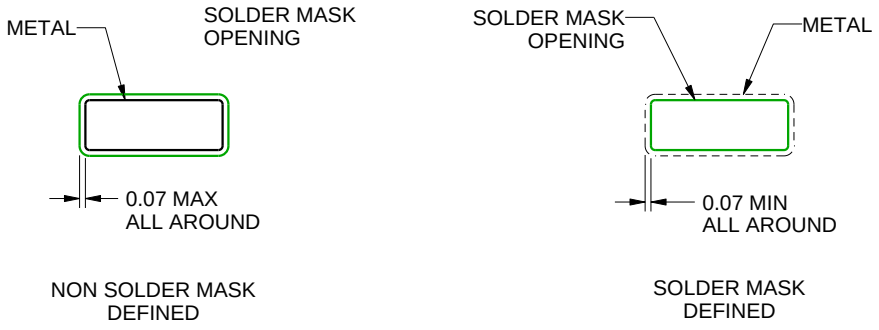


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

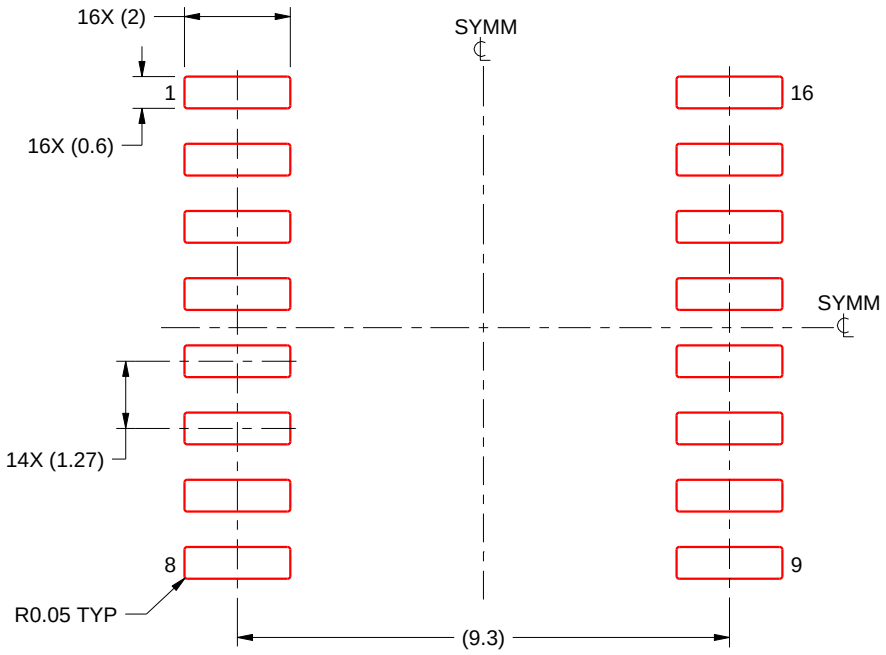


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

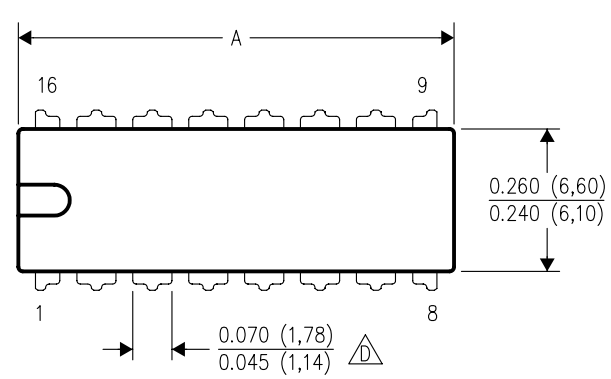
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

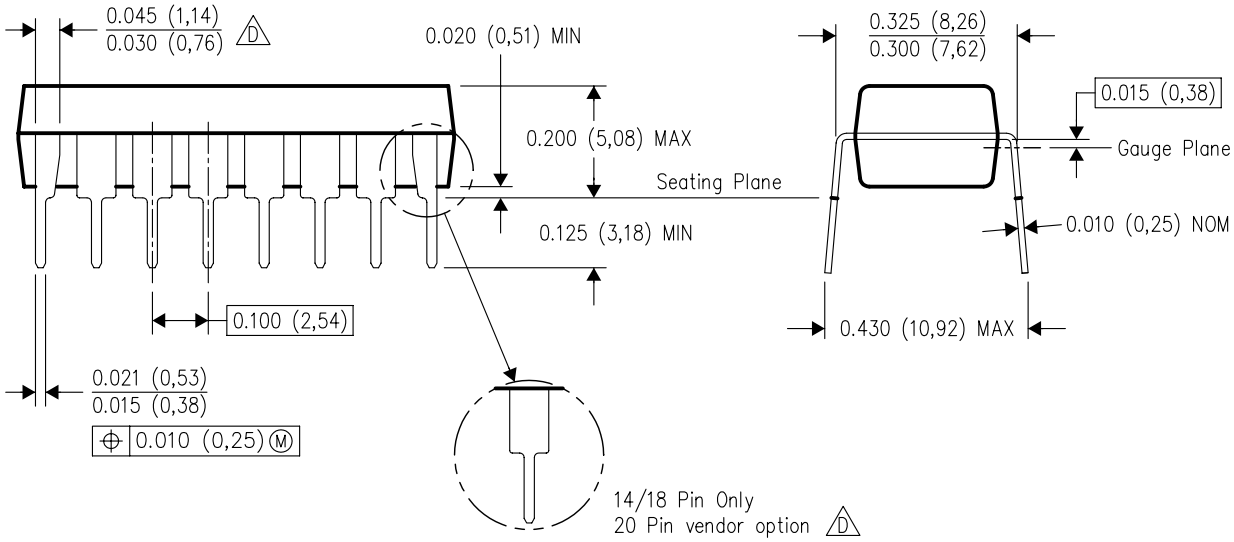
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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