TLC591x 8-Channel Constant-Current LED Sink Drivers

1 Features

- Eight Constant-Current Output Channels
- Output Current Adjusted Through Single External Resistor
- Constant Output Current Range: 3-mA to 120-mA per Channel
- Constant Output Current Invariant to Load Voltage Change
- Open Load, Short Load and Overtemperature Detection
- 256-Step Programmable Global Current Gain
- Excellent Output Current Accuracy:
  - Between Channels: < ±3% (Maximum)
  - Between ICs: < ±6% (Maximum)
- Fast Response of Output Current
- 30-MHz Clock Frequency
- Schmitt-Trigger Input
- 3.3-V or 5-V Supply Voltage
- Maximum LED Voltage 20-V
- Thermal Shutdown for Overtemperature Protection

2 Applications

- General LED Lighting Applications
- LED Display Systems
- LED Signage
- Automotive LED Lighting
- White Goods
- Gaming Machines/Entertainment

3 Description

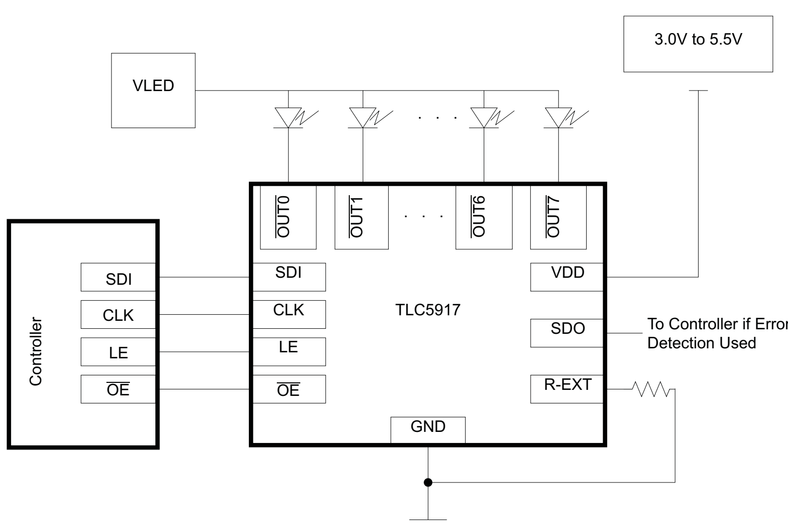
The TLC591x Constant-Current LED Sink Drivers are designed to work alone or cascaded. Since each output is independently controlled, they can be programmed to be on or off by the user. The high LED voltage (VLED) allows for the use of a single LED per output or multiple LEDs on a single string. With independently controlled outputs supplied with constant current, the LEDs can be combined in parallel to create higher currents on a single string. The constant sink current for all channels is set through a single external resistor. This allows different LED drivers in the same application to sink various currents which provides optional implementation of multi-color LEDs. An additional advantage of the independent outputs is the ability to leave unused channels floating. The flexibility of the TLC591x LED drivers is ideal for applications such as (but not limited to): 7-segment displays, scrolling single color displays, gaming machines, white goods, video billboards and video panels.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLC5916	SOIC (16)	9.90 mm × 3.91 mm
	PDIP (16)	19.30 mm × 6.35 mm
	TSSOP (16)	5.00 mm × 4.40 mm
TLC5917	SOIC (16)	9.90 mm × 3.91 mm
	PDIP (16)	19.30 mm × 6.35 mm
	TSSOP (16)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Single Implementation of TLC5916 / TLC5917 Device



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (February 2011) to Revision D — **Page**

- Added *Pin Configuration and Functions* section, *ESD Rating*s table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1

Changes from Revision B (February 2011) to Revision C — **Page**

- Replaced the Power Dissipation and Thermal Impedance table with the Thermal Information tables 4

Changes from Revision A (November 2010) to Revision B — **Page**

- Added Maximum LED Voltage 20-V to Features. 1
- Added Abstract section. 1
- Changed resistor value in Single Implementation diagram from 840Ω to 720Ω. 13
- Changed Default Relationship Curve to reflect correct data. 21
- Changed resistor value in Cascading Implementation diagram from 840Ω to 720Ω. 22
- Changed resistor value in Single Implementation diagram from 840Ω to 720Ω. 24

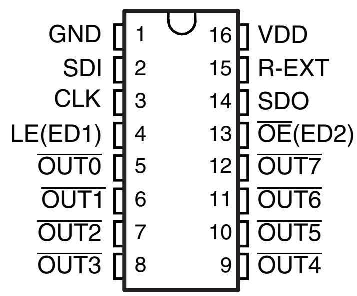
5 Device Comparison Table

DEVICE(1)	OVERTEMPERATURE DETECTION	OPEN-LOAD DETECTION	SHORT TO GND DETECTION	SHORT TO V_{LED} DETECTION
TLC5916	X	X	X	—
TLC5917	X	X	X	X

(1) The device has one single error register for all these conditions (one error bit per channel).

6 Pin Configuration and Functions

16-PIN
D, N, OR PW PACKAGE
(TOP VIEW)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CLK	3	I	Clock input for data shift on rising edge
GND	1	–	Ground for control logic and current sink
LE(ED1)	4	I	Data strobe input Serial data is transferred to the respective latch when LE(ED1) is high. The data is latched when LE(ED1) goes low. Also, a control signal input for an Error Detection Mode and Current Adjust Mode (see Timing Diagram). LE(ED1) has an internal pulldown.
$\overline{OE}$(ED2)	13	I	Output enable. When $\overline{OE}$(ED2) is active (low), the output drivers are enabled; when $\overline{OE}$(ED2) is high, all output drivers are turned OFF (blanked). Also, a control signal input for an Error Detection Mode and Current Adjust Mode (see Figure 11). $\overline{OE}$(ED2) has an internal pullup.
$\overline{OUT0}$ to $\overline{OUT7}$	5 to 12	O	Constant-current outputs
R-EXT	15	I	External Resistor - Connect an external resistor to ground to set the current for all outputs
SDI	2	I	Serial-data input to the Shift register
SDO	14	O	Serial-data output to the following SDI of next driver IC or to the microcontroller
VDD	16	I	Supply voltage

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD}	Supply voltage	0	7	V
V_I	Input voltage	–0.4	V_{DD} + 0.4	V
V_O	Output voltage	–0.5	20	V
f_{clk}	Clock frequency		25	MHz
I_{OUT}	Output current		120	mA
I_{GND}	GND terminal current		960	mA
T_A	Operating free-air temperature	–40	125	°C
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

				MIN	MAX	UNIT
V_{DD}	Supply voltage			3	5.5	V
V_O	Supply voltage to output pins	$\overline{\text{OUT0}}$–$\overline{\text{OUT7}}$			20	V
I_O	Output current	DC test circuit	$V_O \geq 0.6$ V	3		mA
			$V_O \geq 1$ V		120	
I_{OH}	High-level output current source	SDO shorted to GND		–1		mA
I_{OL}	Low-level output current sink	SDO shorted to V_{CC}		1		mA
V_{IH}	High-level input voltage	CLK, $\overline{\text{OE}}$(ED2), LE(ED1), and SDI		0.7 × V_{DD}	V_{DD}	V
V_{IL}	Low-level input voltage	CLK, $\overline{\text{OE}}$(ED2), LE(ED1), and SDI		0	0.3 × V_{DD}	V

7.4 Thermal Information

THERMAL METRIC(1)		TLC5916			TLC5917			UNIT
		16 PINS			16 PINS			
		D	N	PW	D	N	PW	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	87.4	51.8	113.9	87.4	51.8	114.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48.1	39.1	35.2	48.1	39.1	35.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	44.4	31.8	59.2	44.4	31.8	59.8	
ψ_{JT}	Junction-to-top characterization parameter	12.5	23.9	1.3	12.5	23.9	1.3	
ψ_{JB}	Junction-to-board characterization parameter	44.2	31.7	58.5	44.2	31.7	59.2	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	—	—	—	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics: V_{DD} = 3 V

V_{DD} = 3 V, T_J = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{DD}	Input voltage			3		5.5	V
V_O	Supply voltage to the output pins					20	V
I_O	Output current	V_O ≥ 0.6 V		3			mA
		V_O ≥ 1 V				120	
I_{OH}	High-level output current, source			–1			mA
I_{OL}	Low-level output current, sink			1			mA
V_{IH}	High-level input voltage			0.7 × V_{DD}		V_{DD}	V
V_{IL}	Low-level input voltage			GND		0.3 × V_{DD}	V
I_{leak}	Output leakage current	V_{OH} = 17 V	T_J = 25°C			0.5	μA
			T_J = 125°C			2	
V_{OH}	High-level output voltage	SDO, I_{OL} = –1 mA		V_{DD} – 0.4			V
V_{OL}	Low-level output voltage	SDO, I_{OH} = 1 mA				0.4	V
$I_{O(1)}$	Output current 1	V_{OUT} = 0.6 V, R_{ext} = 720 Ω, CG = 0.992			26		mA
	Output current error, die-die	I_{OL} = 26 mA, V_O = 0.6 V, R_{ext} = 720 Ω, T_J = 25°C			±3%	±6%	
	Output current skew, channel-to-channel	I_{OL} = 26 mA, V_O = 0.6 V, R_{ext} = 720 Ω, T_J = 25°C			±1.5%	±3%	
$I_{O(2)}$	Output current 2	V_O = 0.8 V, R_{ext} = 360 Ω, CG = 0.992			52		mA
	Output current error, die-die	I_{OL} = 52 mA, V_O = 0.8 V, R_{ext} = 360 Ω, T_J = 25°C			±2%	±6%	
	Output current skew, channel-to-channel	I_{OL} = 52 mA, V_O = 0.8 V, R_{ext} = 360 Ω, T_J = 25°C			±1.5%	±3%	
I_{OUT} vs V_{OUT}	Output current vs output voltage regulation	V_O = 1 V to 3 V, I_O = 26 mA			±0.1		%/V
		V_{DD} = 3.0 V to 5.5 V, I_O = 26 mA/120 mA			±1		
	Pullup resistance	$\overline{OE}$(ED2)			500		kΩ
	Pulldown resistance	LE(ED1)			500		kΩ
T_{sd}	Overtemperature shutdown(2)			150	175	200	°C
T_{hys}	Restart temperature hysteresis(2)				15		°C
$I_{OUT,Th}$	Threshold current for open error detection	$I_{OUT,target}$ = 3 mA to 120 mA			0.5 × I_{target} %		
$V_{OUT,TTh}$	Trigger threshold voltage for short-error detection (TLC5917 only)	$I_{OUT,target}$ = 3 mA to 120 mA		2.5	2.7	3.1	V
$V_{OUT,RTh}$	Return threshold voltage for short-error detection (TLC5917 only)	$I_{OUT,target}$ = 3 mA to 120 mA		2.2			V
I_{DD}	Supply current	R_{ext} = Open			5	10	mA
		R_{ext} = 720 Ω			8	14	
		R_{ext} = 360 Ω			11	18	
		R_{ext} = 180 Ω			16	22	

(1) Typical values represent the likely parametric nominal values determined at the time of characterization. Typical values depend on the application and configuration and may vary over time. Typical values are not ensured on production material.
(2) Specified by design.

7.6 Electrical Characteristics: V_{DD} = 5.5 V

V_{DD} = 5.5 V, T_J = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP[(1)]	MAX	UNIT
V_{DD}	Input voltage			3		5.5	V
V_O	Supply voltage to the output pins					20	V
I_O	Output current	$V_O \geq 0.6$ V		3			mA
		$V_O \geq 1$ V				120	mA
I_{OH}	High-level output current, source			–1			mA
I_{OL}	Low-level output current, sink			1			mA
V_{IH}	High-level input voltage			0.7 × V_{DD}		V_{DD}	V
V_{IL}	Low-level input voltage			GND		0.3 × V_{DD}	V
I_{leak}	Output leakage current	V_{OH} = 17 V	T_J = 25°C			0.5	µA
			T_J = 125°C			2	µA
V_{OH}	High-level output voltage	SDO, I_{OL} = –1 mA		V_{DD} – 0.4			V
V_{OL}	Low-level output voltage	SDO, I_{OH} = 1 mA				0.4	V
$I_{O(1)}$	Output current 1	V_{OUT} = 0.6 V, R_{ext} = 720 Ω, CG = 0.992			26		mA
	Output current error, die-die	I_{OL} = 26 mA, V_O = 0.6 V, R_{ext} = 720 Ω, T_J = 25°C			±3%	±6%	
	Output current skew, channel-to-channel	I_{OL} = 26 mA, V_O = 0.6 V, R_{ext} = 720 Ω, T_J = 25°C			±1.5%	±3%	
$I_{O(2)}$	Output current 2	V_O = 0.8 V, R_{ext} = 360 Ω, CG = 0.992			52		mA
	Output current error, die-die	I_{OL} = 52 mA, V_O = 0.8 V, R_{ext} = 360 Ω, T_J = 25°C			±2%	±6%	
	Output current skew, channel-to-channel	I_{OL} = 52 mA, V_O = 0.8 V, R_{ext} = 360 Ω, T_J = 25°C			±1.5%	±3%	
I_{OUT} vs V_{OUT}	Output current vs output voltage regulation	V_O = 1 V to 3 V , I_O = 26 mA			±0.1		%/V
		V_{DD} = 3.0 V to 5.5 V, I_O = 26 mA/120 mA			±1		%/V
	Pullup resistance	$\overline{OE}$(ED2),			500		kΩ
	Pulldown resistance	LE(ED1),			500		kΩ
T_{sd}	Overtemperature shutdown[(2)]			150	175	200	°C
T_{hys}	Restart temperature hysteresis[(2)]				15		°C
$I_{OUT,Th}$	Threshold current for open error detection	$I_{OUT,target}$ = 3 mA to 120 mA			0.5 × I_{target}%		
$V_{OUT,TTh}$	Trigger threshold voltage for short-error detection (TLC5917 only)	$I_{OUT,target}$ = 3 mA to 120 mA		2.5	2.7	3.1	V
$V_{OUT,RTh}$	Return threshold voltage for short-error detection (TLC5917 only)	$I_{OUT,target}$ = 3 mA to 120 mA		2.2			V
I_{DD}	Supply current	R_{ext} = Open			6	10	mA
		R_{ext} = 720 Ω			11	14	mA
		R_{ext} = 360 Ω			13	18	mA
		R_{ext} = 180 Ω			19	24	mA

(1) Typical values represent the likely parametric nominal values determined at the time of characterization. Typical values depend on the application and configuration and may vary over time. Typical values are not ensured on production material.
(2) Specified by design.

7.7 Switching Characteristics: V_{DD} = 3 V

V_{DD} = 3 V, T_J = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH1}	Low-to-high propagation delay time, CLK to $\overline{OUTn}$	$V_{IH} = V_{DD}$, V_{IL} = GND, R_{ext} = 360 Ω, V_L = 4 V, R_L = 44 Ω, C_L = 10 pF, CG = 0.992	40	65	95	ns
t_{PLH2}	Low-to-high propagation delay time, LE(ED1) to $\overline{OUTn}$		40	65	95	ns
t_{PLH3}	Low-to-high propagation delay time, $\overline{OE}$(ED2) to $\overline{OUTn}$		40	65	95	ns
t_{PLH4}	Low-to-high propagation delay time, CLK to SDO		12	20	30	ns
t_{PHL1}	High-to-low propagation delay time, CLK to $\overline{OUTn}$			300	365	ns
t_{PHL2}	High-to-low propagation delay time, LE(ED1) to $\overline{OUTn}$			300	365	ns
t_{PHL3}	High-to-low propagation delay time, $\overline{OE}$(ED2) to $\overline{OUTn}$			300	365	ns
t_{PHL4}	High-to-low propagation delay time, CLK to SDO		12	20	30	ns
$t_{w(CLK)}$	Pulse duration, CLK		20			ns
$t_{w(L)}$	Pulse duration, LE(ED1)		20			ns
$t_{w(OE)}$	Pulse duration, $\overline{OE}$(ED2)		500			ns
$t_{w(ED2)}$	Pulse duration, $\overline{OE}$(ED2) in Error Detection Mode		2			μs
$t_{h(ED1,ED2)}$	Hold time, LE(ED1) and $\overline{OE}$(ED2)		10			ns
$t_{h(D)}$	Hold time, SDI		2			ns
$t_{su(D,ED1)}$	Setup time, SDI, LE(ED1)		3			ns
$t_{su(ED2)}$	Setup time, $\overline{OE}$(ED2)		8.5			ns
$t_{h(L)}$	Hold time, LE(ED1), Normal Mode		15			ns
$t_{su(L)}$	Setup time, LE(ED1), Normal Mode		15			ns
t_r	Rise time, CLK(2)				500	ns
t_f	Fall time, CLK(2)				500	ns
t_{or}	Rise time, outputs (off)		40	85	105	ns
t_{or}	Rise time, outputs (off), T_J = 25°C			83	100	ns
t_{of}	Rise time, outputs (on)		100	280	370	ns
t_{of}	Rise time, outputs (on), T_J = 25°C			170	225	ns
f_{CLK}	Clock frequency	Cascade operation			30	MHz

(1) Typical values represent the likely parametric nominal values determined at the time of characterization. Typical values depend on the application and configuration and may vary over time. Typical values are not ensured on production material.
(2) If the devices are connected in cascade and t_r or t_f is large, it may be critical to achieve the timing required for data transfer between two cascaded devices.

7.8 Switching Characteristics: V_{DD} = 5.5 V

V_{DD} = 5.5 V, T_J = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH1}	Low-to-high propagation delay time, CLK to $\overline{OUTn}$	$V_{IH} = V_{DD}$, V_{IL} = GND, R_{ext} = 360 Ω, V_L = 4 V, R_L = 44 Ω, C_L = 10 pF, CG = 0.992	40	65	95	ns
t_{PLH2}	Low-to-high propagation delay time, LE(ED1) to $\overline{OUTn}$		40	65	95	ns
t_{PLH3}	Low-to-high propagation delay time, $\overline{OE}$(ED2) to $\overline{OUTn}$		40	65	95	ns
t_{PLH4}	Low-to-high propagation delay time, CLK to SDO		8	20	30	ns
t_{PHL1}	High-to-low propagation delay time, CLK to $\overline{OUTn}$			300	365	ns
t_{PHL2}	High-to-low propagation delay time, LE(ED1) to $\overline{OUTn}$			300	365	ns
t_{PHL3}	High-to-low propagation delay time, $\overline{OE}$(ED2) to $\overline{OUTn}$			300	365	ns
t_{PHL4}	High-to-low propagation delay time, CLK to SDO		8	20	30	ns
$t_{w(CLK)}$	Pulse duration, CLK		20			ns
$t_{w(L)}$	Pulse duration, LE(ED1)		20			ns
$t_{w(OE)}$	Pulse duration, $\overline{OE}$(ED2)		500			ns
$t_{w(ED2)}$	Pulse duration, $\overline{OE}$(ED2) in Error Detection Mode		2			μs
$t_{h(D,ED1,ED2)}$	Hold time, SDI, LE(ED1), and $\overline{OE}$(ED2)		10			ns
$t_{h(D)}$	Hold time, SDI		2			ns
$t_{su(D,ED1)}$	Setup time, SDI, LE(ED1)		3			ns
$t_{su(ED2)}$	Setup time, $\overline{OE}$(ED2)		8.5			ns
$t_{h(L)}$	Hold time, LE(ED1), Normal Mode		15			ns
$t_{su(L)}$	Setup time, LE(ED1), Normal Mode		15			ns
t_r	Rise time, CLK(2)				500	ns
t_f	Fall time, CLK(2)				500	ns
t_{or}	Rise time, outputs (off)		40	85	105	ns
t_{or}	Rise time, outputs (off), T_J = 25°C			83	100	ns
t_{of}	Rise time, outputs (on)		100	280	370	ns
t_{of}	Rise time, outputs (on), T_J = 25°C			170	225	ns
f_{CLK}	Clock frequency	Cascade operation			30	MHz

(1) Typical values represent the likely parametric nominal values determined at the time of characterization. Typical values depend on the application and configuration and may vary over time. Typical values are not ensured on production material.
(2) If the devices are connected in cascade and t_r or t_f is large, it may be critical to achieve the timing required for data transfer between two cascaded devices.

7.9 Timing Requirements

V_{DD} = 3 V to 5.5 V (unless otherwise noted)

			MIN	MAX	UNIT
$t_{w(L)}$	LE(ED1) pulse duration	Normal Mode	20		ns
$t_{w(CLK)}$	CLK pulse duration	Normal Mode	20		ns
$t_{w(OE)}$	$\overline{\text{OE}}$(ED2) pulse duration	Normal Mode, I_{OUT} < 60 mA	500		ns
		Normal Mode, I_{OUT} > 60 mA	700		
$t_{su(D)}$	Setup time for SDI	Normal Mode	3		ns
$t_{h(D)}$	Hold time for SDI	Normal Mode	2		ns
$t_{su(L)}$	Setup time for LE(ED1)	Normal Mode	15		ns
$t_{h(L)}$	Hold time for LE(ED1)	Normal Mode	15		ns
$t_{w(CLK)}$	CLK pulse duration	Error Detection Mode	20		ns
$t_{w(ED2)}$	$\overline{\text{OE}}$(ED2) pulse duration	Error Detection Mode	2000		ns
$t_{su(ED1)}$	Setup time for LE(ED1)	Error Detection Mode	4		ns
$t_{h(ED1)}$	Hold time for LE(ED1)	Error Detection Mode	10		ns
$t_{su(ED2)}$	Setup time for $\overline{\text{OE}}$(ED2)	Error Detection Mode	6		ns
$t_{h(ED2)}$	Hold time for $\overline{\text{OE}}$(ED2)	Error Detection Mode	10		ns
f_{CLK}	Clock frequency	Cascade operation		30	MHz

7.10 Typical Characteristics

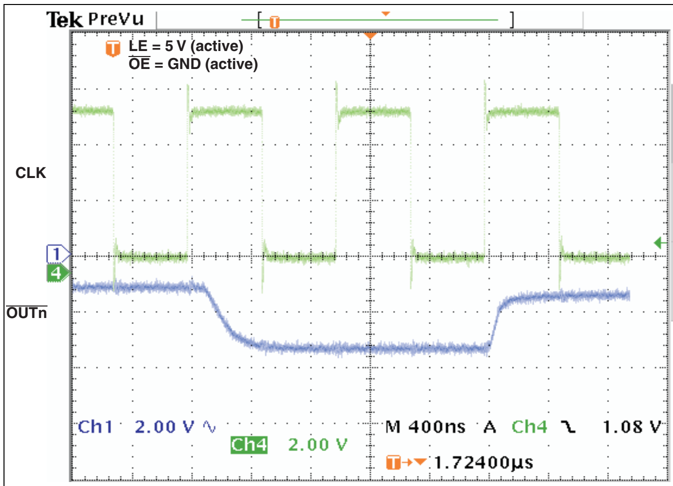


Figure 1. Response Time, CLK to $\overline{\text{OUTn}}$

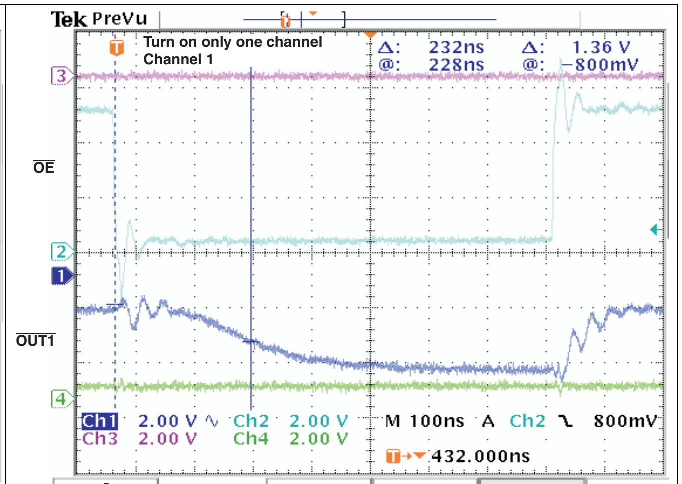


Figure 2. Response Time, $\overline{\text{OE}}$ to $\overline{\text{OUT1}}$

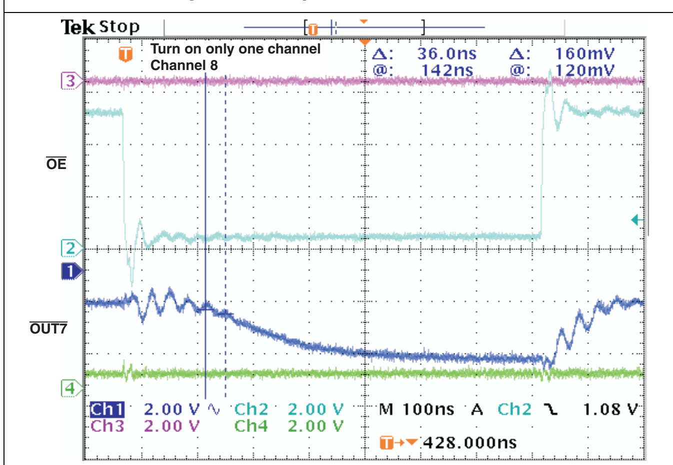


Figure 3. Response Time, $\overline{\text{OE}}$ to $\overline{\text{OUT7}}$

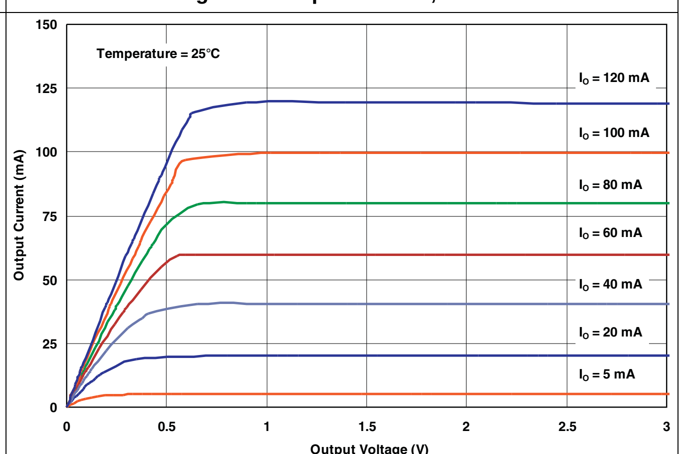


Figure 4. Output Current vs Output Voltage

8 Parameter Measurement Information

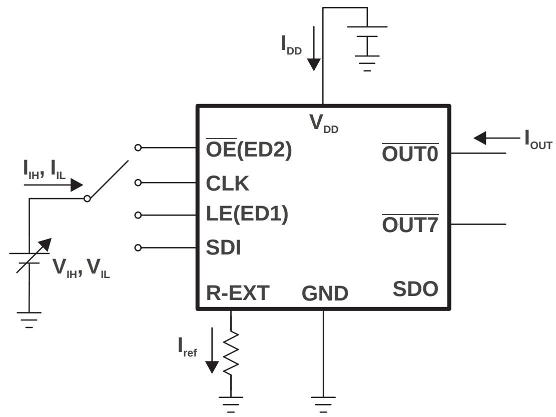


Figure 5. Test Circuit for Electrical Characteristics

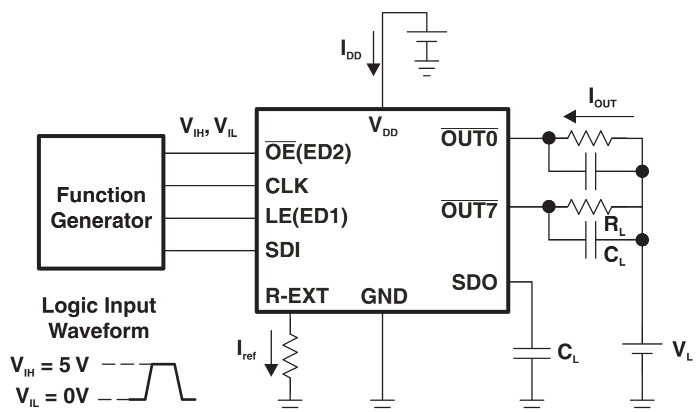


Figure 6. Test Circuit for Switching Characteristics

Parameter Measurement Information (continued)

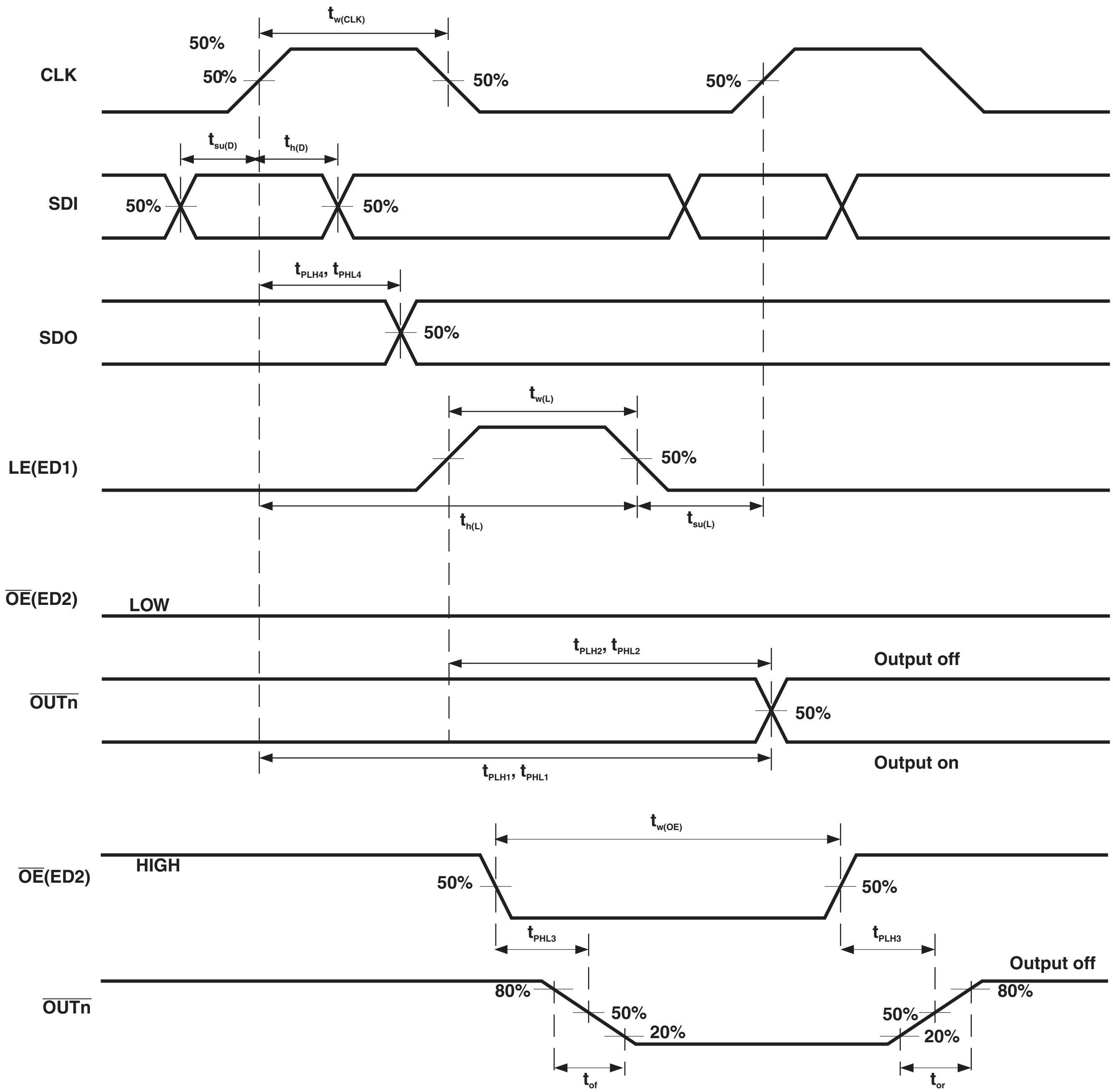


Figure 7. Normal Mode Timing Waveforms

Parameter Measurement Information (continued)

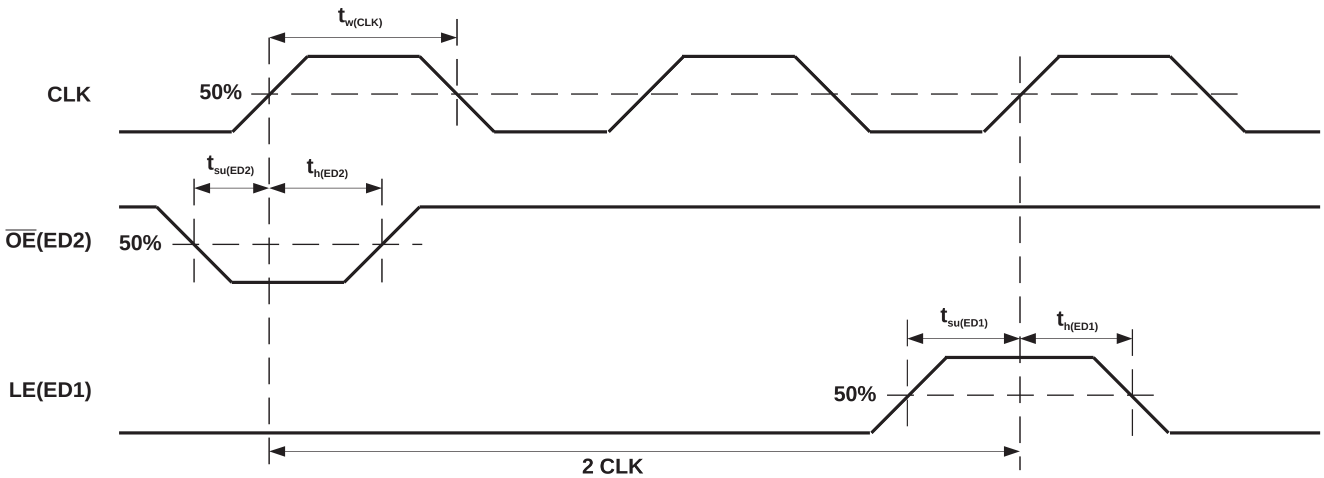


Figure 8. Switching to Special Mode Timing Waveforms

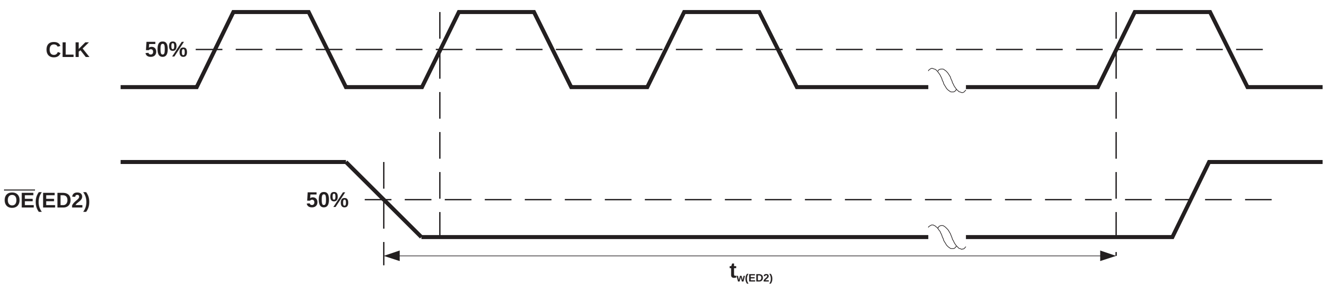


Figure 9. Reading Error Status Code Timing Waveforms

9 Detailed Description

9.1 Overview

The TLC591x is designed for LED displays and LED lighting applications with constant-current control and open-load, shorted-load, and overtemperature detection. The TLC591x contains an 8-bit shift register and data latches, which convert serial input data into parallel output format. At the output stage, eight regulated current ports are designed to provide uniform and constant current for driving LEDs within a wide range of LED Forward Voltage (VF) variations. Used in system design for LED display applications, for example, LED panels, it provides great flexibility and device performance. Users can adjust the output current from 3 mA to 120 mA per channel through an external resistor, R_{ext}, which gives flexibility in controlling the light intensity of LEDs. The devices are designed for up to 20 V at the output port. The high clock frequency, 30 MHz, also satisfies the system requirements of high-volume data transmission.

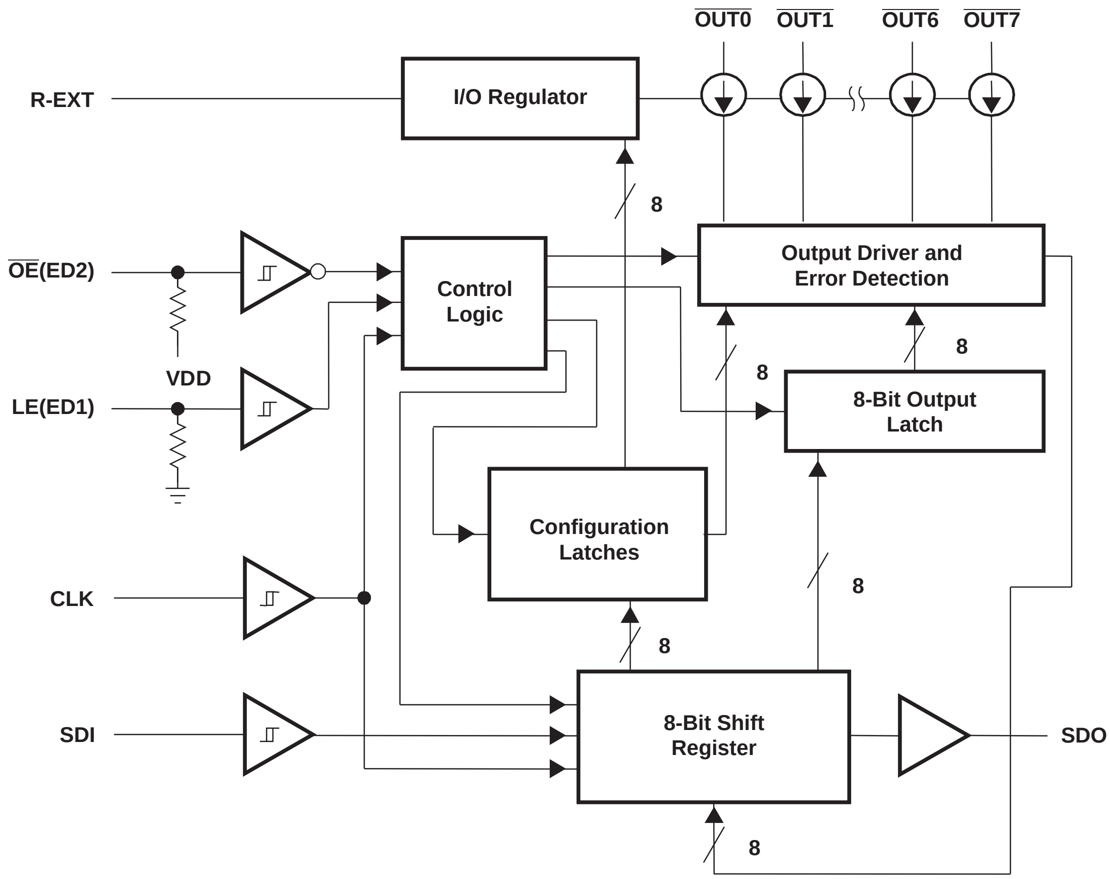
The TLC591x provides two operation modes: Normal Mode and Special Mode. Normal mode is used for shifting LED data into and out of the driver. Special Mode includes two functions: Error Detection and Current Gain Control. The two operation modes include three phases: Normal Mode phase, Mode Switching transition phase, and Special Mode phase. The signal on the multiple function pin $\overline{OE}$(ED2) is monitored to determine the mode. When a one-clock-wide pulse appears on $\overline{OE}$(ED2), the device enters the Mode Switching phase. At this time, the voltage level on LE(ED1) determines which mode the TLC591x switches to.

In the Normal Mode phase, the serial data can be transferred into TLC591x through the pin SDI, shifted in the shift register, and transferred out via the pin SDO. LE(ED1) can latch the serial data in the shift register to the output latch. $\overline{OE}$(ED2) enables the output drivers to sink current.

In the Special Mode phase, the low-voltage-level signal on $\overline{OE}$(ED2) can enable output channels and detect the status of the output current to determine if the driving current level is sufficient. The detected Error Status is loaded into the 8-bit shift register and shifted out via the pin SDO, synchronous to the CLK signal. The system controller can read the error status and determine if the LEDs are properly lit.

In the Special Mode phase, the TLC591x allows users to adjust the output current level by setting a runtime-programmable Configuration Code. The code is sent into the TLC591x through SDI. The positive pulse of LE(ED1) latches the code in the shift register into a built-in 8-bit configuration latch, instead of the output latch. The code affects the voltage at the terminal R-EXT and controls the output-current regulator. The output current can be finely adjusted by a gain ranging from 1/12 to 127/128 in 256 steps. Therefore, the current skew between ICs can be compensated within less than 1%. This feature is suitable for white balancing in LED color display panels.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Open-Circuit Detection Principle

The LED Open-Circuit Detection compares the effective current level I_{out} with the open load detection threshold current $I_{OUT,Th}$. If I_{OUT} is below the $I_{OUT,Th}$ threshold, the TLC591x detects an open-load condition. This error status can be read as an error status code in the Special Mode. For open-circuit error detection, a channel must be on.

Table 1. Open-Circuit Detection

STATE OF OUTPUT PORT	CONDITION OF OUTPUT CURRENT	ERROR STATUS CODE	MEANING
Off	I_{OUT} = 0 mA	0	Detection not possible
On	$I_{OUT} < I_{OUT,Th}$ (1)	0	Open circuit
	$I_{OUT} \geq I_{OUT,Th}$ (1)	Channel n error status bit 1	Normal

(1) $I_{OUT,Th} = 0.5 \times I_{OUT,target}$ (typical)

9.3.2 Short-Circuit Detection Principle (TLC5917 Only)

The LED short-circuit detection compares the effective voltage level (V_{OUT}) with the shorted-load detection threshold voltages $V_{OUT,TTh}$ and $V_{OUT,RTh}$. If V_{OUT} is above the $V_{OUT,TTh}$ threshold, the TLC5917 detects an shorted-load condition. If V_{OUT} is below the $V_{OUT,RTh}$ threshold, no error is detected/error bit is reset. This error status can be read as an error status code in the Special Mode. For short-circuit error detection, a channel must be on.

Table 2. Shorted-Load Detection

STATE OF OUTPUT PORT	CONDITION OF OUTPUT VOLTAGE	ERROR STATUS CODE	MEANING
Off	I_{OUT} = 0 mA	0	Detection not possible
On	$V_{OUT} \geq V_{OUT,TTh}$	0	Short circuit
	$V_{OUT} < V_{OUT,RTh}$	1	Normal

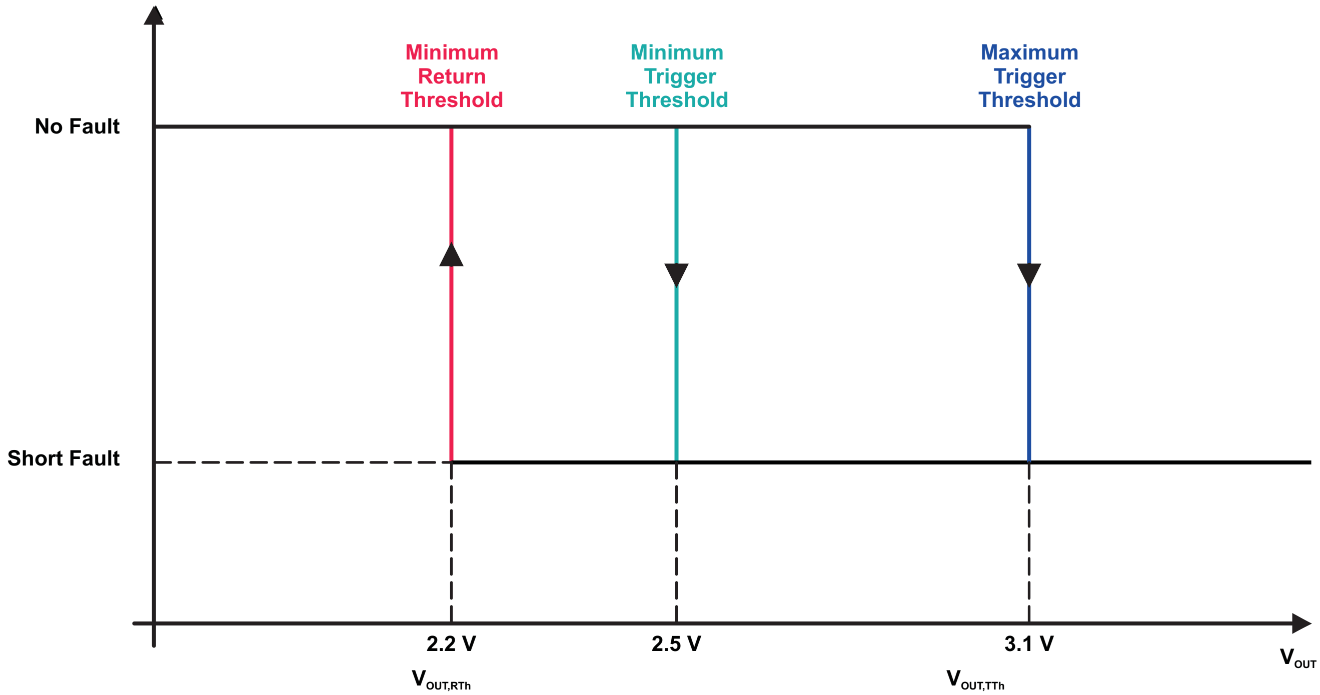


Figure 10. Short-Circuit Detection Principle

9.3.3 Overtemperature Detection and Shutdown

TLC591x is equipped with a global overtemperature sensor and eight individual, channel-specific, overtemperature sensors.

- When the global sensor reaches the trip temperature, all output channels are shut down, and the error status is stored in the internal Error Status register of every channel. After shutdown, the channels automatically restart after cooling down, if the control signal (output latch) remains on. The stored error status is not reset after cooling down and can be read out as the error status code in the Special Mode.
- When one of the channel-specific sensors reaches trip temperature, only the affected output channel is shut down, and the error status is stored only in the internal Error Status register of the affected channel. After shutdown, the channel automatically restarts after cooling down, if the control signal (output latch) remains on. The stored error status is not reset after cooling down and can be read out as error status code in the Special Mode.

For channel-specific overtemperature error detection, a channel must be on.

The error status code is reset when TLC591x returns to Normal Mode.

Table 3. Overtemperature Detection(1)

STATE OF OUTPUT PORT	CONDITION	ERROR STATUS CODE	MEANING
Off	I_{OUT} = 0 mA	0	
On On → all channels Off	$T_j < T_{j,trip}$ global	1	Normal
	$T_j > T_{j,trip}$ global	All error status bits = 0	Global overtemperature
On On → Off	$T_j < T_{j,trip}$ channel n	1	Normal
	$T_j > T_{j,trip}$ channel n	Channel n error status bit = 0	Channel n overtemperature

(1) The global shutdown threshold temperature is approximately 170°C.

9.4 Device Functional Modes

The TLC591x provides two operation modes: Normal Mode and Special Mode. Normal mode is used for shifting LED data into and out of the driver. Special Mode includes two functions: Error Detection and Current Gain Control. The two operation modes include three phases: Normal Mode phase, Mode Switching transition phase, and Special Mode phase. The signal on the multiple function pin OE(ED2) is monitored to determine the mode. When a one-clock-wide pulse appears on OE(ED2), the device enters the Mode Switching phase. At this time, the voltage level on LE(ED1) determines which mode the TLC591x switches to.

In the Normal Mode phase, the serial data can be transferred into TLC591x through the pin SDI, shifted in the shift register, and transferred out via the pin SDO. LE(ED1) can latch the serial data in the shift register to the output latch. OE(ED2) enables the output drivers to sink current.

In the Special Mode phase, the low-voltage-level signal on OE(ED2) can enable output channels and detect the status of the output current to determine if the driving current level is sufficient. The detected Error Status is loaded into the 8-bit shift register and shifted out via the pin SDO, synchronous to the CLK signal. The system controller can read the error status and determine if the LEDs are properly lit.

In the Special Mode phase, the TLC591x allows users to adjust the output current level by setting a runtime-programmable Configuration Code. The code is sent into the TLC591x through SDI. The positive pulse of LE(ED1) latches the code in the shift register into a built-in 8-bit configuration latch, instead of the output latch. The code affects the voltage at the terminal R-EXT and controls the output-current regulator. The output current can be finely adjusted by a gain ranging from 1/12 to 127/128 in 256 steps. Therefore, the current skew between ICs can be compensated within less than 1%. This feature is suitable for white balancing in LED color display panels.

Device Functional Modes (continued)

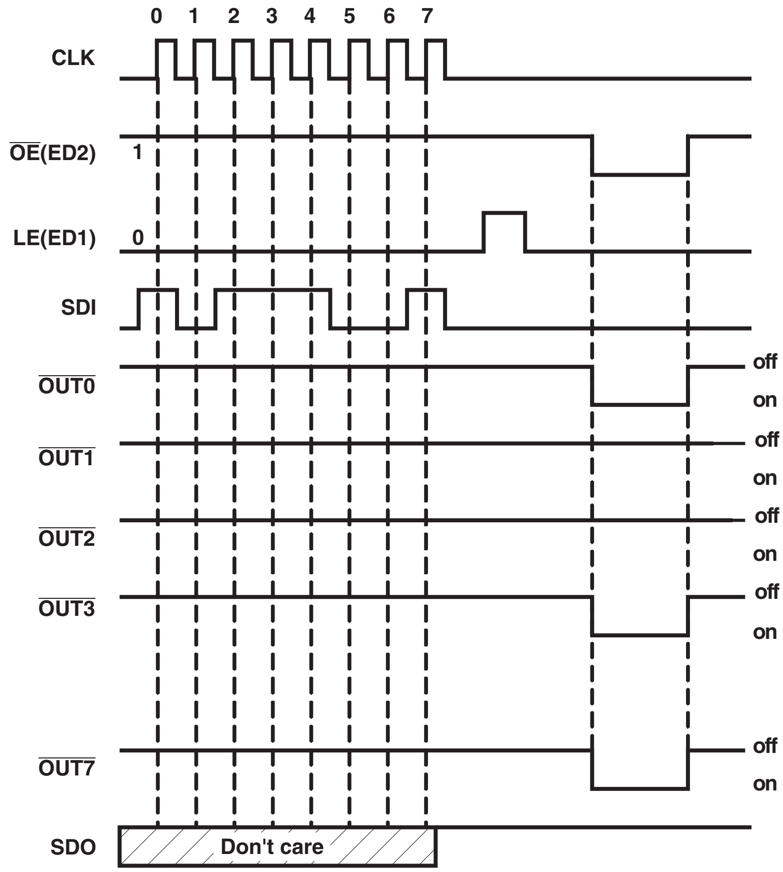


Figure 11. Normal Mode

Table 4. Truth Table in Normal Mode

CLK	LE(ED1)	$\overline{OE}$(ED2)	SDI	$\overline{OUT0}$...$\overline{OUT7}$	SDO
↑	H	L	Dn	Dn...Dn – 7	Dn – 7
↑	L	L	Dn + 1	No change	Dn – 6
↑	H	L	Dn + 2	Dn + 2...Dn – 5	Dn – 5
↓	X	L	Dn + 3	Dn + 2...Dn – 5	Dn – 5
↓	X	H	Dn + 3	Off	Dn – 5

The signal sequence shown in Figure 12 makes the TLC591x enter Current Adjust and Error Detection Mode.

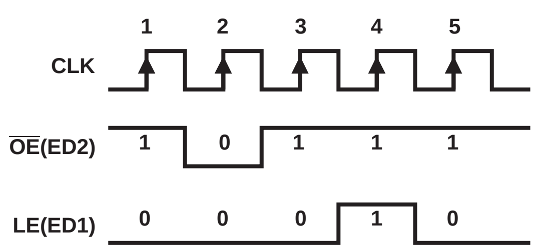


Figure 12. Switching to Special Mode

In the Current Adjust Mode, sending the positive pulse of LE(ED1), the content of the shift register (a current adjust code) is written to the 8-bit configuration latch (see Figure 13).

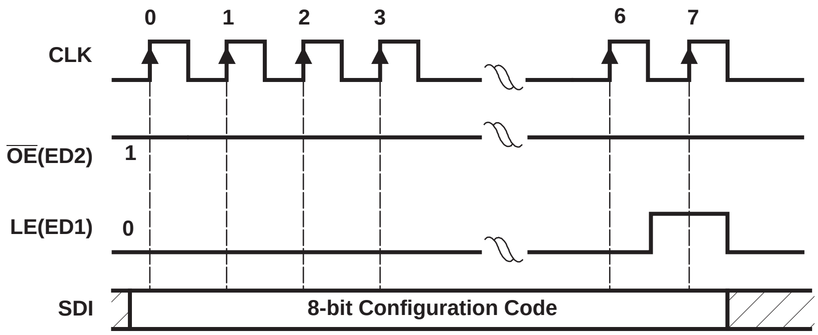


Figure 13. Writing Configuration Code

When the TLC591x is in the Error Detection Mode, the signal sequence shown in Figure 14 enables a system controller to read error status codes through SDO.

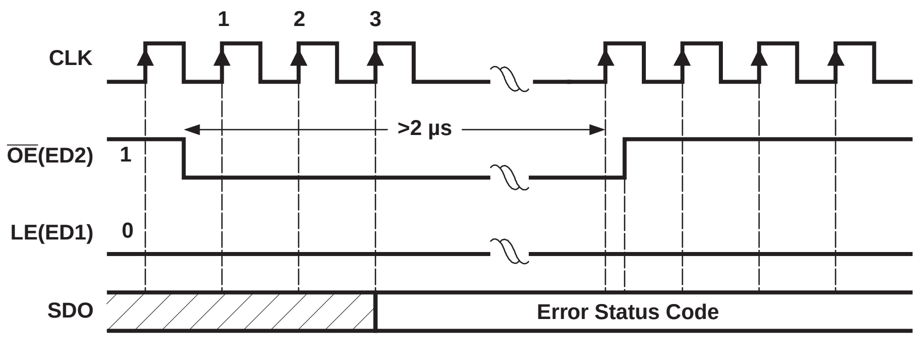


Figure 14. Reading Error Status Code

The signal sequence shown in Figure 15 makes TLC591x resume the Normal Mode. Switching to Normal Mode resets all internal Error Status registers. $\overline{\text{OE}}$(ED2) always enables the output port, whether the TLC591x enters Current Adjust Mode or not.

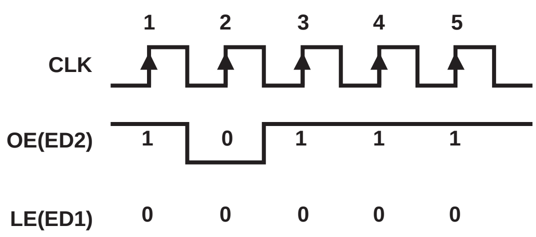


Figure 15. Switching to Normal Mode

9.4.1 Operation Mode Switching

To switch between its two modes, TLC591x monitors the signal $\overline{\text{OE}}$(ED2). When an one-clock-wide pulse of $\overline{\text{OE}}$(ED2) appears, TLC591x enters the two-clock-period transition phase, the Mode Switching phase. After power on, the default operation mode is the Normal Mode (see Figure 16).

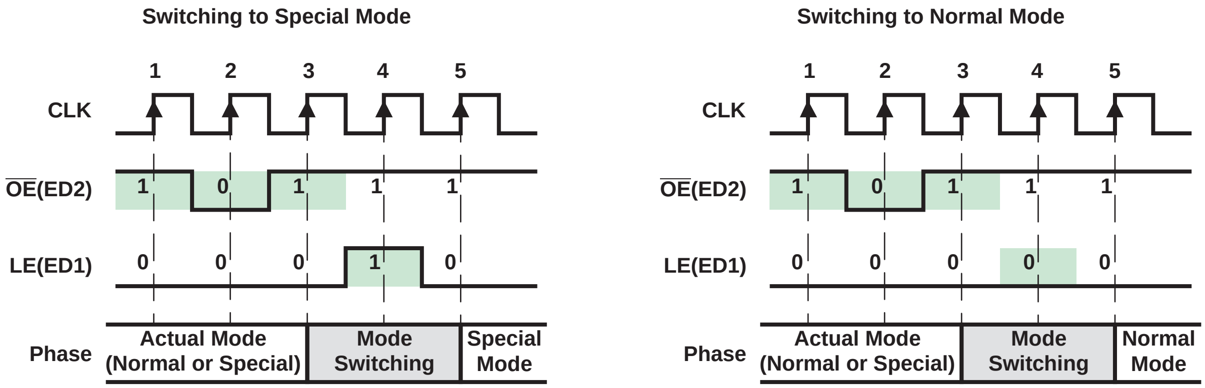


Figure 16. Mode Switching

As shown in Figure 16, once a one-clock-wide short pulse (101) of $\overline{\text{OE}}$(ED2) appears, TLC591x enters the Mode Switching phase. At the fourth rising edge of CLK, if LE(ED1) is sampled as voltage high, TLC591x switches to Special Mode; otherwise, it switches to Normal Mode. The signal LE(ED1) between the third and the fifth rising edges of CLK cannot latch any data. Its level is used only to determine into which mode to switch. However, the short pulse of $\overline{\text{OE}}$(ED2) can still enable the output ports. During mode switching, the serial data can still be transferred through SDI and shifted out from SDO.

NOTE

1. The signal sequence for the mode switching may be used frequently to ensure that TLC591x is in the proper mode.
2. The 1 and 0 on the LE(ED1) signal are sampled at the rising edge of CLK. The X means its level does not affect the result of mode switching mechanism.
3. After power on, the default operation mode is Normal Mode.

9.4.1.1 Normal Mode Phase

Serial data is transferred into TLC591x through SDI, shifted in the Shift Register, and output via SDO. LE(ED1) can latch the serial data in the Shift Register to the Output Latch. $\overline{\text{OE}}$(ED2) enables the output drivers to sink current. These functions differ only as described in Operation Mode Switching, in which case, a short pulse triggers TLC591x to switch the operation mode. However, as long as LE(ED1) is high in the Mode Switching phase, TLC591x remains in the Normal Mode, as if no mode switching occurred.

9.4.1.2 Special Mode Phase

In the Special Mode, as long as $\overline{\text{OE}}$(ED2) is not low, the serial data is shifted to the Shift Register via SDI and shifted out via SDO, as in the Normal Mode. However, there are two differences between the Special Mode and the Normal Mode, as shown in the following sections.

9.4.2 Reading Error Status Code in Special Mode

When $\overline{\text{OE}}$(ED2) is pulled low while in Special Mode, error detection and load error status codes are loaded into the Shift Register, in addition to enabling output ports to sink current. Figure 17 shows the timing sequence for error detection. The 0 and 1 signal levels are sampled at the rising edge of each CLK. At least three zeros must be sampled at the voltage low signal $\overline{\text{OE}}$(ED2). Immediately after the second zero is sampled, the data input source of the Shift Register changes to the 8-bit parallel Error Status Code register, instead of from the serial data on SDI. Normally, the error status codes are generated at least 2 μs after the falling edge of $\overline{\text{OE}}$(ED2). The occurrence of the third or later zero saves the detected error status codes into the Shift Register. Therefore, when $\overline{\text{OE}}$(ED2) is low, the serial data cannot be shifted into TLC591x through SDI. When $\overline{\text{OE}}$(ED2) is pulled high, the data input source of the Shift Register is changed back to SDI. At the same time, the output ports are disabled and the error detection is completed. Then, the error status codes saved in the Shift Register can be shifted out via SDO bit by bit along with CLK, as well as the new serial data can be shifted into TLC591x through SDI.

While in Special Mode, the TLC591x cannot simultaneously transfer serial data and detect LED load error status.

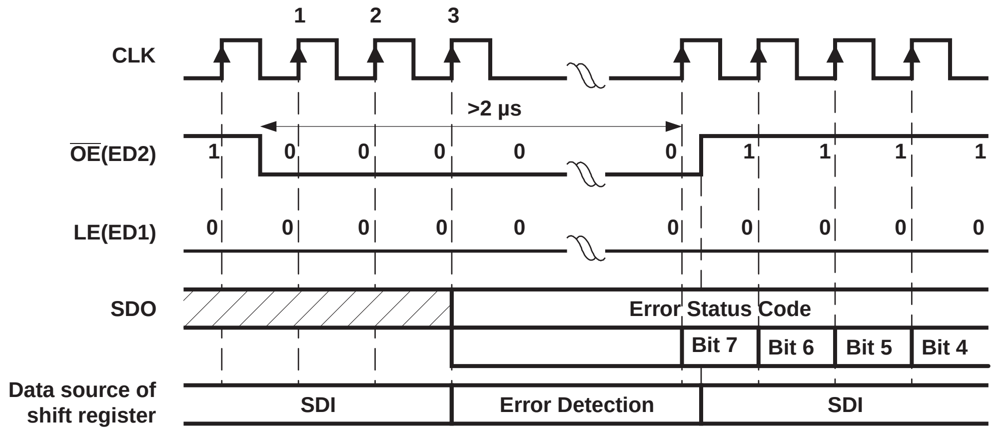


Figure 17. Reading Error Status Code

9.4.3 Writing Configuration Code in Special Mode

When in Special Mode, the active high signal LE(ED1) latches the serial data in the Shift Register to the Configuration Latch, instead of the Output Latch. The latched serial data is used as the Configuration Code.

The code is stored until power off or the Configuration Latch is rewritten. As shown in Figure 18, the timing for writing the Configuration Code is the same as the timing in the Normal Mode to latching output channel data. Both the Configuration Code and Error Status Code are transferred in the common 8-bit Shift Register. Users must pay attention to the sequence of error detection and current adjustment to avoid the Configuration Code being overwritten by Error Status Code.

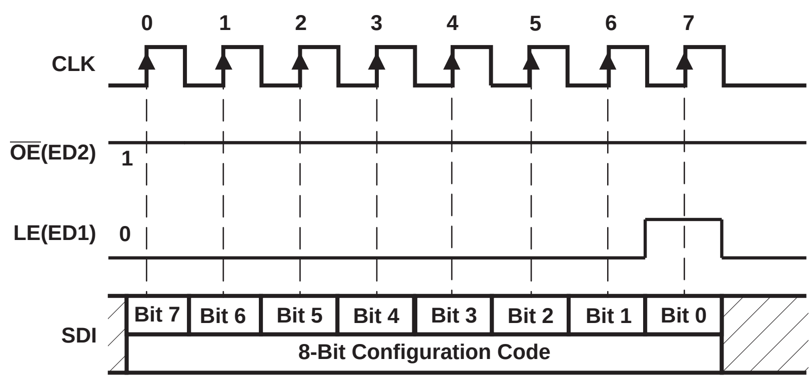


Figure 18. Writing Configuration Code

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 Constant Current

In LED display applications, TLC591x provides nearly no current variations from channel to channel and from IC to IC. While 5 mA ≤ I_{OUT} ≤ 100 mA, the maximum current skew between channels is less than ±3% and between ICs is less than ±6%.

10.1.2 Adjusting Output Current

TLC591x scales up the reference current, I_{ref}, set by the external resistor R_{ext} to sink a current, I_{out}, at each output port. Users can follow the below formulas to calculate the target output current $I_{OUT,target}$ in the saturation region. In the equations,

R_{ext} is the resistance of the external resistor connected between the R-EXT terminal and ground and $V_{R\text{-}EXT}$ is the voltage of R-EXT, which is controlled by the programmable voltage gain (VG). VG is defined by the Configuration Code.

$$V_{R\text{-}EXT} = 1.26\ V \times VG \quad (1)$$

$$I_{ref} = V_{R\text{-}EXT}/R_{ext}, \quad (2)$$

$$I_{OUT,target} = I_{ref} \times 15 \times 3^{CM - 1} \quad (3)$$

The Current Multiplier (CM) determines that the ratio $I_{OUT,target}/I_{ref}$ is 15 or 5. After power on, the default value of VG is 127/128 = 0.992, and the default value of CM is 1, so that the ratio $I_{OUT,target}/I_{ref}$ = 15. Based on the default VG and CM:

$$V_{R\text{-}EXT} = 1.26\ V \times 127/128 = 1.25\ V \quad (4)$$

$$I_{OUT,target} = (1.25\ V/R_{ext}) \times 15 \quad (5)$$

Therefore, the default current is approximately 52 mA at 360 Ω and 26 mA at 720 Ω. The default relationship after power on between $I_{OUT,target}$ and R_{ext} is shown in Figure 19.

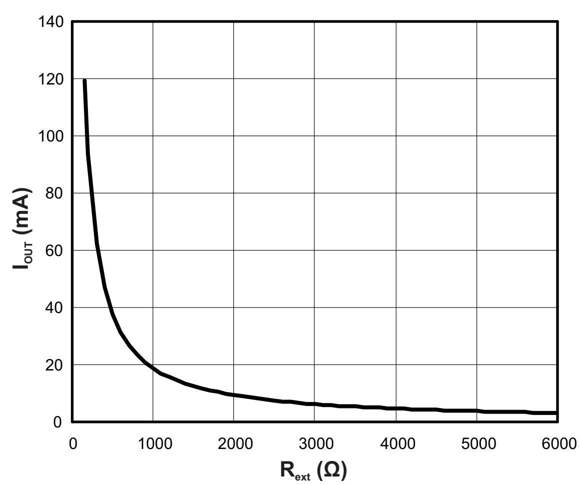


Figure 19. Default Relationship Curve Between $I_{OUT,target}$ and R_{ext} After Power Up

Application Information (continued)

10.1.3 Cascading Implementation of TLC591x Device

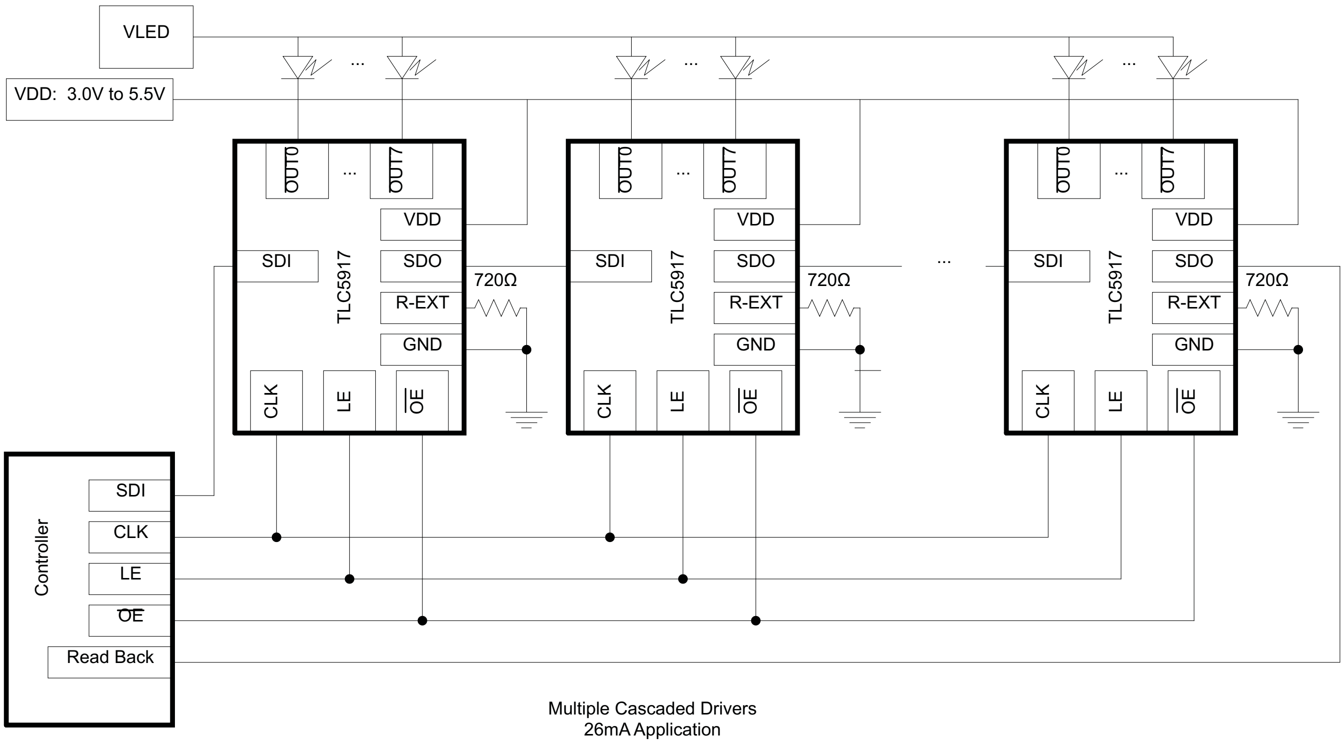


Figure 20. Cascading Implementation of TLC591x Device

Application Information (continued)

10.1.4 8-Bit Configuration Code and Current Gain

Bit definition of the Configuration Code in the Configuration Latch is shown in Table 5.

Table 5. Bit Definition of 8-Bit Configuration Code

	0	1	2	3	4	5	6	7
Meaning	CM	HC	CC0	CC1	CC2	CC3	CC4	CC5
Default	1	1	1	1	1	1	1	1

Bit 7 is first sent into TLC591x through SDI. Bits 1 to 7 {HC, CC[0:5]} determine the voltage gain (VG) that affects the voltage at R-EXT and indirectly affects the reference current, I_{ref}, flowing through the external resistor at R-EXT. Bit 0 is the Current Multiplier (CM) that determines the ratio $I_{OUT,target}/I_{ref}$. Each combination of VG and CM gives a specific Current Gain (CG).

- VG: the relationship between {HC,CC[0:5]} and the voltage gain is calculated as shown in Equation 6 and Equation 7:

  $$VG = (1 + HC) \times (1 + D/64) / 4 \tag{6}$$

  $$D = CC0 \times 2^5 + CC1 \times 2^4 + CC2 \times 2^3 + CC3 \times 2^2 + CC4 \times 2^1 + CC5 \times 2^0 \tag{7}$$

  Where HC is 1 or 0, and D is the binary value of CC[0:5]. So, the VG could be regarded as a floating-point number with 1-bit exponent HC and 6-bit mantissa CC[0:5]. {HC,CC[0:5]} divides the programmable voltage gain VG into 128 steps and two sub-bands:

  Low voltage sub-band (HC = 0): VG = 1/4 ~ 127/256, linearly divided into 64 steps

  High voltage sub-band (HC = 1): VG = 1/2 ~ 127/128, linearly divided into 64 steps

- CM: In addition to determining the ratio $I_{OUT,target}/I_{ref}$, CM limits the output current range.

  High Current Multiplier (CM = 1): $I_{OUT,target}/I_{ref} = 15$, suitable for output current range I_{OUT} = 10 mA to 120 mA.

  Low Current Multiplier (CM = 0): $I_{OUT,target}/I_{ref} = 5$, suitable for output current range I_{OUT} = 3 mA to 40 mA

- CG: The total Current Gain is defined as the following.

  $$V_{R\text{-}EXT} = 1.26\ V \times VG \tag{8}$$

  $$I_{ref} = V_{R\text{-}EXT}/R_{ext}, \text{ if the external resistor, } R_{ext}, \text{ is connected to ground.} \tag{9}$$

  $$I_{OUT,target} = I_{ref} \times 15 \times 3^{CM-1} = 1.26\ V/R_{ext} \times VG \times 15 \times 3^{CM-1} = (1.26\ V/R_{ext} \times 15) \times CG \tag{10}$$

  $$CG = VG \times 3^{CM-1} \tag{11}$$

  Therefore, CG = (1/12) to (127/128), and it is divided into 256 steps. If CG = 127/128 = 0.992, the $I_{OUT,target}$-R_{ext}.

Examples

- Configuration Code {CM, HC, CC[0:5]} = {1,1,111111}
  VG = 127/128 = 0.992 and CG = VG × 3^0 = VG = 0.992
- Configuration Code = {1,1,000000}
  VG = (1 + 1) × (1 + 0/64)/4 = 1/2 = 0.5, and CG = 0.5
- Configuration Code = {0,0,000000}
  VG = (1 + 0) × (1 + 0/64)/4 = 1/4, and CG = (1/4) × 3^{-1} = 1/12

After power on, the default value of the Configuration Code {CM, HC, CC[0:5]} is {1,1,111111}. Therefore, VG = CG = 0.992. The relationship between the Configuration Code and the Current Gain is shown in Figure 21.

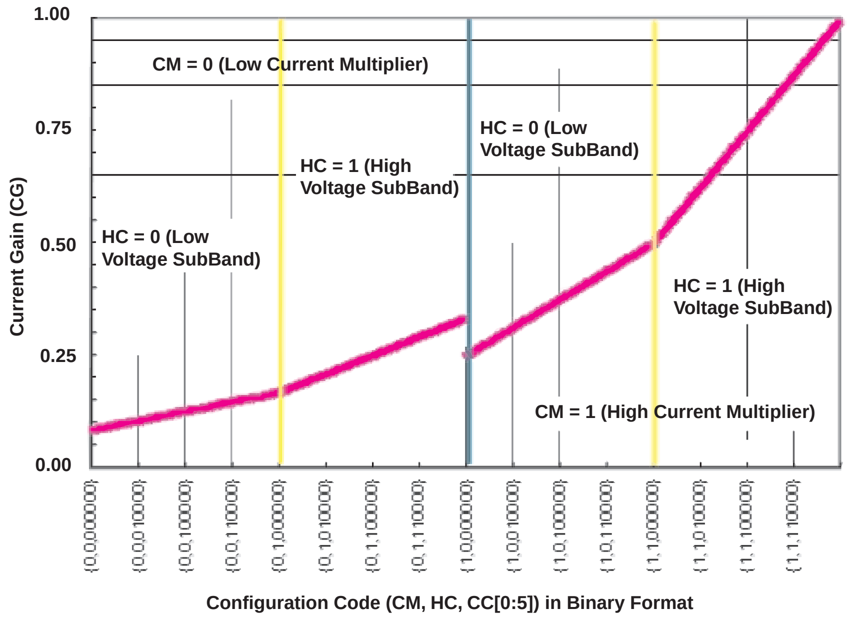


Figure 21. Current Gain vs Configuration Code

10.2 Typical Application

Figure 22 shows implementation of a single TLC591x device. Figure 20 shows a cascaded driver implementation.

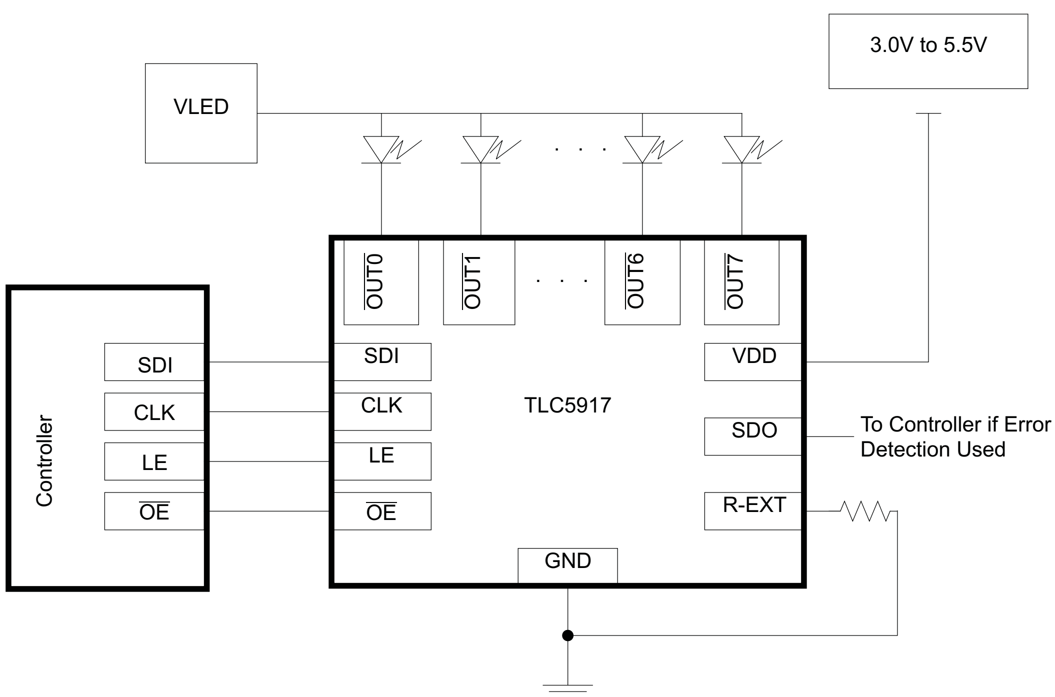


Figure 22. Single Implementation of TLC591x Device

Typical Application (continued)

10.2.1 Design Requirements

For this design example, use the parameters listed in Table 6. The purpose of this design procedure is to calculate the power dissipation in the device and the operating junction temperature.

Table 6. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Number of LED strings	8
Number of LEDs per string	3
LED Current (mA)	20
Forward voltage of each LED (V)	3.5
Junction-to-ambient thermal resistance (°C/W)	87.4
Ambient temperature of application (°C)	115
V_{DD} (V)	5
I_{DD} (mA)	10
Max operating junction temperature (°C)	150

10.2.2 Detailed Design Procedure

$$T_J = T_A + R_{θJA} \times P_{D\_TOT}$$

where

- T_J is the junction temperature.
- T_A is the ambient temperature.
- $R_{θJA}$ is the junction-to-ambient thermal resistance.
- P_{D_TOT} is the total power dissipation in the IC. (12)

$$P_{D\_TOT} = P_{D\_CS} + I_{DD} \times V_{DD}$$

where

- $P_{D_CS}$is the power dissipation in the LED current sinks.
- I_{DD} is the IC supply current.
- V_{DD} is the IC supply voltage. (13)

$$P_{D\_CS} = I_O \times V_O \times n_{CH}$$

where

- I_O is the LED current.
- V_O is the voltage at the output pin.
- n_{CH} is the number of LED strings. (14)

$$V_O = V_{LED} – (n_{LED} \times V_F)$$

where

- V_{LED} is the voltage applied to the LED string.
- n_{LED} is the number of LEDs in the string.
- V_F is the forward voltage of each LED. (15)

V_O must not be too high as this causes excess power dissipation inside the current sink. However, V_O also must not be too low as this does not allow the full LED current (Figure 4). With V_{LED} = 12 V:

$$V_O = 12 \text{ V} – (3 \times 3.5 \text{ V}) = 1.5 \text{ V} \quad (16)$$

$$P_{D\_CS} = 20 \text{ mA} \times 1.5 \text{ V} \times 8 = 0.24 \text{ W} \quad (17)$$

Using P_{D_CS}, calculate:

$$P_{D\_TOT} = P_{D\_CS} + I_{DD} \times V_{DD} = 0.24 \text{ W} + 0.01 \text{ A} \times 5 \text{ V} = 0.29 \text{ W} \quad (18)$$

Using P_{D_TOT}, calculate:

$$T_J = T_A + R_{θJA} \times P_{D\_TOT} = 115°\text{C} + 87.4°\text{C/W} \times 0.29 \text{ W} = 140°\text{C} \quad (19)$$

This design example demonstrates how to calculate power dissipation in the IC and ensure that the junction temperature is kept below 150°C.

NOTE

This design example assumes that all channels have the same electrical parameters (n_{LED}, I_O, V_F, V_{LED}). If the parameters are unique for each channel, then the power dissipation must be calculated for each current sink separately. Then, each result must be added together to calculate the total power dissipation in the current sinks.

10.2.3 Application Curve

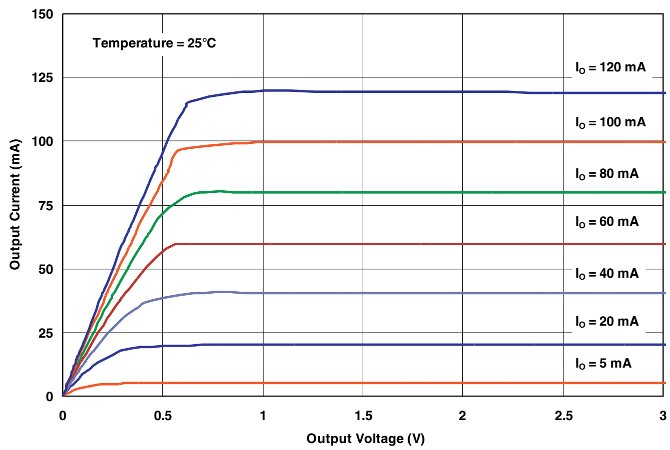


Figure 23. Output Current vs Output Voltage

11 Power Supply Recommendations

The device is designed to operate from a VDD supply between 3 V and 5.5 V. The LED supply voltage is determined by the number of LEDs in each string and the forward voltage of the LEDs.

12 Layout

12.1 Layout Guidelines

The traces that carry current from the LED cathodes to the OUTx pins must be wide enough to support the default current (up to 120 mA).

The SDI, CLK, LE (ED1), OE (ED2), and SDO pins are to be connected to the microcontroller. There are several ways to achieve this, including the following methods:

- Traces may be routed underneath the package on the top layer.
- The signal may travel through a via to another layer.

12.2 Layout Example

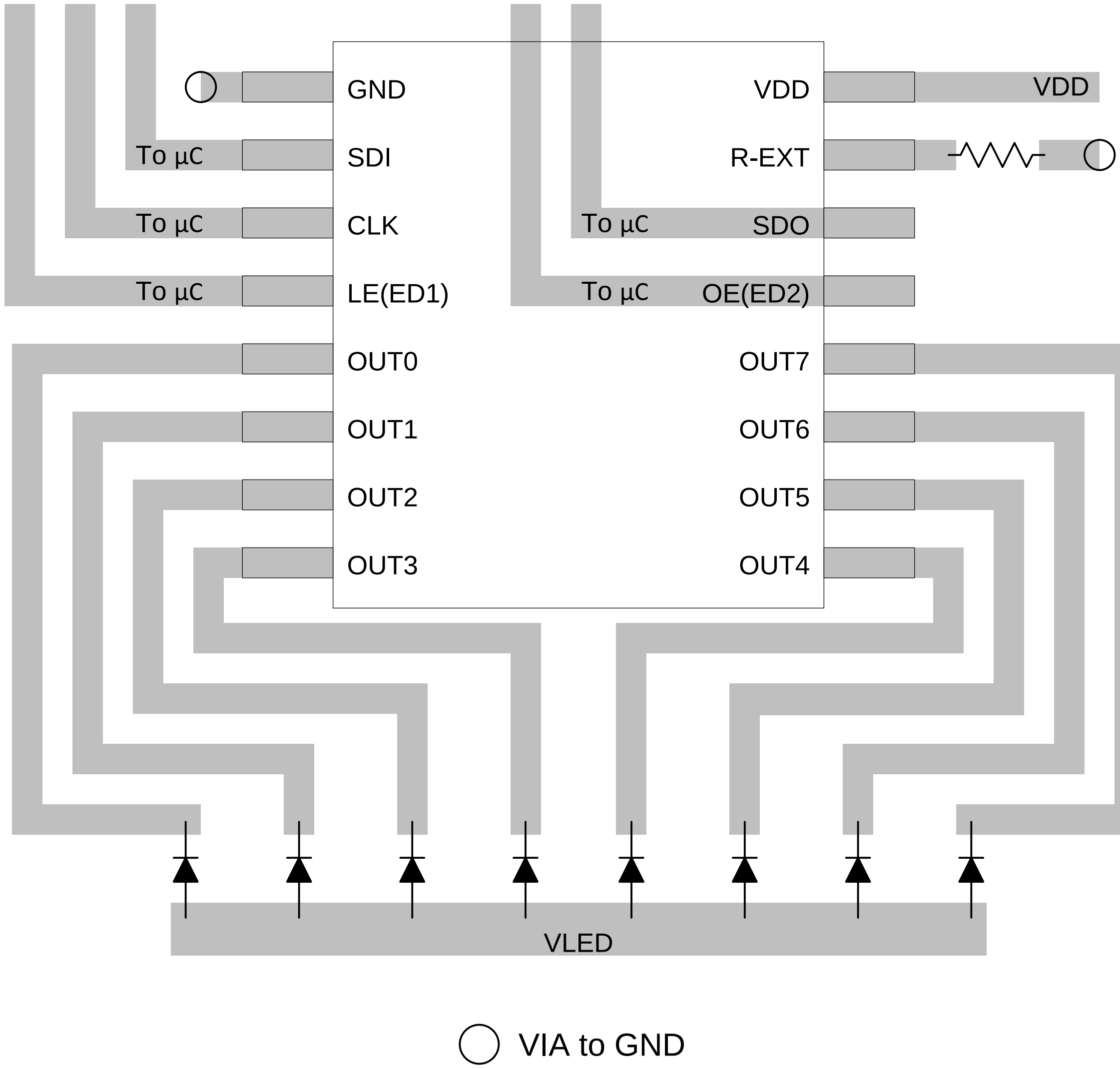


Figure 24. PW Package Layout

Layout Example (continued)

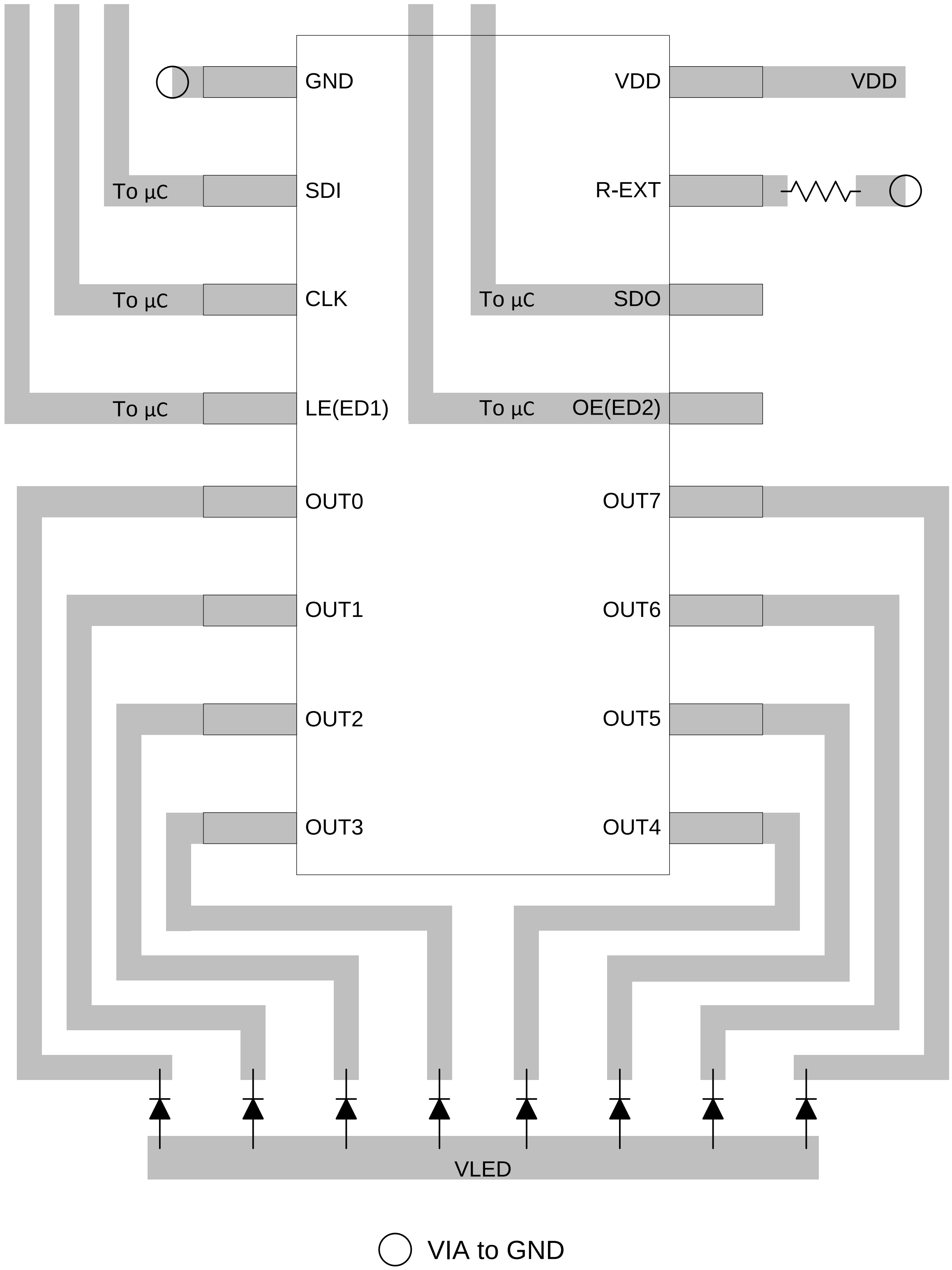


Figure 25. D Package Layout

13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 7. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TLC5916	Click here	Click here	Click here	Click here	Click here
TLC5917	Click here	Click here	Click here	Click here	Click here

13.2 Trademarks

All trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC5916ID	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLC5916I
TLC5916ID.B	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLC5916I
TLC5916IDG4	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLC5916I
TLC5916IDR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLC5916I
TLC5916IDR.B	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLC5916I
TLC5916IN	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TLC5916IN
TLC5916IN.B	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TLC5916IN
TLC5916INE4	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TLC5916IN
TLC5916IPW	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y5916
TLC5916IPW.B	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y5916
TLC5916IPWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y5916
TLC5916IPWR.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y5916
TLC5916IPWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y5916
TLC5917ID	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLC5917I
TLC5917ID.B	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLC5917I
TLC5917IDR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLC5917I
TLC5917IDR.B	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLC5917I
TLC5917IDRG4	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLC5917I
TLC5917IN	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TLC5917IN
TLC5917IN.B	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TLC5917IN
TLC5917INE4	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TLC5917IN
TLC5917IPW	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y5917
TLC5917IPW.B	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y5917
TLC5917IPWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y5917
TLC5917IPWR.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y5917
TLC5917IPWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y5917

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLC5916, TLC5917 :

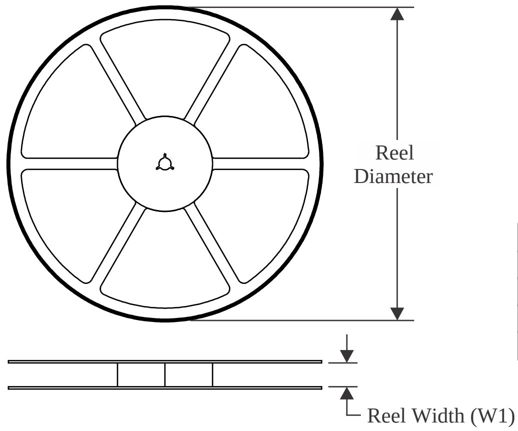
- Automotive : TLC5916-Q1, TLC5917-Q1

NOTE: Qualified Version Definitions:

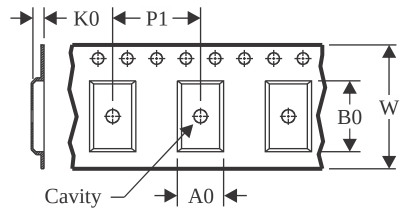
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

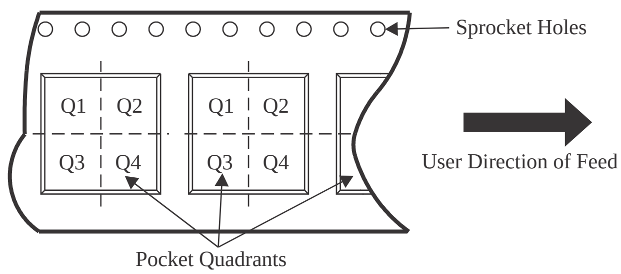


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

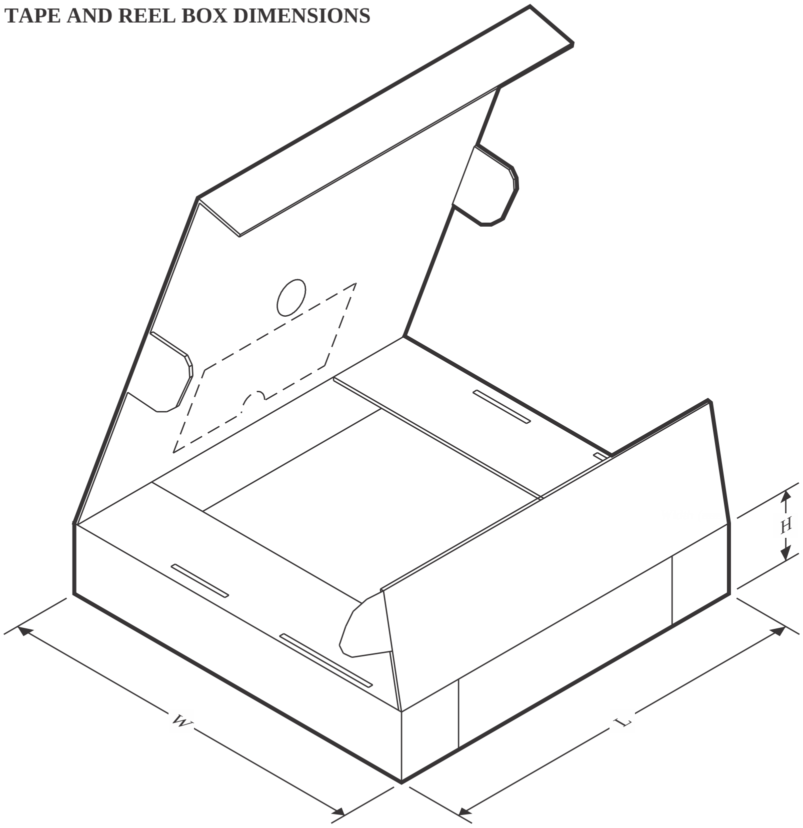
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC5916IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TLC5916IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC5917IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TLC5917IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

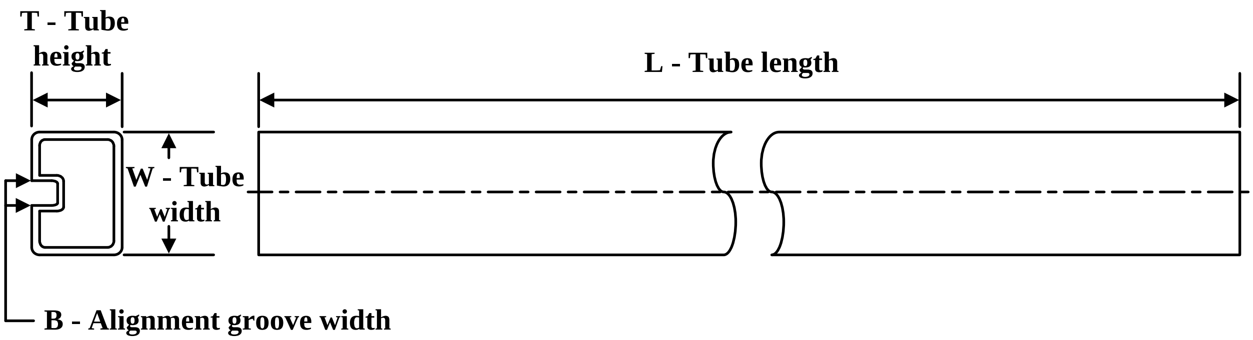
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC5916IDR	SOIC	D	16	2500	353.0	353.0	32.0
TLC5916IPWR	TSSOP	PW	16	2000	353.0	353.0	32.0
TLC5917IDR	SOIC	D	16	2500	353.0	353.0	32.0
TLC5917IPWR	TSSOP	PW	16	2000	353.0	353.0	32.0

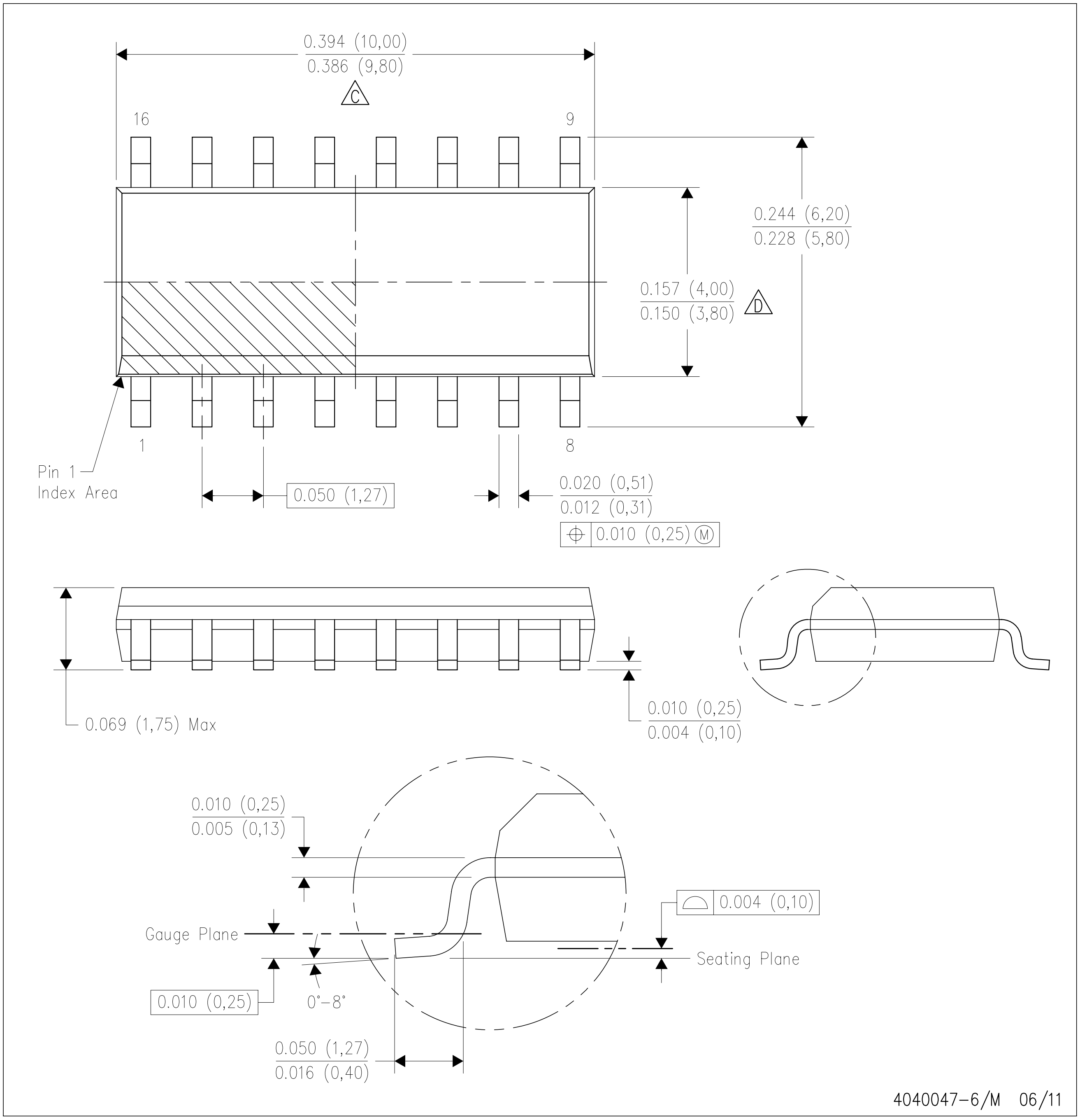
TUBE



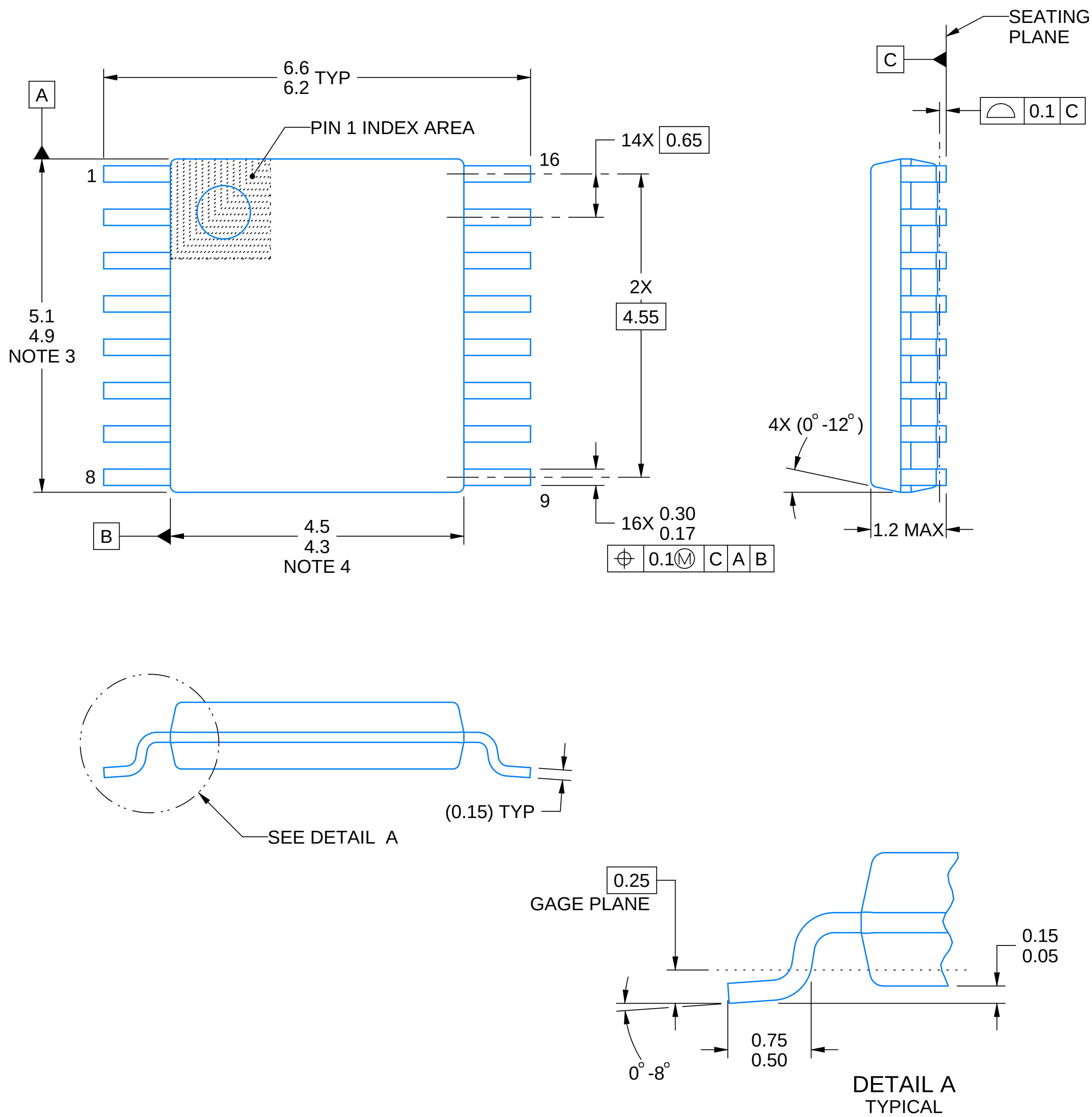
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLC5916ID	D	SOIC	16	40	507	8	3940	4.32
TLC5916ID.B	D	SOIC	16	40	507	8	3940	4.32
TLC5916IDG4	D	SOIC	16	40	507	8	3940	4.32
TLC5916IN	N	PDIP	16	25	506	13.97	11230	4.32
TLC5916IN.B	N	PDIP	16	25	506	13.97	11230	4.32
TLC5916INE4	N	PDIP	16	25	506	13.97	11230	4.32
TLC5916IPW	PW	TSSOP	16	90	530	10.2	3600	3.5
TLC5916IPW.B	PW	TSSOP	16	90	530	10.2	3600	3.5
TLC5917ID	D	SOIC	16	40	507	8	3940	4.32
TLC5917ID.B	D	SOIC	16	40	507	8	3940	4.32
TLC5917IN	N	PDIP	16	25	506	13.97	11230	4.32
TLC5917IN.B	N	PDIP	16	25	506	13.97	11230	4.32
TLC5917INE4	N	PDIP	16	25	506	13.97	11230	4.32
TLC5917IPW	PW	TSSOP	16	90	530	10.2	3600	3.5
TLC5917IPW.B	PW	TSSOP	16	90	530	10.2	3600	3.5

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS–012 variation AC.



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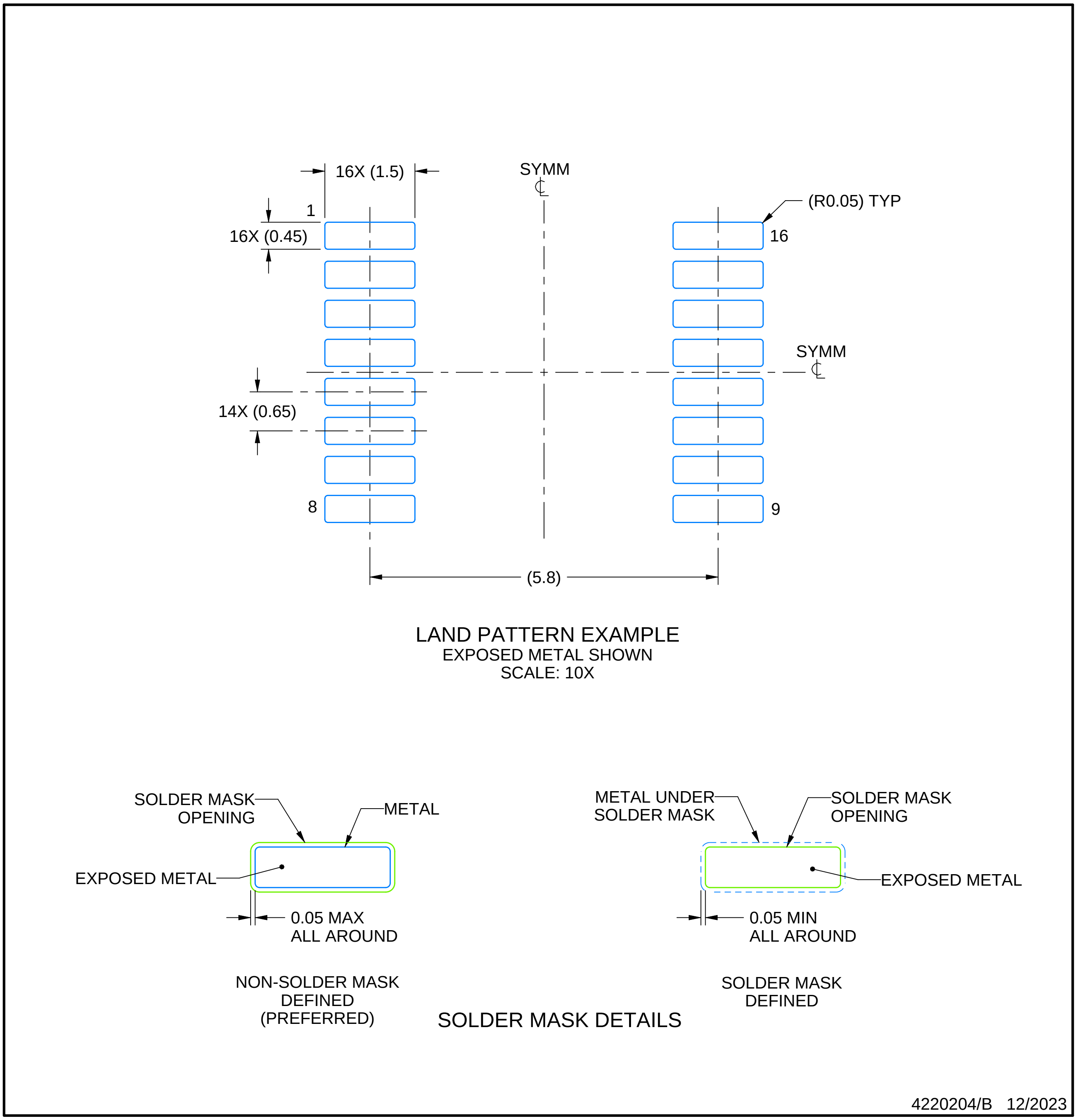
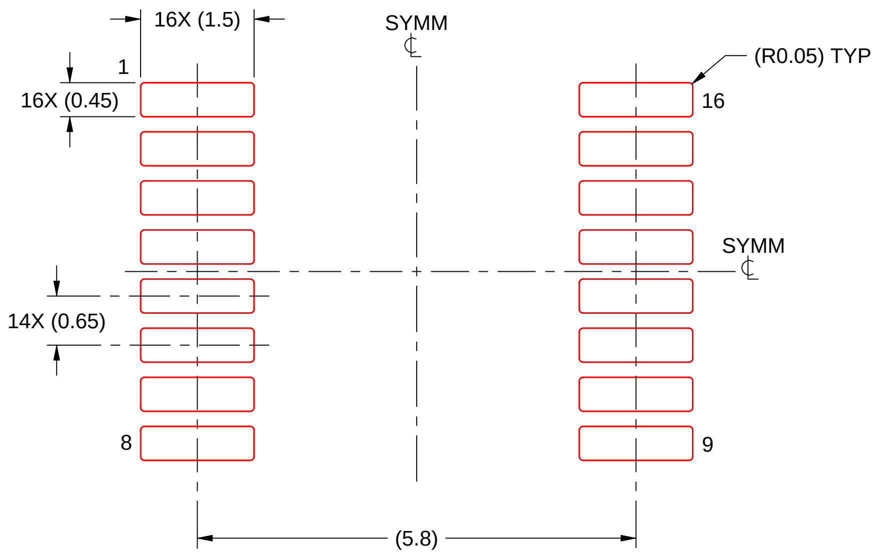
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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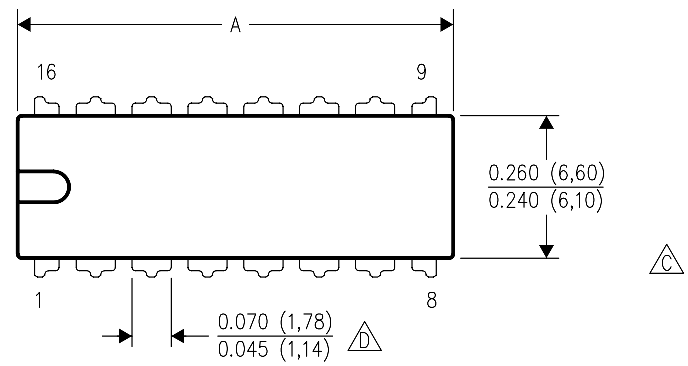
NOTES: (continued)

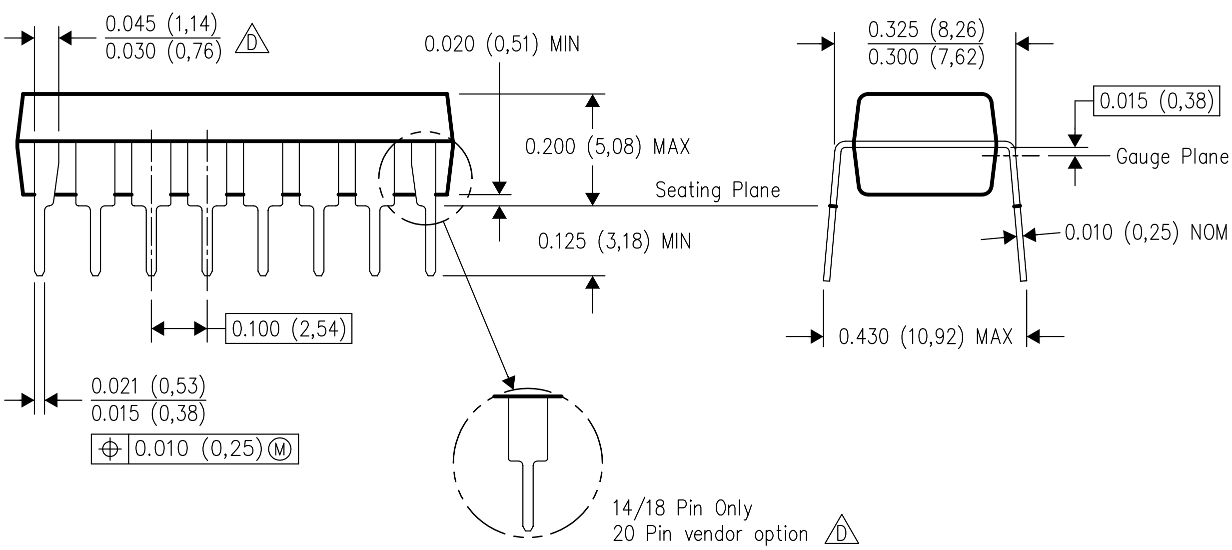
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
C MS–001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.