TLE2142-Q1 Excalibur™ Low-Noise High-Speed Precision Operational Amplifier

1 Features

- Qualified for automotive applications
- Low noise:
  - 10Hz: 15nV/√Hz
  - 1kHz: 10.5nV/√Hz
- Load capability: 10000pF
- Short-circuit output current: 20mA (minimum)
- Slew rate: 27V/µs (minimum)
- High gain-bandwidth product: 5.9MHz
- Single or split supply: 4V to 44V
- Fast settling time
  - 340ns to 0.1%
  - 400ns to 0.01%
- Large output swing:
  V_{CC-} + 0.1V to V_{CC+} – 1V

2 Applications

- Traction inverter
- Onboard charger
- Automatic transmission
- DC/DC converter

3 Description

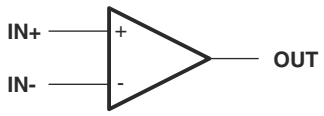
The TLE2142-Q1 device is a high-performance, internally compensated operational amplifier built using the Texas Instruments complementary bipolar Excalibur™ process. The device is a pin-compatible upgrade to standard industry products.

The design incorporates an input stage that simultaneously achieves low audio-band noise of 10.5nV/√Hz with a 10Hz1/f corner and symmetrical 40V/µs slew rate typically with loads up to 800pF. The resulting low distortion and high power bandwidth are important in high-fidelity audio applications. A fast settling time of 430ns to 0.1% of a 10V step with a 2kΩ/100pF load is useful in fast actuator/positioning drivers. Under similar test conditions, settling time to 0.01% is 640ns.

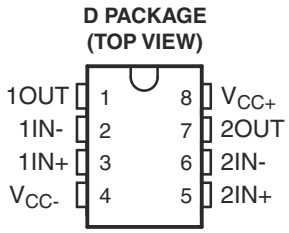
Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TLE2142-Q1	D (SOIC, 8)	4.9mm × 6mm

(1) For all available packages, see Section 8.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Symbol (Each Amplifier)



Pinout

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4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		VALUE	UNIT
V_{CC+}	Supply voltage(2)	22	V
$V_{CC–}$	Supply voltage	–22	V
V_{ID}	Differential input voltage(3)	±44	V
V_I	Input voltage range (any input)	V_{CC+} to ($V_{CC–}$ – 0.3)	V
I_I	Input current (each input)	±1	mA
I_O	Output current	±80	mA
	Total current into V_{CC+}	80	mA
	Total current out of $V_{CC–}$	80	mA
	Duration of short-circuit current at (or below) 25°C(4)	Unlimited	
θ_{JA}	Package thermal impedance(5) (6)	97.1	°C/W
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260	°C
T_A	Operating free-air temperature range	–40 to 125	°C
T_{stg}	Storage temperature	–65 to 150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and $V_{CC–}$.
(3) Differential voltages are at IN+ with respect to IN–. Excessive current flows, if input, are brought below $V_{CC–}$ – 0.3 V.
(4) The output can be shorted to either supply. Temperature and/or supply voltages must be limited to make sure that the maximum dissipation rating is not exceeded.
(5) Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(6) The package thermal impedance is calculated in accordance with JESD 51-7.

4.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±500	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±YYY	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. [Following sentences optional; see the TI Data Sheet Style Guides (STDZ017 or STDZ113).] Manufacturing with less than 500V HBM is possible with the necessary precautions. Pins listed as ±XXXV may actually have higher performance.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process. [Following sentences optional; see the TI Data Sheet Style Guides (STDZ017 or STDZ113).] Manufacturing with less than 250V CDM is possible with the necessary precautions. Pins listed as ±YYYV may actually have higher performance.

4.3 Recommended Operating Conditions

			MIN	MAX	UNIT
$V_{CC±}$	Supply voltage		±2	±22	V
V_{IC}	Common-mode input voltage	V_{CC} = 5V	0	2.7	V
		$V_{CC±}$ = ±15V	–15	12.7	
T_A	Operating free-air temperature		–40	125	°C

4.4 Thermal Information

THERMAL METRIC[1]		D (SOIC)	UNIT
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	107.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter 4.2		°C/W
ψ_{JB}	Junction-to-board characterization parameter	53.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application note.

4.5 Operating Characteristics: V_{CC} = 5V

V_{CC} = 5V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR+	Positive slew rate	A_{VD} = –1, R_L = 2kΩ[1], C_L = 500 pF			45		V/µs
SR–	Negative slew rate	A_{VD} = –1, R_L = 2kΩ[1], C_L = 500 pF			42		V/µs
t_s	Settling time	A_{VD} = –1, 2.5V step	To 0.1%		0.66		µs
			To 0.01%		0.99		
V_n	Equivalent input noise voltage	R_S = 20Ω	f = 10Hz		15		nV/√Hz
			f = 1kHz		10.5		
$V_{n(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1Hz to 1Hz			0.48		µV
		f = 0.1Hz to 10Hz			0.51		
I_n	Equivalent input noise current	f = 10Hz			1.92		pA/√Hz
		f = 1kHz			0.5		
THD+N	Total harmonic distortion plus noise	V_O = 1V to 3V, R_L = 2kΩ[1], A_{VD} = 2, f = 10kHz			0.0052		%
B_1	Unity-gain bandwidth	R_L = 2kΩ[1], C_L = 100pF			5.9		MHz
	Gain-bandwidth product	R_L = 2kΩ[1], C_L = 100pF, f = 100 kHz			5.8		MHz
BOM	Maximum output-swing bandwidth[2]	$V_{O(PP)}$ = 2V, R_L = 2kΩ[1], A_{VD} = 1, C_L = 100pF			380		kHz
φ_m	Phase margin at unity gain	R_L = 2kΩ[1], C_L = 100pF			57		°

(1) R_L terminated at 2.5V.
(2) Measured at -0.1dB.

4.6 Operating Characteristics: V_{CC} = ±15V

V_{CC} = ±15V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR+	Positive slew rate	A_{VD} = –1, R_L = 2kΩ, C_L = 100pF		27[1]	45		V/µs
SR–	Negative slew rate	A_{VD} = –1, R_L = 2kΩ, C_L = 100 pF		27[1]	42		V/µs
t_s	Settling time	A_{VD} = –1, 10V step	To 0.1%		0.43		µs
			To 0.01%		0.64		
V_n	Equivalent input noise voltage	R_S = 20Ω	f = 10Hz		15		nV/√Hz
			f = 1kHz		10.5		
$V_{n(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1Hz to 1Hz			0.48		µV
		f = 0.1Hz to 10Hz			0.51		
I_n	Equivalent input noise current	f = 10Hz			1.89		pA/√Hz
		f = 1kHz			0.47		
THD+N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 20V, R_L = 2kΩ, A_{VD} = 10, f = 10kHz			0.06		%
B_1	Unity-gain bandwidth	R_L = 2kΩ, C_L = 100 pF			6		MHz
	Gain-bandwidth product	R_L = 2kΩ, C_L = 100 pF, f = 100 kHz			5.9		MHz
BOM	Maximum output-swing bandwidth[2]	$V_{O(PP)}$ = 20V, A_{VD} = 1, R_L = 2kΩ, C_L = 100pF			668		kHz
φ_m	Phase margin at unity gain	R_L = 2kΩ, C_L = 100pF			58		°

(1) Specified by characterization.
(2) Measured at -0.1dB.

4.7 Electrical Characteristics: V_{CC} = 5V

V_{CC} = 5V, at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A (1)	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 2.5V, R_S = 50Ω, V_{IC} = 2.5 V	25°C		220	1900	µV
			Full range			2600	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 2.5V, R_S = 50Ω, V_{IC} = 2.5 V	Full range		1.7		µV/°C
I_{IO}	Input offset current	V_O = 2.5V, R_S = 50Ω, V_{IC} = 2.5 V	25°C		8	100	nA
			Full range			200	
I_{IB}	Input bias current	V_O = 2.5V, R_S = 50Ω, V_{IC} = 2.5 V	25°C		–0.8	–2	µA
			Full range			–2.3	
V_{ICR}	Common-mode input voltage range	R_S = 50Ω	25°C	0 to 3	–0.3 to 3.2		V
			Full range	0 to 2.7	–0.3 to 2.9		
V_{OH}	High-level output voltage	I_{OH} = –150µA	25°C	3.9	4.1		V
		I_{OH} = –1.5mA		3.8	4		
		I_{OH} = –15mA		3.4	3.7		
		I_{OH} = –100µA	Full range	3.75			
		I_{OH} = –1mA		3.65			
		I_{OH} = –10mA		3.45			
V_{OL}	Low-level output voltage	I_{OL} = 150µA	25°C		75	125	mV
		I_{OL} = 1.5mA			150	225	
		I_{OL} = 15mA			1.2	1.4	V
		I_{OL} = 100µA	Full range			200	mV
		I_{OL} = 1mA				250	
		I_{OL} = 10mA				1.25	V
A_{VD}	Large-signal differential voltage amplification	V_{IC} = ±2.5V, R_L = 2kΩ, V_O = 1 V to -1.5 V	25°C	50	220		V/mV
			Full range	5			
r_i	Input resistance		25°C		70		MΩ
c_i	Input capacitance		25°C		2.5		pF
z_o	Open-loop output impedance	f = 1MHz	25°C		30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}(min), R_S = 50Ω	25°C	85	118		dB
			Full range	80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5V to ±15V, R_S = 50 Ω	25°C	90	106		dB
			Full range	85			
I_{CC}	Supply current	V_O = 2.5V, No load, V_{IC} = 2.5 V	25°C		6.6	8.8	mA
			Full range			9.2	

(1) Full range is –40°C to 125°C.

4.8 Electrical Characteristics: V_{CC} = ±15V

V_{CC} = ±15V, at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50Ω		25°C		290	1200	µV
				Full range			2000	
α_{VIO}	Temperature coefficient of input offset voltage	V_{IC} = 0, R_S = 50Ω		Full range		1.7		µV/°C
I_{IO}	Input offset current	V_{IC} = 0, R_S = 50Ω		25°C		7	100	nA
				Full range			250	
I_{IB}	Input bias current	V_{IC} = 0, R_S = 50Ω		25°C		–0.7	–1.5	µA
				Full range			–1.8	
V_{ICR}	Common-mode input voltage range	R_S = 50Ω		25°C	–15 to 13	–15.3 to 13.2		V
				Full range	–15 to 12.7	–15.3 to 12.9		
V_{OM+}	Maximum positive peak output voltage swing	I_O = –150µA		25°C	13.8	14.1		V
		I_O = –1.5mA			13.7	14		
		I_O = –15mA			13.3	13.7		
		I_O = –100µA		Full range	13.7			
		I_O = –1mA			13.6			
		I_O = –10mA			13.3			
$V_{OM–}$	Maximum negative peak output voltage swing	I_O = 150µA		25°C	–14.7	–14.9		V
		I_O = 1.5mA			–14.5	–14.8		
		I_O = 15mA			–13.4	–13.8		
		I_O = 100µA		Full range	–14.6			
		I_O = 1mA			–14.5			
		I_O = 10mA			–13.4			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L = 2kΩ		25°C	100	450		V/mV
				Full range	20			
r_i	Input resistance			25°C		65		MΩ
c_i	Input capacitance			25°C		2.5		pF
z_o	Open-loop output impedance	f = 1MHz		25°C		30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}(min), R_S = 50Ω		25°C	85	108		dB
				Full range	80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC±}/\Delta V_{IO}$)	$V_{CC±}$ = ±2.5V to ±15V, R_S = 50 Ω		25°C	90	106		dB
				Full range	85			
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C	–25	–50		mA
			V_{ID} = –1 V		20	31		
I_{CC}	Supply current	V_O = 0, No load, V_{IC} = 2.5 V		25°C		6.9	9	mA
				Full range			9.4	

(1) Full range is –40°C to 125°C.

4.9 Typical Characteristics

Table 4-1. Table of Graphs

V_{IO}	Input offset voltage		Distribution
I_{IO}	Input offset current		vs Free-air temperature
I_{IB}	Input bias current		vs Common-mode input voltage
			vs Free-air temperature
V_{OM+}	Maximum positive peak output voltage		vs Supply voltage
			vs Free-air temperature
			vs Output current
			vs Settling time
$V_{OM–}$	Maximum negative peak output voltage		vs Supply voltage
			vs Free-air temperature
			vs Output current
			vs Settling time
$V_{O(PP)}$	Maximum peak-to-peak output voltage		vs Frequency
V_{OH}	High-level output voltage		vs Output current
V_{OL}	Low-level output voltage		vs Output current
	Phase shift		vs Frequency
A_{VD}	Large-signal differential voltage amplification		vs Frequency
			vs Free-air temperature
z_o	Closed-loop output impedance		vs Frequency
I_{OS}	Short-circuit output current		vs Free-air temperature
CMRR	Common-mode rejection ratio		vs Frequency
			vs Free-air temperature
k_{SVR}	Supply-voltage rejection ratio		vs Frequency
			vs Free-air temperature
I_{CC}	Supply current		vs Supply voltage
			vs Free-air temperature
V_n	Equivalent input noise voltage		vs Frequency
V_n	Input noise voltage		Over a 10-second period
I_n	Noise current		vs Frequency
THD+N	Total harmonic distortion plus noise		vs Frequency
SR	Slew rate		vs Free-air temperature
			vs Load capacitance
	Pulse response	Noninverting large signal	vs Time
		Inverting large signal	vs Time
		Small signal	vs Time
B_1	Unity-gain bandwidth		vs Load capacitance
	Gain margin		vs Load capacitance
φ_m	Phase margin		vs Load capacitance

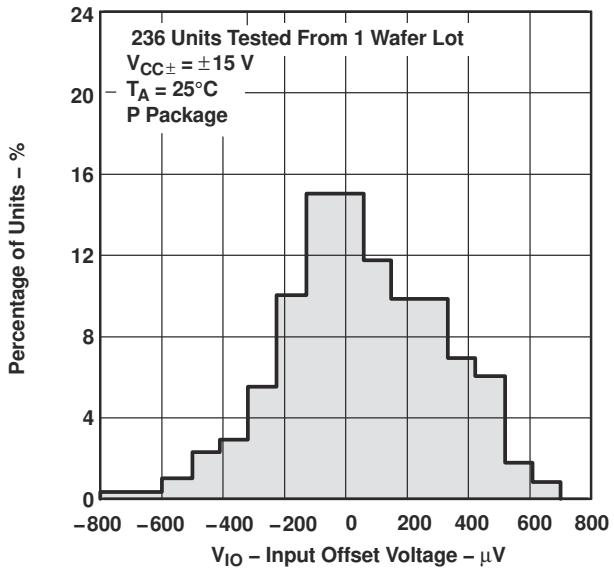


Figure 4-1.

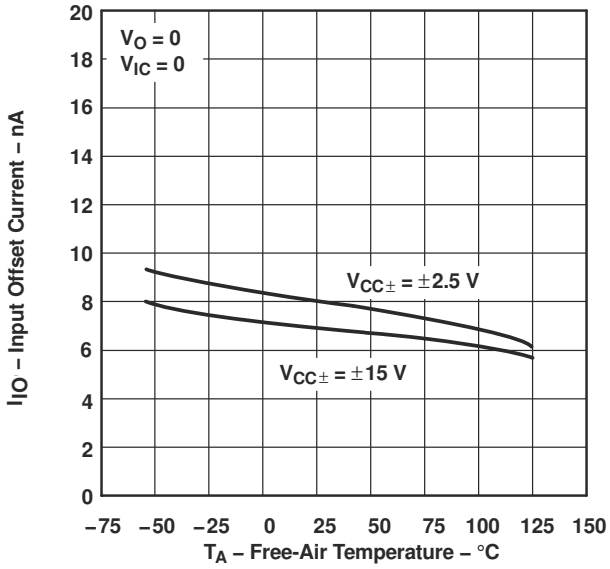


Figure 4-2.

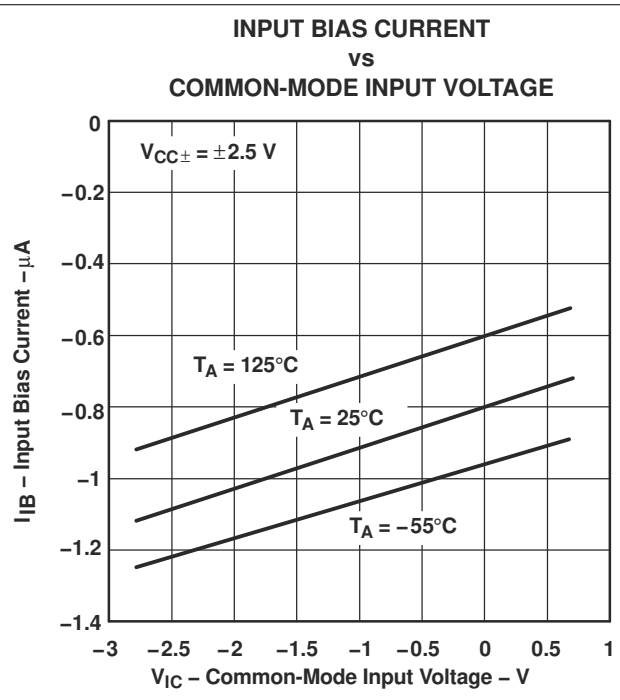


Figure 4-3.

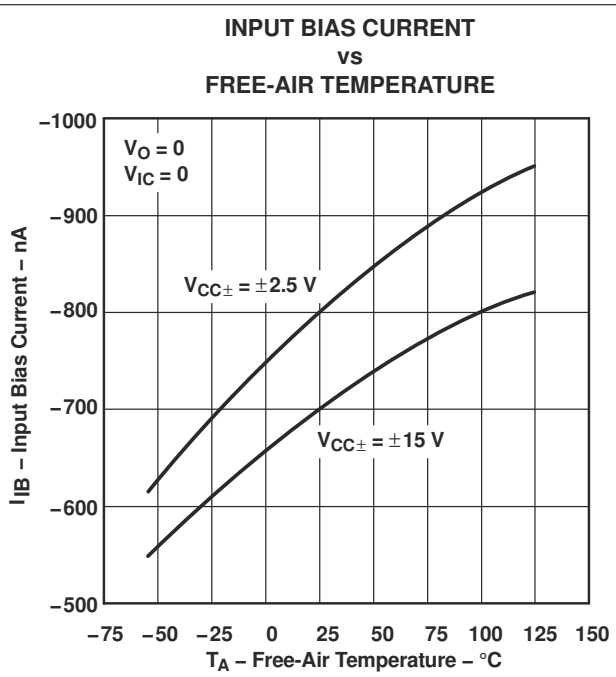


Figure 4-4.

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

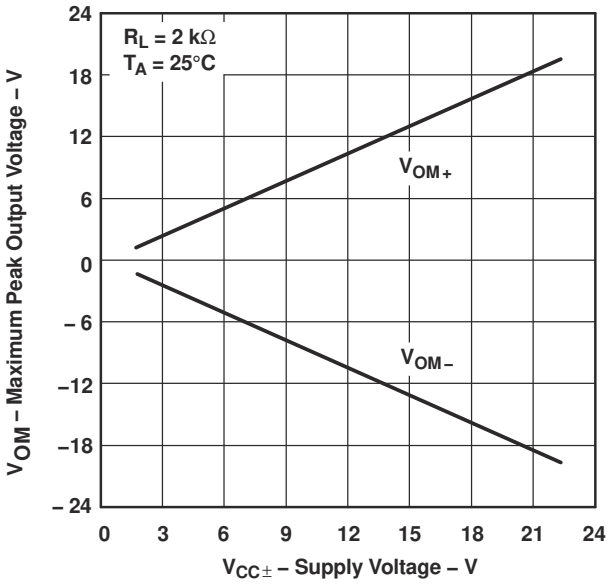


Figure 4-5.

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

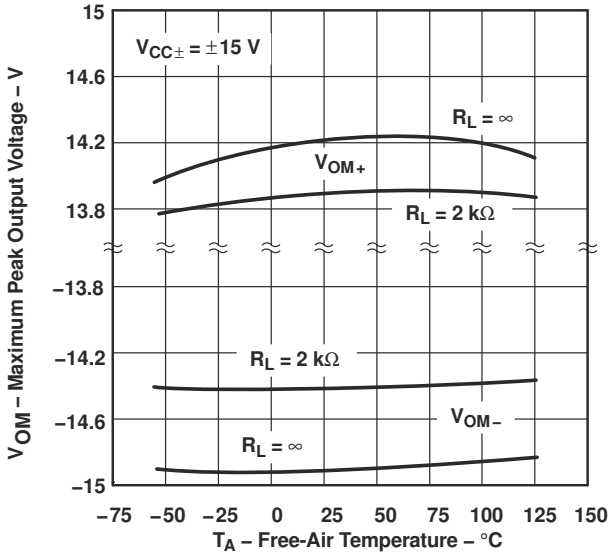


Figure 4-6.

MAXIMUM POSITIVE PEAK
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

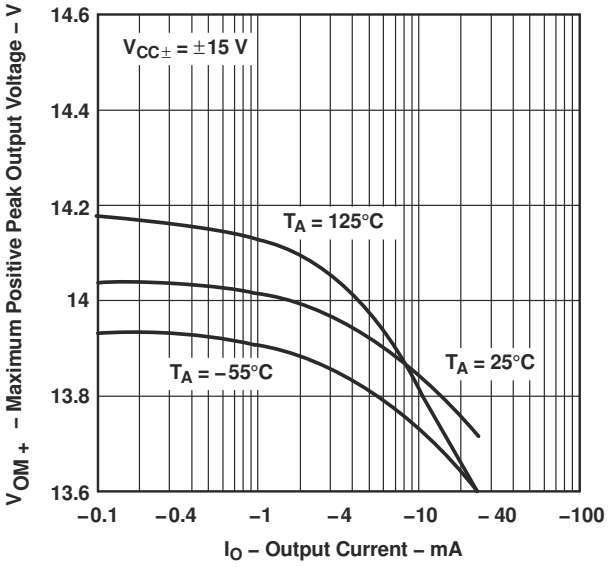


Figure 4-7.

MAXIMUM NEGATIVE PEAK
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

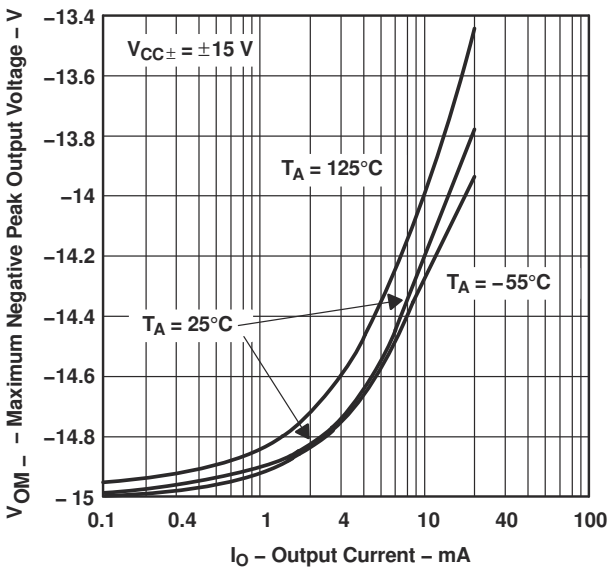


Figure 4-8.

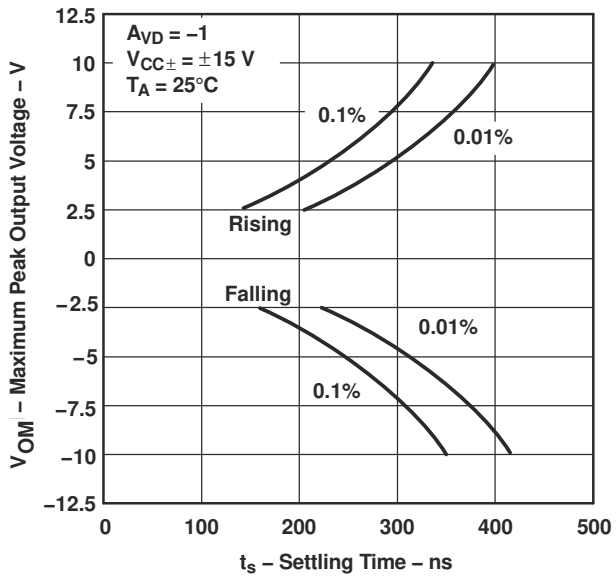


Figure 4-9.

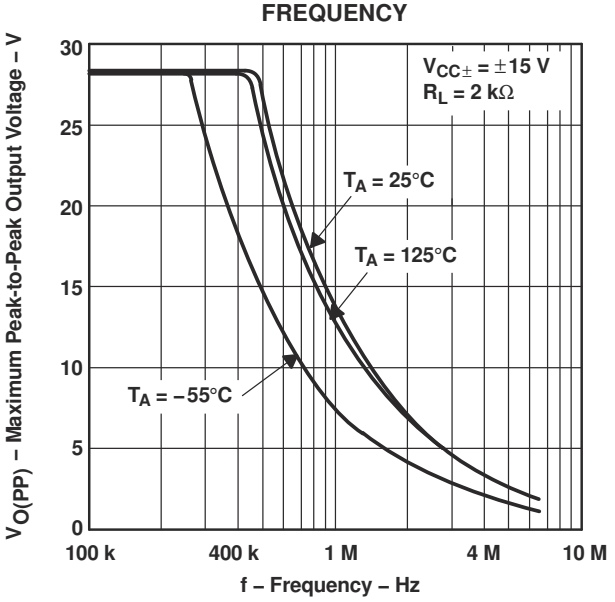


Figure 4-10.

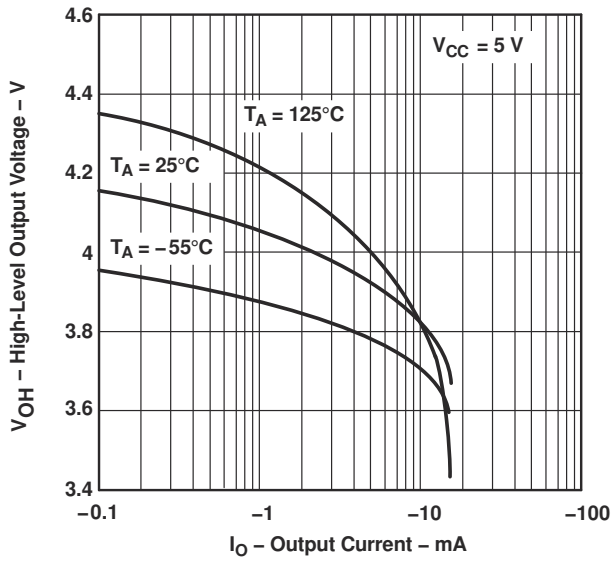


Figure 4-11.

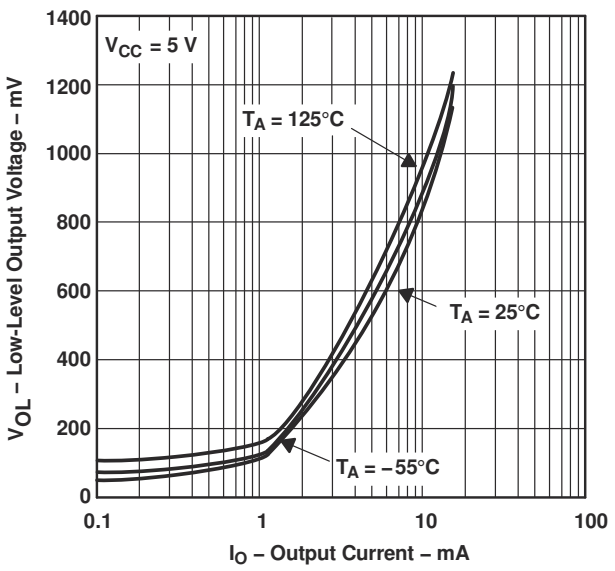


Figure 4-12.

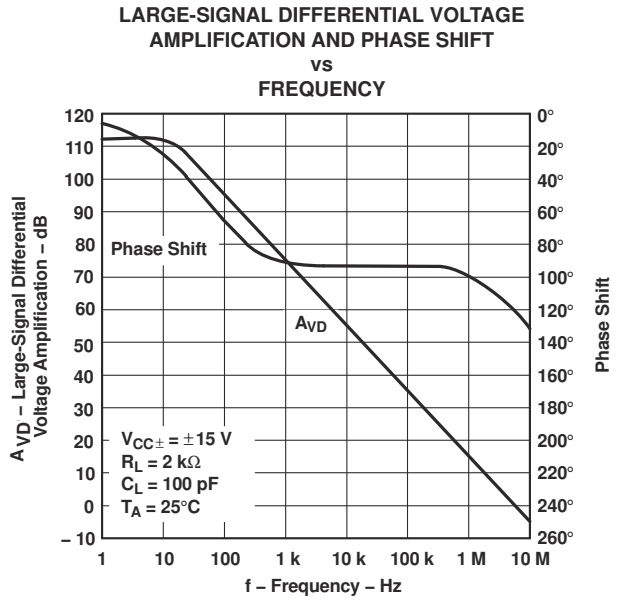


Figure 4-13.

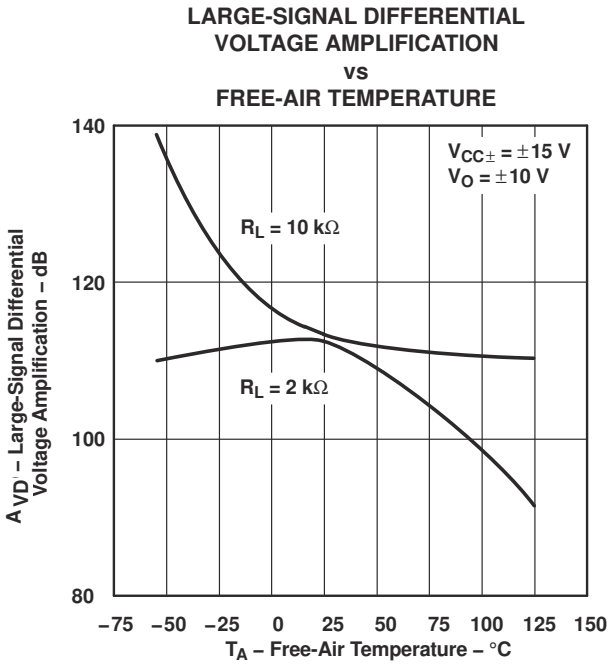


Figure 4-14.

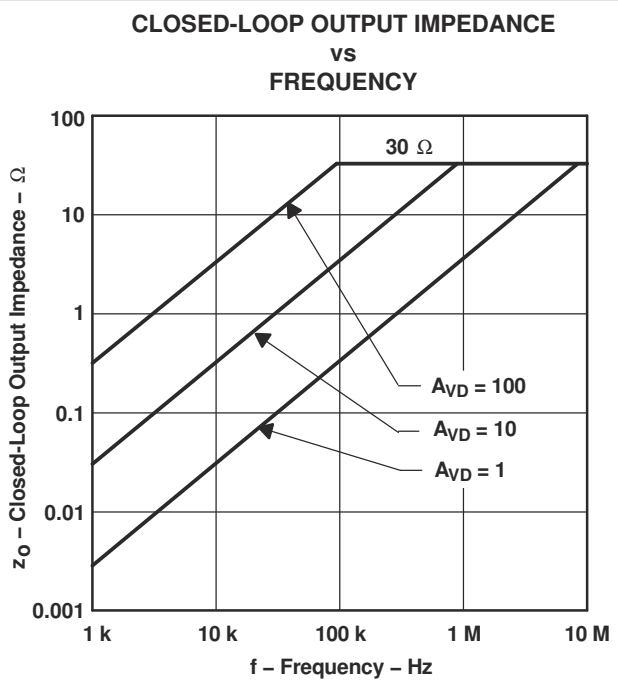


Figure 4-15.

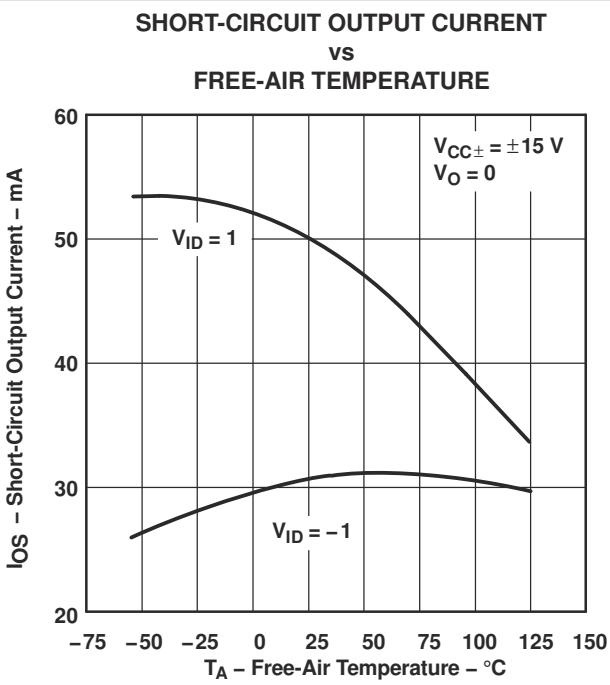


Figure 4-16.

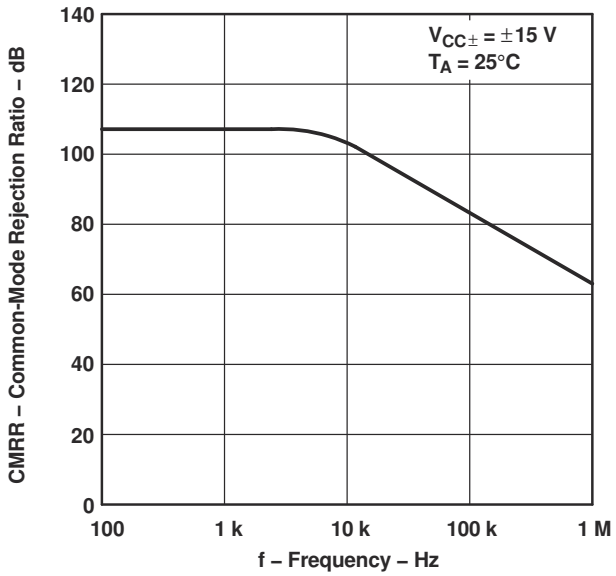


Figure 4-17.

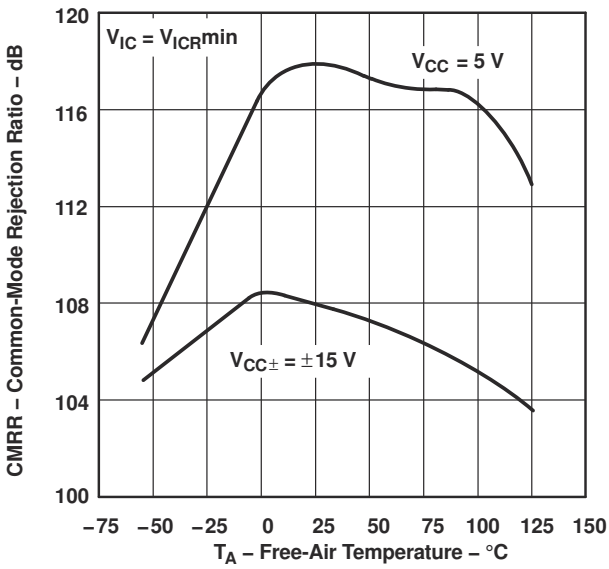


Figure 4-18.

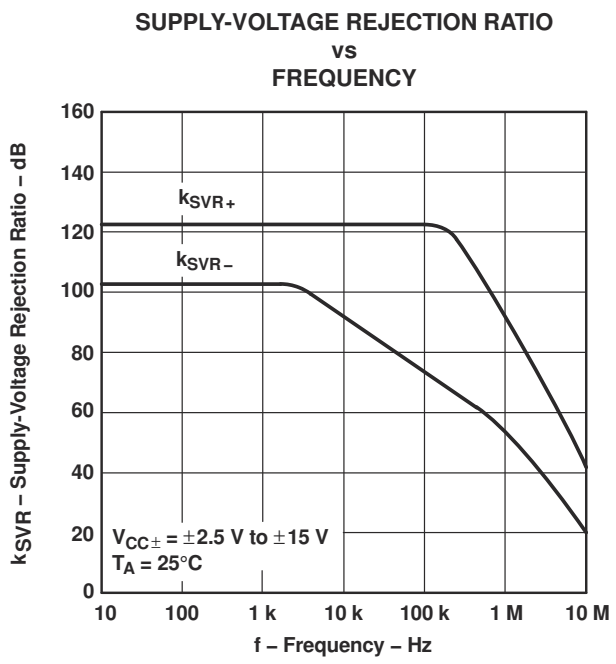
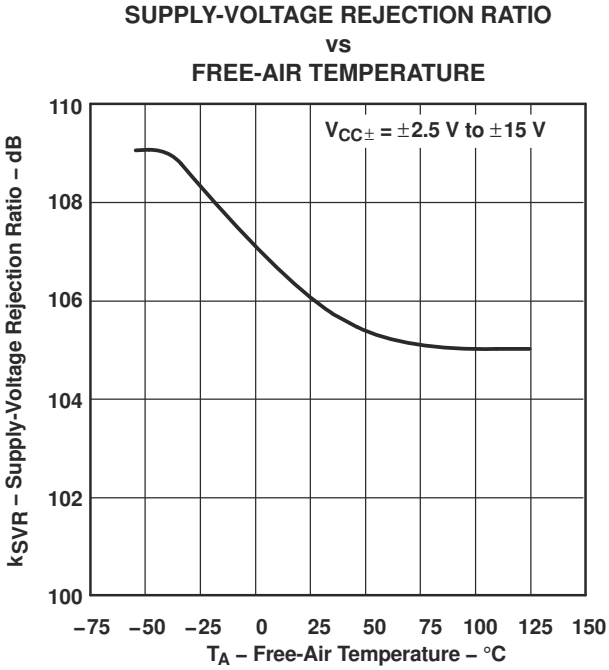


Figure 4-19.



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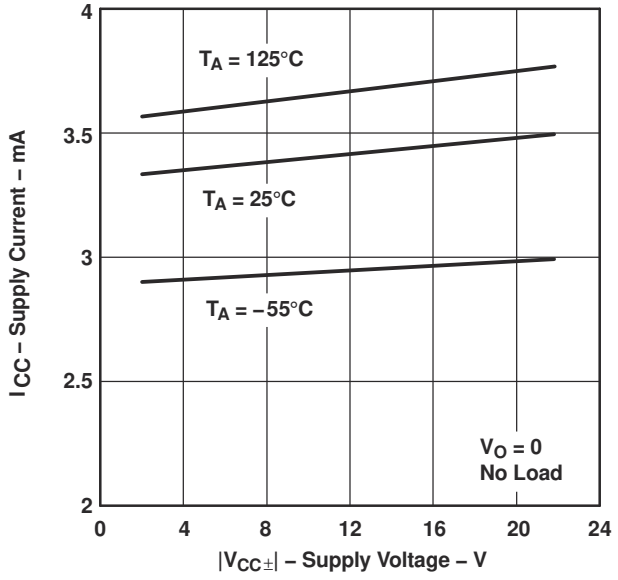

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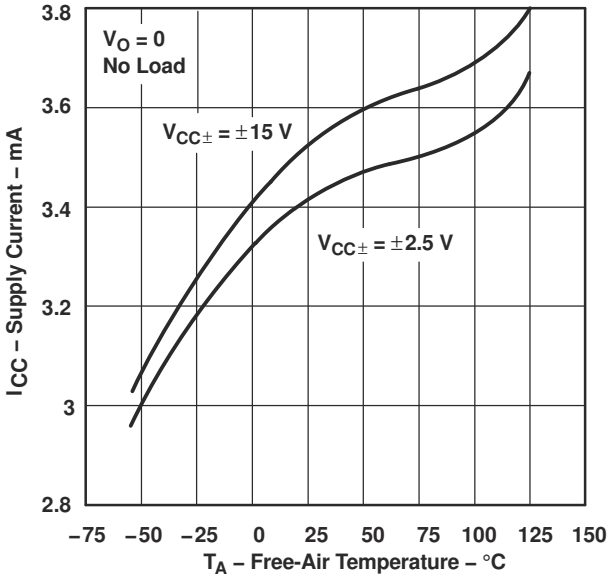

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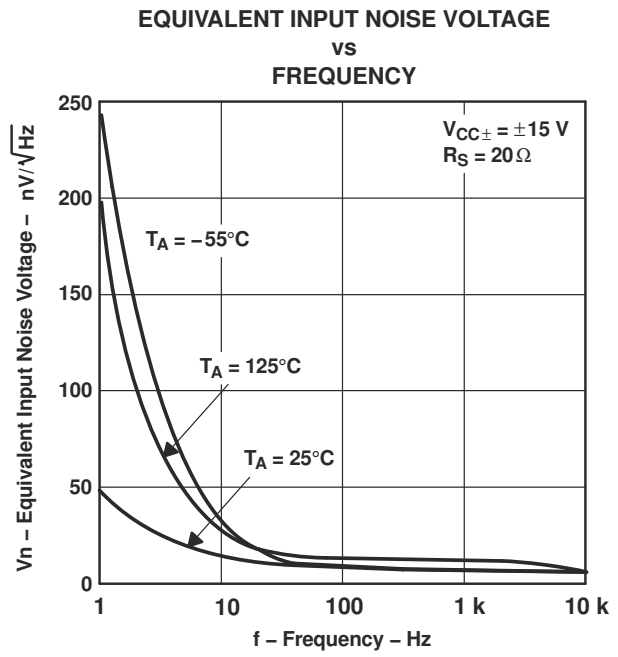
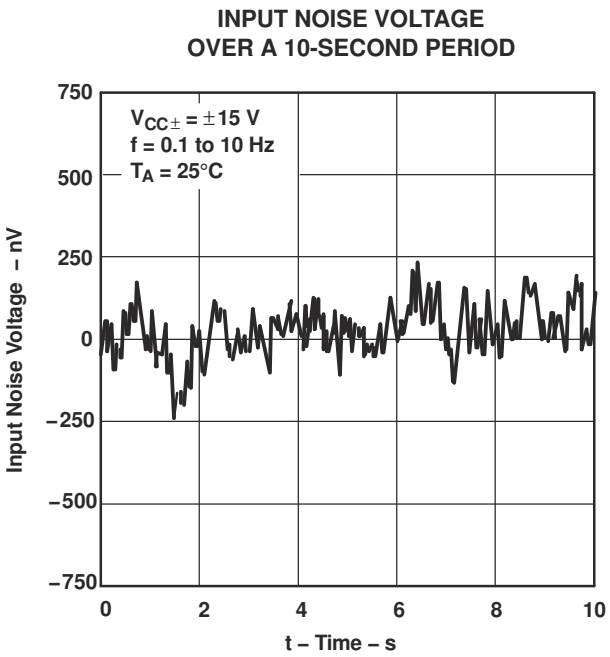


Figure 4-23.



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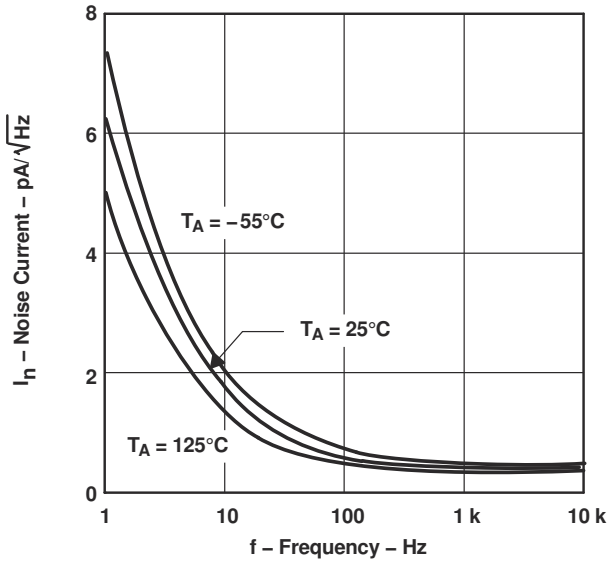

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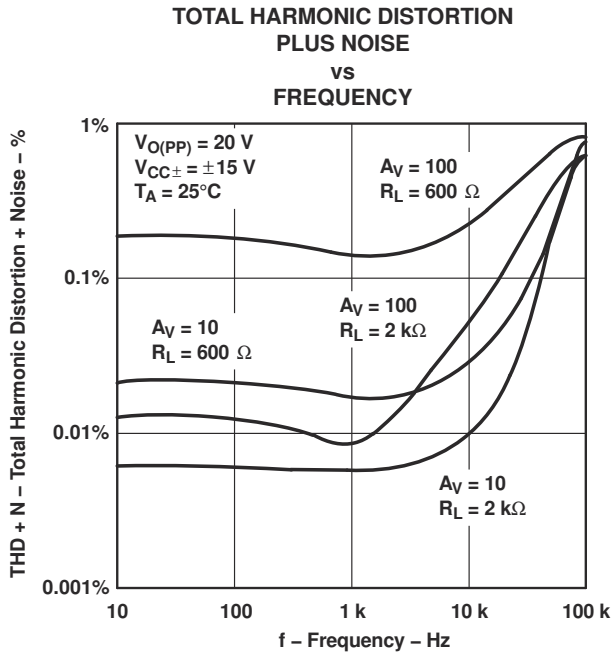
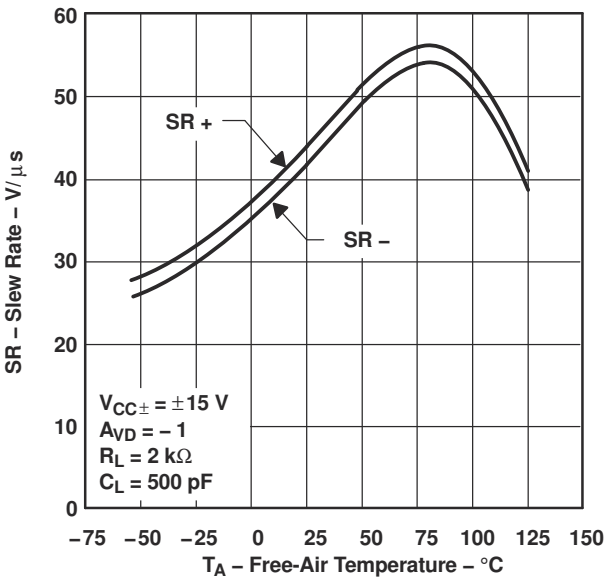


Figure 4-26.



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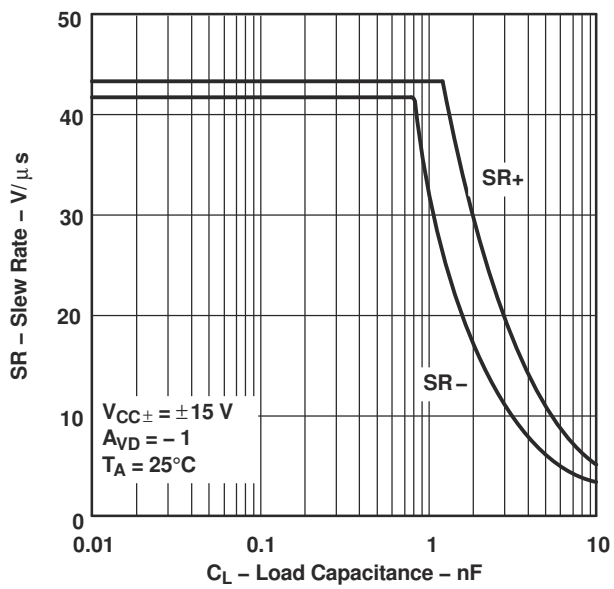

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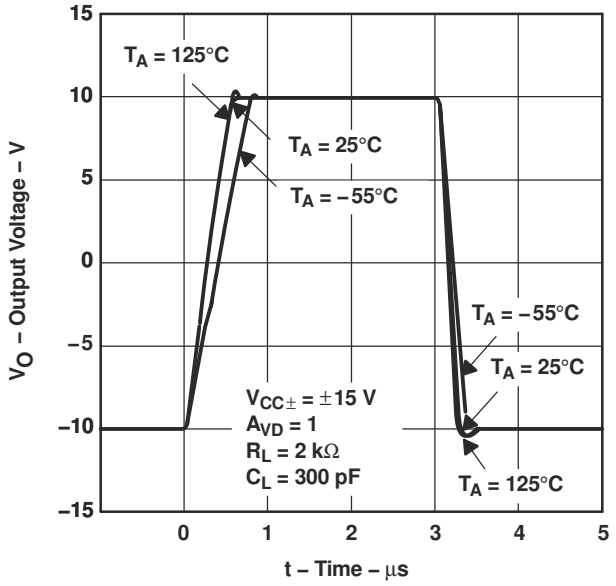

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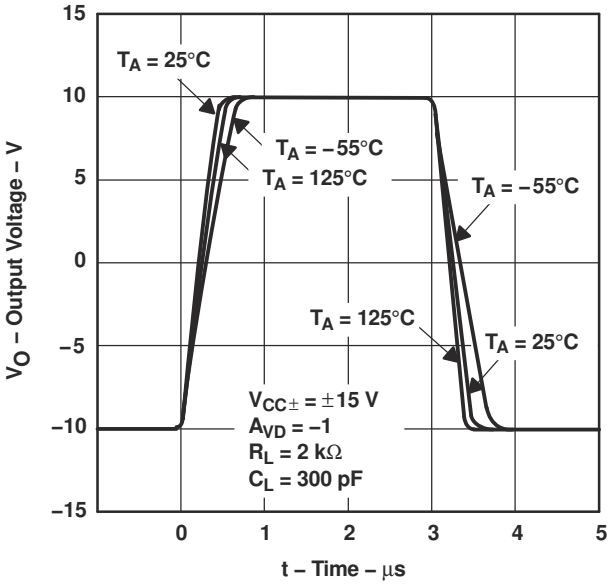

Figure 4-30.

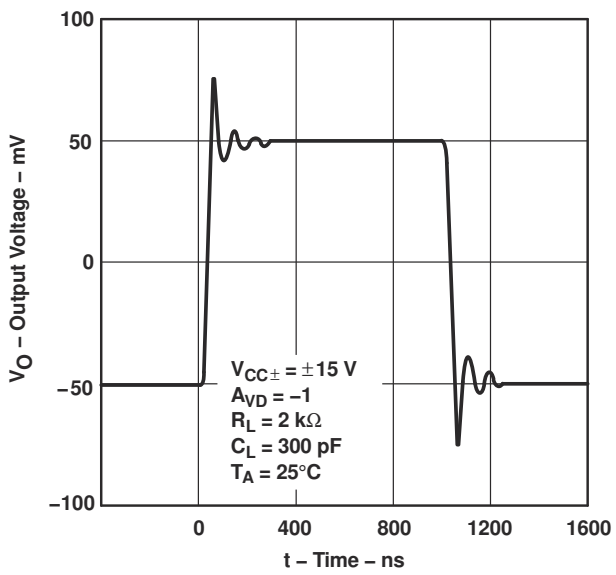

Figure 4-31.

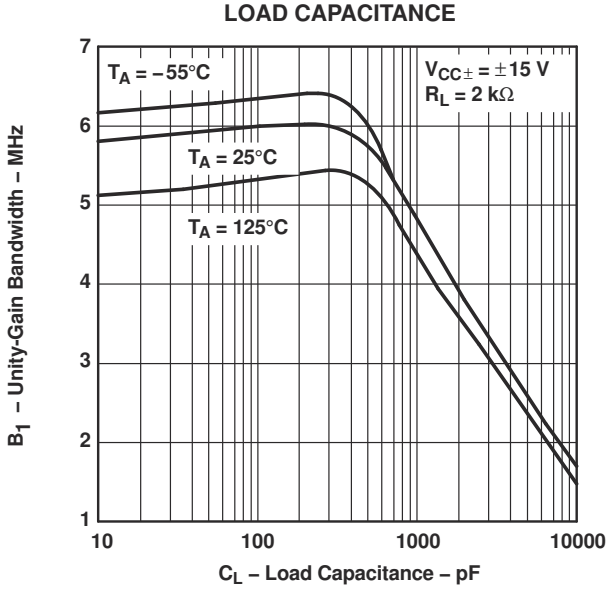

Figure 4-32.

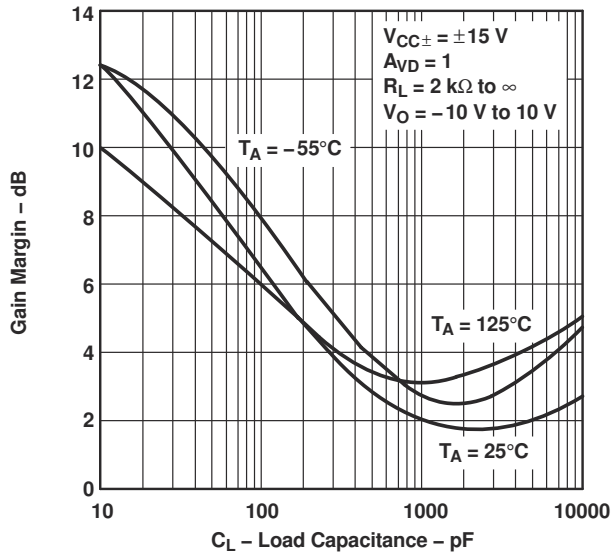

Figure 4-33.

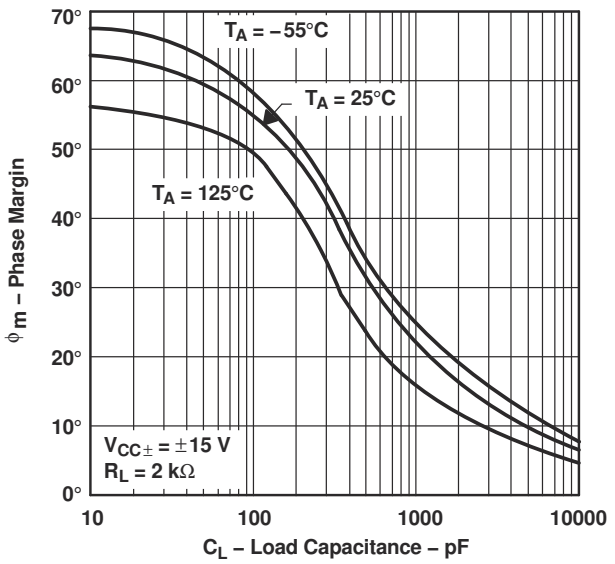

Figure 4-34.

5 Detailed Description

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

5.1 Overview

The TLE2142-Q1 is stable with capacitive loads up to 10nF, although the 6MHz bandwidth decreases to 1.8MHz at this high loading level. As such, this device is useful for low-droop sample-and-holds and direct buffering of long cables, including 4mA to 20mA current loops.

The special design also exhibits an improved insensitivity to inherent integrated circuit component mismatches as is evidenced by a 500µV maximum offset voltage and 1.7µV/°C typical drift. Minimum common-mode rejection ratio and supply-voltage rejection ratio are 85dB and 90dB, respectively.

Device performance is relatively independent of supply voltage over the ±2V to ±22V range. Inputs can operate between $V_{CC–}$ – 0.3V to V_{CC+} – 1.8V without inducing phase reversal, although excessive input current can flow out of each input exceeding the lower common-mode input range. The all-npn output stage provides a nearly rail-to-rail output swing of $V_{CC–}$ + 0.1V to V_{CC+} – 1V under light current-loading conditions. The device can sustain shorts to either supply, because output current is internally limited, but care must be taken to make sure that maximum package power dissipation is not exceeded.

The TLE2142-Q1 can also be used as a comparator. Differential inputs of $V_{CC±}$ can be maintained without damage to the device. Open-loop propagation delay with TTL supply levels is typically 200ns. This gives a good indication as to output stage saturation recovery when the device is driven beyond the limits of recommended output swing.

The TLE2142-Q1 is available in an industry-standard 8-pin small-outline (D) packages. The device is characterized for operation from –40°C to 125°C.

6 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

6.3 Trademarks

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All trademarks are the property of their respective owners.

6.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.5 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (July 2009) to Revision A (July 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Changed typical settling time specification from 0.34µs (0.1%, ±15V V_S) to 0.43µs, 0.4µs (0.01%, ±15V V_S) to 0.64µs, 0.16µs (0.1%, 5V V_S) to 0.66µs, and 0.22µs (0.01%, 5V V_S) to 0.99µs	3
• Changed typical THD+N specification at ±15V V_S from 0.01% to 0.06%	3
• Changed typical maximum output bandwidth specification at 5V V_S from 660kHz to 380kHz	3
• Added *ESD Ratings* table	3
• Added *Thermal Information* table	4

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLE2142QDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2142Q
TLE2142QDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2142Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TLE2142-Q1 :

- Catalog : TLE2142

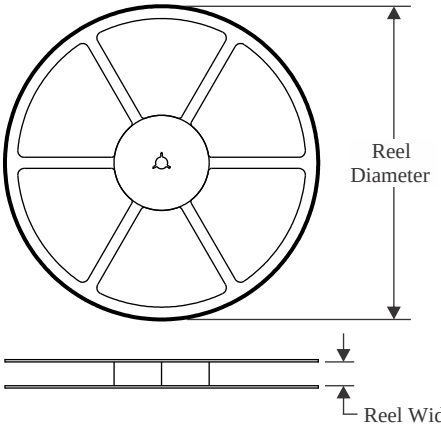
- Military : TLE2142M

NOTE: Qualified Version Definitions:

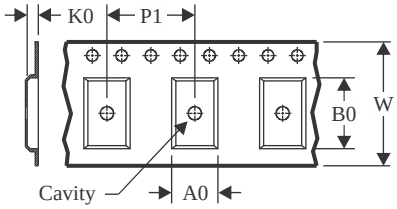
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

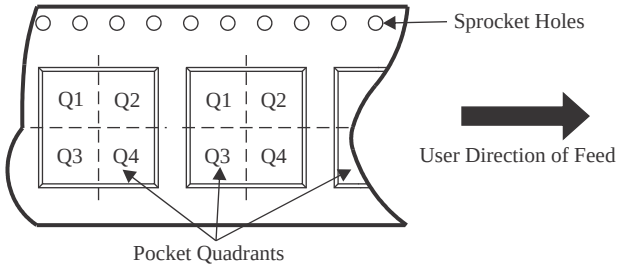


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

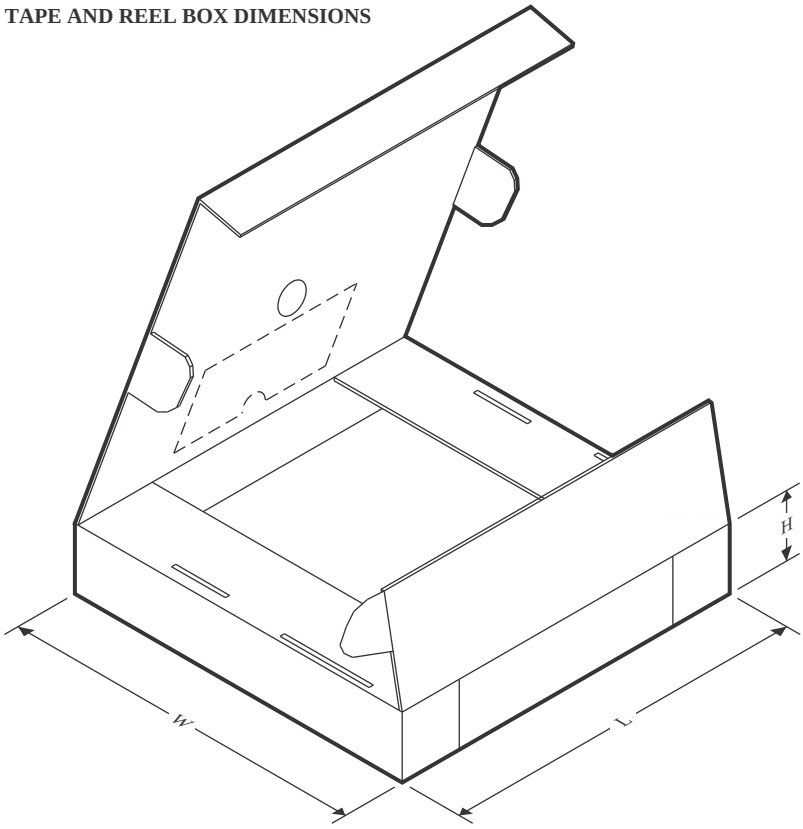
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

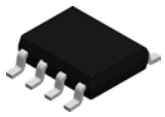
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLE2142QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLE2142QDRQ1	SOIC	D	8	2500	353.0	353.0	32.0

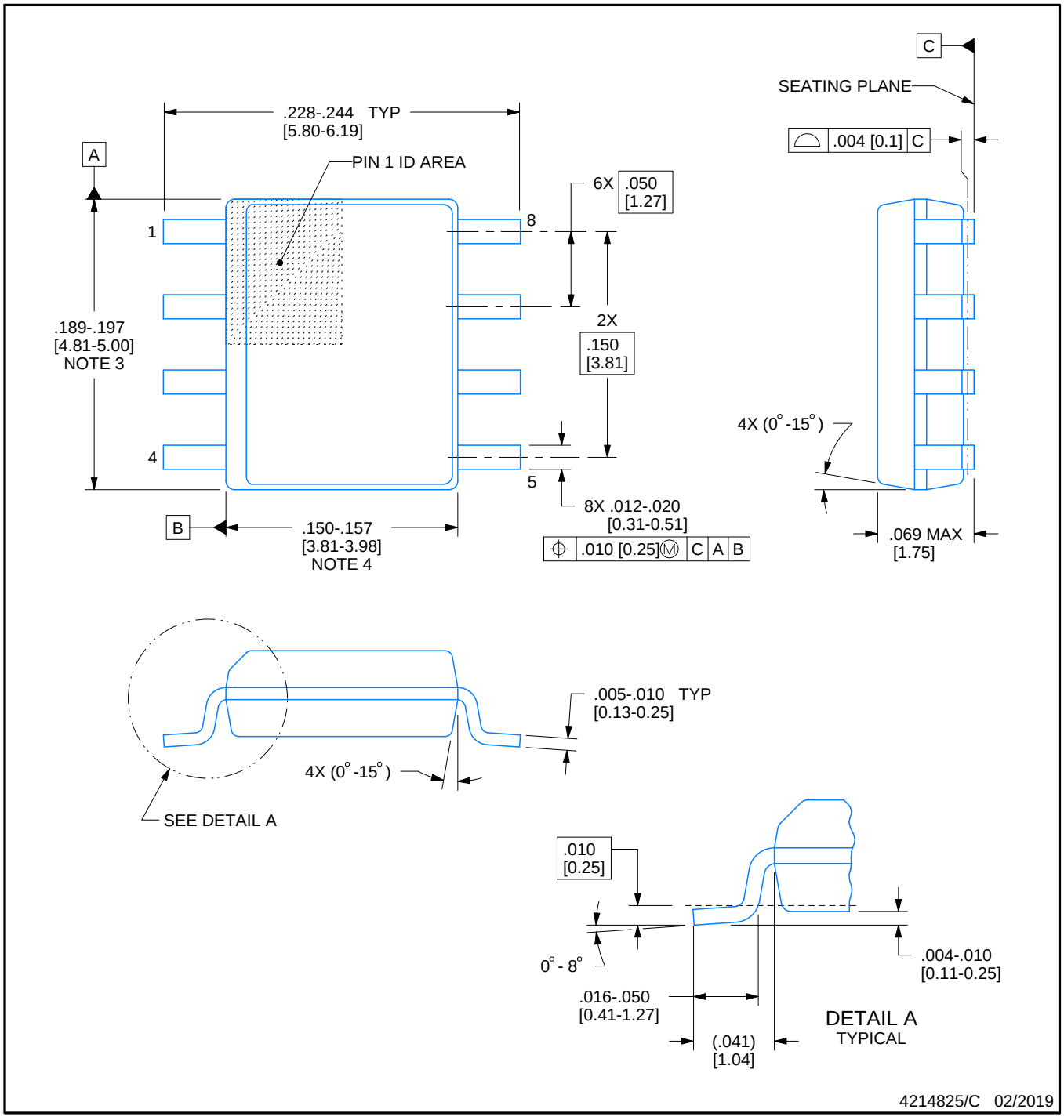


PACKAGE OUTLINE

D0008A

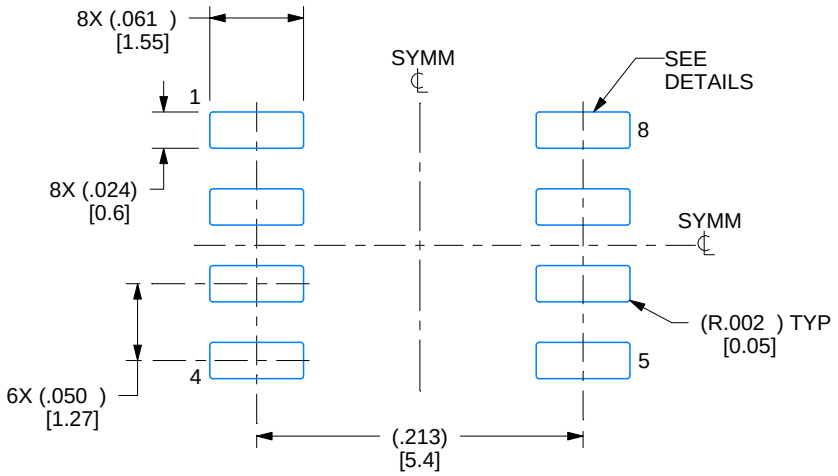
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

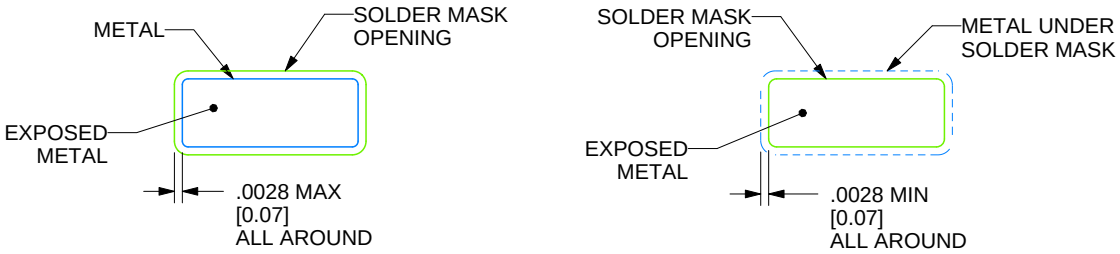


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

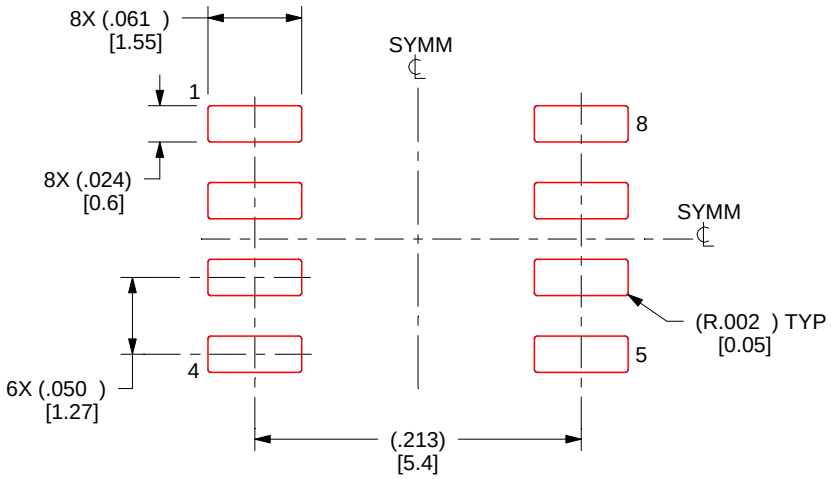
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025