TLIN829-Q1 Automotive Fault-Protected LIN Transceiver with Dominant State Timeout

1 Features

- AEC-Q100 Qualified for automotive applications
- Compliant with LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A and ISO 17987–4 electrical physical layer (EPL) specification
- Conforms to SAE J2602-1 LIN network for vehicle applications
- Functional Safety-Capable
  - Documentation available to aid in functional safety system design
- Supports 12V applications
- LIN transmit data rate up to 20kbps
- LIN receive data rate up to 100kbps
- Wide operational supply voltage range from 5.5V to 28V
- Sleep mode: ultra-low current consumption allows wake-up event from:
  - LIN bus
  - Local wake up through EN
- Power up and down glitch free operation on LIN bus and RXD output
- Protection features:
  - ±40V LIN bus fault tolerant
  - Under voltage protection on V_{SUP}
  - TXD Dominant time out protection (DTO)
  - Thermal shutdown protection
  - Unpowered node or ground disconnection failsafe at system level.
- Available in SOIC (8) and leadless VSON (8) with wettable flanks

2 Applications

- Body electronics and lighting
- Infotainment and cluster
- Hybrid electric vehicles and power train systems
- Passive safety
- Appliances

3 Description

The TLIN829-Q1 is a local interconnect network (LIN) physical layer transceiver with integrated wake-up and protection features, compliant with LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A and ISO/DIS 17987–4 standards. LIN is a single-wire bidirectional bus typically used for in-vehicle networks using data rates up to 20kbps. The TLIN829-Q1 is designed to support 12V applications with wider operating voltage and additional bus-fault protection.

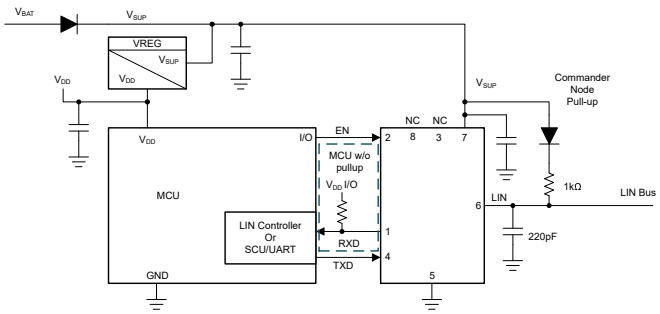
The LIN receiver supports data rates up to 100kbps for faster in-line programming. The TLIN829-Q1 converts the data stream on the TXD input into a LIN bus signal using a current-limited wave-shaping driver which reduces electromagnetic emissions (EME). The receiver converts the data stream to logic level signals that are sent to the microprocessor through the open-drain RXD pin. Ultra-low current consumption is possible using the sleep mode which allows wake-up via LIN bus or EN pin.

The TLIN829-Q1 integrates a resistor for LIN responder node applications, ESD protection, and fault protection which allow for a reduced amount of external components in the applications. The device prevents back-feed current through LIN to the supply input in case of a ground shift or supply voltage disconnection. The device also includes undervoltage detection, temperature shutdown protection, and loss-of-ground protection.

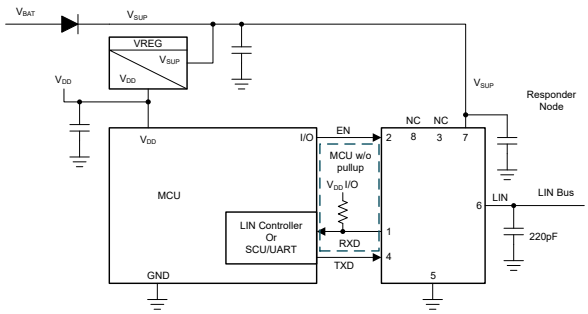
Package Information

PART NUMBER	PACKAGE(1)	PACFKAGE SIZE(2)
TLIN829-Q1	SOIC (D) (8)	4.9mm × 6mm
	VSON (DRB) (8)	3mm × 3mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematics, Commander Mode



Simplified Schematics, Responder Mode

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4 Pin Configuration and Functions

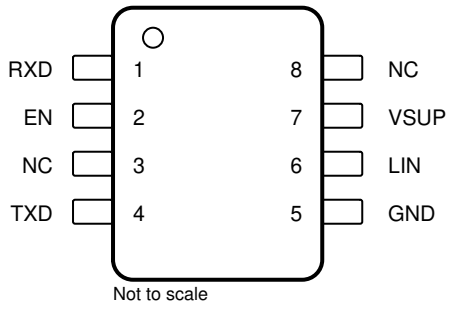

Figure 4-1. D Package, 8-Pin (SOIC), Top View

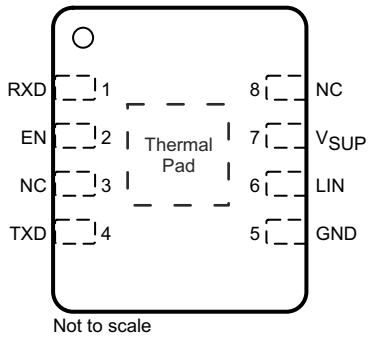

Figure 4-2. DRB Package, 8-Pin (VSON), Top View

Table 4-1. Pin Functions

PIN		Type	DESCRIPTION
Name	No.		
RXD	1	DO	RXD output (open-drain) interface reporting state of LIN bus voltage
EN	2	DI	Enable input - High puts the device in normal operation mode and low puts the device in sleep mode
NC	3	–	Not connected
TXD	4	DI	TXD input interface to control state of LIN output - Internally pulled to ground
GND	5	GND	Ground
LIN	6	HV I/O	LIN bus single-wire transmitter and receiver
V_{SUP}	7	HV Supply	Device supply voltage (connected to battery in series with external reverse blocking diode)
NC	8	–	Not connected
Thermal Pad		-	Can be connected to the PCB ground plane to improve thermal coupling (DRB package only)

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5 Specifications

5.1 Absolute Maximum Ratings

(1) (2)

		MIN	MAX	UNIT
V_{SUP}	Supply voltage range (ISO 17987)	–0.3	40	V
V_{LIN}	LIN Bus input voltage (ISO 17987)	–40	40	V
V_{LOGIC_INPUT}	Logic input voltage	–0.3	6	V
V_{LOGIC_OUTPUT}	Logic output voltage	–0.3	6	V
I_O	Digital pin output current		8	mA
T_J	Junction Temp	–40	165	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to the ground terminal.

5.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM) classification level 3A: LIN with respect to ground		±6000	V
		Human body model (HBM) classification level 3A: VSUP with respect to ground		±4000	V
		Human body model (HBM) classification level 2: RXD, EN, TXD, per AEC Q100-002(1)		±2000	V
		Charged device model (CDM) classification level C5, per AEC Q100-011	All pins	±500	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 ESD Ratings - IEC Specification

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	LIN, V_{SUP} terminal to GND(1)	IEC 62228-2 per ISO 10605 Contact discharge R = 330Ω, C = 150pF (IEC 61000-4-2)	±6000	V
		LIN terminal to GND(1)	IEC 62228-2 per ISO 10605 Indirect contact discharge R = 330Ω, C = 150pF (IEC 61000-4-2)	±8000	
V_{ESD}	Electrostatic discharge	LIN terminal to GND(2)	SAE J2962-1 per ISO 10605 R = 2kΩ, C = 330pF unpowered Contact discharge	±4000	V
			SAE J2962-1 per ISO 10605 R = 2kΩ, C = 330pF Powered Contact discharge	±8000	V
			SAE J2962-1 per ISO 10605 R = 2kΩ, C = 330pF Air discharge	±15000	V
			SAE J2962-1 per ISO 10605 R = 2kΩ, C = 150pF Air discharge	±25000	V

(1) Results given here are specific to the IEC 62228-2 Integrated circuits – EMC evaluation of transceivers – Part 2: LIN transceivers. Testing performed by OEM approved independent 3rd party, EMC report available upon request.
(2) Results given here are specific to the SAE J2962-1 Communication Transceivers Qualification Requirements - LIN. Testing performed by OEM approved independent 3rd party, EMC report available upon request.

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5.4 Thermal Information

THERMAL METRIC[1]		TLIN829D-Q1 SOIC 8 PINS	TLIN829DRB-Q1 VSON 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	TBA	TBA	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	TBA	TBA	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	TBA	TBA	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	TBA	TBA	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	TBA	TBA	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	TBA	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Recommended Operating Conditions

parameters valid across -40°C ≤ T_J ≤ 150°C (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{SUP}	Supply Voltage	5.5		28	V
V_{LIN}	LIN Bus input voltage	0		28	V
V_{LOGIC}	Logic Pin Voltage	0		5.25	V
T_J	Operating virtual junction temperature range	-40		150	°C
T_{SDR}	Thermal shutdown rising	160			°C
T_{SDF}	Thermal shutdown falling			150	°C
$T_{SD(HYS)}$	Thermal shutdown hysteresis		10		°C

5.6 Power Supply Characteristics

parameters valid across –40°C ≤ T_J ≤ 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage and Current						
V_{SUP}	Operational supply voltage	Device is operational beyond the LIN defined nominal supply voltage range	5.5		28	V
	Nominal supply voltage	Normal and standby modes [1]	5.5		24	V
		Sleep mode	5.5		24	V
I_{SUP}	Supply current Bus dominant	Normal mode EN = High, R_{LIN} ≥ 500Ω, C_{LIN} ≤ 10nF, INH = WAKE = V_{SUP}, V_{SUP} = 12V		1.2	3	mA
		Standby mode EN = 0V, R_{LIN} ≥ 500Ω, C_{LIN} ≤ 10nF, INH = WAKE = V_{SUP}, V_{SUP} = 12V		0.7	1.2	mA
	Supply current Bus recessive	Normal mode EN = High, INH = WAKE = V_{SUP}, V_{SUP} = 12V		300	700	µA
		Standby mode EN = 0V, INH = WAKE = V_{SUP}, V_{SUP} = 12V		20	55	µA
	Supply current Sleep mode	V_{SUP} = 12V, EN = 0V, LIN = WAKE = V_{SUP}, TXD and RXD floating		9	18	µA
		5.5V < V_{SUP} ≤ 24V, T_J = 150°C EN = 0V, LIN = WAKE = V_{SUP}, TXD and RXD floating			22	µA
UV_{SUPR}	Under voltage V_{SUP} threshold	Ramp up		4.6	4.9	V
UV_{SUPF}	Under voltage V_{SUP} threshold	Ramp down	4.1	4.45		V
U_{VHYS}	Delta hysteresis voltage for V_{SUP} under voltage threshold			0.15		V

(1) Normal mode ramp V_{SUP} while LIN signal is a 10kHz square wave with 50% duty cycle and 28V swing.

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5.7 Electrical Characteristics

parameters valid across –40°C ≤ T_J ≤ 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RXD Output Terminal						
V_{OL}	Low-level voltage	Based upon external pull-up to V_{CC} (4)			0.6	V
I_{OL}	Low-level output current, open drain	LIN = 0V, RXD = 0.4V	1.5			mA
I_{LKG}	Leakage current, high-level	LIN = V_{SUP}, RXD = V_{CC}	–5		5	µA
TXD Input Terminal						
V_{IL}	Low-level input voltage				0.8	V
V_{IH}	High-level input voltage		2			V
I_{LKG}	Low-level input leakage current	TXD = 0V	–5		5	µA
R_{TXD}	Internal pull-down resistor value		140	50	1200	kΩ
EN Input Terminal						
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{IH}	High-level input voltage		2		5.25	V
V_{HYS}	Hysteresis voltage	By design and characterization	30		500	mV
I_{IL}	Low-level input current	EN = 0V	–5		5	µA
R_{EN}	Internal pull-down resistor		140	500	1200	kΩ
LIN Terminal (Referenced to V_{SUP})						
V_{OH}	LIN recessive high-level output voltage(1) (2) (3)	TXD = High, I_O = 0mA 7V ≤ V_{SUP} ≤ 28V	0.8			V_{SUP}
V_{OH}	LIN recessive high-level output voltage(1) (2) (3)	TXD = High, I_O = 0mA 5.5V ≤ V_{SUP} ≤ 7V	3			V
V_{OL}	LIN dominant low-level output voltage(1) (2) (3)	TXD = 0V 7V ≤ V_{SUP} ≤ 28V			0.2	V_{SUP}
V_{OL}	LIN dominant low-level output voltage(1) (2) (3)	TXD = 0V 5.5V ≤ V_{SUP} ≤ 7V			1.2	V
V_{BUSdom}	Low-level input voltage(3)	LIN dominant (including LIN dominant for wake up)			0.4	V_{SUP}
V_{BUSrec}	High-level input voltage(3)	Lin recessive	0.6			V_{SUP}
V_{IH}	LIN recessive high-level input voltage(1) (2)	7V ≤ V_{SUP} ≤ 18V	0.47		0.6	V_{SUP}
V_{IL}	LIN dominant low-level input voltge(1) (2)	7V ≤ V_{SUP} ≤ 18V	0.4		0.53	V_{SUP}
$V_{SUP_NON_OP}$	V_{SUP} where impact of recessive LIN bus < 5%(3)	TXD & RXD open 5.5V ≤ V_{LIN} ≤ 40V	–0.3		40	V
V_{BUS_CNT}	Receiver center threshold(3)	V_{BUS_CNT} = (V_{BUSrec} + V_{BUSdom})/2	0.475	0.5	0.525	V_{SUP}
V_{HYS}	Hysteresis voltage (ISO 17987)	V_{HYS} = V_{BUSrec} - V_{BUSdom}			0.175	V_{SUP}
V_{HYS}	Hysteresis voltage (SAE J2602)	V_{HYS} = V_{IH} - V_{IL}	0.07		0.175	V_{SUP}
V_{SERIAL_DIODE}	Serial diode LIN termination pull-up path	I_{SERIAL_DIODE} = 10µA	0.4	0.7	1.0	V
$I_{BUS(LIM)}$	Limiting current ISO 17987 Param 12	TXD = 0V, V_{LIN} = 18V, V_{SUP} = 18V	40	90	200	mA
$I_{BUS_PAS_dom}$	Receiver leakage current, dominant	Driver off/recessive, LIN = 0V V_{SUP} = 12V	–1			mA
$I_{BUS_PAS_rec1}$	Receiver leakage current, recessive	Driver off/recessive, LIN ≥ V_{SUP} 5.5V ≤ V_{SUP} ≤ 28V			20	µA
$I_{BUS_PAS_rec2}$	Receiver leakage current, recessive	Driver off/recessive, LIN = V_{SUP}	–5		5	µA
$I_{BUS_NO_GND}$	Leakage current, loss of ground	GND_{Device} = V_{SUP} = 18V R_{Meas} = 1kΩ 0V < V_{LIN} < 18V	–1		1	mA
$I_{leak\ gnd(dom)}$	Leakage current, loss of ground(5)	V_{SUP} = 8V, GND = open, V_{SUP} = 18V, GND = open $R_{Commander}$ = 1kΩ, C_L = 1nF $R_{Responder}$ = 20kΩ, C_L = 1nF LIN = dominant	–1		1	mA

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parameters valid across –40°C ≤ T_J ≤ 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{leak\ gnd(rec)}$	Leakage current, loss of ground[5]	V_{SUP} = 8V, GND = open, V_{SUP} = 18V, GND = open $R_{Commander}$ = 1kΩ, C_L = 1nF $R_{Responder}$ = 20kΩ, C_L = 1nF LIN = recessive	–100		100	µA
$I_{BUS_NO_BAT}$	Leakage current, loss of supply	V_{SUP} = GND 0V ≤ V_{LIN} ≤ 18V			5	µA
I_{RSLEEP}	Pull-up current source to V_{SUP} sleep mode	V_{SUP} = 14V, LIN = GND	–20		–1.5	µA
R_{PU_SLP}	Internal pull-up resistor to V_{SUP} sleep mode	EN = 0V	1000	1700	2500	kΩ
R_{PU}	Internal pull-up resistor to V_{SUP}		27.66	37	48	kΩ
C_{LIN}	Capacitance of the LIN pin	V_{SUP} = 14V			25	pF
Duty Cycle Characteristics						
D1	Duty cycle 1[3] ISO 17987 Param 27/SAE J2602 Responder/ Commander	$TH_{REC(MAX)}$ = 0.744 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.581 x V_{SUP}, V_{SUP} = 7V to 18V, t_{BIT} = 50µs/52µs D1 = $t_{BUS_rec(min)}$/(2 x t_{BIT})	0.396			
$D1_{LB}$	Duty cycle 1[1] [2] [3] [6] ISO 17987 Low Battery Param 88/SAE J2602 Responder/Commander	$TH_{REC(MAX)}$ = 0.665 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.499 x V_{SUP} V_{SUP} = 5.5V to 7V, t_{BIT} = 50µs/52µs D1 = $t_{BUS_rec(min)}$/(2 x t_{BIT})	0.396			
D2	Duty cycle 2[3] ISO 17987 Param 28/SAE J2602 Responder/ Commander	$TH_{REC(MIN)}$ = 0.422 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.284 x V_{SUP}, V_{SUP} = 7.6V to 18V, t_{BIT} = 50µs/52µs D2 = $t_{BUS_rec(MAX)}$/(2 x t_{BIT})			0.581	
$D2_{LB}$	Duty cycle 2[1] [2] [3] [6] ISO 17987 Low Battery Param 89/SAE J2602 Responder/Commander	$TH_{REC(MIN)}$ = 0.496 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.361 x V_{SUP}, V_{SUP} = 6.1V to 7.6V, t_{BIT} = 50µs/52µs D2 = $t_{BUS_rec(MAX)}$/(2 x t_{BIT})			0.581	
D3	Duty cycle 3[3] ISO 17987 Param 29/SAE J2602 Responder/ Commander	$TH_{REC(MAX)}$ = 0.778 x V_{SUP} $TH_{DOM(MAX)}$ = 0.616 x V_{SUP} V_{SUP} = 7V to 18V, t_{BIT} = 96µs D3 = $t_{BUS_rec(min)}$/(2 x t_{BIT})	0.417			
$D3_{LB}$	Duty cycle 3[1] [2] [3] [6] ISO 17987 Low Battery Param 90/SAE J2602 Responder/Commander	$TH_{REC(MAX)}$ = 0.665 x V_{SUP} $TH_{DOM(MAX)}$ = 0.499 x V_{SUP} V_{SUP} = 5.5V to 7V, t_{BIT} = 96µs D3 = $t_{BUS_rec(min)}$/(2 x t_{BIT})	0.417			
D4	Duty cycle 4[3] ISO 17987 Param 30/SAE J2602 Responder/ Commander	$TH_{REC(MIN)}$ = 0.389 x V_{SUP} $TH_{DOM(MIN)}$ = 0.251 x V_{SUP} V_{SUP} = 7.6V to 18V, t_{BIT} = 96µs D4 = $t_{BUS_rec(MAX)}$/(2 x t_{BIT})			0.59	
$D4_{LB}$	Duty cycle 4[1] [2] [3] [6] ISO 17987 Low Battery Param 91/SAE J2602 Responder/Commander	$TH_{REC(MAX)}$ = 0.496 x V_{SUP} $TH_{DOM(MAX)}$ = 0.361 x V_{SUP} V_{SUP} = 6.1V to 7.6V, t_{BIT} = 96µs D4 = $t_{BUS_rec(MAX)}$/(2 x t_{BIT})			0.59	
$T_{r\text{-}d\ max}$	Transmitter propagation delay timings for the duty cycle[1] [2] [6] Recessive to dominant	$TH_{REC(MAX)}$ = 0.744 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.581 x V_{SUP} 7V ≤ V_{SUP} ≤ 18V, t_{BIT} = 52µs $t_{REC(MAX)_D1}$ - $t_{DOM(MIN)_D1}$			10.8	µs
$T_{d\text{-}r\ max}$	Transmitter propagation delay timings for the duty cycle[1] [2] [6] Dominant to recessive	$TH_{REC(MAX)}$ = 0.422 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.284 x V_{SUP} 7.6V ≤ V_{SUP} ≤ 18V, t_{BIT} = 52µs $t_{DOM(MAX)_D2}$ - $t_{REC(MIN)_D2}$			8.4	µs
$T_{r\text{-}d\ max}$	Transmitter propagation delay timings for the duty cycle[1] [2] [6] Recessive to dominant	$TH_{REC(MAX)}$ = 0.778 x V_{SUP} $TH_{DOM(MAX)}$ = 0.616 x V_{SUP} 7V ≤ V_{SUP} ≤ 18V, t_{BIT} = 96µs $t_{REC(MAX)_D3}$ - $t_{DOM(MIN)_D3}$			15.9	µs
$T_{d\text{-}r\ max}$	Transmitter propagation delay timings for the duty cycle[1] [2] [6] Dominant to recessive	$TH_{REC(MIN)}$ = 0.389 x V_{SUP} $TH_{DOM(MIN)}$ = 0.251 x V_{SUP} 7.6V ≤ V_{SUP} ≤ 18V, t_{BIT} = 96µs $t_{DOM(MAX)_D4}$ - $t_{REC(MIN)_D4}$			17.28	µs
$T_{r\text{-}d\ max_low}$	Low battery transmitter propagation delay timings for the duty cycle[1] [2] [6] Recessive to dominant	$TH_{REC(MAX)}$ = 0.665 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.499 x V_{SUP} 5.5V ≤ V_{SUP} ≤ 7V, t_{BIT} = 52µs $t_{REC(MAX)_low}$ - $t_{DOM(MIN)_low}$			10.8	µs

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parameters valid across –40°C ≤ T_J ≤ 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_{d\text{-}r\ max_low}$	Low battery transmitter propagation delay timings for the duty cycle(1) (2) (6) Dominant to recessive	$TH_{REC(MAX)}$ = 0.496 x V_{SUP} $TH_{DOM(MAX)}$ = 0.361 x V_{SUP} 6.1V ≤ V_{SUP} ≤ 7.6V, t_{BIT} = 52µs $t_{DOM(MAX)_low}$ - $t_{REC(MIN)_low}$			8.4	µs

(1) SAE 2602 commander node load conditions: 5.5nF/4kΩ and 899pF/20kΩ; t_{BIT} = 52µs and 96µs
(2) SAE 2602 responder node load conditions: 5.5nF/875Ω and 899pF/900Ω; t_{BIT} = 52µs and 96µs
(3) ISO 17987 bus load conditions (C_{LINBUS}, R_{LINBUS}) include 1nF/1kΩ; 6.8nF/660Ω; 10nF/500Ω; t_{BIT} = 50µs and 96µs
(4) RXD uses open drain output structure therefore V_{OL} level is based upon microcontroller supply voltage.
(5) $I_{leak\ gnd}$ = (V_{BAT} - V_{LIN})/R_{Load}
(6) Specified by design

5.8 AC Switching Characteristics

parameters valid across -40°C ≤ T_J ≤ 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Device Switching Characteristics						
t_{rx_pdf}	Receiver falling propagation delay time ISO 17987 Param 31	5.5V ≤ VSUP, R_{RXD} = 2.4kΩ, C_{RXD} = 20pF			6	µs
t_{rx_pdf}	Receiver falling propagation delay time ISO 17987 Param 31				6	µs
t_{rs_sym}	Symmetry of receiver propagation delay time Receiver rising propagation delay time ISO 17987 Param 32	Rising edge with respect to falling edge t_{rx_sym} = t_{rx_pdf} – t_{rx_pdr}), R_{RXD} = 2.4kΩ, C_{RXD} = 20pF	–2		2	µs
t_{LINBUS}	Minimum dominant time on LIN bus for wake-up		25	65	150	µs
t_{CLEAR}	Time to clear false wake-up prevention logic if LIN bus had a bus stuck dominant fault (recessive time on LIN bus to clear bus stuck dominant fault)		8	25	50	µs
t_{MODE_CHANGE}	Mode change delay time	Time to change from normal mode to sleep mode through EN pin	2		15	µs
t_{NOMINT}	Normal mode initialization time(1)	Time for normal mode to initialize and data on RXD pin to be valid, includes t_{MODE_CHANGE} for standby to normal mode.			45	µs
t_{PWR}	Power-up time	Time it takes for valid data on RXD upon power-up			1.5	ms
t_{TXD_DTO}	Dominant state time out		20	50	80	ms

(1) The transition time from sleep mode to normal mode includes both t_{MODE_CHANGE} and t_{NOMINT}.

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6 Parameter Measurement Information

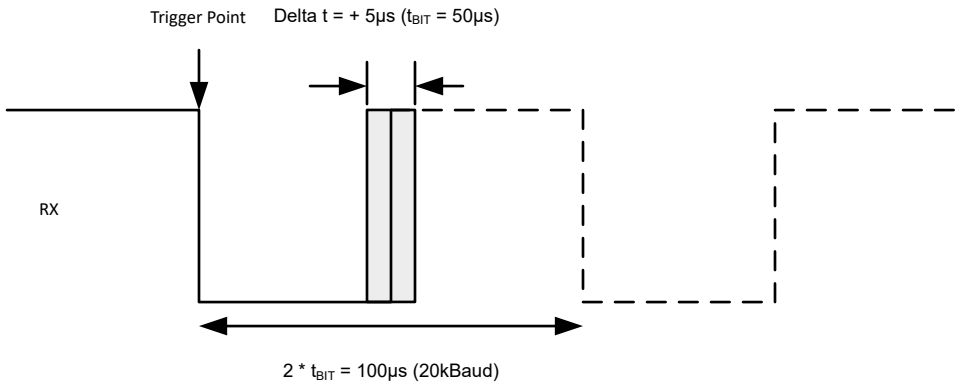

Figure 6-1. RX Response: Operating Voltage Range

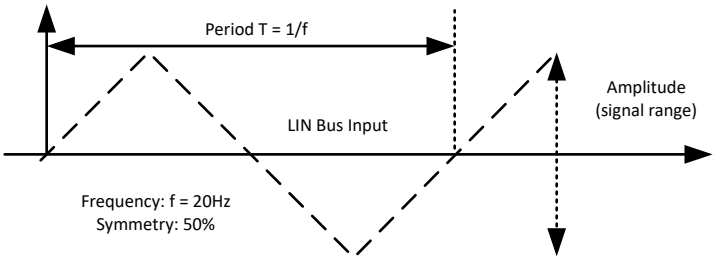

Figure 6-2. LIN Bus Input Signal

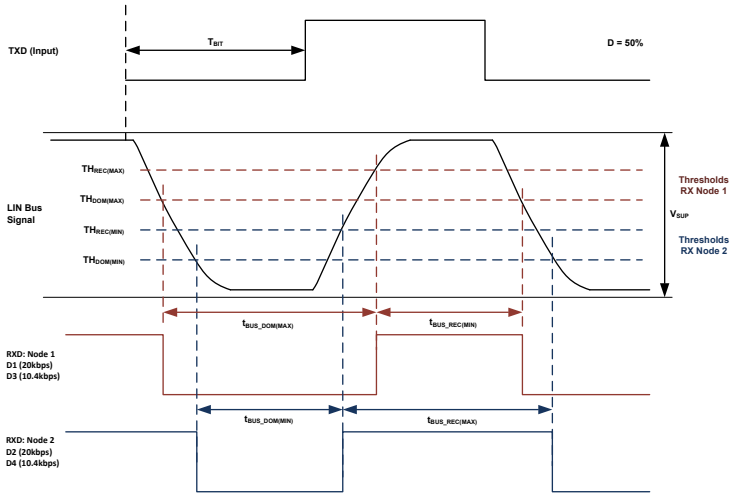

Figure 6-3. Definition of Bus Timing Parameters

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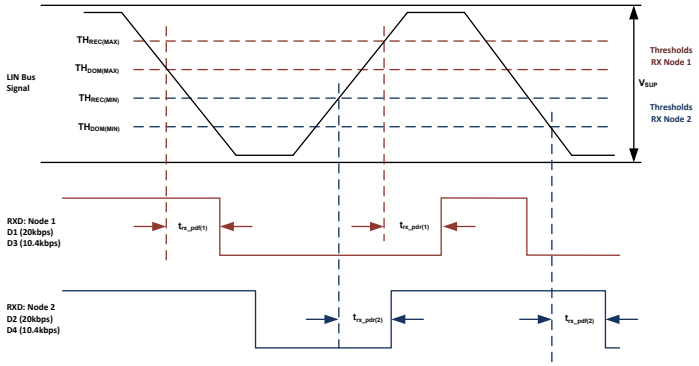

Figure 6-4. Propagation Delay

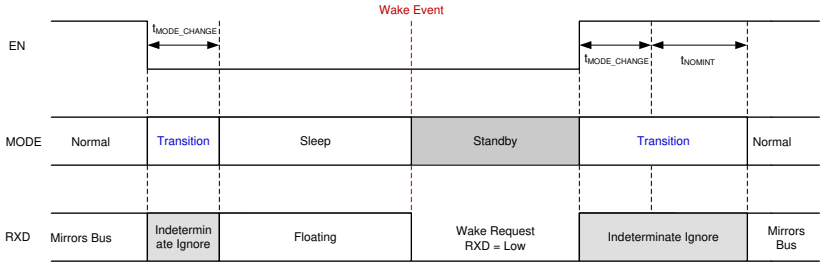

Figure 6-5. Mode Transitions

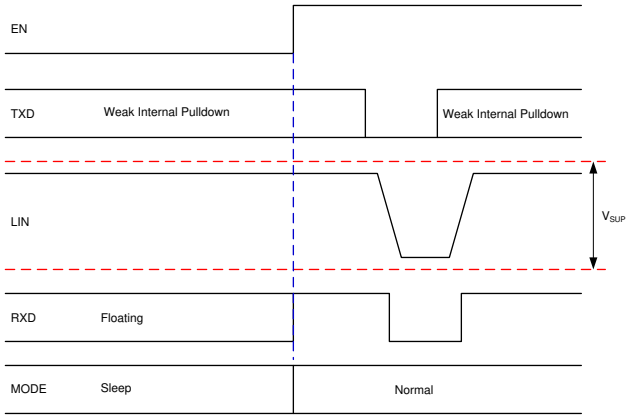

Figure 6-6. Wakeup Through EN

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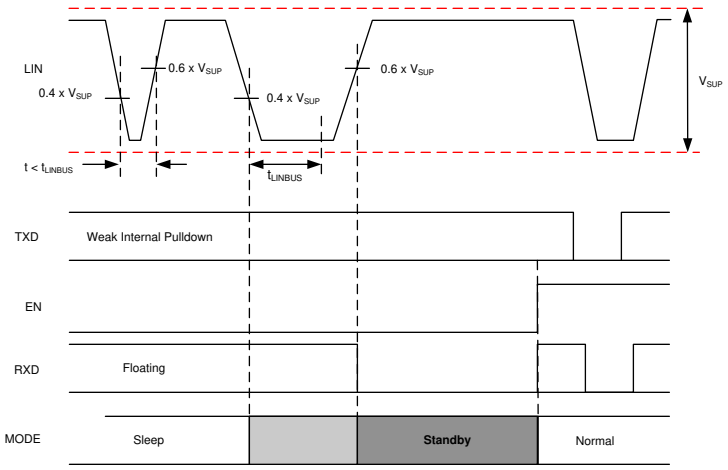

Figure 6-7. Wakeup through LIN

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7 Detailed Description

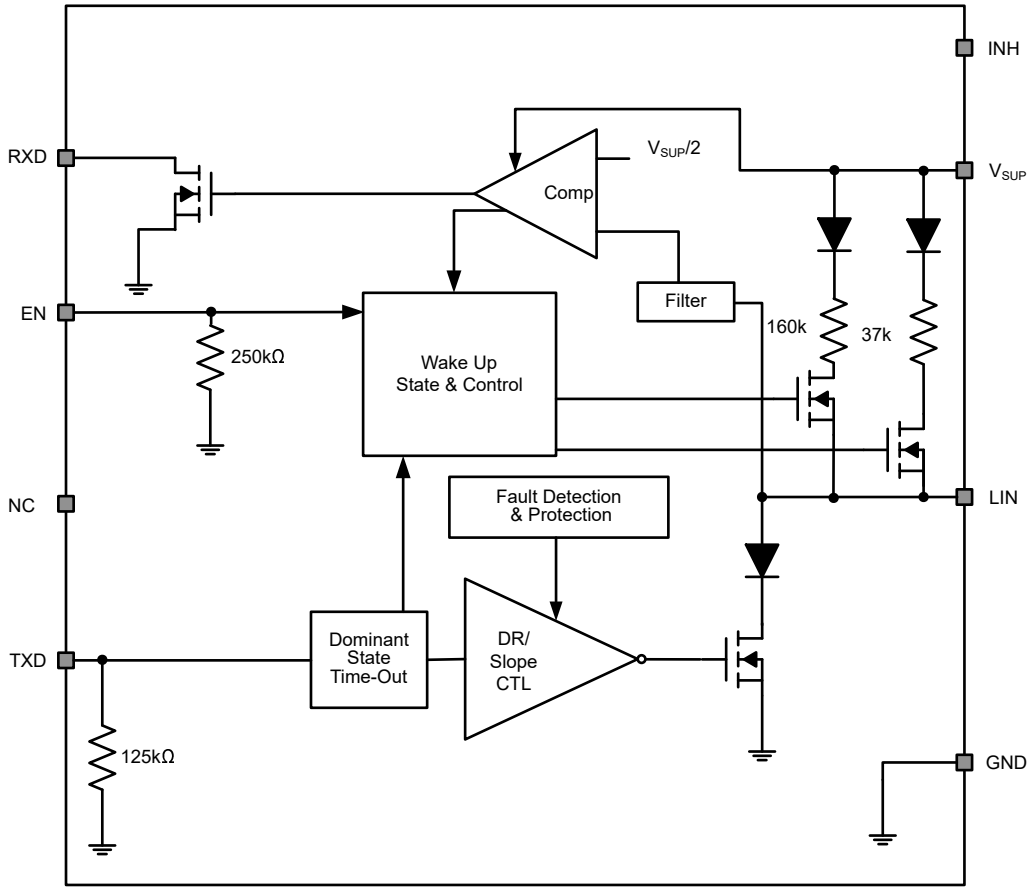
7.1 Overview

The TLIN829-Q1 is a Local Interconnect Network (LIN) physical layer transceiver, compliant with LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A and ISO/DIS 17987–4 standards, with integrated wake-up and protection features. The LIN bus is a single-wire bidirectional bus typically used for low speed in-vehicle networks. The device transmitter supports data rates from 2.4kbps to 20kbps and the receiver works up to 100kbps supporting in-line programming. The LIN protocol data stream on the TXD input is converted by the TLIN829-Q1 into a LIN bus signal using a current-limited wave-shaping driver as outlined by the LIN physical layer specification. The receiver converts the data stream to logic-level signals that are sent to the microprocessor through the open-drain RXD pin. The LIN bus has two states: dominant state (voltage near ground) and recessive state (voltage near battery). In the recessive state, the LIN bus is pulled high by the internal pull-up resistor (37kΩ) and a series diode. No external pull-up components are required for responder node applications. commander node applications require an external pull-up resistor (1kΩ) plus a series diode per the LIN specification.

The device is designed to support 12V applications with a wide input voltage operating range and also supports low-power sleep mode. The device also provides two methods to wake up: EN pin and from the LIN bus.

The TLIN829-Q1 integrates ESD protection and fault protection which allow for a reduction in the required external components in the applications. In the event of a ground shift or supply voltage disconnection, the device prevents back-feed current through LIN to the supply input. The device also includes undervoltage detection, temperature shutdown protection, and loss-of-ground protection.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 LIN (Local Interconnect Network) Bus

This high voltage input/output pin is a single-wire LIN bus transmitter and receiver. The LIN pin can survive transient voltages up to 40V. Reverse currents from the LIN to supply (V_{SUP}) are minimized with blocking diodes, even in the event of a ground shift or loss of supply (V_{SUP}).

7.3.1.1 LIN Transmitter Characteristics

The transmitter has thresholds and AC parameters according to the LIN specification. The transmitter is a low-side transistor with internal current limitation and thermal shutdown. During a thermal shut-down condition, the transmitter is disabled to protect the device. There is an internal pull-up resistor with a serial diode structure to V_{SUP}, so no external pull-up components are required for the LIN responder node applications. An external pull-up resistor and series diode to V_{SUP} must be added when the device is used for a commander node application.

7.3.1.2 LIN Receiver Characteristics

The receiver characteristic thresholds are proportional to the device supply pin in accordance to the LIN specification.

The receiver is capable of receiving higher data rates (> 100kbps) than supported by LIN or SAEJ2602 specifications. This allows the TLIN829-Q1 to be used for high speed downloads at the end-of-line production or other applications. The actual data rate achievable depends on system time constants (bus capacitance and pull-up resistance) and driver characteristics used in the system.

7.3.1.2.1 Termination

There is an internal pull-up resistor with a serial diode structure to V_{SUP}, so no external pull-up components are required for the LIN responder node applications. An external pull-up resistor (1kΩ) and a series diode to V_{SUP} must be added when the device is used for commander node applications as per the LIN specification.

Figure 7-1 shows a commander node configuration and how the voltage levels are defined

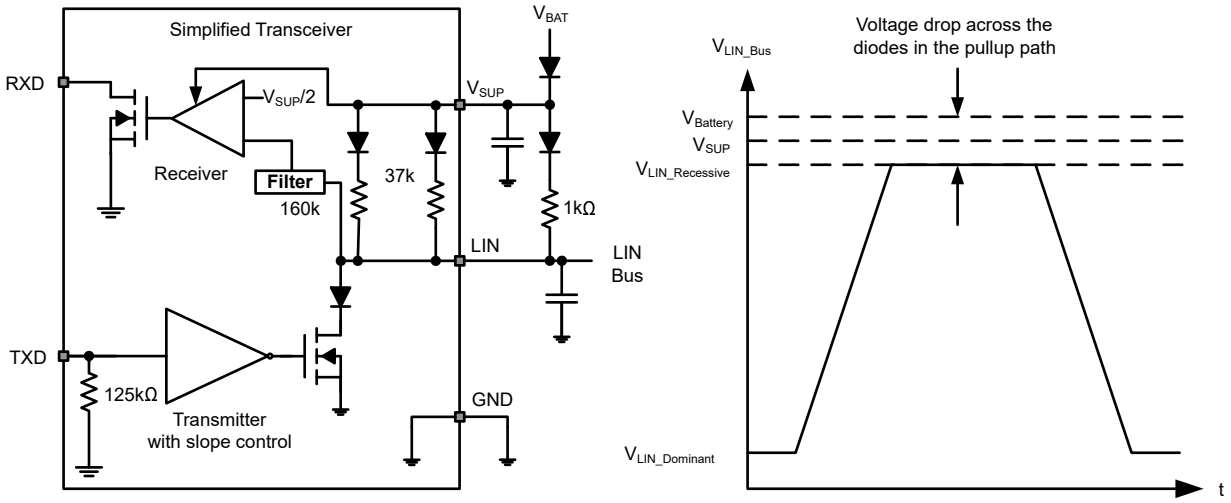

Figure 7-1. Commander Node Configuration with Voltage Levels

7.3.2 TXD (Transmit Input and Output)

TXD is the interface to the MCUs LIN protocol controller or SCI and UART that is used to control the state of the LIN output. When TXD is low, the LIN output is dominant (near ground). When TXD is high, the LIN output is recessive (near $V_{Battery}$). See Figure 7-1. The TXD input structure is compatible with microcontrollers with 3.3V and 5V I/O interfaces.

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7.3.3 RXD (Receive Output)

RXD is the interface to the MCU LIN protocol controller or SCI and UART, which reports the state of the LIN bus voltage. LIN recessive (near $V_{Battery}$) is represented by a high level on the RXD and LIN dominant (near ground) is represented by a low level on the RXD pin. The RXD output structure is an open-drain output stage. This allows the device to be used with 3.3V and 5V I/O microcontrollers. If the microcontroller RXD pin does not have an integrated pull-up, an external pull-up resistor to the microcontroller I/O supply voltage is required. In standby mode, the RXD pin is driven low to indicate a wake up request from the LIN bus.

7.3.4 V_{SUP} (Supply Voltage)

V_{SUP} is the power supply pin. V_{SUP} is connected to the battery through an external reverse-blocking diode (Figure 7-1). If there is a loss of power at the ECU level, the device has low leakage from the LIN pin, which does not load the bus down. This is appropriate for LIN systems in which some of the nodes are unpowered (ignition supplied) while the rest of the network remains powered (battery supplied).

7.3.5 GND (Ground)

GND is the device ground connection. The device can operate with a ground shift as long as the ground shift does not reduce the V_{SUP} below the minimum operating voltage, as well as ensuring the input and output voltages are within their appropriate thresholds. If there is a loss of ground at the ECU level, the device has extremely low leakage from the LIN pin, which does not load the bus down. This is optimal for LIN systems in which some of the nodes are unpowered (ignition supplied) while the rest of the network remains powered (battery supplied).

7.3.6 EN (Enable Input)

EN controls the operational modes of the device. When EN is high the device is in normal operating mode allowing a transmission path from TXD to LIN and from LIN to RXD. When EN is low the device is put into sleep mode and there are no transmission paths available. The device can enter normal mode only after wake up. EN has an internal pull-down resistor to make sure the device remains in low-power mode even if EN floats.

7.3.7 Protection Features

The TLIN829-Q1 has several protection features described as follows.

7.3.8 TXD Dominant Time Out (DTO)

During normal mode, if TXD is inadvertently driven permanently low by a hardware or software application failure, the LIN bus is protected by the dominant state timeout timer. This timer is triggered by a falling edge on the TXD pin. If the low signal remains on TXD for longer than t_{DST}, the transmitter is disabled, thus allowing the LIN bus to return to recessive state and communication to resume on the bus. The protection is cleared and the t_{DST} timer is reset by a rising edge on TXD. The TXD pin has an internal pull-down to ensure the device fails to a known state if TXD is disconnected. During this fault, the transceiver remains in normal mode (assuming no change of stated request on EN), the transmitter is disabled, the RXD pin reflects the LIN bus and the LIN bus pull-up termination remains on.

7.3.9 Bus Stuck Dominant System Fault: False Wake Up Lockout

The TLIN829-Q1 contains logic to detect bus stuck dominant system faults and prevents the device from waking up falsely during the system fault. Upon entering sleep mode, the device detects the state of the LIN bus. If the bus is dominant, the wake-up logic is locked out until a valid recessive on the bus *clears* the bus stuck dominant, preventing excessive current consumption. Figure 7-2 and Figure 7-3 show the behavior of this protection.

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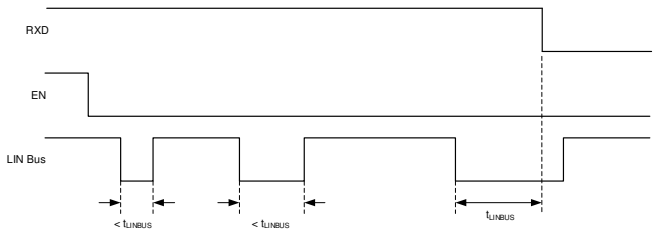

Figure 7-2. No Bus Fault: Entering Sleep Mode with Bus Recessive Condition and Wakeup

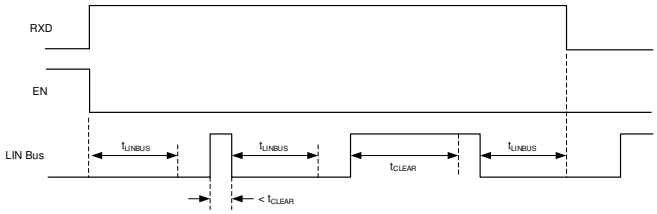

Figure 7-3. Bus Fault: Entering Sleep Mode with Bus Stuck Dominant Fault, Clearing, and Wakeup

7.3.10 Thermal Shutdown

The LIN transmitter is protected by current limiting circuitry; however, if the junction temperature of the device exceeds the thermal shutdown threshold, the device puts the LIN transmitter into the recessive state. Once the over-temperature fault condition has been removed and the junction temperature has cooled beyond the hysteresis temperature, the transmitter is re-enabled, assuming the device remained in the normal operation mode. During this fault, the transceiver remains in normal mode (assuming no change of state request on EN), the transmitter is in recessive state, the RXD pin reflects the LIN bus and LIN bus pull-up termination remains on.

7.3.11 Under Voltage on V_{SUP}

The TLIN829-Q1 contains a power-on reset circuit to avoid false bus messages during under voltage conditions when V_{SUP} is less than UV_{SUP}.

7.3.12 Unpowered Device and LIN Bus

In automotive applications, some LIN nodes in a system can be unpowered (ignition supplied) while others in the network remain powered by the battery. The TLIN829-Q1 has low unpowered leakage current from the bus, so an unpowered node does not affect the network or load it down.

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7.4 Device Functional Modes

The TLIN829-Q1 has three functional modes of operation: normal, sleep, and standby. The next sections describes these modes as well as how the device moves between the different modes. Figure 7-4 graphically shows the relationship while Table 7-1 shows the state of pins.

Table 7-1. Operating Modes

MODE	EN	RXD	LIN BUS TERMINATION	TRANSMITTER	COMMENT
Sleep	Low	Floating	Weak current pull-up	Off	
Standby	Low	Low	37kΩ (typical)	Off	Wake-up event detected, waiting on MCU to set EN
Normal	High	LIN bus data	37kΩ (typical)	On	LIN transmission up to 20kbps

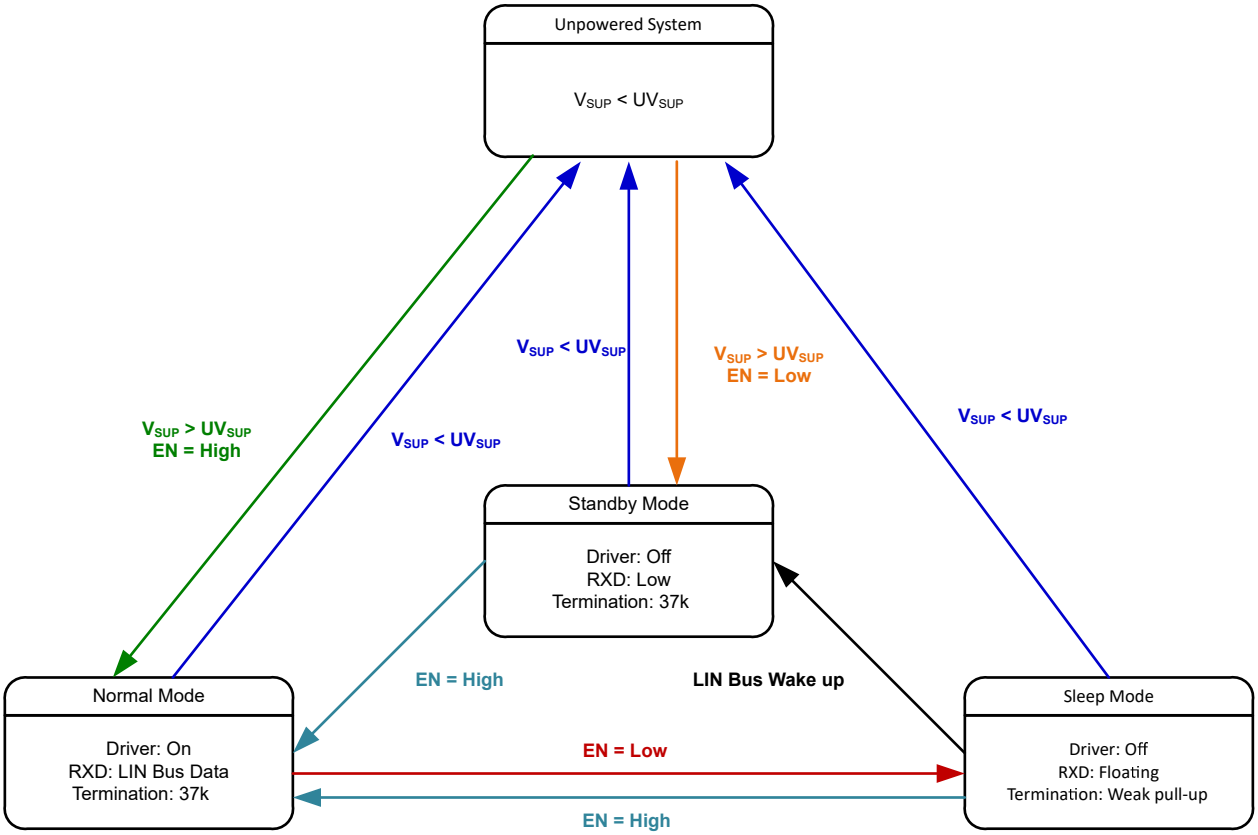

Figure 7-4. Operating State Diagram

7.4.1 Normal Mode

If the EN pin is high at power up, the device will power up in normal mode. If the EN pin is low, it will power up in standby mode. The EN pin controls the mode of the device. In normal operational mode the receiver and transmitter are active and the LIN transmission up to the LIN specified maximum of 20kbps is supported. The receiver detects the data stream on the LIN bus and outputs it on RXD for the LIN controller. A recessive signal on the LIN bus is a logic high and a dominant signal on the LIN bus is a logic low. The driver transmits input data from TXD to the LIN bus. Normal mode is entered as EN transitions high while the TLIN829-Q1 is in sleep or standby mode for > t_{MODE_CHANGE} plus t_{NOMINT}.

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7.4.2 Sleep Mode

Sleep mode is the power saving mode for the TLIN829-Q1. Sleep mode is only entered when the EN pin is low and from normal mode. Even with extremely low current consumption in this mode, the TLIN829-Q1 can still wake up from LIN bus through a wake-up signal or if EN is set high for ≥ t_{MODE_CHANGE}. The LIN bus is filtered to prevent false wake up events. The wake-up events must be active for the respective time periods (t_{LINBUS}).

The sleep mode is entered by setting EN low for longer than t_{MODE_CHANGE}.

While the device is in sleep mode, the following conditions exist:

- The LIN bus driver is disabled and the internal LIN bus termination is switched off (to minimize power loss if LIN is short circuited to ground). However, the weak current pull-up is active to prevent false wake up events in case an external connection to the LIN bus is lost.
- The normal receiver is disabled.
- EN input and LIN wake up receiver are active.

7.4.3 Standby Mode

This mode is entered whenever a wake up event occurs through LIN bus while the device is in sleep mode. The LIN bus responder mode termination circuit is turned on when standby mode is entered. Standby mode is signaled through a low level on RXD. See the *Standby Mode Application Note* section for more application information.

When EN is set high for longer than t_{MODE_CHANGE} while the device is in standby mode, the device returns to normal mode. The normal transmission paths from TXD to LIN bus and LIN bus to RXD are enabled.

7.4.4 Wake Up Events

There are two ways to wake up from sleep mode:

- Remote wake up initiated by the falling edge of a recessive (high) to dominant (low) state transition on LIN bus where the dominant state is be held for t_{LINBUS} filter time. After this t_{LINBUS} filter time has been met and a rising edge on the LIN bus going from dominant state to recessive state initiates a remote wake up event, eliminating false wake ups from disturbances on the LIN bus or if the bus is shorted to ground.
- Local wake up through EN being set high for longer than t_{MODE_CHANGE}.

7.4.4.1 Wake Up Request (RXD)

When the TLIN829-Q1 encounters a wake up event from the LIN bus, RXD goes low and the device transitions to standby mode until EN is reasserted high and the device enters normal mode. Once the device enters normal mode, the RXD pin releases the wake up request signal and the RXD pin then reflects the receiver output from the LIN bus.

7.4.4.2 Mode Transitions

When the TLIN829-Q1 is transitioning from normal to sleep or standby modes, the device needs the time t_{MODE_CHANGE} to allow the change to fully propagate from the EN pin through the device into the new state. When transitioning from sleep or standby to normal mode the device needs t_{MODE_CHANGE} plus t_{NOMINT}.

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8 Application Information Disclaimer

Note

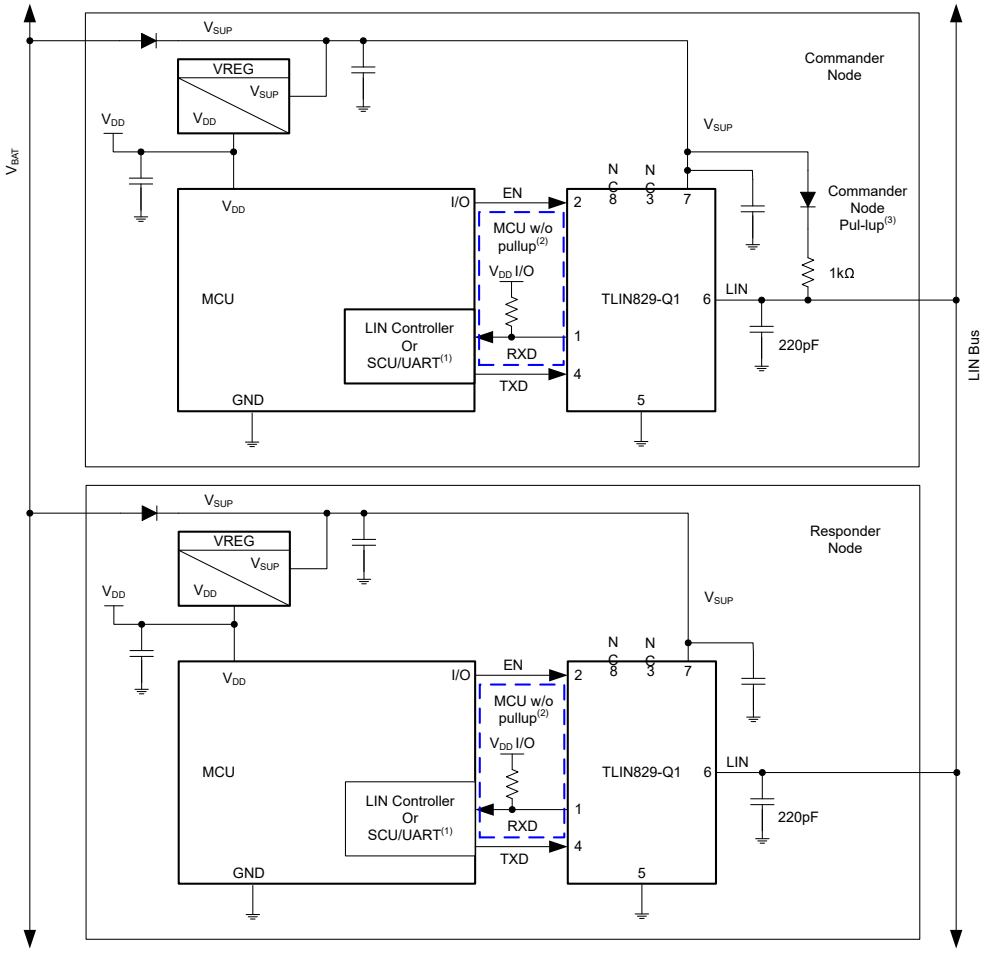
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TLIN829-Q1 can be used as both a responder node device and a commander node device in a LIN network. The device comes with the ability to support both remote wake up request and local wake up request.

8.2 Typical Application

The device integrates a 37kΩ pull-up resistor and series diode for responder node applications. For commander applications, an external 1kΩ pull-up resistor with series blocking diode can be used. Figure 8-1 shows the device being used in both commander mode and responder mode applications.



A. If RXD on MCU on LIN responder node has internal pullup; no external pullup resistor is needed.
B. If RXD on MCU or LIN responder node does not have an internal pullup requires external pullup resistor.
C. Commander node applications require and external 1kΩ pullup resistor and serial diode.
D. Decoupling capacitor values on V_{SUP} are system dependent but typically have 100nF, 1µF and ≥ 10µF.

Figure 8-1. Typical LIN Bus

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8.2.1 Design Requirements

The RXD output structure is an open-drain output stage. This allows the TLIN829-Q1 to be used with 3.3V and 5V I/O processor. If the RXD pin of the processor does not have an integrated pull-up, an external pull-up resistor to the processor I/O supply voltage is required. The select external pull-up resistor value must be between 1kΩ to 10kΩ, depending on supply used (See I_{OL} in the *Electrical Characteristics*). The V_{SUP} pin of the device must be decoupled with a 100nF capacitor by placing the capacitor close to the V_{SUP} supply pin. The system should include additional decoupling on the V_{SUP} line as needed per the application requirements.

8.2.2 Detailed Design Procedures

8.2.2.1 Normal Mode Application Note

When using the TLIN829-Q1 in systems which are monitoring the RXD pin for a wake up request, special care must be taken during the mode transitions. The output of the RXD pin is indeterminate for the transition period between states as the receivers are switched. The application software must not look for an edge on the RXD pin indicating a wake up request until t_{MODE_CHANGE}. This is shown in Figure 6-5

8.2.2.2 Standby Mode Application Note

If the TLIN829-Q1 detects an under voltage on V_{SUP}, the RXD pin transitions low and signals to the software that the TLIN829-Q1 is in standby mode, and must be returned to sleep mode for the lowest power state.

8.3 Power Supply Recommendations

The TLIN829-Q1 is designed to operate directly off a car battery, or any other DC supply ranging from 4V to 36V. A 100nF decoupling capacitor must be placed as close to the V_{SUP} pin of the device as possible. A good practice for some applications with noisier supplies is to also include 1µF and 10µF decoupling capacitor.

8.4 Layout

For the PCB design to be successful, start with design of the protection and filtering circuitry. Because ESD transients have a wide frequency bandwidth from approximately 3MHz to 3GHz, high frequency layout techniques must be applied during PCB design. Placement at the connector also prevents these noisy events from propagating further into the PCB and system.

8.4.1 Layout Guidelines

- **Pin 1 (RXD):** The pin is an open-drain output and requires an external pull-up resistor in the range of 1kΩ to 10kΩ to function properly. Note that the minimum value depends on the VIO supply used. See I_{OL} in electrical specifications. If the microprocessor paired with the transceiver does not have an integrated pull-up, an external resistor must be placed between RXD and the regulated voltage supply for the microprocessor.
- **Pin 2 (EN):** EN is an input pin that is used to place the device in a low-power sleep mode. If this feature is not used, the pin must be pulled high to the regulated voltage supply of the microprocessor through a series resistor between 1kΩ and 10kΩ. Additionally, a series resistor can be placed on the pin to limit current on the digital lines in the case of an over voltage fault.
- **Pin 3 (NC):** Not Connected.
- **Pin 4 (TXD):** The TXD pin is used to transmit the input signal from the microcontroller. A series resistor can be placed to limit the input current to the device in the case of an over-voltage on this pin. A capacitor to ground can be placed close to the input pin of the device to filter noise.
- **Pin 5 (GND):** This is the ground connection for the device. This pin must be tied to the ground plane through a short trace with the use of two vias to limit total return inductance.
- **Pin 6 (LIN):** This pin connects to the LIN bus. For responder mode applications a 220pF capacitor to ground is implemented. For commander mode applications an additional series resistor and blocking diode must be placed between the LIN pin and the V_{SUP} pin. See Figure 8-1.
- **Pin 7 (VSUP):** This is the supply pin for the device. A 100nF decoupling capacitor must be placed as close to the device as possible.
- **Pin 8 (NC):** Not Connected.

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Note

All ground and power connections must be made as short as possible and use at least two vias to minimize the total loop inductance.

8.4.2 Layout Example

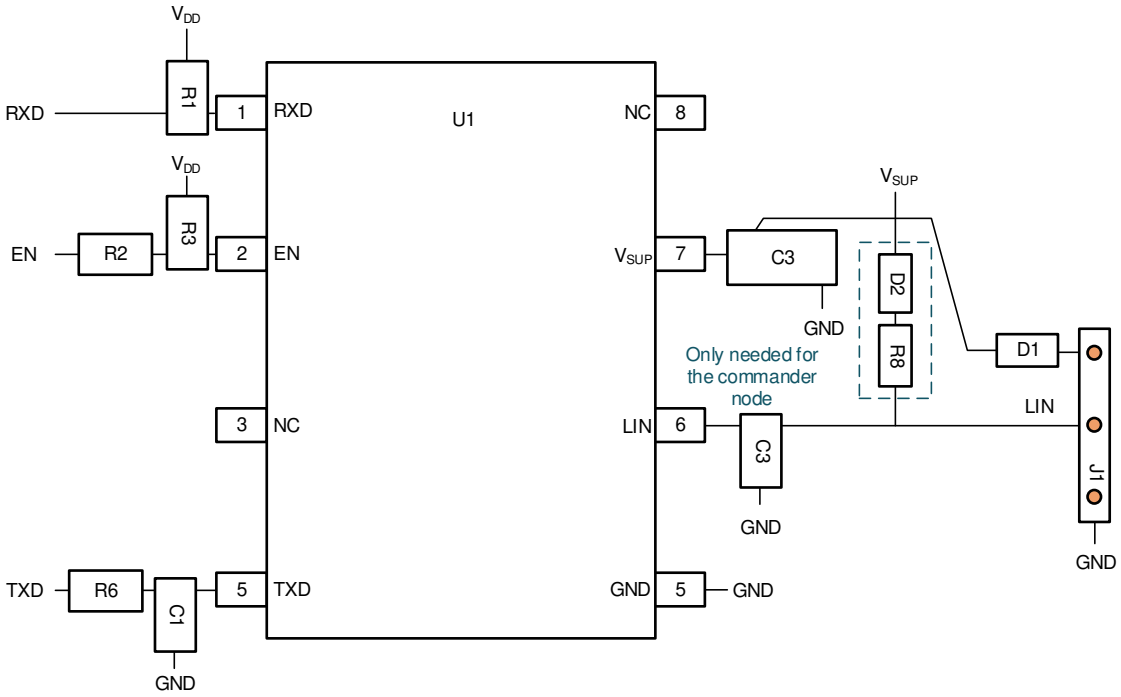

Figure 8-2. Layout Example

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9 Device and Documentation Support

9.1 Documentation Support

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
March 2026	*	Initial release.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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11.1 Package Option Addendum

Table 11-1. Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish(4)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking(5) (6)
TLIN1029ADRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL029
TLIN1029ADRBRQ1	ACTIVE	VSON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL029

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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ADVANCE INFORMATION

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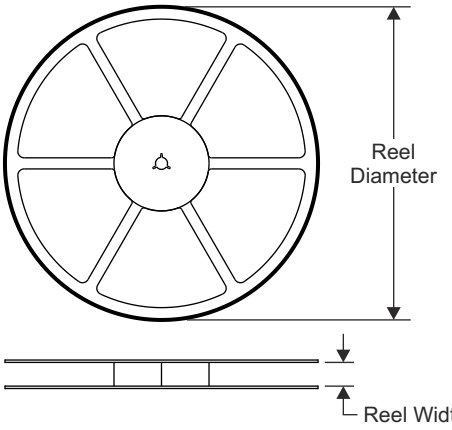
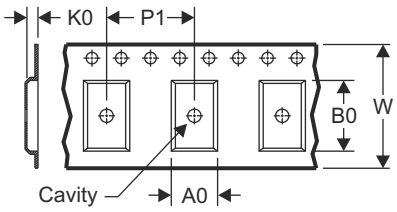
11.2 Tape and Reel Information

REEL DIMENSIONS

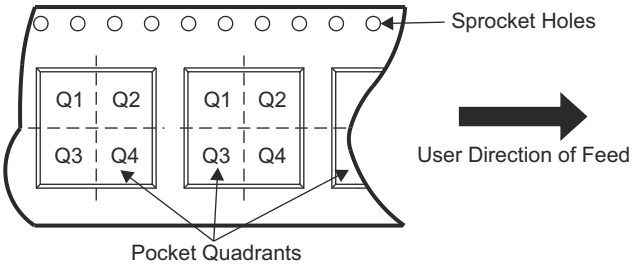


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLIN1029DRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLIN1029DRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TLIN1029DRBTQ1	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLIN1029MDRBRQ1	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

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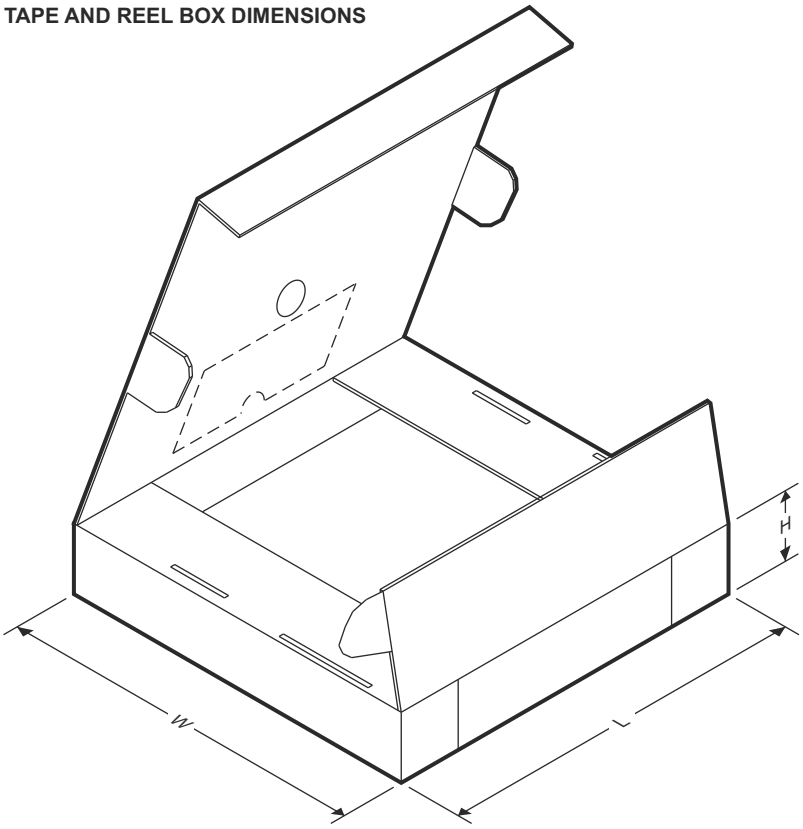
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLIN1029ADRQ1	SOIC	D	8	2500	366.0	364.0	50.0
TLIN1029ADRBRQ1	SON	DRB	8	3000	220.0	205.0	50.0
TLIN2029ADRBTQ1	SON	DRB	8	3000	370.0	355.0	55.0
TLIN1029AMDRBRQ1	SON	DRB	8	3000	370.0	355.0	55.0

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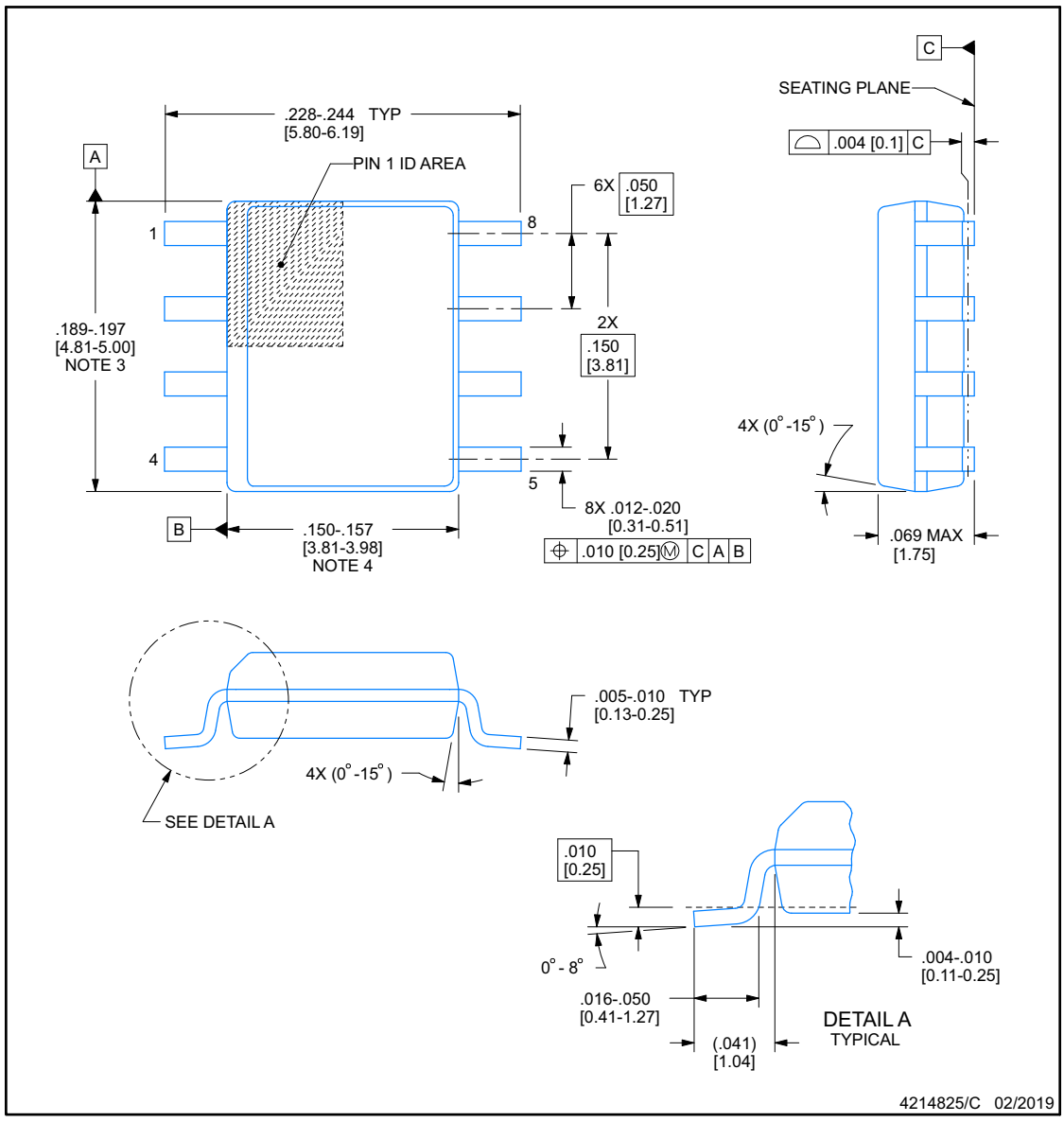
11.3 Mechanical Data

PACKAGE OUTLINE

D0008A — **SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

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ADVANCE INFORMATION

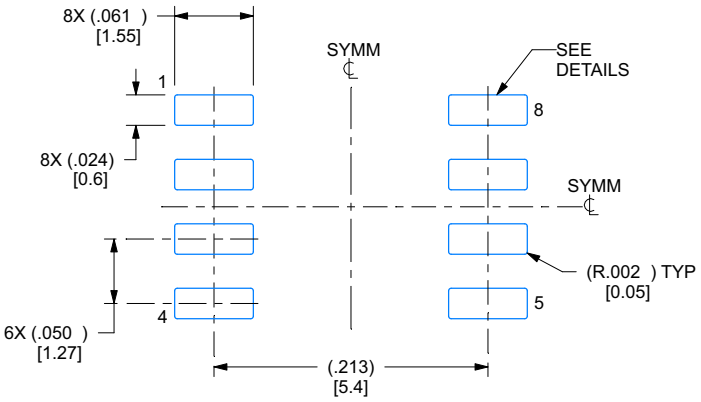
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

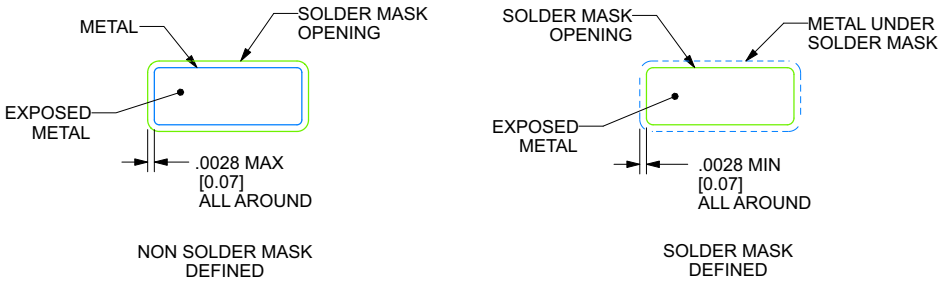
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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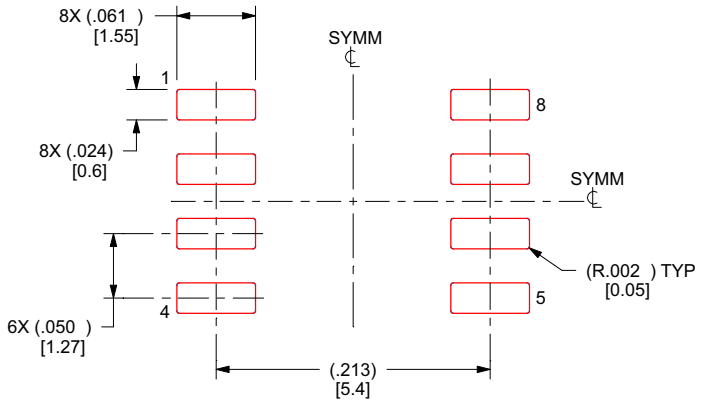
EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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ADVANCE INFORMATION

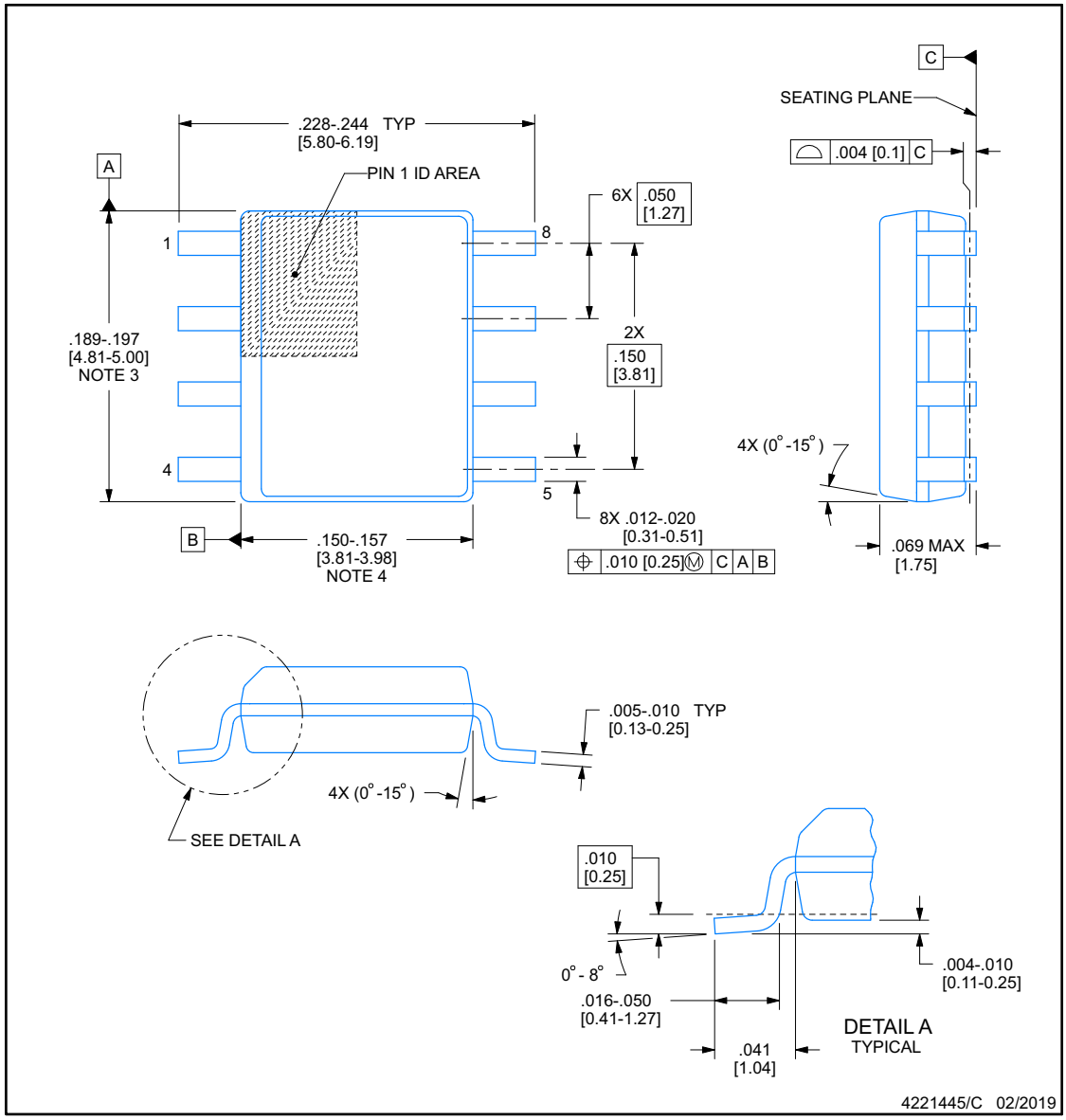
ADVANCE INFORMATION

PACKAGE OUTLINE

D0008B

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15], per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

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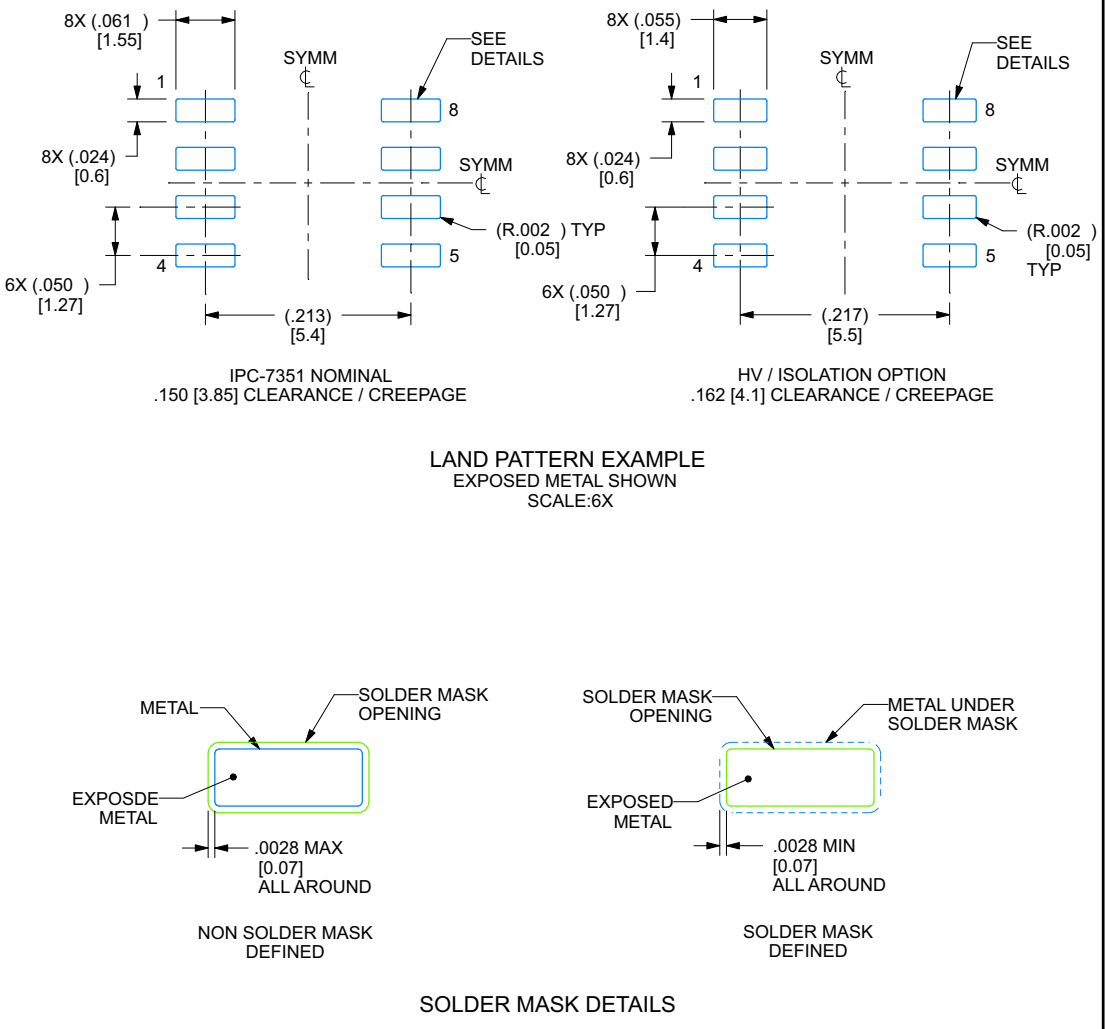
EXAMPLE BOARD LAYOUT

D0008B

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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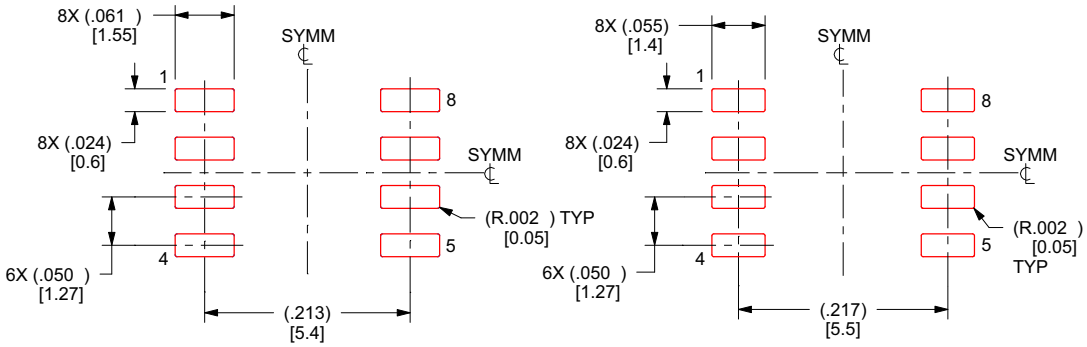
EXAMPLE STENCIL DESIGN

D0008B — SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



IPC-7351 NOMINAL
.150 [3.85] CLEARANCE / CREEPAGE

HV / ISOLATION OPTION
.162 [4.1] CLEARANCE / CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:6X

4221445/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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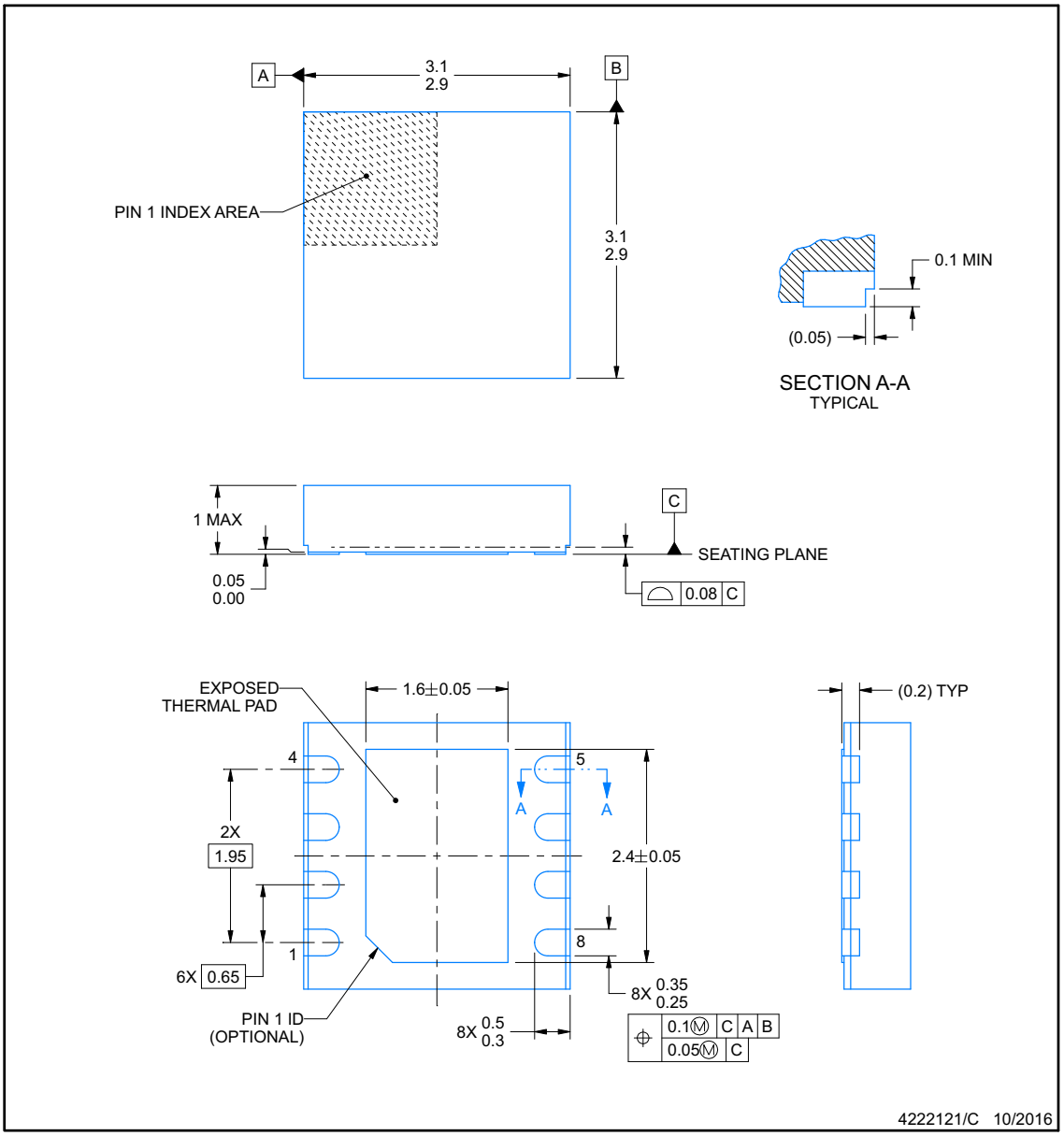
PACKAGE OUTLINE

DRB0008F

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

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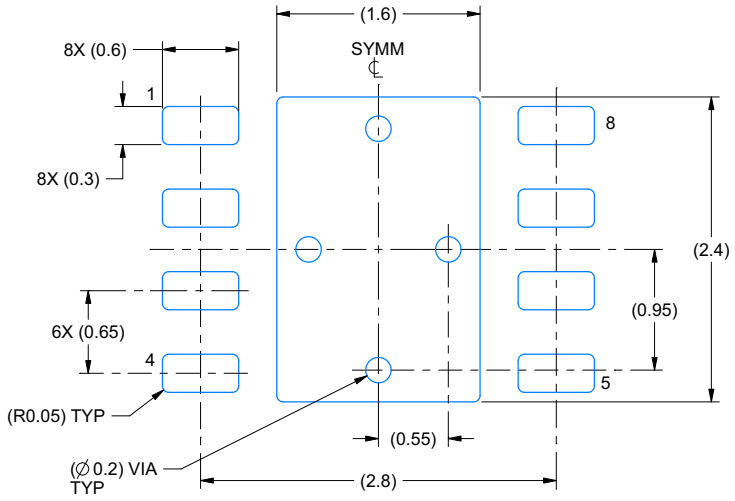
EXAMPLE BOARD LAYOUT

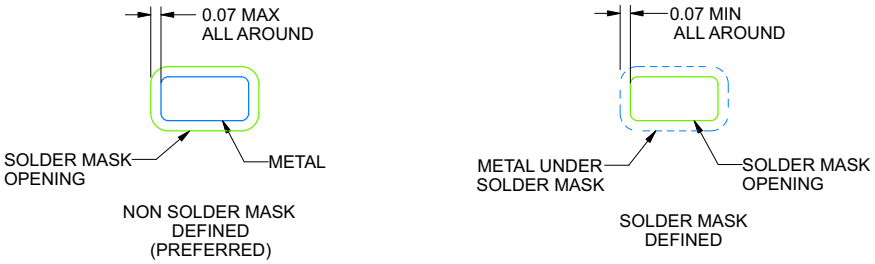
DRB0008F

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4222121/C 10/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

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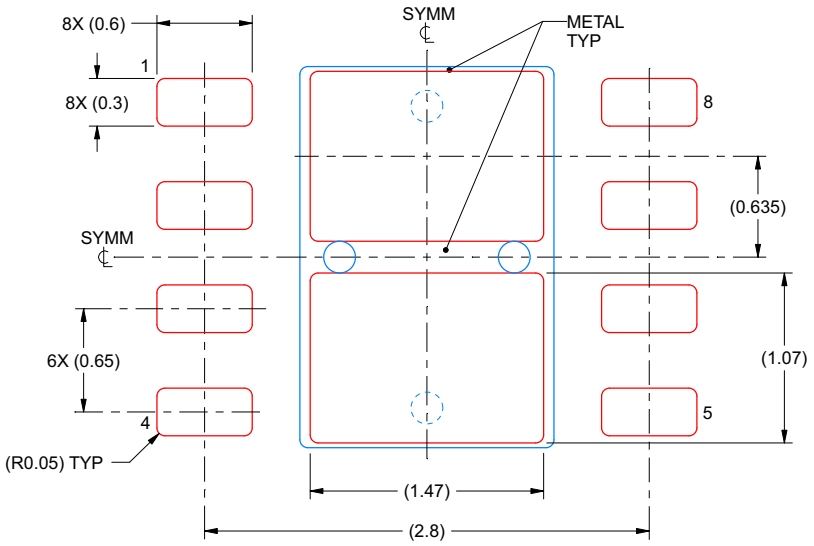
EXAMPLE STENCIL DESIGN

DRB0008F

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
82% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4222121/C 10/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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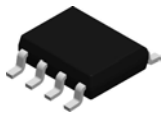
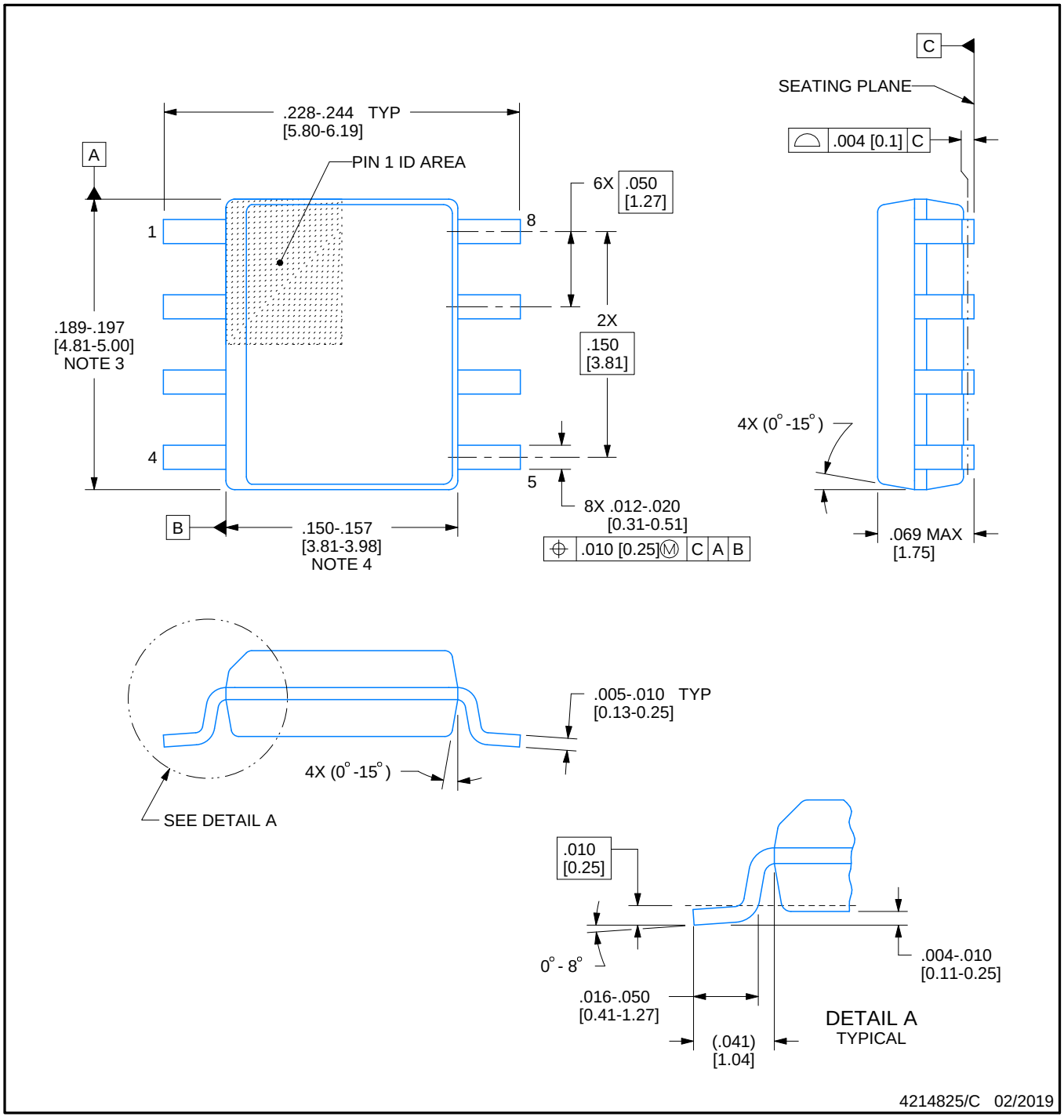


PACKAGE OUTLINE

D0008A

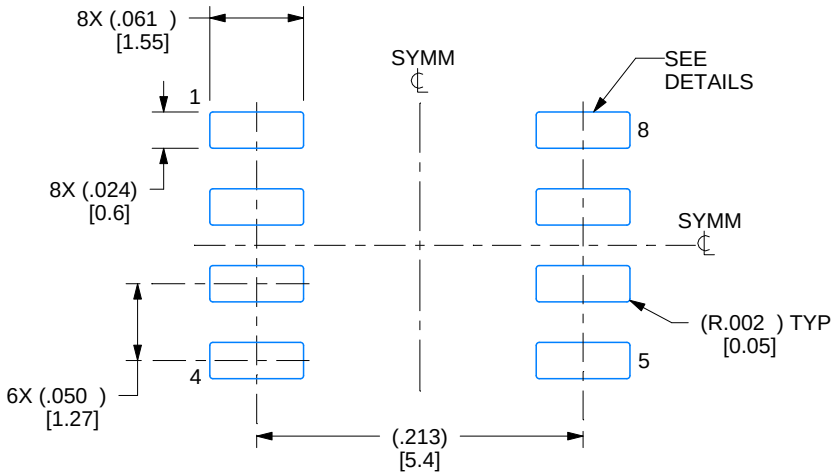
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

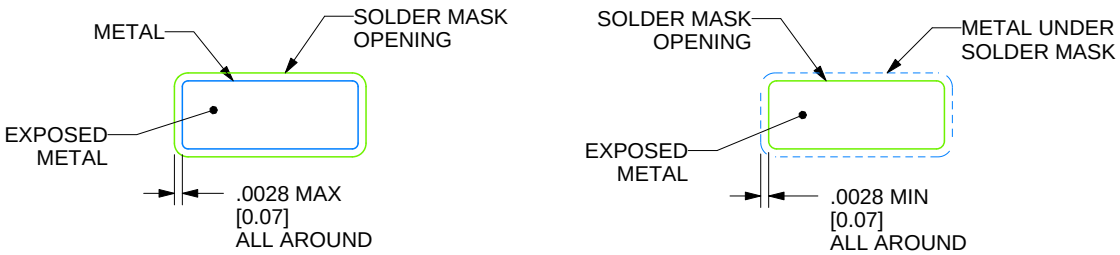


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

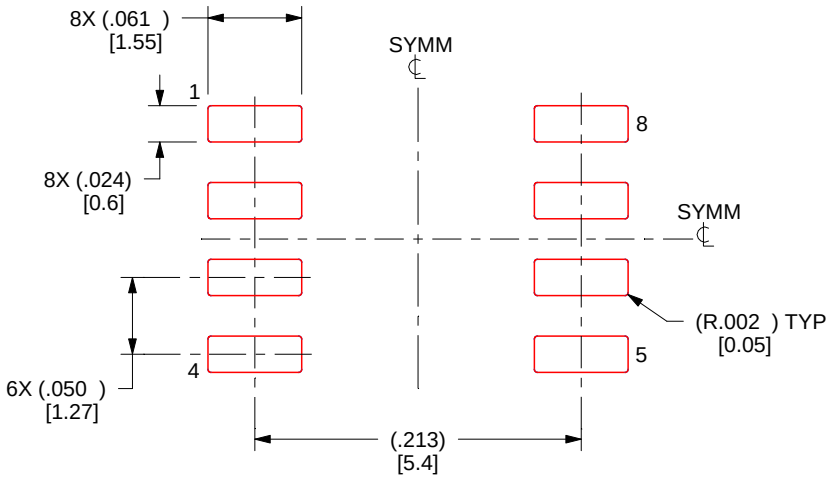
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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