TMUX28xx ±5.5V Beyond the Supply, 1:1 2-Channel, 2:1 1-Channel, Power-Off Protection Switch, with 0.16Ω Ron, 1.2V and 1.8V Compatible Logic

1 Features

- Supply range: 1.8V to 5.5V
- Beyond the supply signal range: -5.5V to 5.5V
- High current support: 1.1A (maximum)
- Ultra-low on-resistance: 0.16Ω
- Low on-resistance flatness: 1.0mΩ
- Low THD+N: 0.001% (-100dB)
- –40°C to +125°C operating temperature
- Power-Off Protection
- 1.8V logic compatible at 5V V_{DD}
- 1.2V logic compatible at 1.8V V_{DD}
- Integrated Pull-Down Resistor on Logic Pins
- Fail-safe logic
- Break-before-make switching

2 Applications

- Land mobile radios
- Defense radios
- Audio input or output switching
- Ultrasonic gas flow transmitters
- Analog input modules
- Industrial module detection

3 Description

The TMUX28xx is a complementary metal-oxide semiconductor (CMOS) multiplexer with 2 configurations available: 1:1, single-pole, single-throw (SPST) 2-channel (TMUX2821) and 2:1, single-pole, double-throw (SPDT) 1-channel (TMUX2819). This device works with a single supply (1.8V to 5.5V), but can pass bidirectional analog and digital signals beyond the supply from -5.5V to 5.5V.

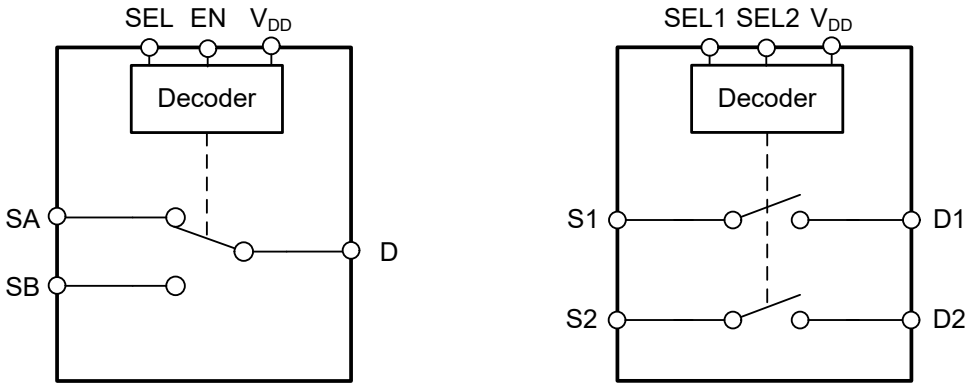
The TMUX28xx also features bidirectional powered off protection up to ±5.5V, which isolates the switch even when there is no supply voltage present (V_{DD} = 0V). Without this protection feature, any voltage on the switch can back-power the supply rail through an internal ESD diode and cause potential damage to the rest of the system.

With 0.001% THD+N and 1mΩ R_{ON}-flatness, the TMUX28xx is an excellent choice for passing precision analog and audio signals without adding distortion.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TMUX2819 TMUX2821	DSG (SON, 8)	2mm × 2mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



TMUX2819 and TMUX2821 Block Diagram

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4 Pin Configuration and Functions

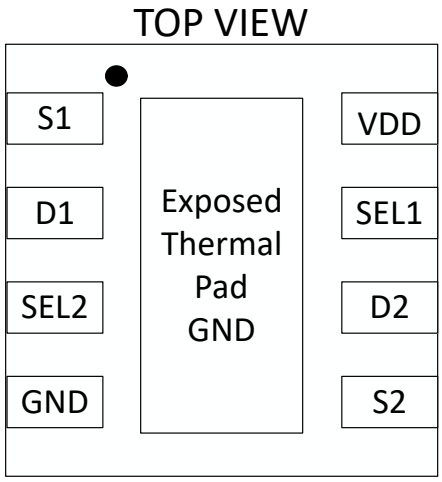


Figure 4-1. DSG Package TMUX2821 (1:1 2ch)

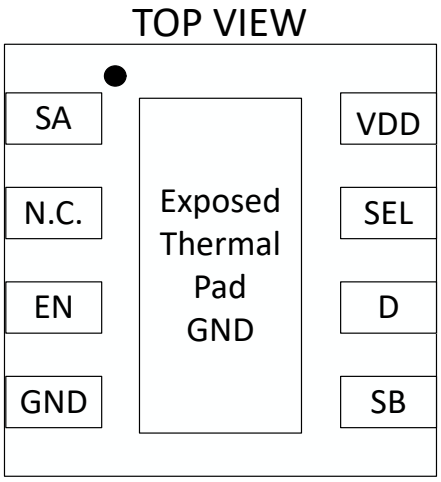


Figure 4-2. DSG Package TMUX2819 (2:1 1ch)

Pin Functions

PIN			TYPE[1]	DESCRIPTION
NO.	TMUX2821	TMUX2819		
1	S1	SA	I/O	Source pin 1 OR A. Can be an input or output.
2	D1	N.C	I/O	Drain pin 1. Can be an input or output. For N.C. connect pin to GND to keep pin in a known state (Not internally connected).
3	SEL2	EN	I	Logic control input. Controls the switch connection
4	GND	GND	GND	Ground (0V) reference
5	S2	SB	I/O	Source pin 2 OR B. Can be an input or output.
6	D2	D	I/O	Drain pin 2 OR Drain. Can be an input or output.
7	SEL1	SEL	I	Logic control input. Controls the switch connection.
8	VDD	VDD	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1µF to 10µF between VDD and GND. Controls the switch connection as provided in Table 7-1
Thermal Pad	GND	GND	GND	Ground (0V) reference

(1) I = input, I/O = input or output, GND = ground, P = power.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
V_{DD} to GND	Supply voltage	–0.5	6	V
V_{SEL} to GND	Logic control input pin voltage	–0.5	6	V
V_S or V_D to GND	Source or drain voltage (Sx, Dx) to ground	-7.5	7.5	V
I_{SEL}	Logic control input pin current	–30	30	mA
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (Sx, Dx)		I_{DC} + 10 %(3)	mA
T_A	Ambient temperature	–55	150	°C
T_{stg}	Storage temperature	–65	150	°C
T_J	Junction temperature		150	°C
P_{tot}	Total power dissipation(4)		750	mW

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) Refer to *Source or Drain Continuous Current* table for I_{DC} specifications.
(4) For WCSP package: P_{tot} derates linearly above T_A = 70°C by 9.4mW/°C.

5.2 ESD Ratings

				VALUE	UNIT
TMUX2889					
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)		±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Thermal Information

THERMAL METRIC(1)		TMUX28xx DSG 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	70	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	85	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	36	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	36	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	15	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Positive power supply voltage	1.8		5.5	V
V_S or V_D	Signal path input/output voltage (source or drain pin) (Sx, D)	-5.5		5.5	V
V_{SEL} or V_{EN}	Address or enable pin voltage	0		5.5	V
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (Sx, D)			I_{DC} (1)	A
T_A	Ambient temperature	–40		125	°C

(1) Refer to *Source or Drain Continuous Current* table for I_{DC} specifications.

5.5 Source or Drain Continuous Current

V_{DD} = 3.3V, GND = 0V (unless otherwise noted)

CONTINUOUS CURRENT PER CHANNEL (I_{DC})(1)				
PACKAGE	25°C	85°C	125°C	UNIT
DSG	1.1	0.87	0.27	A

(1) Refer to Total power dissipation (P_{tot}) limits in *Absolute Maximum Ratings* table that must be followed with max continuous current specification.

5.6 Source or Drain RMS Current

V_{DD} = 3.3V, GND = 0V (unless otherwise noted)

RMS CURRENT PER CHANNEL (I_{RMS})(1)				
PACKAGE	25°C	85°C	125°C	UNIT
DSG	1.1	1.1	0.54	A

(1) Refer to Total power dissipation (P_{tot}) limits in *Absolute Maximum Ratings* table that must be followed with max RMS current specification.

5.7 Electrical Characteristics

V_{DD} = 3.3V, GND = 0V (unless otherwise noted)
Typical at V_{DD} = 3.3V T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = –5V to +5V I_D = –100mA	25°C		0.16	0.20	Ω
			–40°C to +85°C			0.225	Ω
			–40°C to +125°C			0.3	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = –5V to +5V I_D = –100mA	25°C		0.001	0.035	Ω
			–40°C to +85°C			0.04	Ω
			–40°C to +125°C			0.06	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = –5V to +5V I_D = –100mA	25°C		0.001	0.015	Ω
			–40°C to +85°C			0.07	Ω
			–40°C to +125°C			0.09	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0V, I_S = –100mA	–40°C to +125°C		0.001		Ω/°C
$I_{S(POFF)}$	Source powered-off leakage current	V_{DD} = 0V V_S = +5V / 0V V_D = 0V / + 5V	25°C		0.02		uA
			–40°C to +85°C	-0.1		0.1	uA
			–40°C to +125°C	-2		2	uA
$I_{D(POFF)}$	Drain powered-off leakage current	V_{DD} = 0V V_S = +5V / 0V V_D = 0V / + 5V	25°C		0.02		uA
			–40°C to +85°C	-0.1		0.1	uA
			–40°C to +125°C	-2		2	uA
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 3.3V Switch state is off V_S = +5V / –5V V_D = –5V / + 5V	25°C		0.02		uA
			–40°C to +85°C	-0.1		0.1	uA
			–40°C to +125°C	-1		1	uA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = 3.3V Switch state is on V_S = V_D = ±5V	25°C		0.02		uA
			–40°C to +85°C	-0.1		0.1	uA
			–40°C to +125°C	-1		1	uA
LOGIC INPUTS (SEL / EN pins)							
V_{IH}	Logic voltage high	V_{DD} = 5.5V	–40°C to +125°C	1.2		5.5	V
		V_{DD} = 3.3V		1.1		5.5	
		V_{DD} = 1.8V		0.8		5.5	
V_{IL}	Logic voltage low	V_{DD} = 5.5V	–40°C to +125°C	0		0.6	V
		V_{DD} = 3.3V		0		0.6	
		V_{DD} = 1.8V		0		0.42	
I_{IH}	Input leakage current		–40°C to +125°C		1	1.5	µA
I_{IL}	Input leakage current		–40°C to +125°C	-10	-1		nA
C_{IN}	Logic input capacitance		–40°C to +125°C		5		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 1.6V to 5.5V Logic inputs = 0V, 5V, or V_{DD}	25°C		55	125	µA
			–40°C to +85°C			130	µA
			–40°C to +125°C			140	µA

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

5.8 Switching Characteristics

V_{DD} = 3.3V, GND = 0V (unless otherwise noted)
Typical at V_{DD} = 3.3V, T_A = 25℃ (unless otherwise noted)

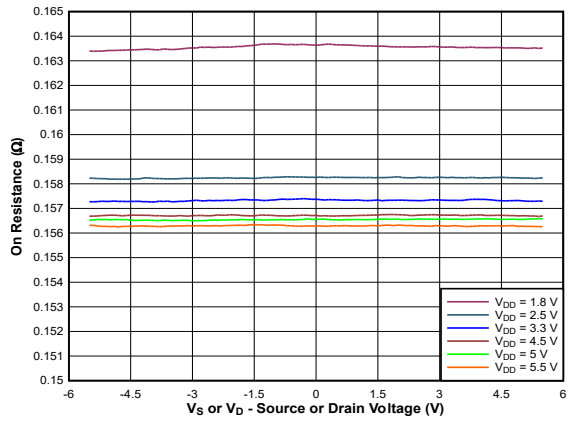
PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{TRAN}	Transition time from control input	V_{DD} = 2.5V to 5.5V V_S = 3.3V R_L = 50Ω, C_L = 35pF	25°C		80	185	us
			–40°C to +85°C			220	us
			–40°C to +125°C			220	us
		V_{DD} = 1.8V to 2.5V V_S = 3.3V R_L = 50Ω, C_L = 35pF	25°C		10	340	us
			–40°C to +125°C			490	us
			–40°C to +125°C			490	us
t_{ON}	Turn-on time from control input	V_S = 3.3V R_L = 50Ω, C_L = 35pF	25°C		155	300	us
			–40°C to +85°C			400	us
			–40°C to +125°C			450	us
t_{OFF}	Turn-off time from control input	V_{DD} = 2.5V to 5.5V V_S = 3.3V R_L = 50Ω, C_L = 35pF	25°C	40		185	us
			–40°C to +85°C	40		220	us
			–40°C to +125°C	40		220	us
t_{BBM}	Break-before-make time delay	V_{DD} = 2.5V to 5.5V V_S = 3.3V R_L = 50Ω, C_L = 35pF	25°C	40		300	us
			–40°C to +85°C	40		300	us
			–40°C to +125°C	40		300	us
		V_{DD} = 1.8V to 2.5V V_S = 3.3V R_L = 50Ω, C_L = 35pF	25°C	40		420	us
			–40°C to +125°C	40		490	us
			–40°C to +125°C	40		490	us
$t_{ON\ (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 1µs R_L = 50Ω, C_L = 35pF	25°C		175		us
Q_{INJ}	Charge injection	V_S = 0V, C_L = 100pF	25°C		5		pC
O_{ISO}	Off-isolation	R_L = 50Ω , C_L = 5pF V_S = 200mV_{RMS}, V_{BIAS}=0V, f = 100kHz	25°C		–50		dB
X_{TALK}	Crosstalk - 2821	R_L = 50Ω , C_L = 5pF V_S = 200mV_{RMS}, V_{BIAS}=0V, f = 100kHz	25°C		–100		dB
	Crosstalk - 2819	R_L = 50Ω , C_L = 5pF V_S = 200mV_{RMS}, V_{BIAS}=0V, f = 100kHz	25°C		–55		dB
BW	–3dB Bandwidth	R_L = 50Ω , C_L = 5pF V_S = 200mV_{RMS}, V_{BIAS}=0V	25°C		100		MHz
I_L	Insertion loss	R_L = 50Ω , C_L = 5pF V_S = 200mV_{RMS}, V_{BIAS}=0V, f = 1MHz	25°C		-0.01		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62V on V_{DD} R_L = 32Ω , C_L = 5pF, f = 20kHz	25°C		–100		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 0.5V, V_{BIAS} = 0V R_L = 600Ω f = 20Hz to 20kHz	25°C		-107		dB
			–40°C to +85°C		-105		
			–40°C to +125°C		-105		
		V_{PP} = 0.5V, V_{BIAS} = 0V R_L = 32Ω f = 20Hz to 20kHz	25°C		-102		
			–40°C to +85°C		-102		
			–40°C to +125°C		-102		
$C_{S(OFF)}$	Source off capacitance	V_S = 0V, f = 1MHz	25°C		70		pF

V_{DD} = 3.3V, GND = 0V (unless otherwise noted)
Typical at V_{DD} = 3.3V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance	V_S = 0V, f = 1MHz	25°C		40		pF

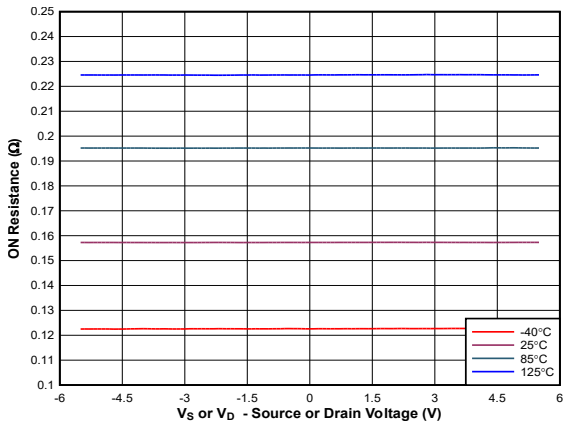
5.9 Typical Characteristics

at T_A = 25°C (unless otherwise noted)



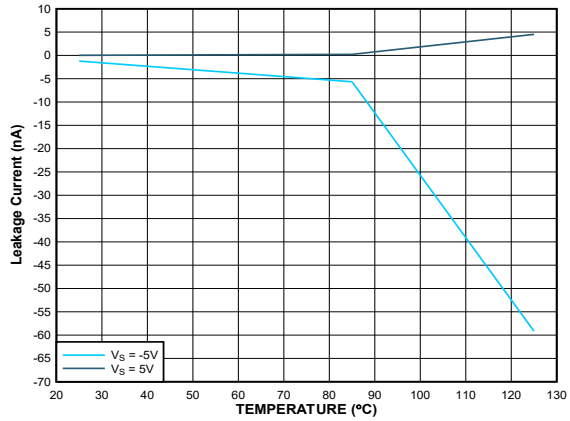
T_A = 25°C

Figure 5-1. On-Resistance vs Source or Drain Voltage



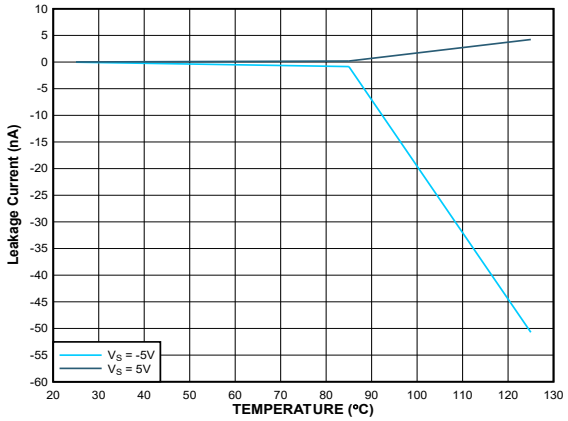
V_{DD} = 3.3V

Figure 5-2. On-Resistance vs Source or Drain Voltage Across Temperature



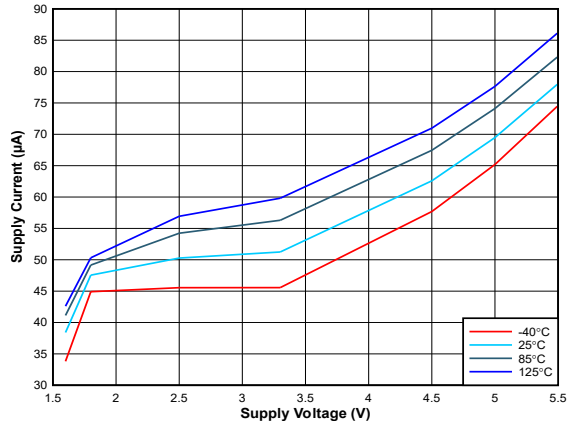
V_{DD} = 1.8V

Figure 5-3. ION Leakage vs Temperature



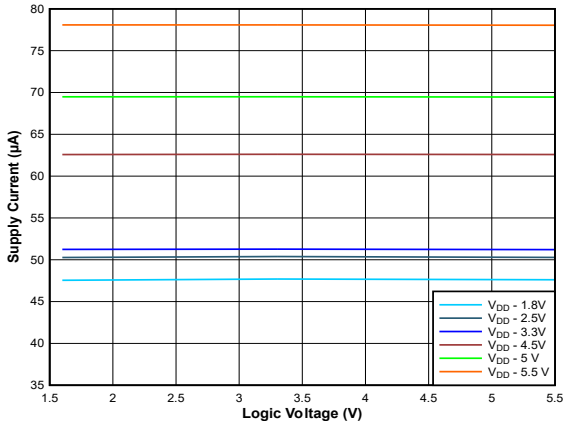
V_{DD} = 3.3V

Figure 5-4. ION Leakage vs Temperature



T_A = 25°C

Figure 5-5. Supply Current vs Supply Voltage



T_A = 25°C, V_S = 5V

Figure 5-6. Supply Current vs Logic Voltage

5.9 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)

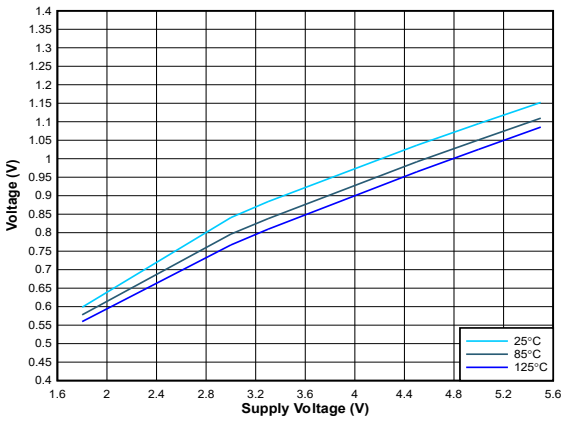


Figure 5-7. V_{IH} Logic Threshold vs Supply Voltage

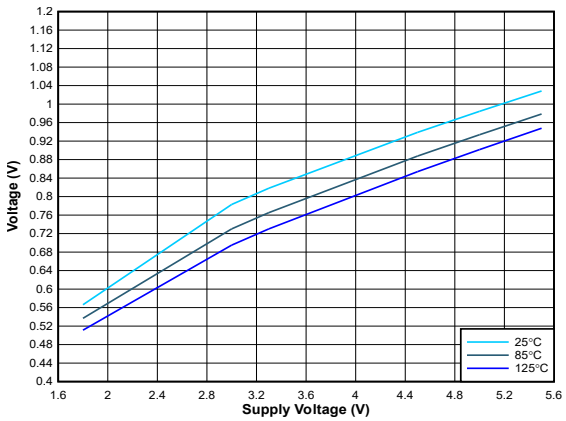
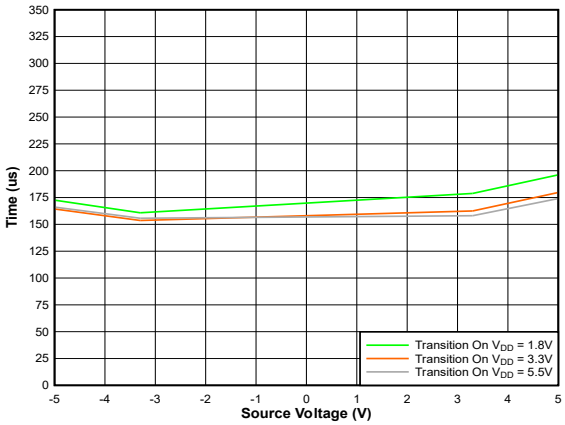
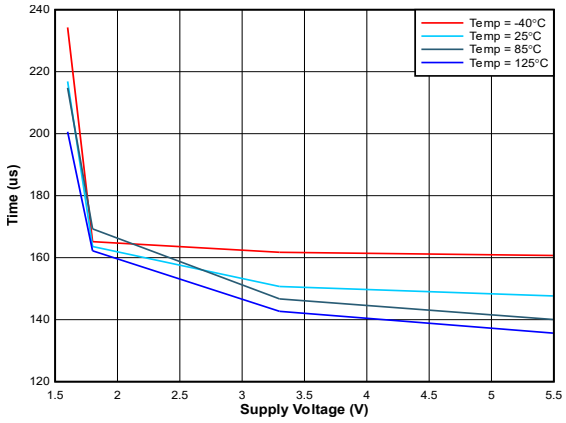


Figure 5-8. V_{IL} Logic Threshold vs Supply Voltage



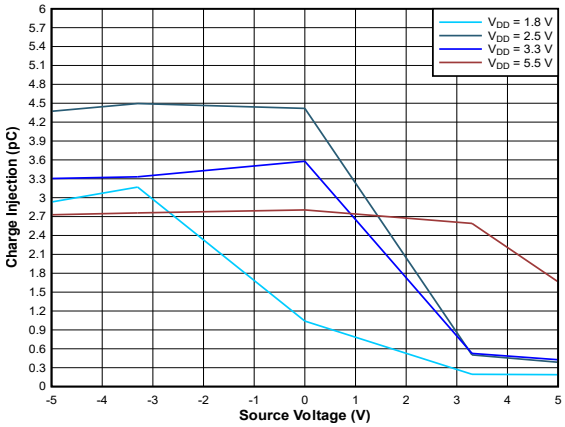
T_A = 25°C

Figure 5-9. Transition Time vs Source Voltage



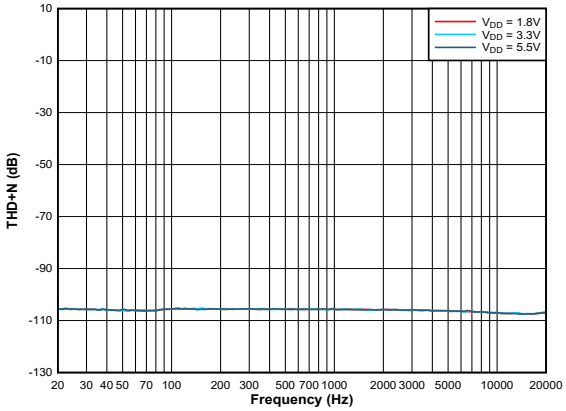
T_S = 3.3V

Figure 5-10. tBBM vs Supply Voltage



T_A = 25°C

Figure 5-11. Charge Injection vs Source Voltage

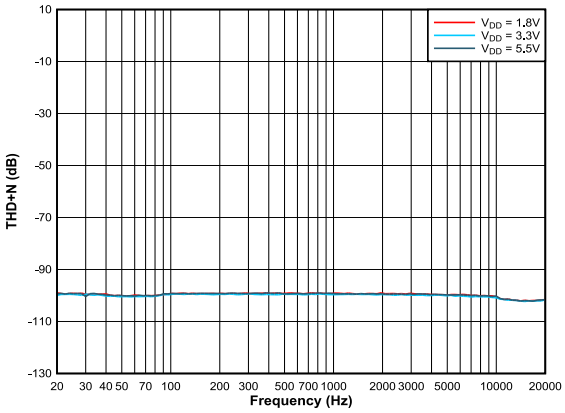


R_{LOAD} = 600Ω, T_A = 25°C

Figure 5-12. THD+N vs Frequency

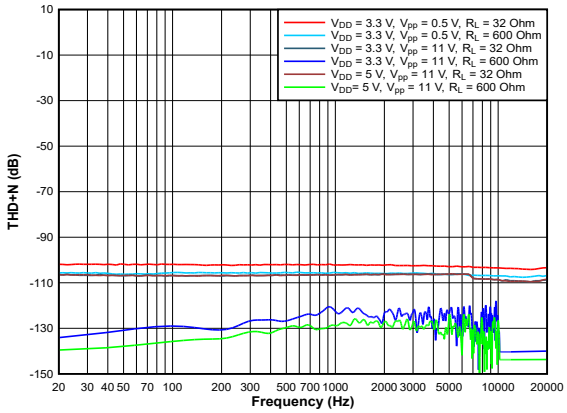
5.9 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)



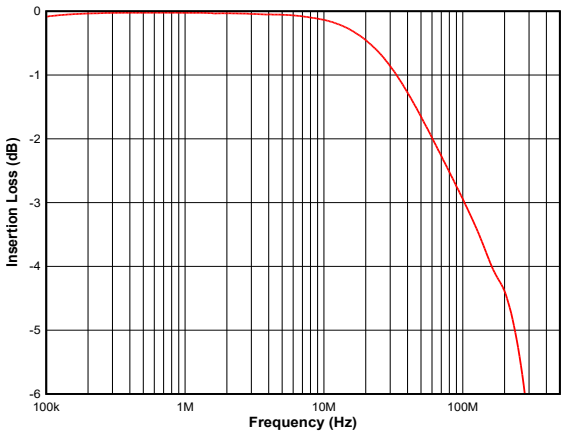
R_{LOAD} = 32Ω, T_A = 25°C

Figure 5-13. THD+N vs Frequency



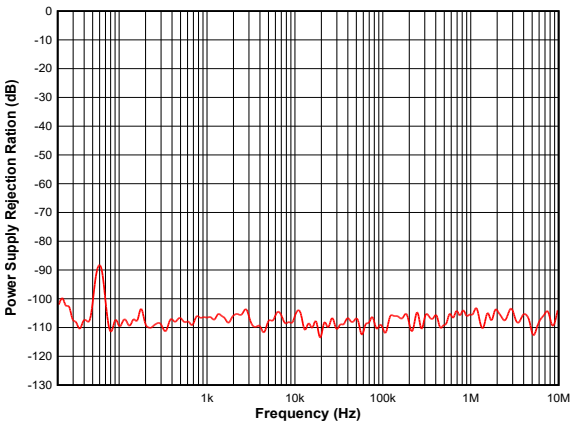
T_A = 25°C

Figure 5-14. THD+N vs Frequency



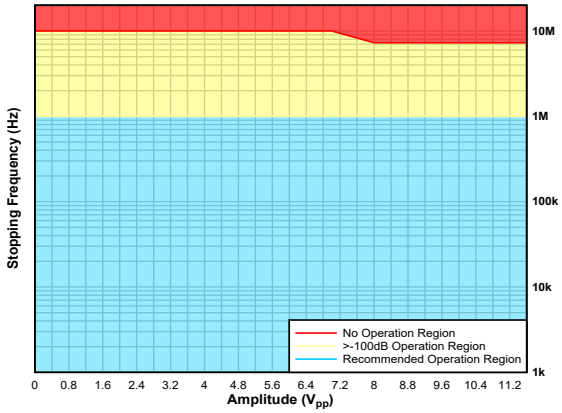
V_{DD} = 3.3V, T_A = 25°C

Figure 5-15. Insertion Loss vs Frequency



V_{DD} = 3.3V, T_A = 25°C

Figure 5-16. ACPSRR vs Frequency



V_{DD} = 5V

Figure 5-17. Maximum Sinusoidal Signal Swing

6 Parameter Measurement Information

6.1 On-Resistance

The on-resistance of a device is the ohmic resistance between the source (Sx) and drain (Dx) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. Figure 6-1 shows the measurement setup used to measure R_{ON}. Voltage (V) and current (I_{SD}) are measured using this setup, and R_{ON} is computed with $R_{ON} = V / I_{SD}$.

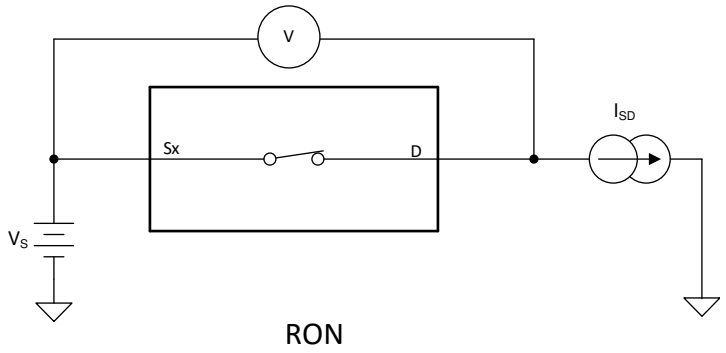


Figure 6-1. On-Resistance Measurement Setup

6.2 On-Leakage Current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol $I_{S(ON)}$. Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol $I_{D(ON)}$. Either the source pin or drain pin is left floating during the measurement. Figure 6-2 shows the circuit used for measuring the on-leakage current, denoted by $I_{S(ON)}$ or $I_{D(ON)}$.

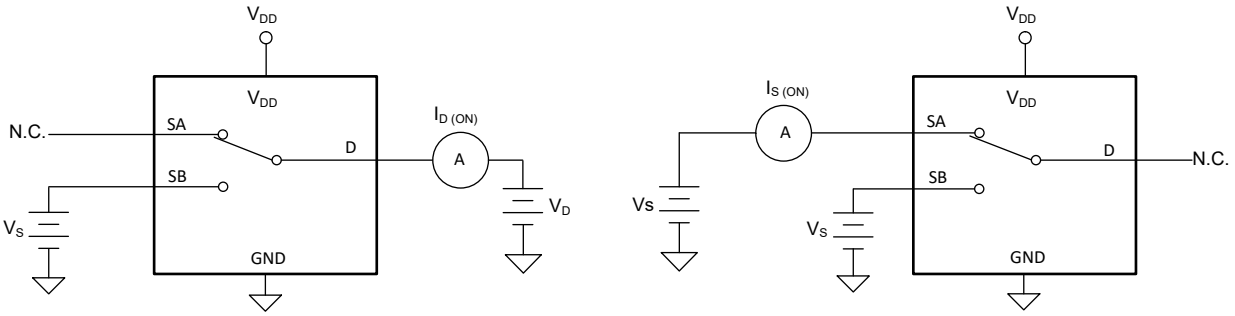


Figure 6-2. On-Leakage Measurement Setup

6.3 Off-Leakage Current

Source and drain off-leakage current is defined as the leakage current flowing into or out of the source or drain pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$ and $I_{D(OFF)}$. Figure 6-3 shows the setup used to measure off-leakage current.

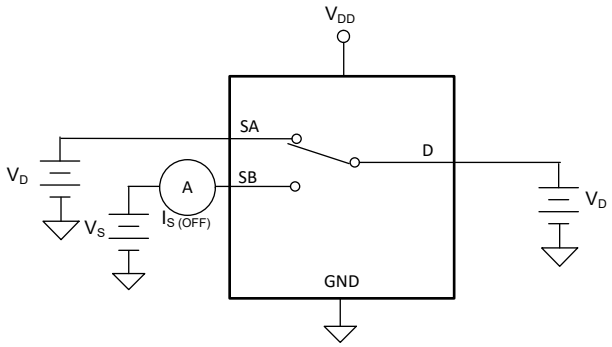


Figure 6-3. Off-Leakage Measurement Setup

6.4 Power-Off Leakage Current

Powered-off source and drain leakage current is defined as the leakage current flowing into or out of the source or drain pin when the device is powered off. This current is denoted by the symbol $I_{PS(OFF)}$ and $I_{PD(OFF)}$. Figure 6-4 shows the setup used to measure off-leakage current.

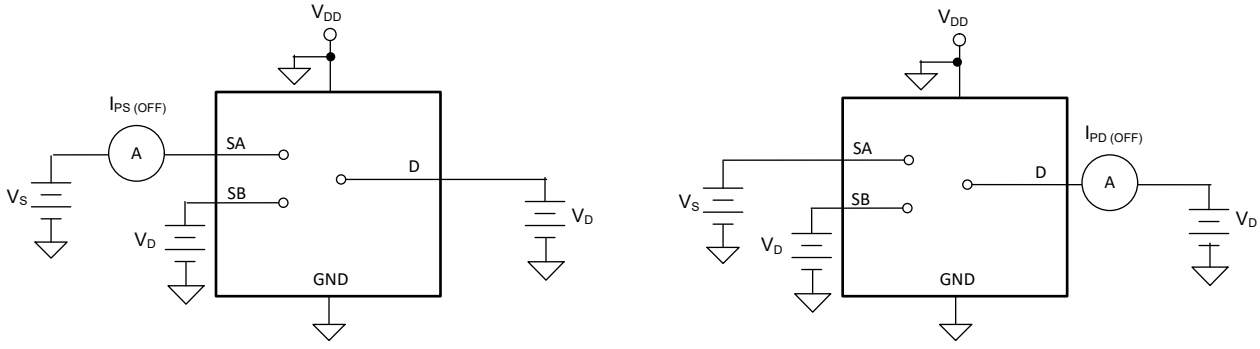


Figure 6-4. Power-Off Leakage Measurement Setup

6.5 Propagation Delay

Propagation delay is defined as the time taken by the output of the device to rise or fall 50% after the input signal has risen or fallen past the 50% threshold. Figure 6-5 shows the setup used to measure propagation delay, denoted by the symbol t_{PD}.

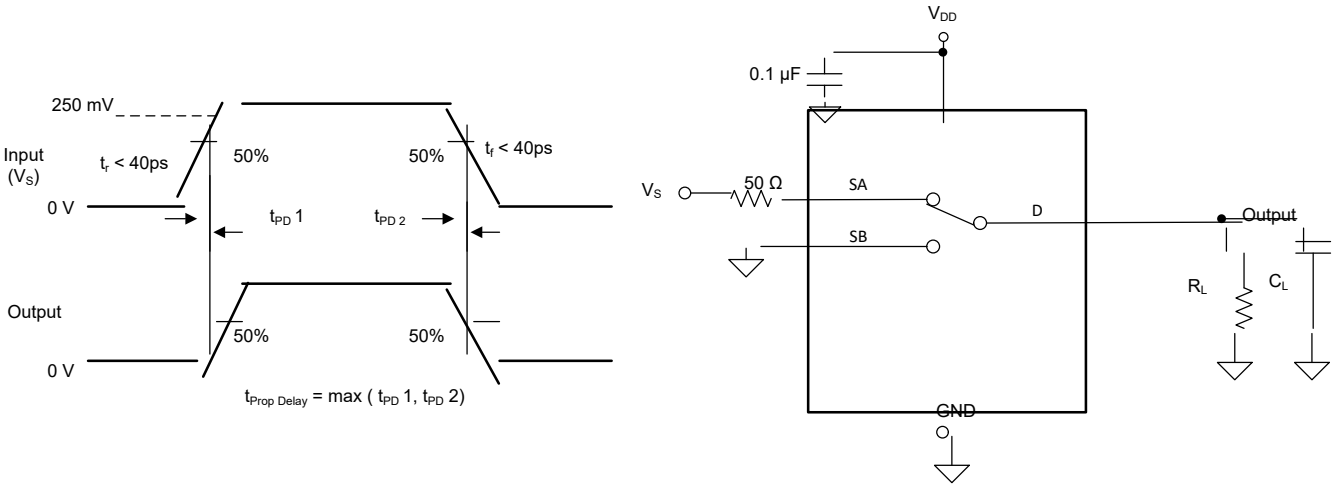


Figure 6-5. Propagation Delay Measurement Setup

6.6 $t_{ON\ (VDD)}$ and $t_{OFF\ (VDD)}$ Time

The $t_{ON\ (VDD)}$ time is defined as the time taken by the output of the device to rise 90% after the supply has risen past the supply threshold. The 90% measurement is used to provide the timing of the device turning on in the system. Figure 6-6 shows the setup used to measure turn on time, denoted by the symbol $t_{ON\ (VDD)}$

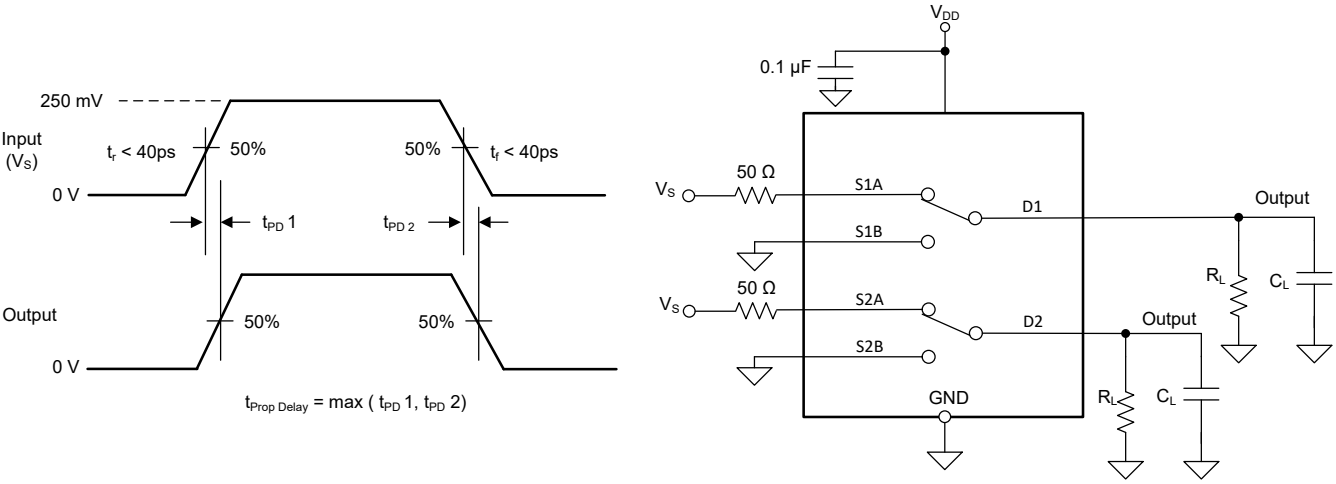


Figure 6-6. $t_{ON\ (VDD)}$ and $t_{OFF\ (VDD)}$ Time Measurement Setup

6.7 Transition Time

Transition time is defined as the time taken by the output of the device to rise or fall 10% after the control signal has risen or fallen past the logic threshold. The 10% transition measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. Figure 6-7 shows the setup used to measure transition time, denoted by the symbol $t_{TRANSITION}$.

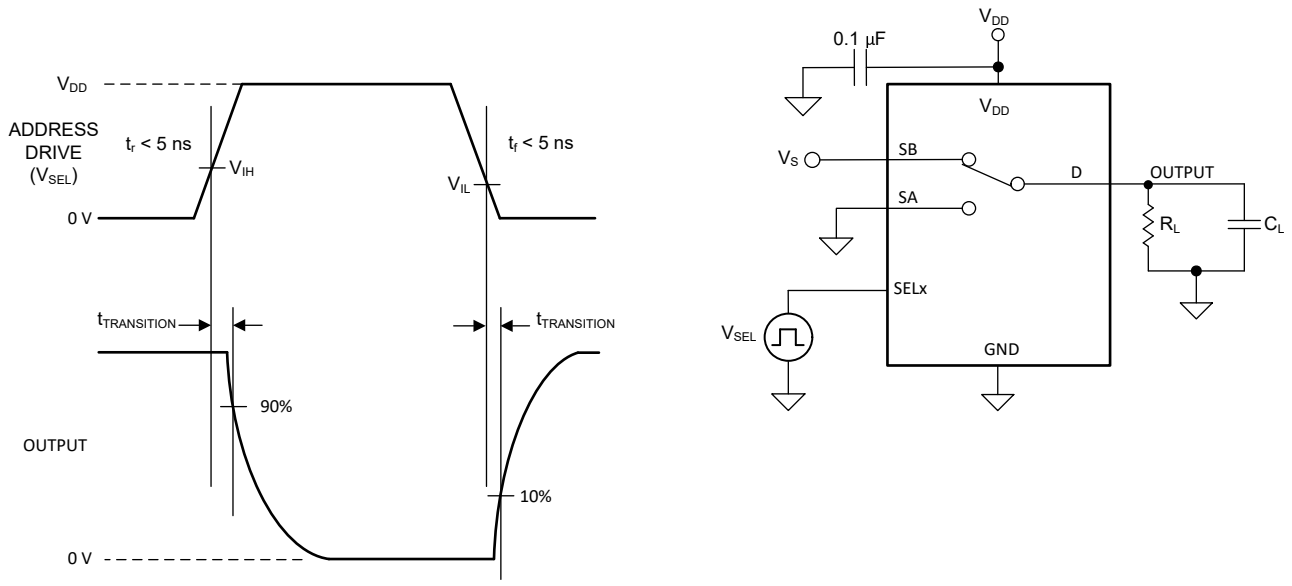


Figure 6-7. Transition-Time Measurement Setup

6.8 Break-Before-Make

Break-before-make delay is a safety feature that prevents two inputs from connecting when the device is switching. The output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the *break* and the *make* is known as break-before-make delay. Figure 6-8 shows the setup used to measure break-before-make delay, denoted by the symbol $t_{OPEN(BBM)}$.

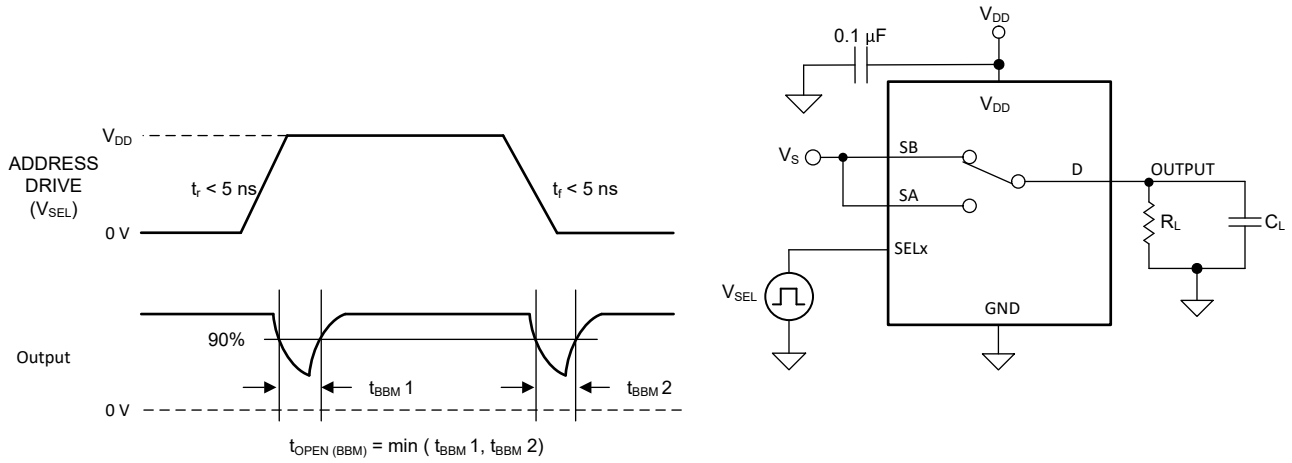


Figure 6-8. Break-Before-Make Delay Measurement Setup

6.9 THD + Noise

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion, and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the mux output. The on-resistance of the device varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD + N.

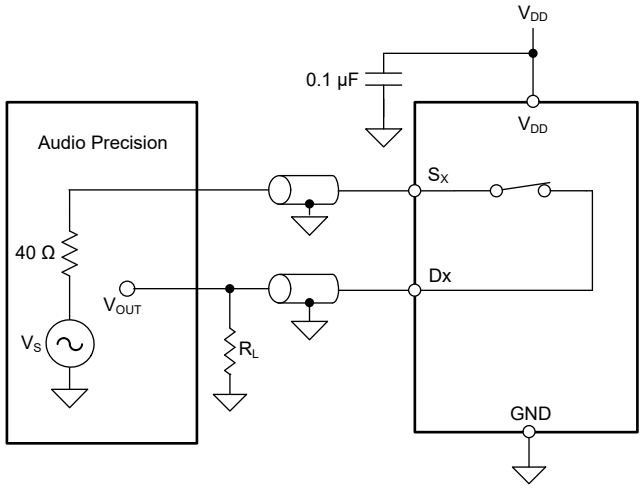


Figure 6-9. THD + N Measurement Setup

6.10 Power Supply Rejection Ratio (PSRR)

PSRR measures the ability of a device to prevent noise and spurious signals that appear on the supply voltage pin from coupling to the output of the switch. The DC voltage on the device supply is modulated by a sine wave of 100mV$_{PP}$. The ratio of the amplitude of signal on the output to the amplitude of the modulated signal is the AC PSRR.

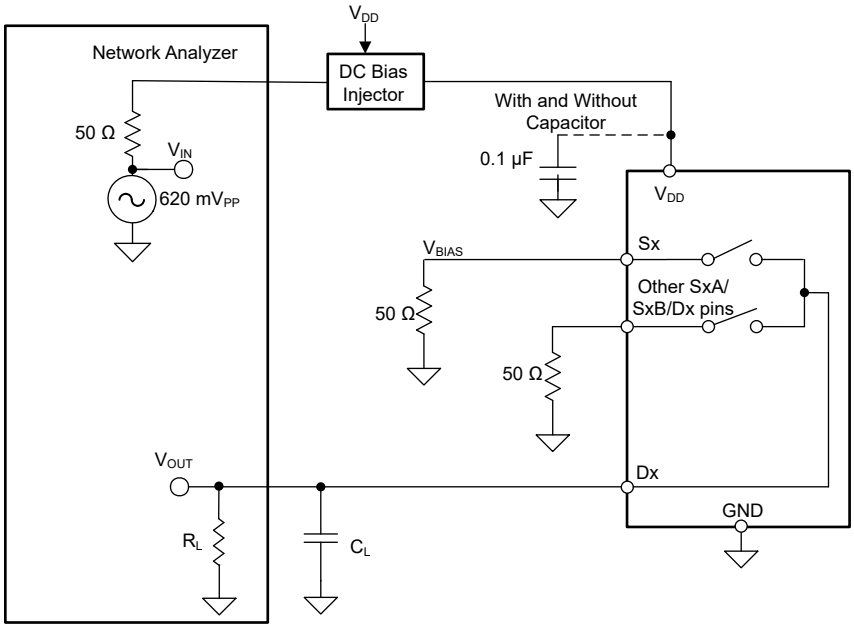


Figure 6-10. AC PSRR Measurement Setup

6.11 Charge Injection

Any mismatch in capacitance results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_C. Figure 6-11 shows the setup used to measure charge injection from Drain (D) to Source (Sx).

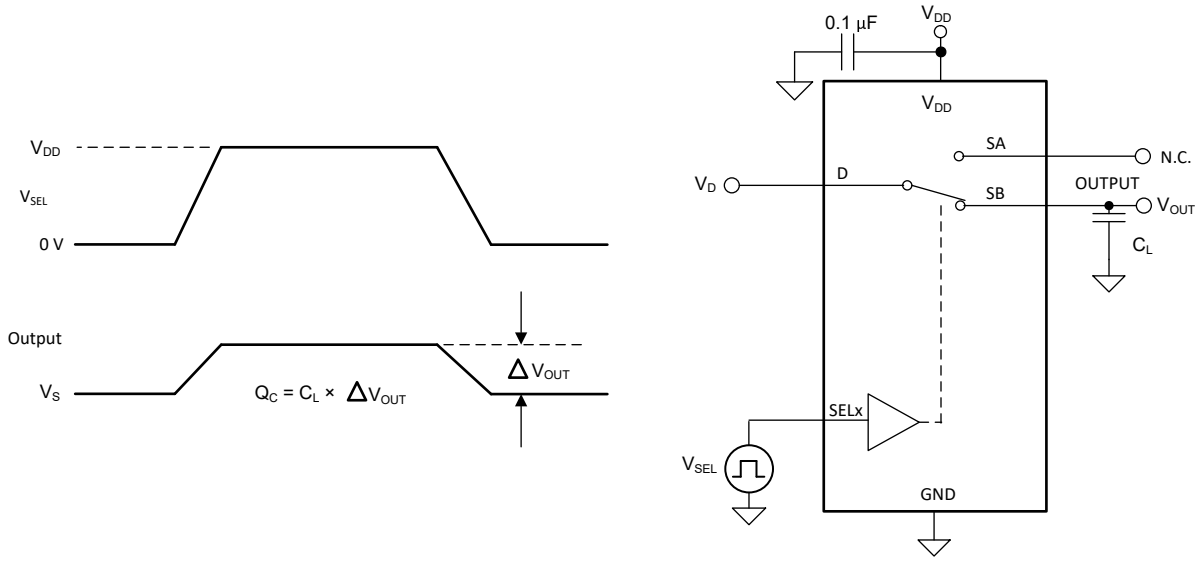


Figure 6-11. Charge Injection Measurement Setup

6.12 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (Dx) of the device. Figure 6-12 shows the setup used to measure bandwidth.

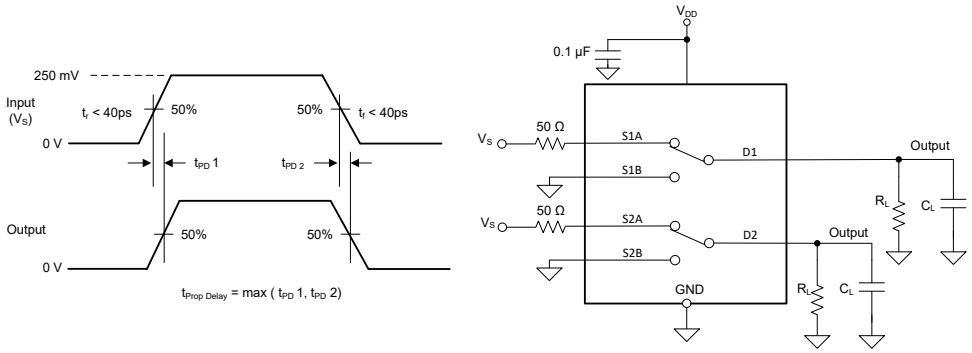


Figure 6-12. Bandwidth Measurement Setup

6.13 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (D) of the device when a signal is applied to the source pin (Sx) of an off-channel. Figure 6-13 shows the setup used to measure, and the equation used to calculate off isolation.

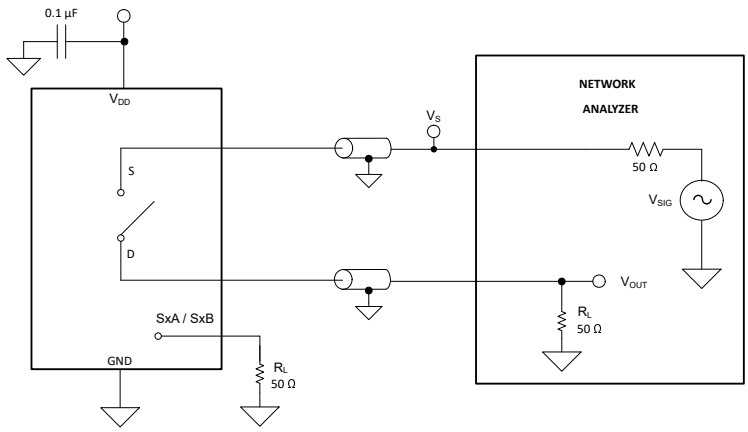


Figure 6-13. Off Isolation Measurement Setup

$$Off\ Isolation\ =\ 20\ \times\ Log\left(\frac{V_{OUT}}{V_S}\right) \quad (1)$$

6.14 Crosstalk

Crosstalk is defined as the ratio of the signal at the drain pin (D) of a different channel, when a signal is applied at the source pin (Sx) of an on-channel. Figure 6-14 shows the setup used to measure, and the equation used to calculate crosstalk.

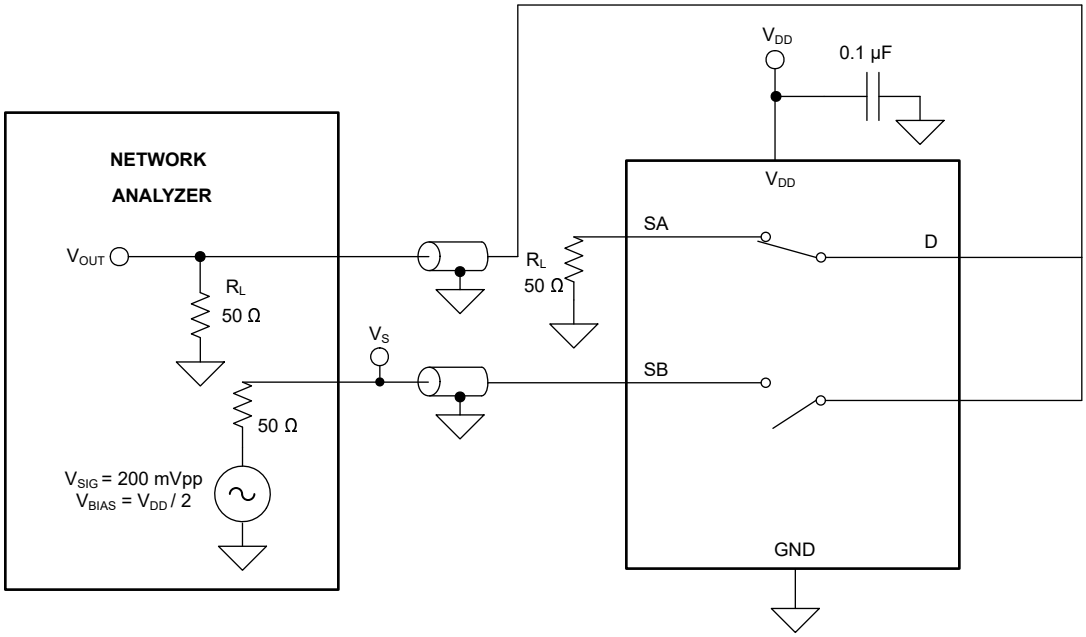


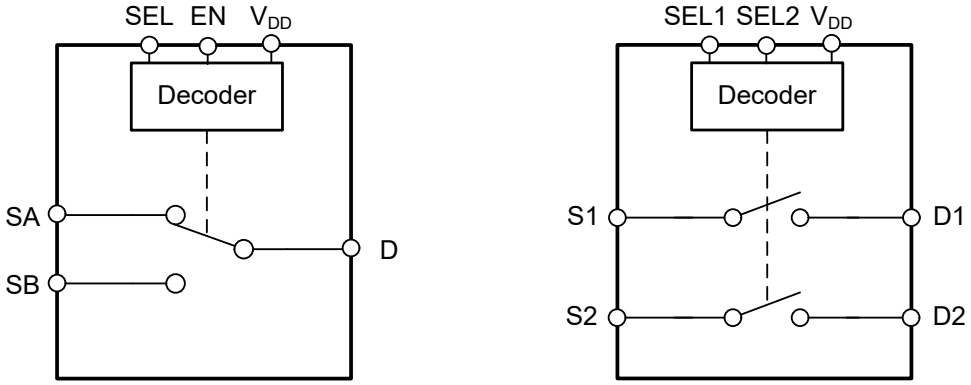
Figure 6-14. Crosstalk Measurement Setup

$$Channel-to-Channel\ Crosstalk\ =\ 20\ \times\ Log\left(\frac{V_{OUT}}{V_S}\right) \quad (2)$$

7 Detailed Description

7.1 Functional Block Diagram

The TMUX2821 is a 1:1, 2-channel and the TMUX2819 is a 2:1 1-channel multiplexer or demultiplexer. Each input is turned on or turned off based on the state of the select lines and V_{DD} pin.



7.2 Device Functional Modes

Table 7-1 provides the truth table for the TMUX28xx.

Table 7-1. TMUX2821 Truth Table

VDD	SELx	Channel x
0	X(1)	All channels are off (Hi-Z). Device is in power-off protection.
1	0	Channel x OFF
1	1	Channel x ON

Table 7-2. TMUX2819 Truth Table

VDD	SEL	EN	Selected Input Connected To Drain (D) Pin
0	X(1)	X	All channels are off (Hi-Z). Device is in power-off protection.
1	X	0	All channels are off (Hi-Z). Device is in power-off protection.
1	0	1	SxA
1	1	1	SxB

(1) X denotes *do not care*.

7.3 Feature Description

7.3.1 Beyond the Supply

The TMUX28xx supports signal voltages beyond the supply on the source (Sx) and drain (Dx) pins up to ±5.5V. This feature allows both AC and DC bidirectional signals above V_{DD} and below ground to pass through the switch without distortion, using a unidirectional supply. The device remains within the performance mentioned in the *Electrical Characteristics*.

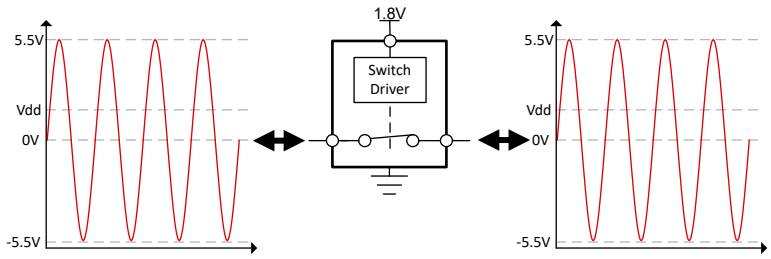


Figure 7-1. Beyond the Supply Signal Support

7.3.2 Bidirectional Operation

The TMUX28xx conducts equally well from source (Sx) to drain (Dx) or from drain (Dx) to source (Sx). Each channel has very similar characteristics in both directions and supports both analog and digital signals.

7.3.3 Power-Off Protection

The TMUX28xx has powered-off protection up to ±5.5V on the switch path. This keeps the switch in a high impedance mode and isolates the source (Sx) and drain (Dx) pins when the supply is removed (Vdd = 0V). Powered-off protection minimizes system complexity by removing the need for power supply sequencing on the signal path. The device performance remains within the leakage performance mentioned in the Electrical Specifications. For more information on powered-off protection, refer to *Eliminate Power Sequencing with Powered-off Protection Signal Switches*.

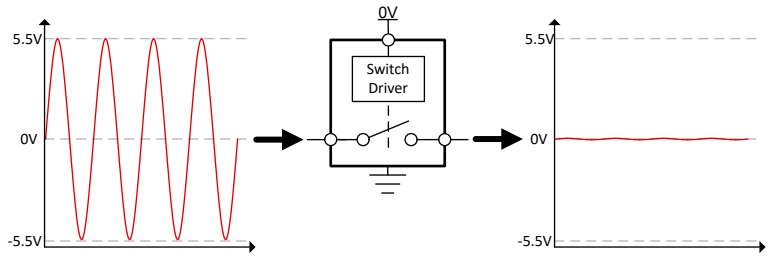


Figure 7-2. Beyond the Supply Power-Off Protection

7.3.4 1.2V and 1.8V Logic Compatible Inputs

The TMUX28xx has 1.2V logic compatibility with a supply of 1.8V and a 1.8V logic compatibility with a 5V supply (V_{DD}). Having lower logic level inputs allows the device to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and bill of material (BOM) cost. For more information on 1.8V logic implementations, refer to Simplifying Design with 1.8V logic Muxes and Switches

7.3.5 Integrated Pull-Down Resistor on Logic Pins

The TMUX28xx has internal weak pull-down resistors to GND so the logic pins are not left floating. This feature integrates up to two external components and reduces system size and cost.

The value of this pull-down resistor is approximately 6MΩ.

7.3.6 Fail-Safe Logic

The TMUX28xx supports Fail-Safe Logic on the control input pin (SEL) allowing for operation up to 5.5V, regardless of the state of the supply pin. This feature allows voltages on the control pin to be applied before the supply pin, protecting the device from potential damage. Fail-Safe Logic minimizes system complexity by removing the need for power supply sequencing on the logic control pins. For example, the Fail-Safe Logic feature allows the logic input pin of the TMUX28xx to be ramped to 5.5V while V_{DD} = 0V. The logic control input is protected against positive faults of up to 5.5V in powered-off condition, but does not offer protection against negative overvoltage conditions.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

TMUX2821 and TMUX2819 are part of the *beyond the supply switches and multiplexers* family of devices. This means that this device can switch signals from -5.5V to 5.5V with a low voltage supply from 1.8V to 5.5V. Additionally, TMUX28xx features powered-off protection, which by design keeps the switches open even when there is no supply. This unique feature combination enables the TMUX28xx to be extremely versatile for a wide variety of applications such as boosted outputs and high common mode offsets.

8.2 Typical Applications

8.2.1 Audio Input or Output Switching

When there are multiple audio inputs available such as a line-in and a wireless connection, a switch/multiplexer is needed to switch between audio sources. This same scheme can be used in systems where there are multiple speaker outputs and one source as well. A TMUX2819 can be used for all of these use cases, easily supporting line-in audio up to ±5.5V with a supply/battery voltage from 1.8V to 5.5V. Figure 8-1 shows the block diagram for these applications. Additionally, if IEC protection is needed on the external connectors (audio jack input or external speaker), 2 TPD1E10B06 can be used.

The TMUX2819 features excellent THD+N performance, so there is minimal impact to the audio signal quality through the switch. This allows the system designer to save a significant portion of board area without impacting signal integrity. Additionally, because of the low supply current requirement, the device's supply can be driven directly with a GPIO, allowing the user to put the device into a ultra-low power mode. In this mode the TMUX2819 operates with powered-off protection, so any high voltage present on the inputs will not propagate to the outputs. This helps keep correct power up cycling and increases system robustness.

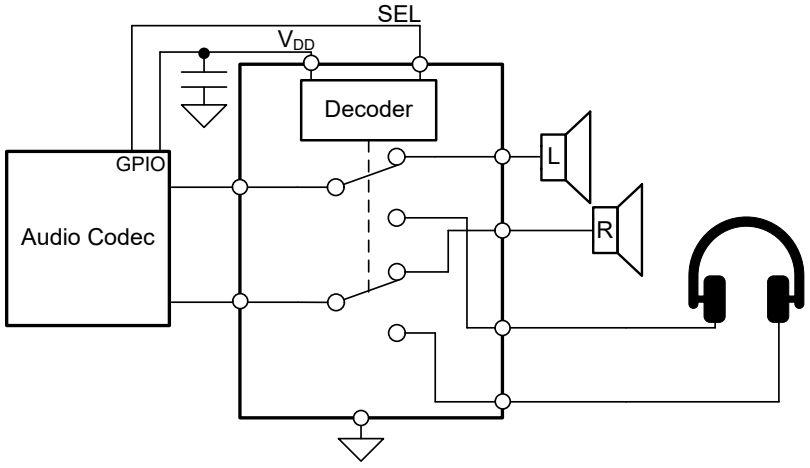


Figure 8-1. Audio Headphone and Speaker Output Switching

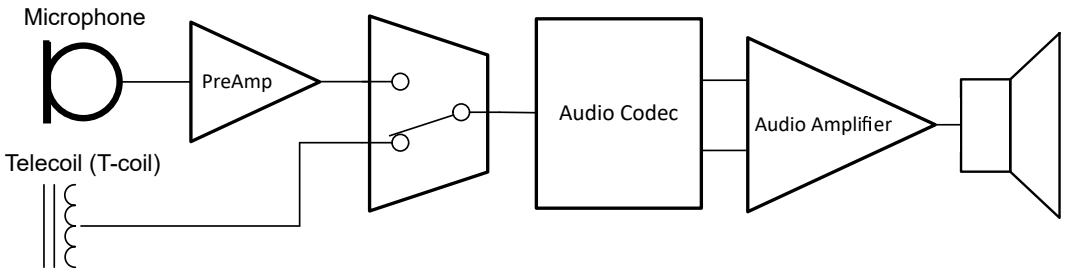


Figure 8-2. Hearing Aid Telecoil MUX

8.3 Power Supply Recommendations

The operates across a wide supply range from 1.8V to 5.5V, while supporting input or output signals from -5.5V to 5.5V.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the supply rails to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1 µF to 10 µF at V_{DD} to ground. Place the bypass capacitors as close to the power supply pin of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes.

For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground and power planes. Always confirm that the ground (GND) connection is established before supplies are ramped.

8.4 Layout

8.4.1 Layout Guidelines

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 8-3 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

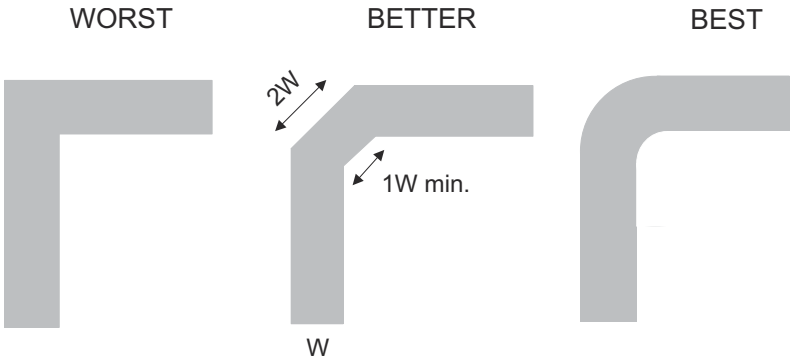


Figure 8-3. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

Some key considerations are as follows:

- For reliable operation, connect a decoupling capacitor ranging from 0.1µF to 10µF between VDD and GND. TI recommends a 0.1µF and 1µF capacitor, placing the lowest value capacitor as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the supply voltage.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.
- Using multiple vias in parallel will lower the overall inductance and is beneficial for connection to ground planes.

8.4.2 Layout Example

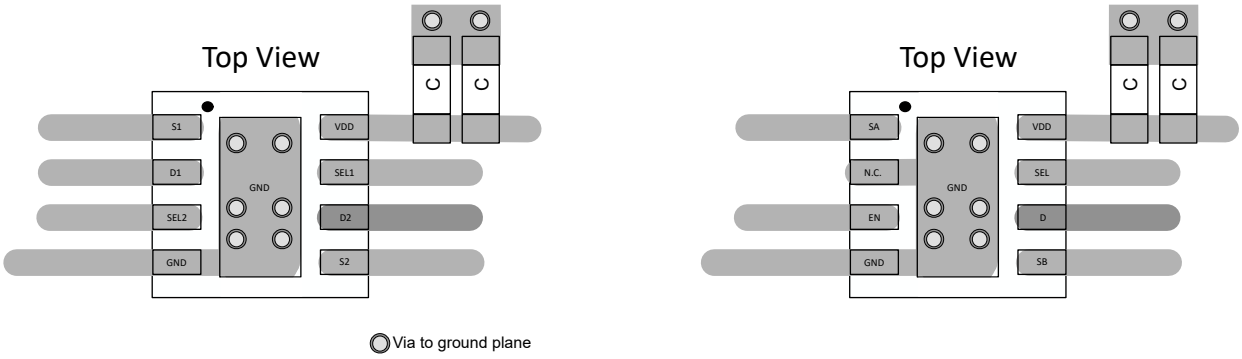


Figure 8-4. TMUX28xx Layout Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Eliminate Power Sequencing with Powered-off Protection Signal Switches* application brief
- Texas Instruments, *Simplifying Design with 1.8V logic Muxes and Switches* application brief

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2025	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMUX2819DSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T281
TMUX2821DSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T282

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

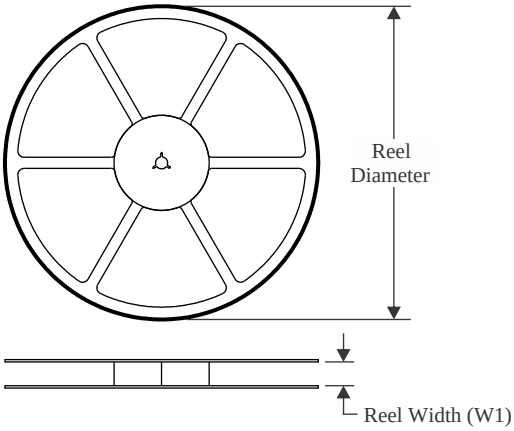
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

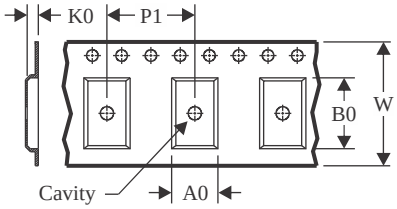
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

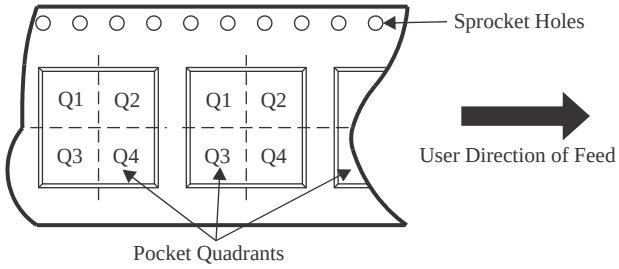


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

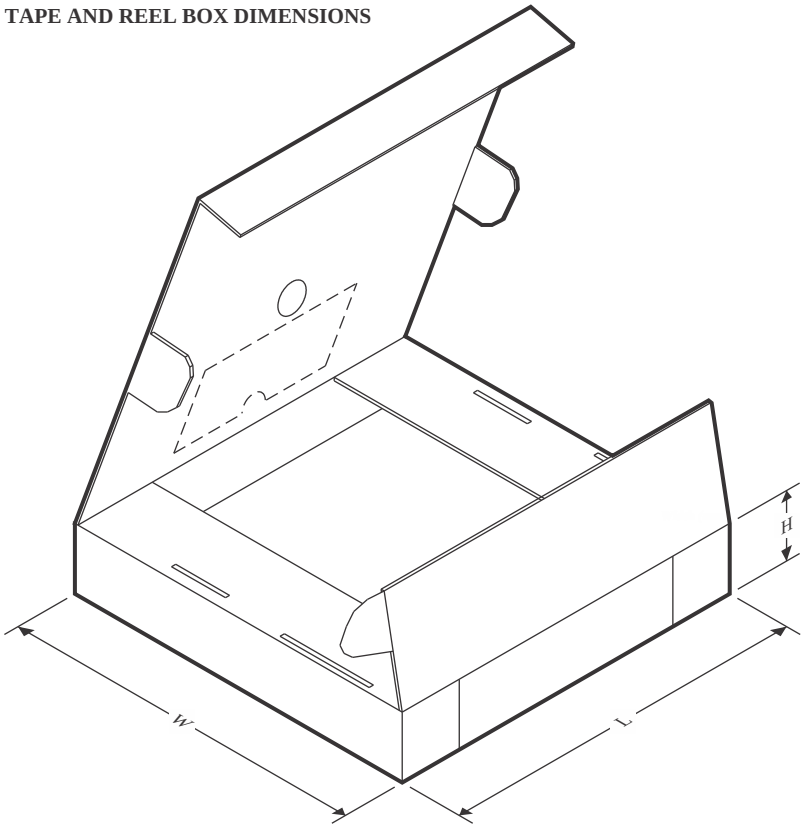
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX2819DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TMUX2821DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX2819DSGR	WSON	DSG	8	3000	182.0	182.0	20.0
TMUX2821DSGR	WSON	DSG	8	3000	182.0	182.0	20.0

GENERIC PACKAGE VIEW

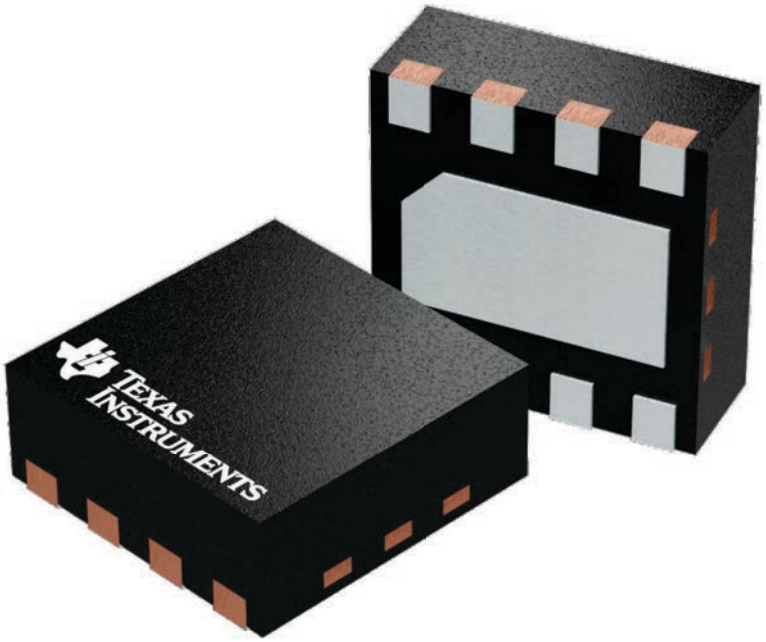
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



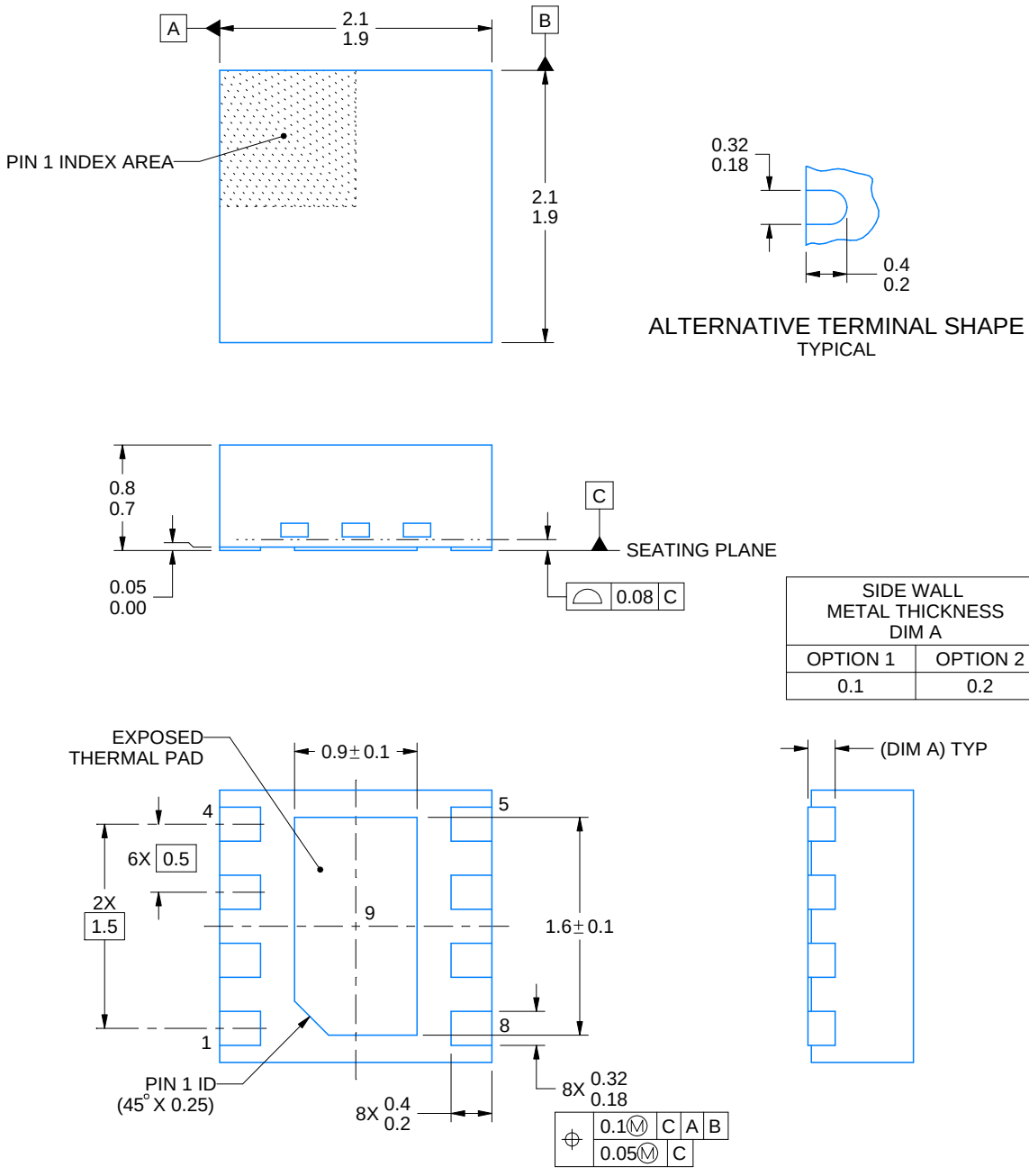
4224783/A

PACKAGE OUTLINE

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



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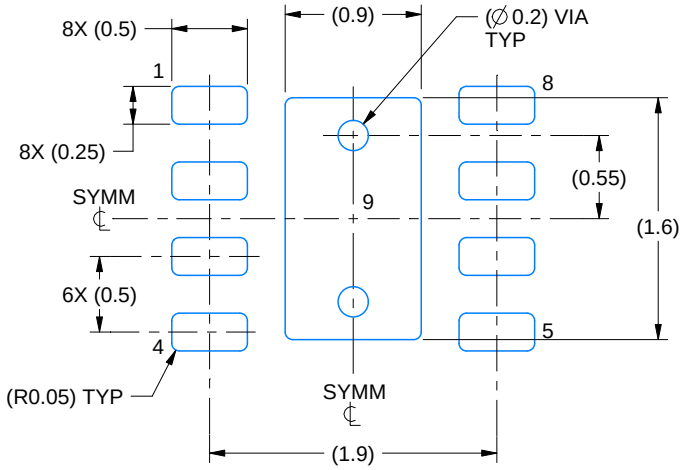
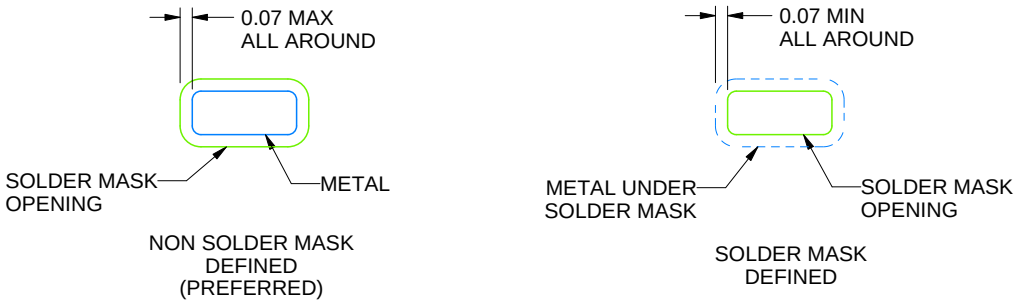
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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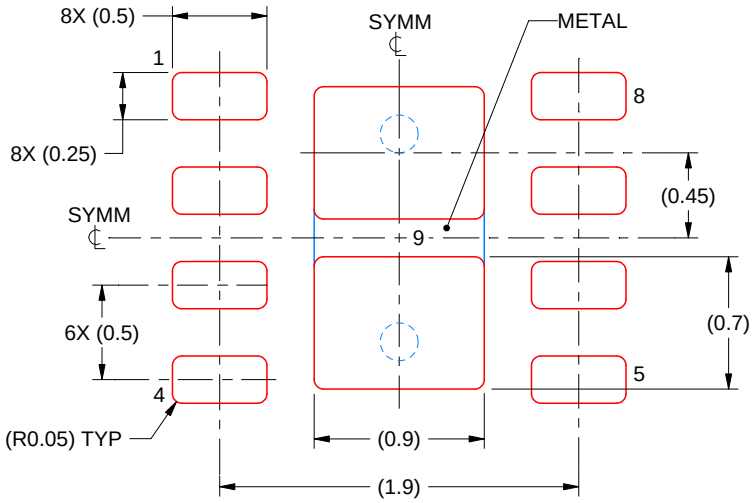
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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