6-W STEREO CLASS-D AUDIO POWER AMPLIFIER

Check for Samples: TPA3005D2

FEATURES

- **6-W/Ch Into an 8-Ω Load From a 12-V Supply**
- **Up to 92% Efficient, Class-D Operation Eliminates Need For Heatsinks**
- **8.5-V to 18-V Single-Supply Operation**
- **Four Selectable, Fixed Gain Settings**
- **Differential Inputs Minimizes Common-Mode Noise**
- **Space-Saving, Thermally Enhanced PowerPAD™ Packaging**
- **Thermal Protection and Short Circuit**
- **Pinout Similar to TPA3002D2, TPA3003D2, and TPA3004D2**

APPLICATIONS

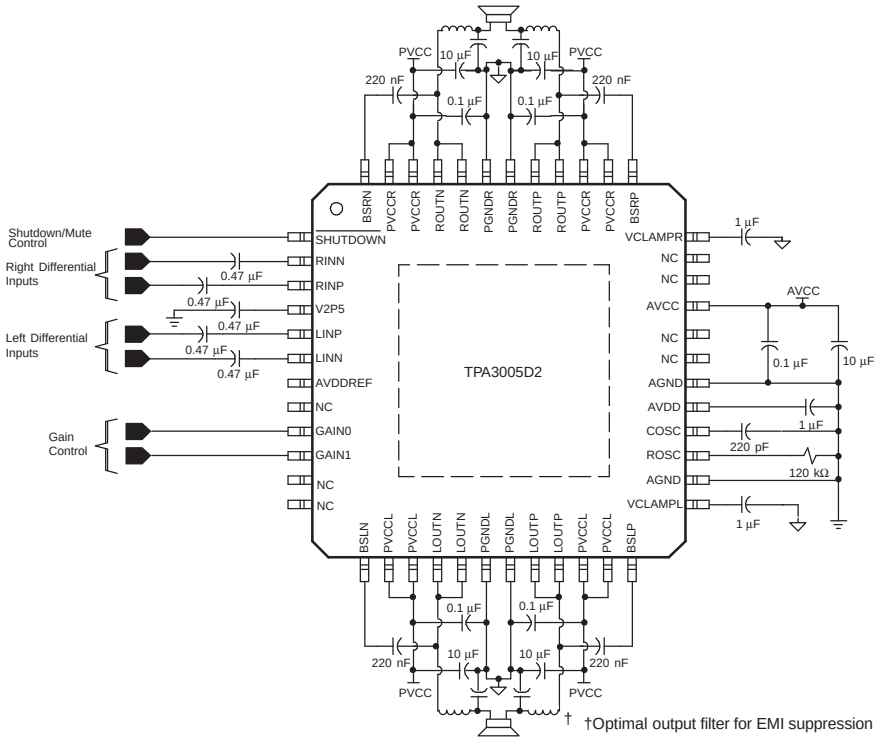
- **LCD Monitors and TVs**
- **All-In-One PCs**

DESCRIPTION

The TPA3005D2 is a 6-W (per channel) efficient, Class-D audio amplifier for driving bridged-tied stereo speakers. The TPA3005D2 can drive stereo speakers as low as 8 Ω. The high efficiency of the TPA3005D2 eliminates the need for external heatsinks when playing music.

The gain of the amplifier is controlled by two gain select pins. The gain selections are 15.3, 21.2, 27.2, and 31.8 dB.

The outputs are fully protected against shorts to GND, VCC, and output-to-output shorts. Thermal protection ensures the maximum junction temperature is not exceeded.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICE 48-PIN HTQFP (PHP)(1) (2)
-40°C to 85°C	TPA3005D2PHP

(1) The PHP package is available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA3005D2PHPR).
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		TPA3005D2
Supply voltage range	AV_{CC}, PV_{CC}	-0.3 V to 20 V
Load Impedance, R_L		≥ 6 Ω
Input voltage range, V_I	$\overline{\text{SHUTDOWN}}$	-0.3 V to VCC + 0.3 V
	GAIN0, GAIN1, RINN, RINP, LINN, LINP	-0.3 V to 6 V
Continuous total power dissipation		See Thermal Information Table
Operating free–air temperature range, T_A		- 40°C to 85°C
Operating junction temperature range, T_J		- 40°C to 150°C
Storage temperature range, T_{stg}		- 65°C to 150°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1) (2)		TPA3005D2 PHP (48 PINS)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	27.7	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	14.8	
θ_{JB}	Junction-to-board thermal resistance	9.4	
ψ_{JT}	Junction-to-top characterization parameter	0.6	
ψ_{JB}	Junction-to-board characterization parameter	5.6	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	0.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
Supply voltage, V_{CC}	PV_{CC}, AV_{CC}	8.5	18	V
High-level input voltage, V_{IH}	$\overline{\text{SHUTDOWN}}$, GAIN0, GAIN1	2		V
Low-level input voltage, V_{IL}	$\overline{\text{SHUTDOWN}}$, GAIN0, GAIN1		0.8	V
High-level input current, I_{IH}	$\overline{\text{SHUTDOWN}}$, $V_I = V_{CC}$ = 18 V		10	µA
	GAIN0, GAIN1, V_I = 5.5 V, V_{CC} = 18 V		1	µA
Low-level input current, I_{IL}	$\overline{\text{SHUTDOWN}}$, V_I = 0 V, V_{CC} = 18 V		1	µA
	GAIN0, GAIN1, V_I = 5.5 V, V_{CC} = 18 V		1	µA
Oscillator frequency, f_{OSC}	Frequency is set by selection of ROSC and COSC (see the *Application Information Section*).	200	300	kHz
Operating free–air temperature, T_A		-40	85	°C

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 12 V, R_L = 8 Ω (unless otherwise noted)

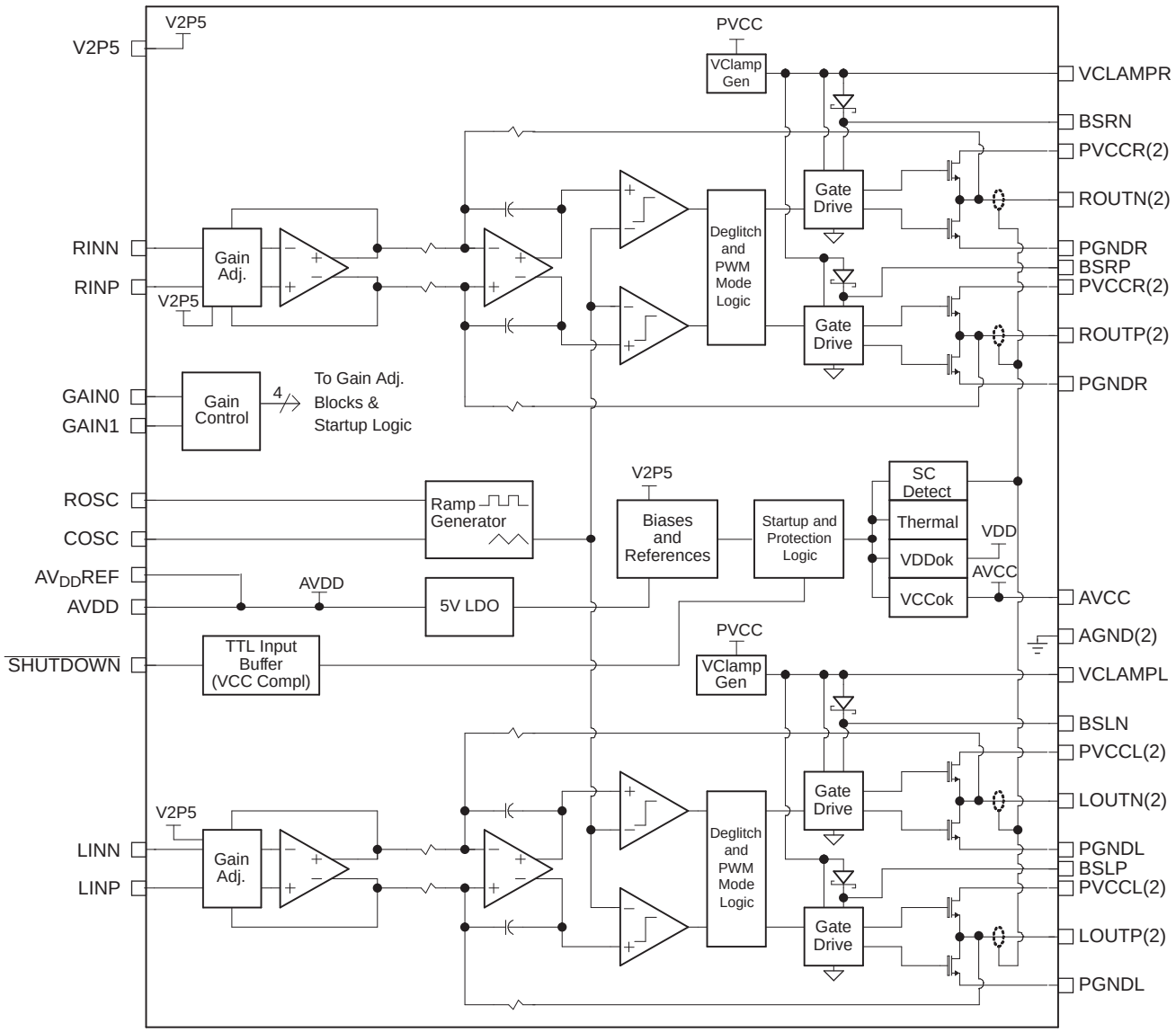
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\|V_{OO}\|$	Class-D output offset voltage (measured differentially)	INN and INP connected together, Gain = 36 dB			5	55	mV
V2P5	2.5-V Bias voltage	No load			2.5		V
AV_{DD}	+5-V internal supply voltage	I_L = 10 mA, $\overline{SHUTDOWN}$ = 2 V, V_{CC} = 8.5 V to 18 V		4.5	5	5.5	V
PSRR	Power supply rejection ratio	V_{CC} = 11.5 V to 12.5 V			-80		dB
I_{CC}	Quiescent supply current	$\overline{SHUTDOWN}$ = 2 V, no load			11	22	mA
$I_{CC(SD)}$	Quiescent supply current in shutdown mode	$\overline{SHUTDOWN}$ = 0 V			1.6	25	µA
$r_{DS(on)}$	Drain-source on-state resistance	V_{CC} = 12 V, I_O = 1 A, T_J = 25°C	High side		600		mΩ
			Low side		500		
			Total		1100	1300	
G	Gain	GAIN1 = 0.8 V	GAIN0 = 0.8 V	14.6	15.3	16.2	dB
			GAIN0 = 2 V	20.5	21.2	21.8	
		GAIN1 = 2 V	GAIN0 = 0.8 V	26.4	27.2	27.8	
			GAIN0 = 2 V	31.1	31.8	32.5	
t_{on}	Turn-on time	$C_{(V2P5)}$ = 1 µF, $\overline{SHUTDOWN}$ = 2 V			16		ms
t_{off}	Turn-off time	$C_{(V2P5)}$ = 1 µF, $\overline{SHUTDOWN}$ = 0.8 V			60		µs

AC ELECTRICAL CHARACTERISTICS

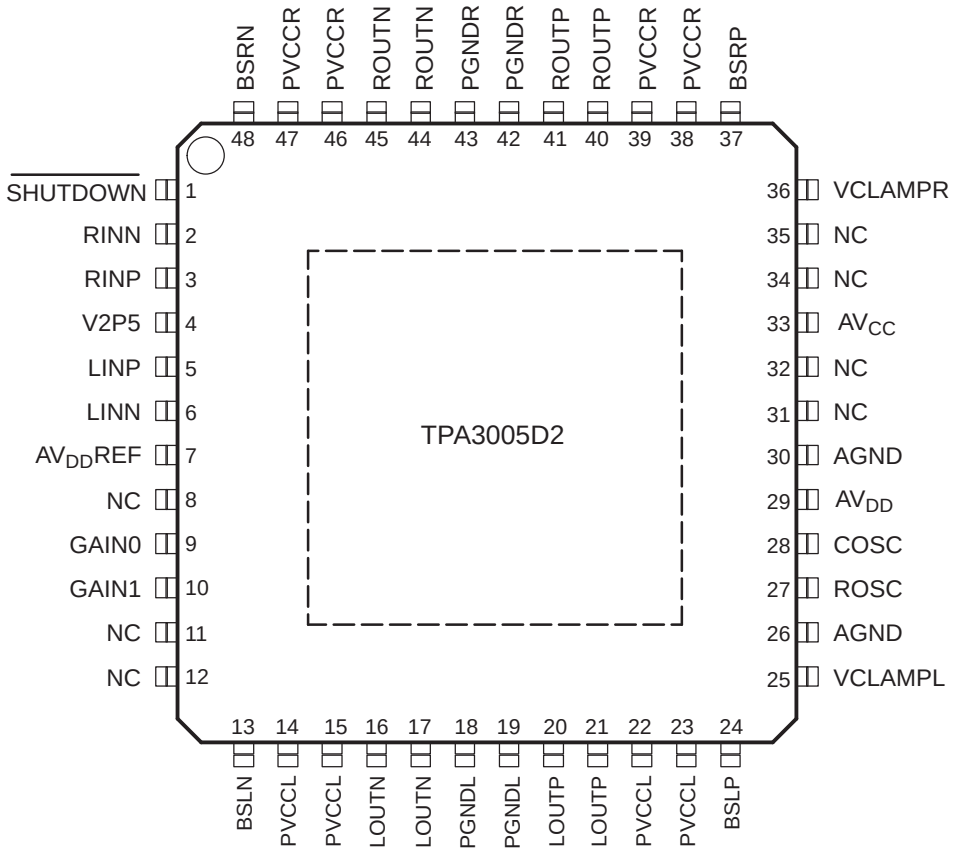
T_A = 25°C, V_{CC} = 12 V, R_L = 8 Ω, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
k_{SVR}	Supply voltage rejection ratio	200 mV_{PP} ripple from 20 Hz to 1 kHz, Gain = 15.6 dB, Inputs ac-coupled to GND		-70		dB
P_O	Continuous output power	THD+N = 0.13%, f = 1 kHz, R_L = 8 Ω		3		W
		THD+N = 0.23%, f = 1 kHz, R_L = 8 Ω		6		
THD+N	Total harmonic distortion plus noise	P_O = 1 W, f = 1 kHz, R_L = 8 Ω		0.1%		
V_n	Output integrated noise floor	20 Hz to 22 kHz, A-weighted filter, Gain = 15.6 dB		-80		dB
	Crosstalk	P_O = 1 W, R_L = 8 Ω, Gain = 15.6 dB, f = 1 kHz		-93		dB
SNR	Signal-to-noise ratio	Maximum output at THD+N < 0.5%, f = 1 kHz, Gain = 15.6 dB		97		dB
	Thermal trip point			150		°C
	Thermal hystersis			20		°C

FUNCTIONAL BLOCK DIAGRAM



PHP PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

PIN NAME	PIN NUMBER	I/O	DESCRIPTION
AGND	26, 30	-	Analog ground for digital/analog cells in core
AV_{CC}	33	-	High-voltage analog power supply, not connected internally to PVCCR or PVCCL
AV_{DD}	29	O	5-V Regulated output for use by internal cells and GAIN0, GAIN1 pins only. Not specified for driving other external circuitry.
AV_{DD}REF	7	O	5-V Reference output—connect to gain setting resistor or directly to GAIN0, GAIN1.
BSLN	13	-	Bootstrap I/O for left channel, negative high-side FET
BSLP	24	-	Bootstrap I/O for left channel, positive high-side FET
BSRN	48	-	Bootstrap I/O for right channel, negative high-side FET
BSRP	37	-	Bootstrap I/O for right channel, positive high-side FET
COSC	28	I/O	I/O for charge/discharging currents onto capacitor for ramp generator.
GAIN0	9	I	Gain select least significant bit. TTL logic levels with compliance to AV_{DD}.
GAIN1	10	I	Gain select most significant bit. TTL logic levels with compliance to AV_{DD}.
LINN	6	I	Negative audio input for left channel
LINP	5	I	Positive audio input for left channel
LOUTN	16, 17	O	Class-D 1/2-H-bridge negative output for left channel
LOUTP	20, 21	O	Class-D 1/2-H-bridge positive output for left channel
NC	8, 11, 12, 31, 32, 34, 35	-	No internal connection
PGNDL	18, 19	-	Power ground for left channel H-bridge
PGNDR	42, 43	-	Power ground for right channel H-bridge
PVCCL	14, 15	-	Power supply for left channel H-bridge (internally connected to pins 22 and 23), not connected to PVCCR or AV_{CC}.
PVCCL	22, 23	-	Power supply for left channel H-bridge (internally connected to pins 14 and 15), not connected to PVCCR or AV_{CC}.
PVCCR	38, 39	-	Power supply for right channel H-bridge (internally connected to pins 46 and 47), not connected to PVCCL or AV_{CC}.
PVCCR	46, 47	-	Power supply for right channel H-bridge (internally connected to pins 38 and 39), not connected to PVCCL or AV_{CC}.
RINP	3	I	Positive audio input for right channel
RINN	2	I	Negative audio input for right channel
ROSC	27	I/O	I/O current setting resistor for ramp generator.
ROUTN	44, 45	O	Class-D 1/2-H-bridge negative output for right channel
ROUTP	40, 41	O	Class-D 1/2-H-bridge positive output for right channel
$\overline{\text{SHUTDOWN}}$	1	I	Shutdown signal for IC (low = shutdown, high = operational). TTL logic levels with compliance to V_{CC}.
VCLAMPL	25	-	Internally generated voltage supply for left channel bootstrap capacitors.
VCLAMPR	36	-	Internally generated voltage supply for right channel bootstrap capacitors.
V2P5	4	O	2.5-V Reference for analog cells.
Thermal Pad	-	-	Connect to AGND and PGND—should be the center point for both grounds. Internal resistive connection to AGND.

TYPICAL CHARACTERISTICS

Table 1. TABLE OF GRAPHS

			FIGURE
THD+N	Total harmonic distortion + noise	vs Output power	1, 2
		vs Frequency	3, 4, 5, 6
	Closed loop response		7
I_{CC}	Supply current	vs Output power	8
	Efficiency	vs Output power	9
	Output power	vs Supply voltage	10, 11

TYPICAL CHARACTERISTICS (continued)

Table 1. TABLE OF GRAPHS (continued)

	Crosstalk	vs Frequency	12
k_{SVR}	Supply ripple rejection ratio	vs Frequency	13
CMRR	Commom-mode rejection ratio	vs Frequency	14

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

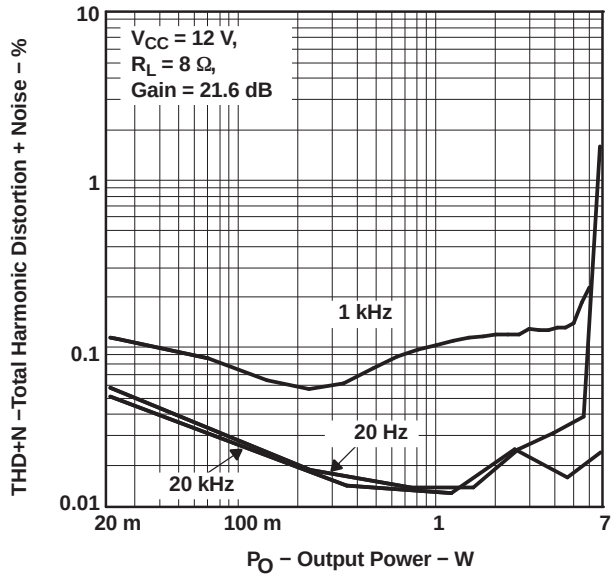


Figure 1.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

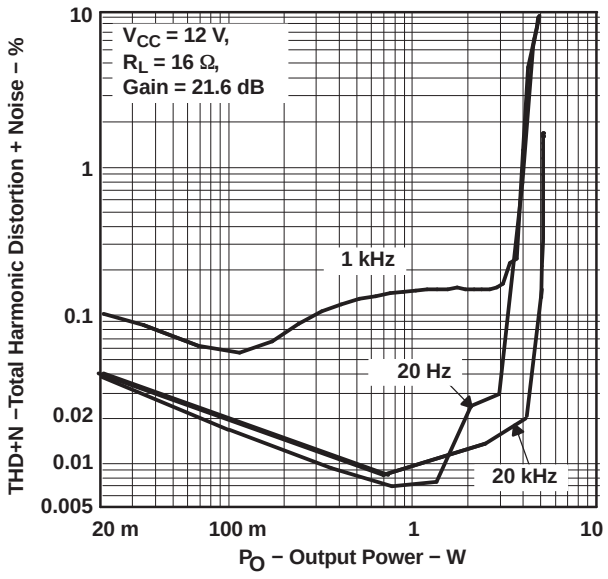


Figure 2.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

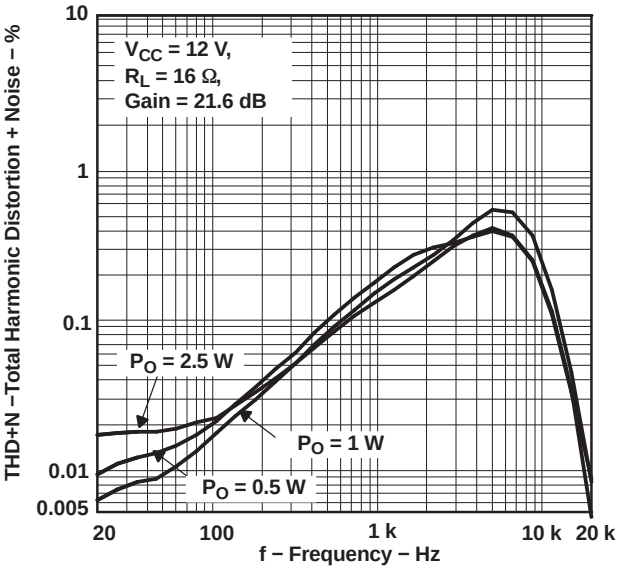


Figure 3.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

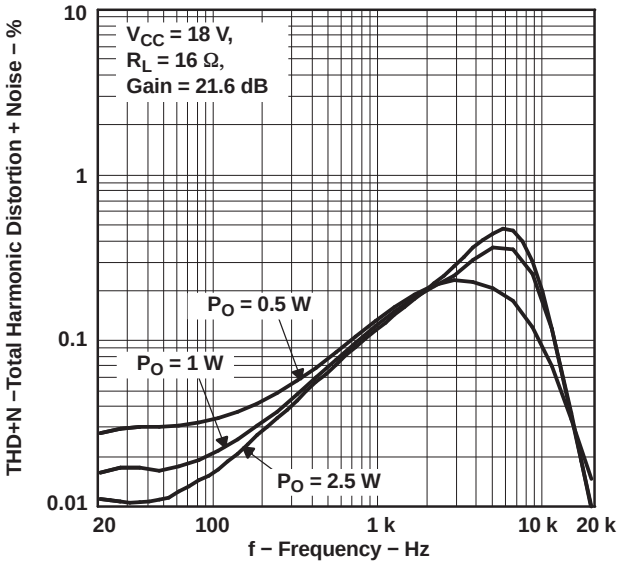


Figure 4.

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY

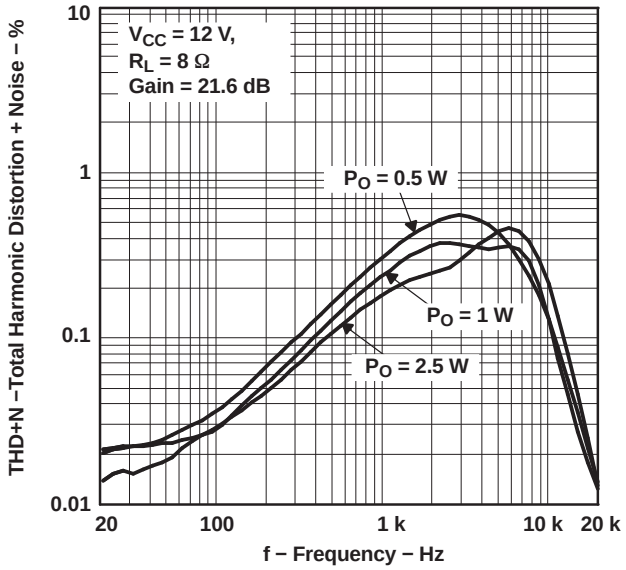


Figure 5.

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY

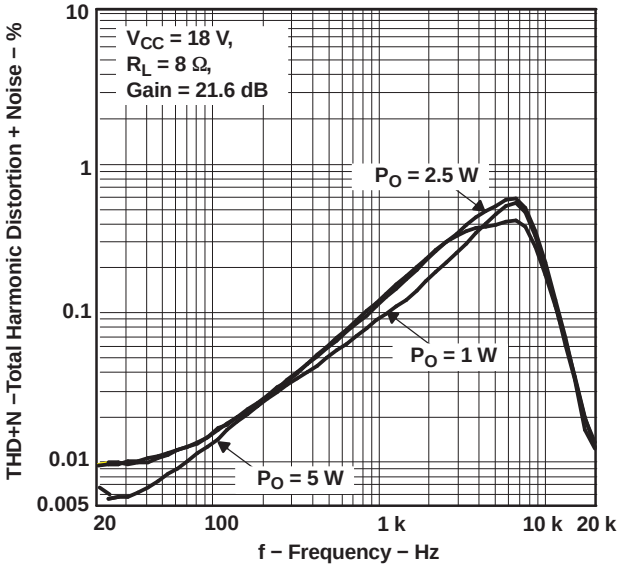


Figure 6.

CLOSED LOOP RESPONSE

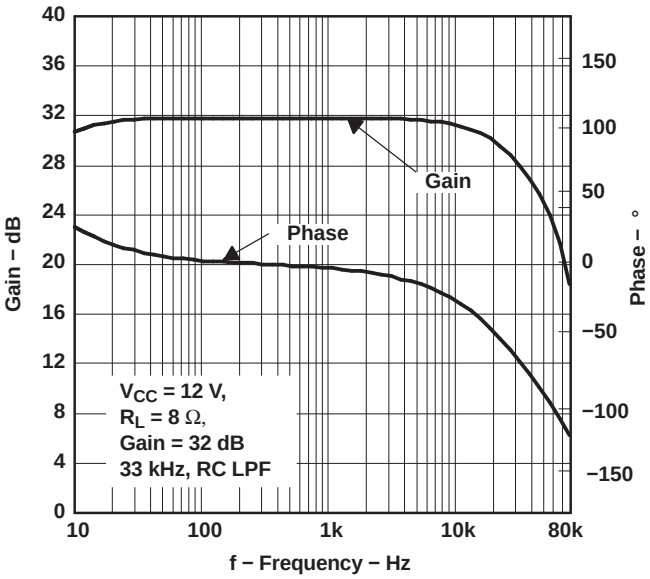


Figure 7.

SUPPLY CURRENT
vs
TOTAL OUTPUT POWER

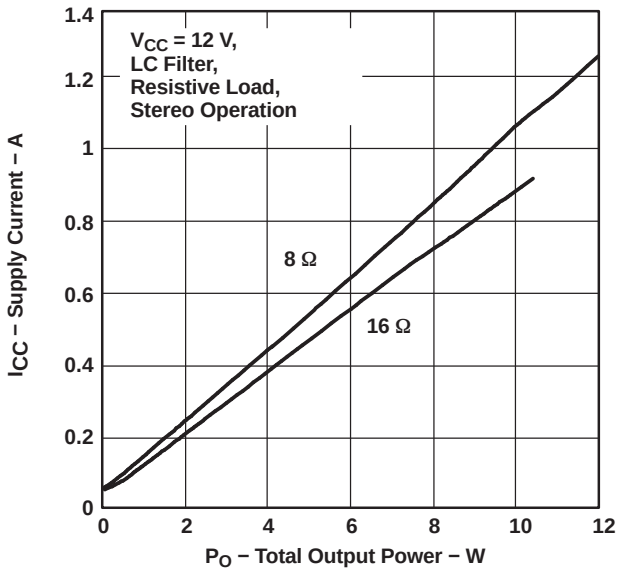


Figure 8.

EFFICIENCY vs TOTAL OUTPUT POWER

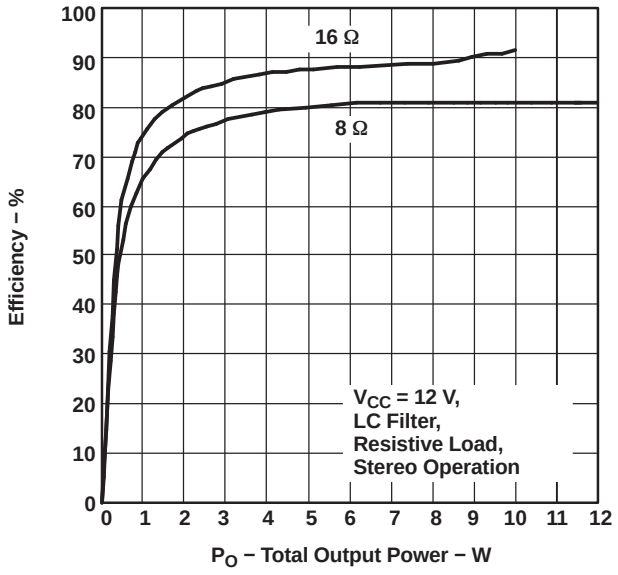


Figure 9.

OUTPUT POWER vs SUPPLY VOLTAGE

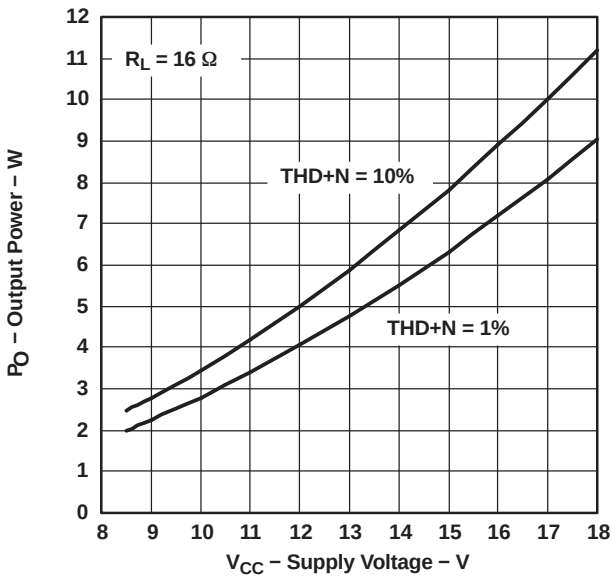


Figure 10.

OUTPUT POWER vs SUPPLY VOLTAGE

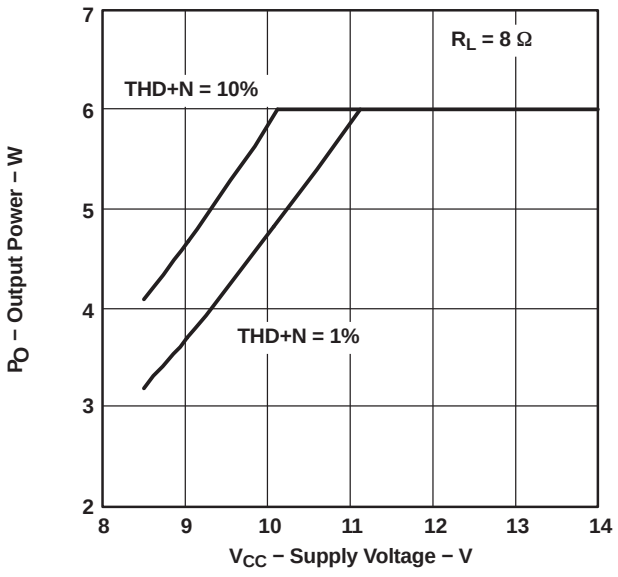


Figure 11.

CROSSTALK vs FREQUENCY

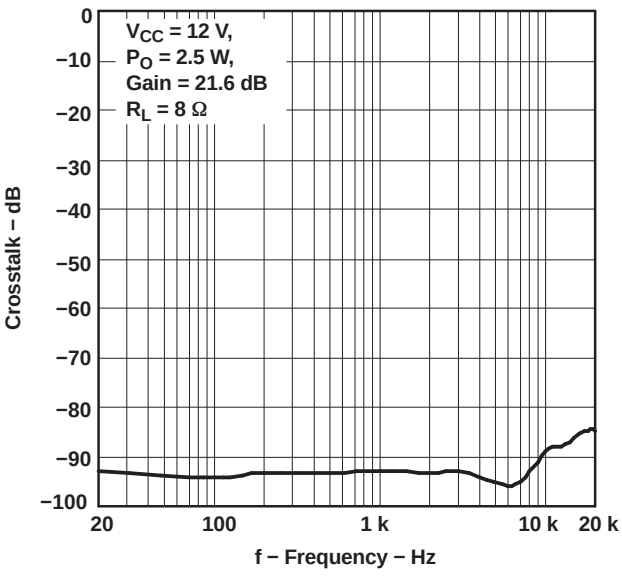


Figure 12.

SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY

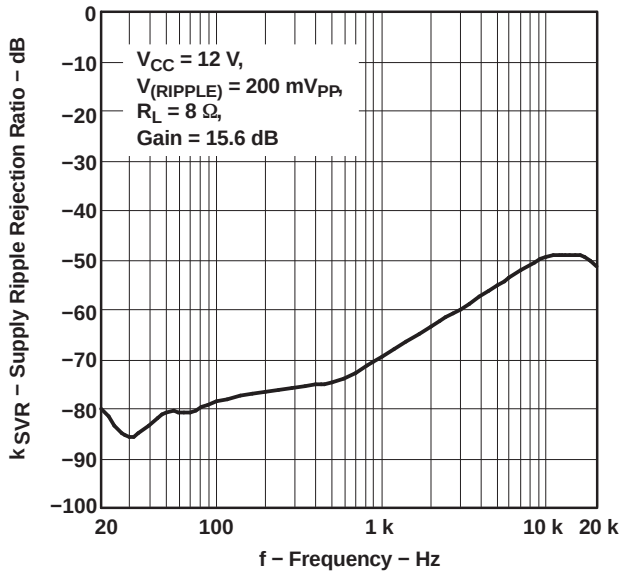


Figure 13.

COMMON-MODE REJECTION RATIO vs FREQUENCY

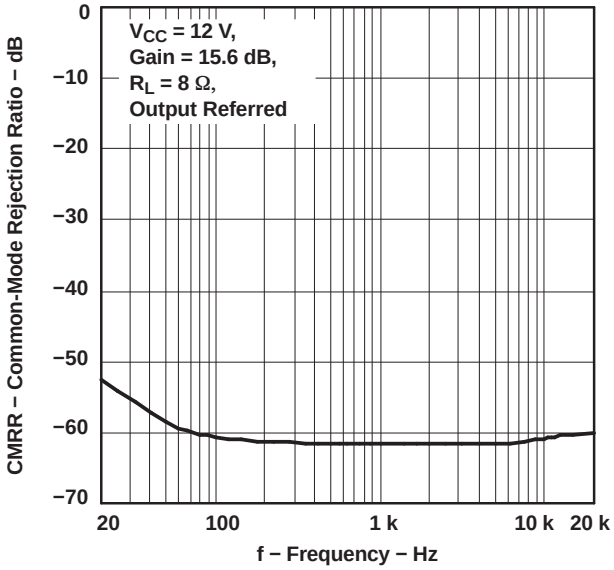


Figure 14.

APPLICATION INFORMATION

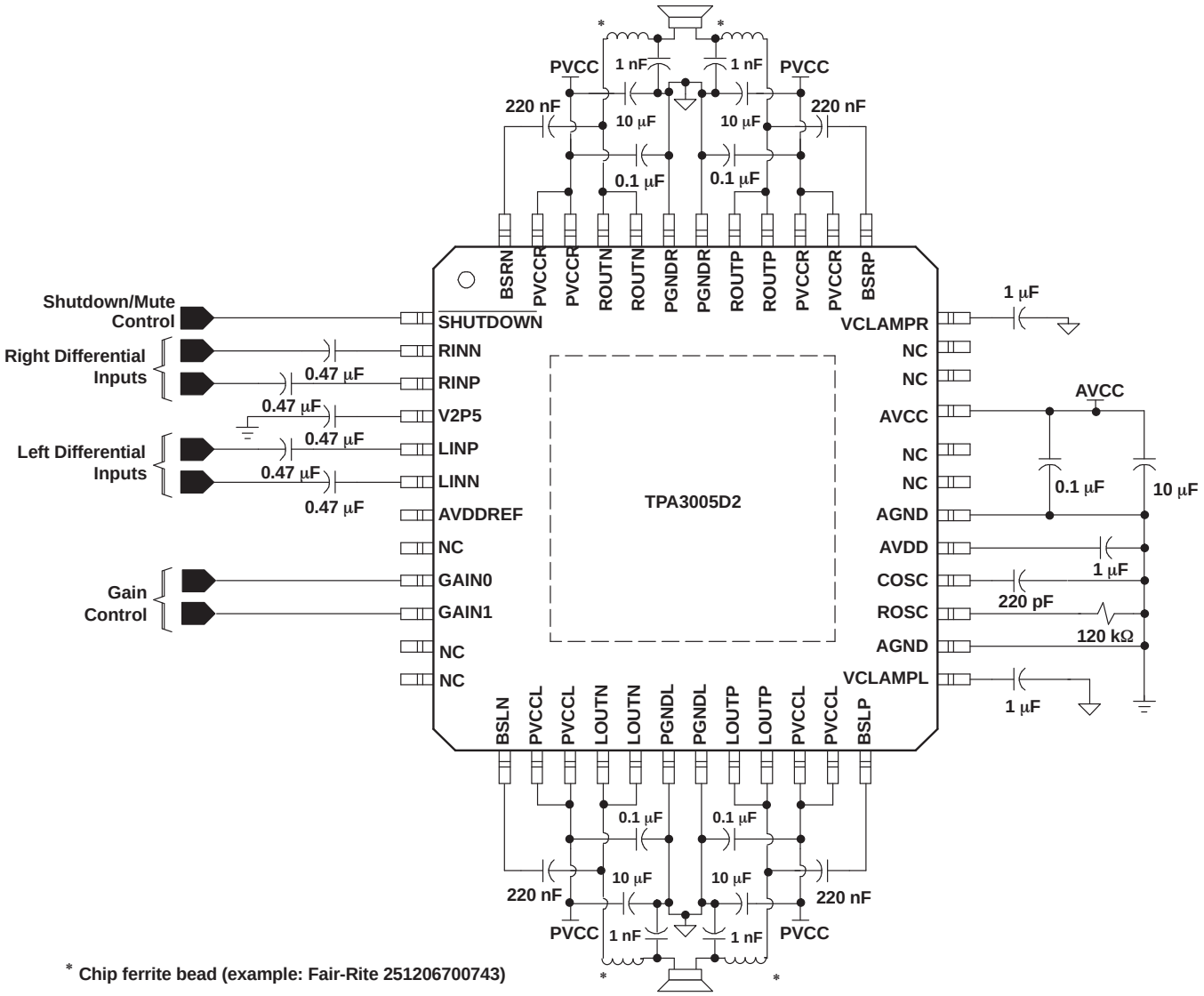


Figure 15. Stereo Class-D With Differential Inputs

CLASS-D OPERATION

This section focuses on the class-D operation of the TPA3005D2.

Traditional Class-D Modulation Scheme

The traditional class-D modulation scheme, which is used in the TPA032D0x family, has a differential output where each output is 180 degrees out of phase and changes from ground to the supply voltage, V_{CC}. Therefore, the differential prefiltered output varies between positive and negative V_{CC}, where filtered 50% duty cycle yields 0 V across the load. The traditional class-D modulation scheme with voltage and current waveforms is shown in Figure 16. Note that even at an average of 0 V across the load (50% duty cycle), the current to the load is high, causing high loss and thus causing a high supply current.

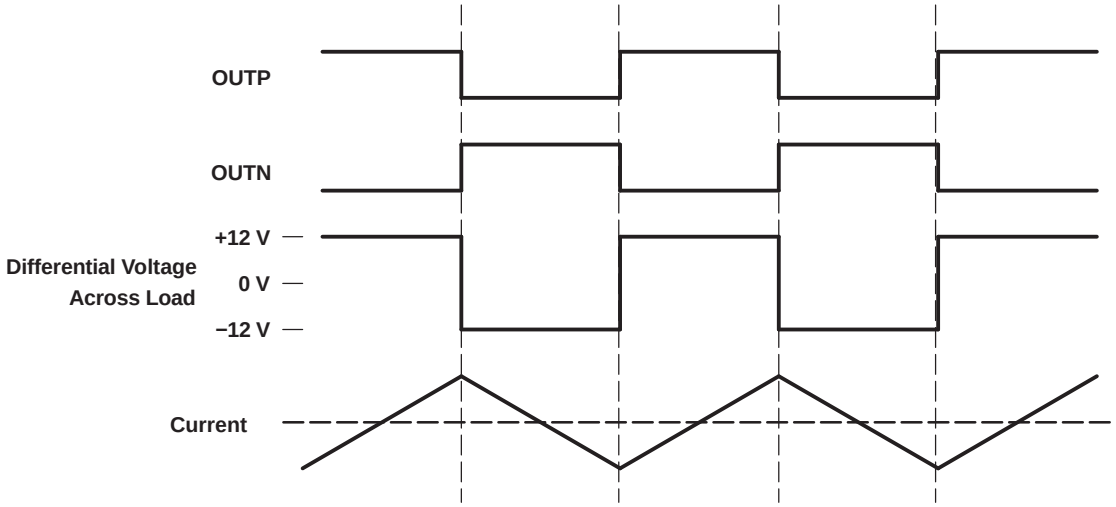


Figure 16. Traditional Class-D Modulation Scheme's Output Voltage and Current Waveforms Into an Inductive Load With No Input

TPA3005D2 Modulation Scheme

The TPA3005D2 uses a modulation scheme that still has each output switching from 0 to the supply voltage. However, OUTP and OUTN are now in phase with each other with no input. The duty cycle of OUTP is greater than 50% and OUTN is less than 50% for positive output voltages. The duty cycle of OUTP is less than 50% and OUTN is greater than 50% for negative output voltages. The voltage across the load sits at 0 V throughout most of the switching period, greatly reducing the switching current, which reduces any I^2R losses in the load.

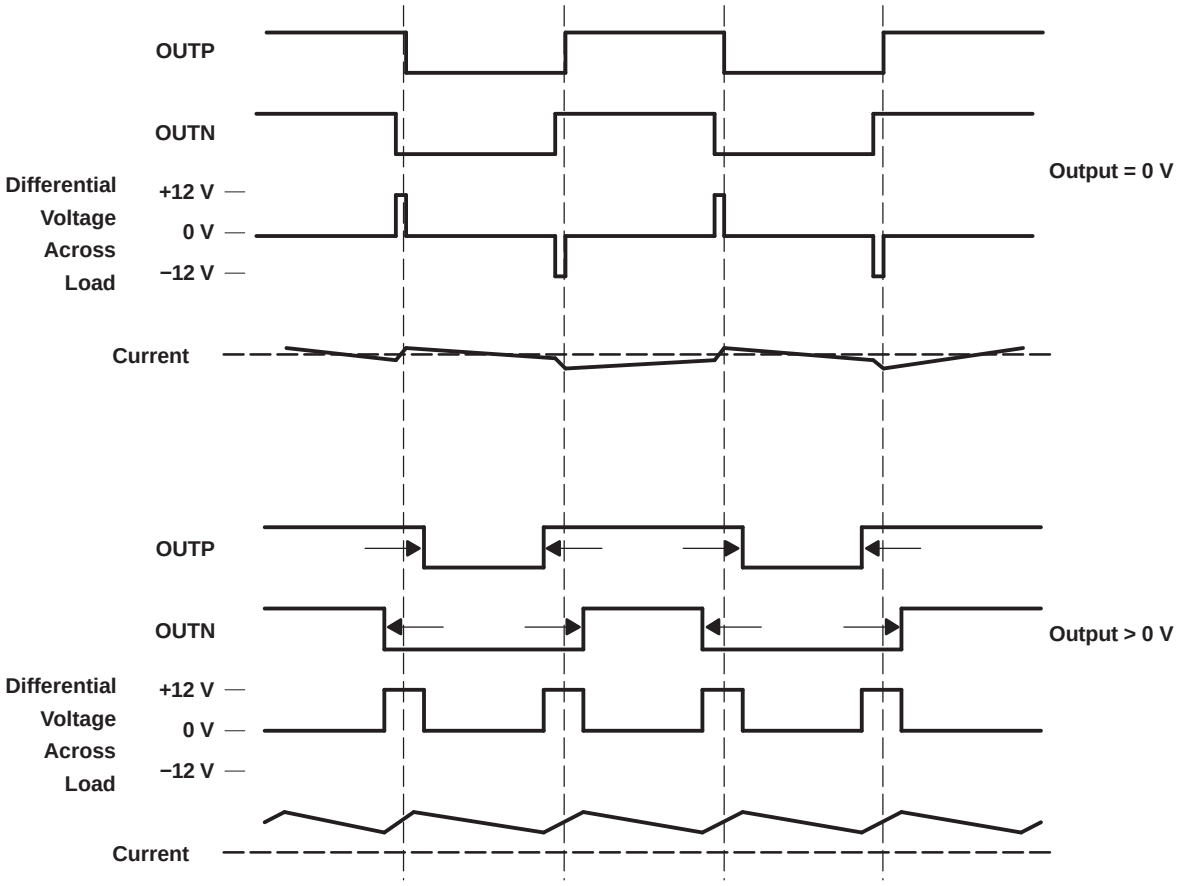


Figure 17. The TPA3005D2 Output Voltage and Current Waveforms Into an Inductive Load

Efficiency: LC Filter Required With the Traditional Class-D Modulation Scheme

The main reason that the traditional class-D amplifier needs an output filter is that the switching waveform results in maximum current flow. This causes more loss in the load, which causes lower efficiency. The ripple current is large for the traditional modulation scheme, because the ripple current is proportional to voltage multiplied by the time at that voltage. The differential voltage swing is 2 x V_{CC}, and the time at each voltage is half the period for the traditional modulation scheme. An ideal LC filter is needed to store the ripple current from each half cycle for the next half cycle, while any resistance causes power dissipation. The speaker is both resistive and reactive, whereas an LC filter is almost purely reactive.

The TPA3005D2 modulation scheme has little loss in the load without a filter because the pulses are short and the change in voltage is V_{CC} instead of 2 x V_{CC}. As the output power increases, the pulses widen, making the ripple current larger. Ripple current could be filtered with an LC filter for increased efficiency, but for most applications the filter is not needed.

An LC filter with a cutoff frequency less than the class-D switching frequency allows the switching current to flow through the filter instead of the load. The filter has less resistance than the speaker, which results in less power dissipation, therefore increasing efficiency.

Effects of Applying a Square Wave Into a Speaker

Audio specialists have advised for years not to apply a square wave to speakers. If the amplitude of the waveform is high enough and the frequency of the square wave is within the bandwidth of the speaker, the square wave could cause the voice coil to jump out of the air gap and/or scar the voice coil. A 250-kHz switching frequency, however, does not significantly move the voice coil, as the cone movement is proportional to $1/f^2$ for frequencies beyond the audio band.

Damage may occur if the voice coil cannot handle the additional heat generated from the high-frequency switching current. The amount of power dissipated in the speaker may be estimated by first considering the overall efficiency of the system. If the on-resistance (rds(on)) of the output transistors is considered to cause the dominant loss in the system, then the maximum theoretical efficiency for the TPA3005D2 with an 8-Ω load is as follows:

$$\text{Efficiency (theoretical, \%)} = \frac{R_L}{\left(R_L + r_{ds(on)}\right)} \times 100\% = \frac{8}{(8 + 1.3)} \times 100\% = 86\% \quad (1)$$

The maximum measured output power is approximately 6 W with an 12-V power supply. The total theoretical power supplied (P(total)) for this worst-case condition would therefore be as follows:

$$P_{(total)} = \frac{P_O}{\text{Efficiency}} = \frac{6\ W}{0.86} = 6.98\ W \quad (2)$$

The efficiency measured in the lab using an 8-W speaker was 81%. The power not accounted for as dissipated across the $r_{DS(on)}$ may be calculated by simply subtracting the theoretical power from the measured power:

$$\text{Other losses} = P_{(total)}\text{(measured)} - P_{(total)}\text{ (theoretical)} = 7.41 - 6.98 = 0.43\ W \quad (3)$$

The quiescent supply current at 12 V is measured to be 22 mA. It can be assumed that the quiescent current encapsulates all remaining losses in the device, i.e., biasing and switching losses. It may be assumed that any remaining power is dissipated in the speaker and is calculated as follows:

$$P_{(dis)} = 0.43\ W - (12\ V \times 22\ mA) = 0.17\ W \quad (4)$$

Note that these calculations are for the worst-case condition of 6 W delivered to the speaker. Because the 0.17 W is only 3% of the power delivered to the speaker, it may be concluded that the amount of power actually dissipated in the speaker is relatively insignificant. Furthermore, this power dissipated is well within the specifications of most loudspeaker drivers in a system, as the power rating is typically selected to handle the power generated from a clipping waveform.

When to use an Output Filter

Design the TPA3005D2 without the filter if the traces from amplifier to speaker are short (< 50 cm). Powered speakers, where the speaker is in the same enclosure as the amplifier, is a typical application for class-D without a filter.

Most applications require a ferrite bead filter. The ferrite filter reduces EMI around 1 MHz and higher (FCC and CE only test radiated emissions greater than 30 MHz). When selecting a ferrite bead, choose one with high impedance at high frequencies, but low impedance at low frequencies.

Use a LC output filter if there are low frequency (<1 MHz) EMI-sensitive circuits and/or there are long wires from the amplifier to the speaker.

When both a LC filter and a ferrite bead filter are used, the LC filter should be placed as close as possible to the IC followed by the ferrite bead filter.

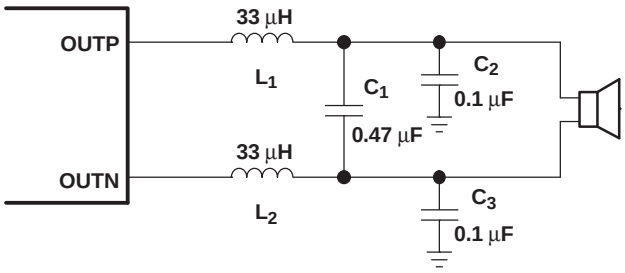


Figure 18. Typical LC Output Filter, Cutoff Frequency of 27 kHz, Speaker Impedance = 8 Ω

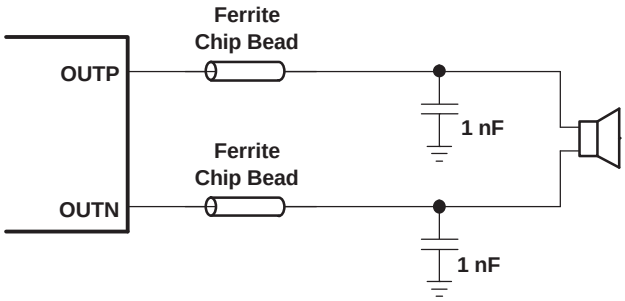


Figure 19. Typical Ferrite Chip Bead Filter (Chip bead example: Fair-Rite 2512067007Y3)

Gain setting via GAIN0 and GAIN1 inputs

The gain of the TPA3005D2 is set by two input terminals, GAIN0 and GAIN1.

The gains listed in Table 2 are realized by changing the taps on the input resistors inside the amplifier. This causes the input impedance (Z_i) to be dependent on the gain setting. The actual gain settings are controlled by ratios of resistors, so the gain variation from part-to-part is small. However, the input impedance may shift by 20% due to shifts in the actual resistance of the input resistors.

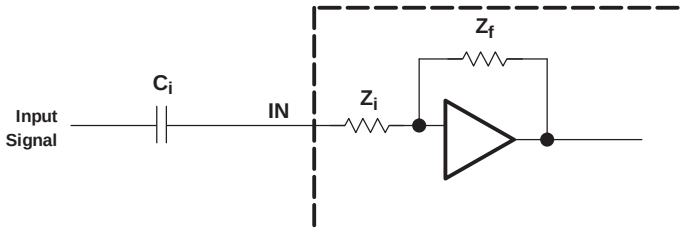
For design purposes, the input network (discussed in the next section) should be designed assuming an input impedance of 26 kΩ, which is the absolute minimum input impedance of the TPA3005D2. At the lower gain settings, the input impedance could increase as high as 165 kΩ

Table 2. Gain Setting

GAIN1	GAIN0	AMPLIFIER GAIN (dB)	INPUT IMPEDANCE (kΩ)
		TYP	TYP
0	0	15.3	137
0	1	21.2	88
1	0	27.2	52
1	1	31.8	33

INPUT RESISTANCE

Each gain setting is achieved by varying the input resistance of the amplifier that can range from its smallest value, 33 kΩ, to the largest value, 137 kΩ. As a result, if a single capacitor is used in the input high-pass filter, the -3 dB or cutoff frequency changes when changing gain steps.



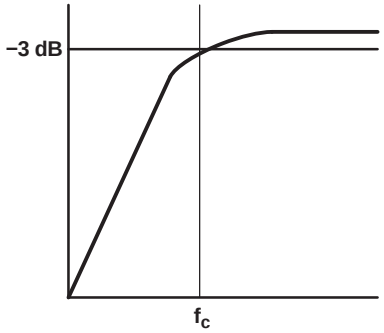
The -3-dB frequency can be calculated using Equation 5. Use Table 2 for Z_i values.

$$f = \frac{1}{2\pi Z_i C_i} \quad (5)$$

INPUT CAPACITOR, C_I

In the typical application an input capacitor (C_i) is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_i and the input impedance of the amplifier (Z_i) form a high-pass filter with the corner frequency determined in Equation 6.

$$f_c = \frac{1}{2\pi Z_i C_i} \quad (6)$$



The value of C_i is important, as it directly affects the bass (low frequency) performance of the circuit. Consider the example where Z_i is 137 kΩ and the specification calls for a flat bass response down to 20 Hz. Equation 6 is reconfigured as Equation 7.

$$C_i = \frac{1}{2\pi Z_i f_c} \quad (7)$$

In this example, C_i is 58 nF, so one would likely choose a value of 0.1 µF as this value is commonly used. If the gain is known and is constant, use Z_i from Table 2 to calculate C_i. A further consideration for this capacitor is the leakage path from the input source through the input network (C_i) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at 2.5 V, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application.

For the best pop performance, C_I should be less than or equal to 1µF.

Power Supply Decoupling,C_S

The TPA3005D2 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 µF placed as close as possible to the device V_{CC} lead works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 µF or greater placed near the audio power amplifier is recommended. The 10-µF capacitor also serves as local storage capacitor for supplying current during large signal transients on the amplifier outputs.

BSN and BSP Capacitors

The full H-bridge output stages use only NMOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 220-nF ceramic capacitor, rated for at least 25 V, must be connected from each output to its corresponding bootstrap input. Specifically, one 220-nF capacitor must be connected from xOUTP to xBSP, and one 220-nF capacitor must be connected from xOUTN to xBSN. (See the application circuit diagram in Figure 15).

The bootstrap capacitors connected between the BSxx pins and corresponding output function as a floating power supply for the high-side N-channel power MOSFET gate drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

VCLAMP Capacitors

To ensure that the maximum gate-to-source voltage for the NMOS output transistors is not exceeded, two internal regulators clamp the gate voltage. Two 1-µF capacitors must be connected from VCLAMPL (pin 25) and VCLAMPR (pin 36) to ground and must be rated for at least 25 V. The voltages at the VCLAMP terminals vary with V_{CC} and may not be used for powering any other circuitry.

Internal Regulated 5-V Supply (AV_{DD})

The AV_{DD} terminal (pin 29) is the output of an internally-generated 5-V supply, used for the oscillator, preamplifier, and volume control circuitry. It requires a 1-µF capacitor, placed close to the pin, to keep the regulator stable.

This regulated voltage can be used to control GAIN0 and GAIN1 terminals, but should not be used to drive external circuitry.

Differential Input

The differential input stage of the amplifier cancels any noise that appears on both input lines of the channel. To use the TPA3005D2 with a differential source, connect the positive lead of the audio source to the INP input and the negative lead from the audio source to the INN input. To use the TPA3005D2 with a single-ended source, ac ground the INP or INN input through a capacitor equal in value to the input capacitor on INN or INP and apply the audio source to either input. In a single-ended input application, the unused input should be ac-grounded at the audio source instead of at the device input for best noise performance.

$\overline{\text{SHUTDOWN}}$ OPERATION

The TPA3005D2 employs a shutdown mode of operation designed to reduce supply current (I_{CC}) to the absolute minimum level during periods of nonuse for power conservation. The $\overline{\text{SHUTDOWN}}$ input terminal should be held high (see specification table for trip point) during normal operation when the amplifier is in use. Pulling $\overline{\text{SHUTDOWN}}$ low causes the outputs to mute and the amplifier to enter a low-current state. Never leave $\overline{\text{SHUTDOWN}}$ unconnected because amplifier operation would be unpredictable.

For the best power-off pop performance, place the amplifier in the shutdown mode prior to removing the power supply voltage.

USING LOW-ESR CAPACITORS

Low-ESR capacitors are recommended throughout this application section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

SHORT-CIRCUIT PROTECTION

The TPA3005D2 has short-circuit protection circuitry on the outputs that prevents damage to the device during output-to-output shorts, output-to-GND shorts, and output-to-V_{CC} shorts. When a short-circuit is detected on the outputs, the part immediately disables the output drive. This is a latched fault and must be reset by cycling the voltage on the $\overline{\text{SHUTDOWN}}$ pin to a logic low and back to the logic high state for normal operation. This clears the short-circuit flag and allow for normal operation if the short was removed. If the short was not removed, the protection circuitry again activates.

THERMAL PROTECTION

Thermal protection on the TPA3005D2 prevents damage to the device when the internal die temperature exceeds 150°C. There is a ±15 degree tolerance on this trip point from device to device. Once the die temperature exceeds the thermal set point, the device enters into the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 20°C. The device begins normal operation at this point with no external system interaction.

PRINTED-CIRCUIT BOARD (PCB) LAYOUT

Because the TPA3005D2 is a class-D amplifier that switches at a high frequency, the layout of the printed-circuit board (PCB) should be optimized according to the following guidelines for the best possible performance.

- Decoupling capacitors—The high-frequency 0.1-µF decoupling capacitors should be placed as close to the PVCC (pins 14, 15, 22, 23, 38, 39, 46, and 47) and AV_{CC} (pin 33) terminals as possible. The V2P5 (pin 4) capacitor, AV_{DD} (pin 29) capacitor, and VCLAMP (pins 25, 36) capacitor should also be placed as close to the device as possible. Large (10 µF or greater) bulk power supply decoupling capacitors should be placed near the TPA3005D2 on the PVCCL, PVCCR, and AV_{CC} terminals.
- Grounding—The AV_{CC} (pin 33) decoupling capacitor, AV_{DD} (pin 29) capacitor, V2P5 (pin 4) capacitor, COSC (pin 28) capacitor, and ROSC (pin 27) resistor should each be grounded to analog ground (AGND, pin 26 and pin 30). The PVCC decoupling capacitors should each be grounded to power ground (PGND, pins 18, 19, 42, and 43). Analog ground and power ground may be connected at the PowerPAD, which should be used as a central ground connection or star ground for the TPA3005D2. Basically, an island should be created with a single connection to PGND at the PowerPAD.
- Output filter—The ferrite EMI filter (Figure 19) should be placed as close to the output terminals as possible for the best EMI performance. The LC filter (Figure 18) should be placed close to the outputs. The capacitors used in both the ferrite and LC filters should be grounded to power ground. If both filters are used, the LC filter should be placed first, following the outputs.
- PowerPAD—The PowerPAD must be soldered to the PCB for proper thermal performance and optimal reliability. The dimensions of the PowerPAD thermal land should be 5 mm by 5 mm (197 mils by 197 mils). The PowerPAD size measures 4,55 x 4,55 mm. Four rows of solid vias (four vias per row, 0,3302 mm or 13 mils diameter) should be equally spaced underneath the thermal land. The vias should connect to a solid copper plane, either on an internal layer or on the bottom layer of the PCB. The vias must be solid vias, not thermal relief or webbed vias. For additional information, see the PowerPAD Thermally Enhanced Package application note, (SLMA002).

For an example layout, see the TPA3005D2 Evaluation Module (TPA3005D2EVM) User Manual, (SLOU165). Both the EVM user manual and the PowerPAD application note are available on the TI Web site at http://www.ti.com.

BASIC MEASUREMENT SYSTEM

This application note focuses on methods that use the basic equipment listed below:

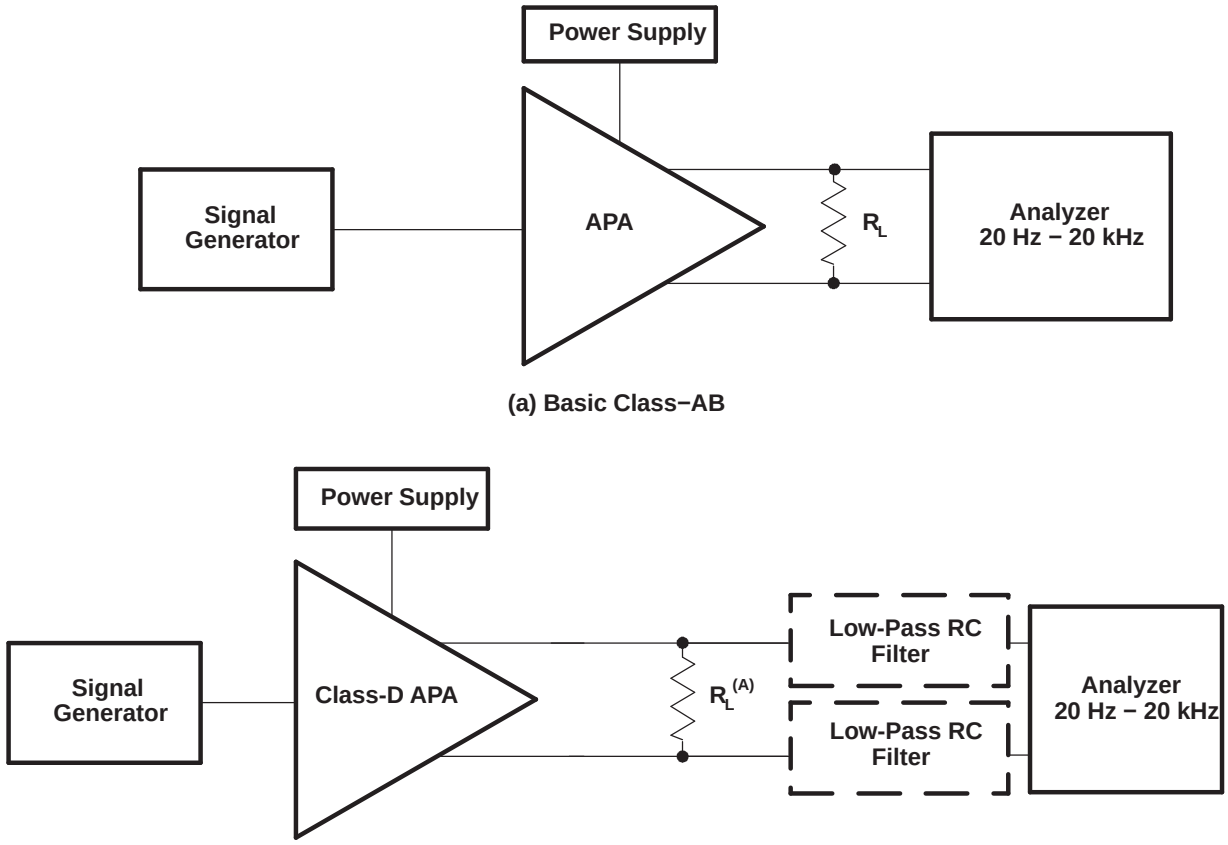
- Audio analyzer or spectrum analyzer
- Digital multimeter (DMM)
- Oscilloscope
- Twisted-pair wires
- Signal generator
- Power resistor(s)
- Linear regulated power supply
- Filter components
- EVM or other complete audio circuit

Figure 20 shows the block diagrams of basic measurement systems for class-AB and class-D amplifiers. A sine wave is normally used as the input signal because it consists of the fundamental frequency only (no other harmonics are present). An analyzer is then connected to the APA output to measure the voltage output. The analyzer must be capable of measuring the entire audio bandwidth. A regulated dc power supply is used to reduce the noise and distortion injected into the APA through the power pins. A System Two audio measurement system (AP-II) (Reference 1) by Audio Precision includes the signal generator and analyzer in one package.

The generator output and amplifier input must be ac-coupled. However, the EVMs already have the ac-coupling capacitors, (C_{IN}), so no additional coupling is required. The generator output impedance should be low to avoid attenuating the test signal, and is important because the input resistance of APAs is not high. Conversely, the analyzer-input impedance should be high. The output impedance, R_{OUT}, of the APA is normally in the hundreds of milliohms and can be ignored for all but the power-related calculations.

Figure 20(a) shows a class-AB amplifier system. They take an analog signal input and produce an analog signal output. These amplifier circuits can be directly connected to the AP-II or other analyzer input.

This is not true of the class-D amplifier system shown in Figure 20(b), which requires low-pass filters in most cases in order to measure the audio output waveforms. This is because it takes an analog input signal and converts it into a pulse-width modulated (PWM) output signal that is not accurately processed by some analyzers.



(A) For efficiency measurements with filter-free class-D, R_L should be an inductive load like a speaker.

Figure 20. Audio Measurement Systems

The TPA3005D2 uses a modulation scheme that does not require an output filter for operation, but they do sometimes require an RC low-pass filter when making measurements. This is because some analyzer inputs cannot accurately process the rapidly changing square-wave output and therefore record an extremely high level of distortion. The RC low-pass measurement filter is used to remove the modulated waveforms so the analyzer can measure the output sine wave.

DIFFERENTIAL INPUT AND BTL OUTPUT

All of the class-D APAs and many class-AB APAs have differential inputs and bridge-tied load (BTL) outputs. Differential inputs have two input pins per channel and amplify the difference in voltage between the pins. Differential inputs reduce the common-mode noise and distortion of the input circuit. BTL is a term commonly used in audio to describe differential outputs. BTL outputs have two output pins providing voltages that are 180 degrees out of phase. The load is connected between these pins. This has the added benefits of quadrupling the output power to the load and eliminating a dc blocking capacitor.

A block diagram of the measurement circuit is shown in Figure 21. The differential input is a balanced input, meaning the positive (+) and negative (-) pins have the same impedance to ground. Similarly, the BTL output equates to a balanced output.

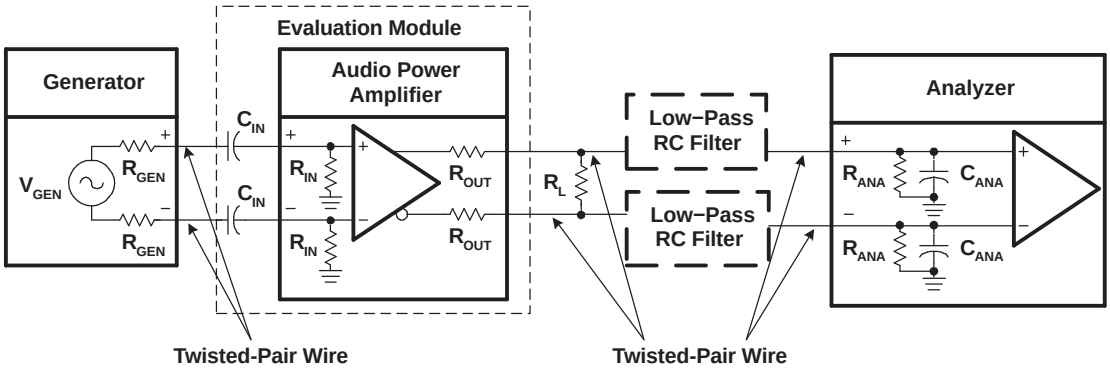


Figure 21. Differential Input, BTL Output Measurement Circuit

The generator should have balanced outputs and the signal should be balanced for best results. An unbalanced output can be used, but it may create a ground loop that affects the measurement accuracy. The analyzer must also have balanced inputs for the system to be fully balanced, thereby cancelling out any common mode noise in the circuit and providing the most accurate measurement.

The following general rules should be followed when connecting to APAs with differential inputs and BTL outputs:

- Use a balanced source to supply the input signal.
- Use an analyzer with balanced inputs.
- Use twisted-pair wire for all connections.
- Use shielding when the system environment is noisy.
- Ensure that the cables from the power supply to the APA, and from the APA to the load, can handle the large currents (see Table 3).

Table 3 shows the recommended wire size for the power supply and load cables of the APA system. The real concern is the dc or ac power loss that occurs as the current flows through the cable. These recommendations are based on 12-inch long wire with a 20-kHz sine-wave signal at 25°C.

Table 3. Recommended Minimum Wire Size for Power Cables

P_{OUT} (W)	R_L(Ω)	AWG Size		DC POWER LOSS (MW)		AC POWER LOSS (MW)	
10	4	18	22	16	40	18	42
2	4	18	22	3.2	8	3.7	8.5
1	8	22	28	2	8	2.1	8.1
< 0.75	8	22	28	1.5	6.1	1.6	6.2

CLASS-D RC LOW-PASS FILTER

An RC filter is used to reduce the square-wave output when the analyzer inputs cannot process the pulse-width modulated class-D output waveform. This filter has little effect on the measurement accuracy because the cutoff frequency is set above the audio band. The high frequency of the square wave has negligible impact on measurement accuracy because it is well above the audible frequency range, and the speaker cone cannot respond at such a fast rate. The RC filter is not required when an LC low-pass filter is used, such as with the class-D APAs that employ the traditional modulation scheme (TPA032D0x, TPA005Dxx).

The component values of the RC filter are selected using the equivalent output circuit as shown in Figure 22. R_L is the load impedance that the APA is driving for the test. The analyzer input impedance specifications should be available and substituted for R_{ANA} and C_{ANA}. The filter components, R_{FILT} and C_{FILT}, can then be derived for the system. The filter should be grounded to the APA near the output ground pins or at the power supply ground pin to minimize ground loops.

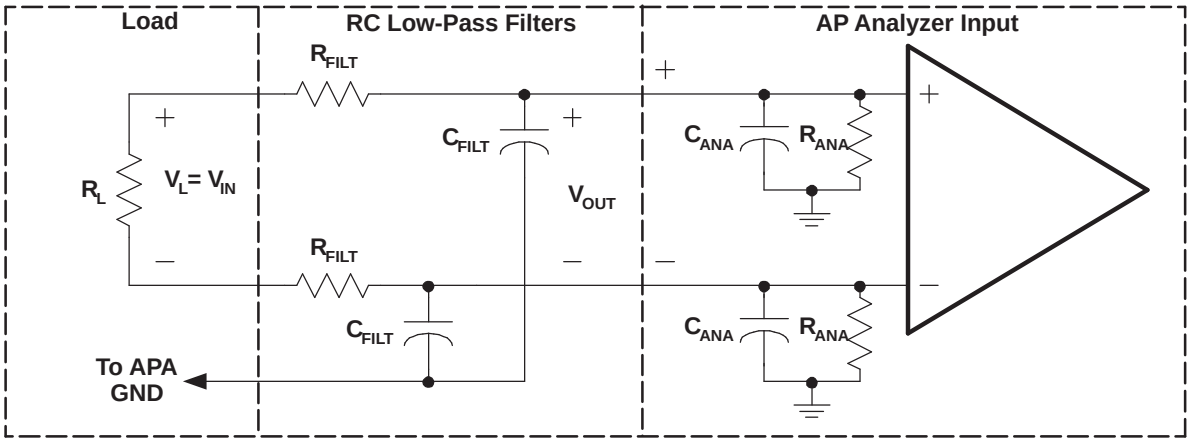


Figure 22. Measurement Low-Pass Filter Derivation Circuit-Class-D APAs

The transfer function for this circuit is shown in Equation 8 where $\omega_O = R_{EQ}C_{EQ}$, $R_{EQ} = R_{FILT} \parallel R_{ANA}$ and $C_{EQ} = (C_{FILT} + C_{ANA})$. The filter frequency should be set above f_{MAX}, the highest frequency of the measurement bandwidth, to avoid attenuating the audio signal. Equation 9 provides this cutoff frequency, f_C. The value of R_{FILT} must be chosen large enough to minimize current that is shunted from the load, yet small enough to minimize the attenuation of the analyzer-input voltage through the voltage divider formed by R_{FILT} and R_{ANA}. A rule of thumb is that R_{FILT} should be small (~100 Ω) for most measurements. This reduces the measurement error to less than 1% for $R_{ANA} \geq 10$ kΩ.

$$\left(\frac{V_{OUT}}{V_{IN}}\right) = \frac{\left(\frac{R_{ANA}}{R_{ANA}+R_{FILT}}\right)}{1 + j\left(\frac{\omega}{\omega_O}\right)} \tag{8}$$

$$f_C = \sqrt{2} \times f_{MAX} \tag{9}$$

An exception occurs with the efficiency measurements, where R_{FILT} must be increased by a factor of ten to reduce the current shunted through the filter. C_{FILT} must be decreased by a factor of ten to maintain the same cutoff frequency. See Table 4 for the recommended filter component values.

Once f_C is determined and R_{FILT} is selected, the filter capacitance is calculated using Equation 9. When the calculated value is not available, it is better to choose a smaller capacitance value to keep f_C above the minimum desired value calculated in Equation 10.

$$C_{FILT} = \frac{1}{2\pi \times f_C \times R_{FILT}} \tag{10}$$

Table 4 shows recommended values of R_{FILT} and C_{FILT} based on common component values. The value of f_C was originally calculated to be 28 kHz for an f_{MAX} of 20 kHz. C_{FILT}, however, was calculated to be 57,000 pF, but the nearest values of 56,000 pF and 51,000 pF were not available. A 47,000-pF capacitor was used instead, and f_C is 34 kHz, which is above the desired value of 28 kHz.

Table 4. Typical RC Measurement Filter Values

MEASUREMENT	R_{FILT}	C_{FILT}
Efficiency	1000 Ω	5,600 pF
All other measurements	100 Ω	56,000 pF

REVISION HISTORY

Changes from Original (May 2004) to Revision A	Page
• Replaced the DISSIPATION RATING TABLE with the Thermal Inforamtion Table	2

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPA3005D2PHP	Active	Production	HTQFP (PHP) | 48	250 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3005D2
TPA3005D2PHP.A	Active	Production	HTQFP (PHP) | 48	250 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3005D2
TPA3005D2PHPR	Active	Production	HTQFP (PHP) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3005D2
TPA3005D2PHPR.A	Active	Production	HTQFP (PHP) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3005D2
TPA3005D2PHPRG4	Active	Production	HTQFP (PHP) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3005D2

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

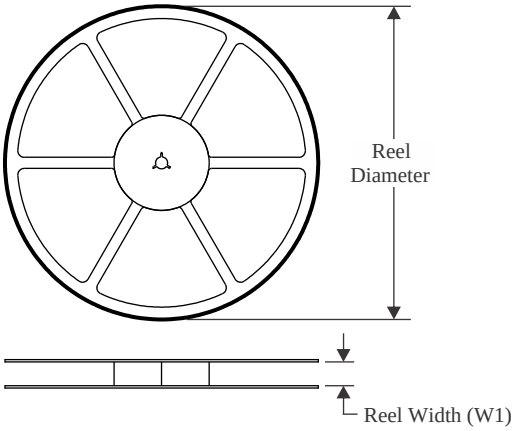
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

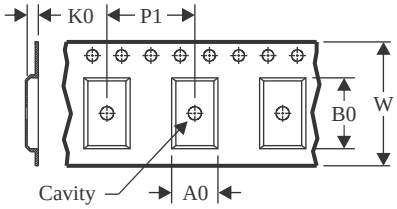
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

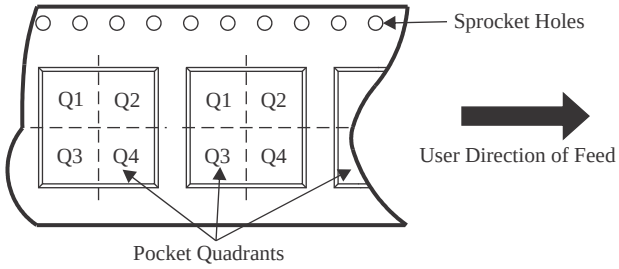


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

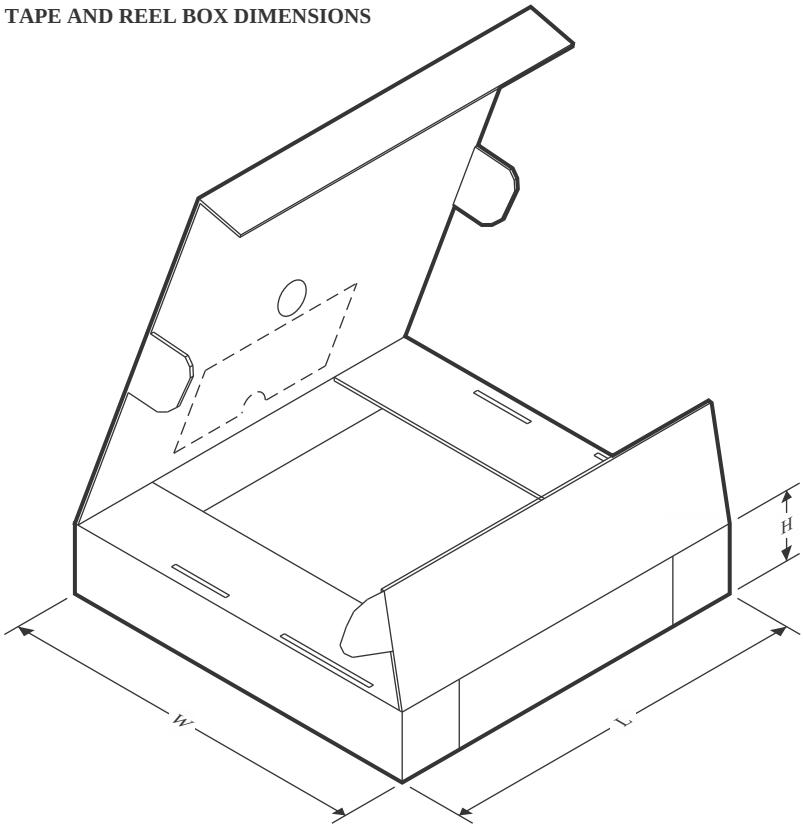
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA3005D2PHPR	HTQFP	PHP	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2

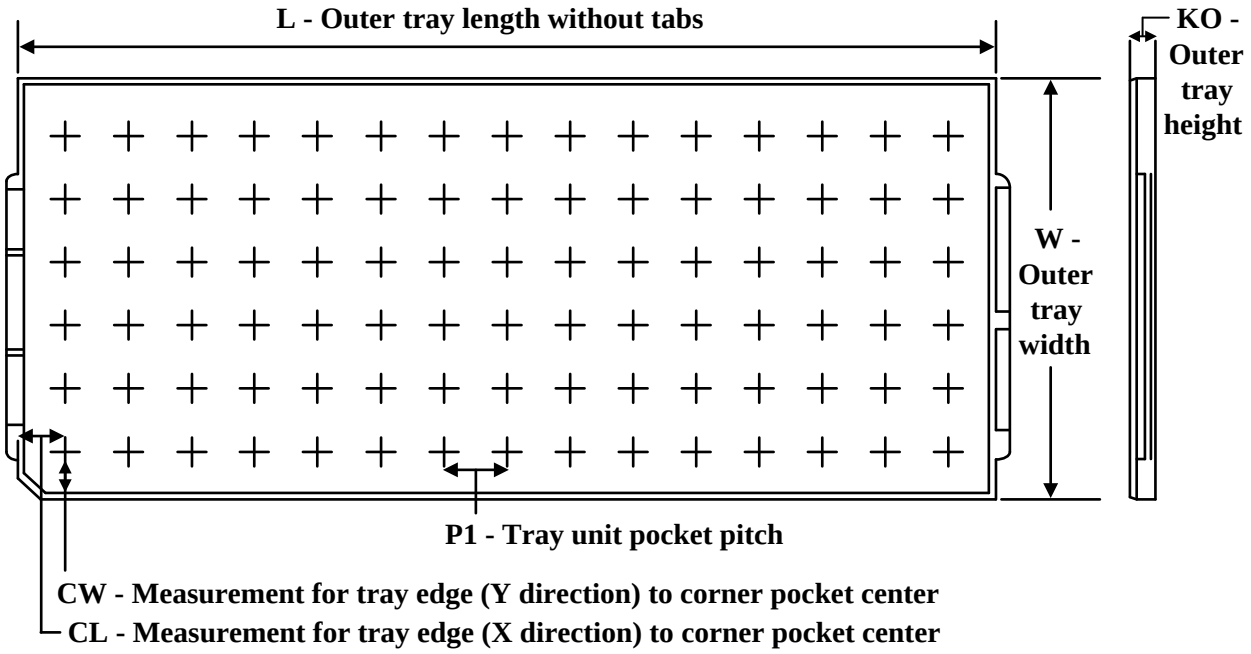
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA3005D2PHPR	HTQFP	PHP	48	1000	350.0	350.0	43.0

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
TPA3005D2PHP	PHP	HTQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
TPA3005D2PHP.A	PHP	HTQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25

GENERIC PACKAGE VIEW

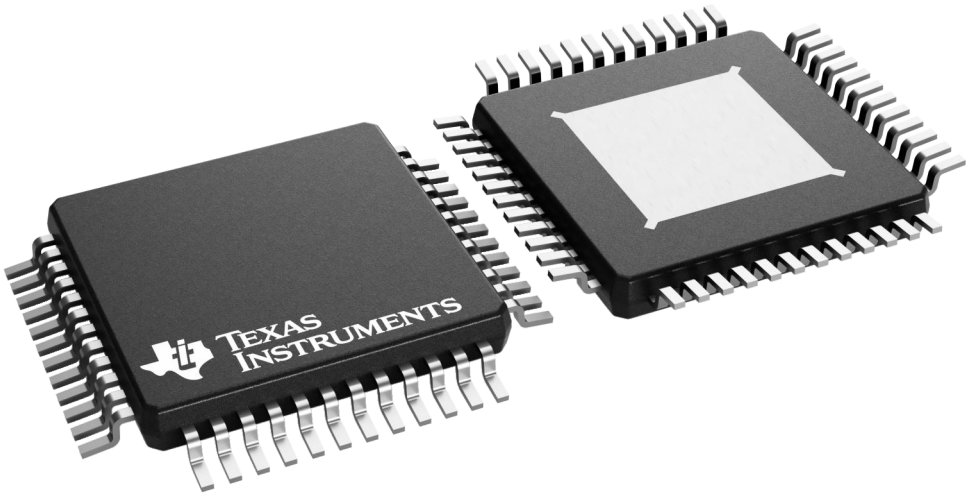
PHP 48

TQFP - 1.2 mm max height

7 x 7, 0.5 mm pitch

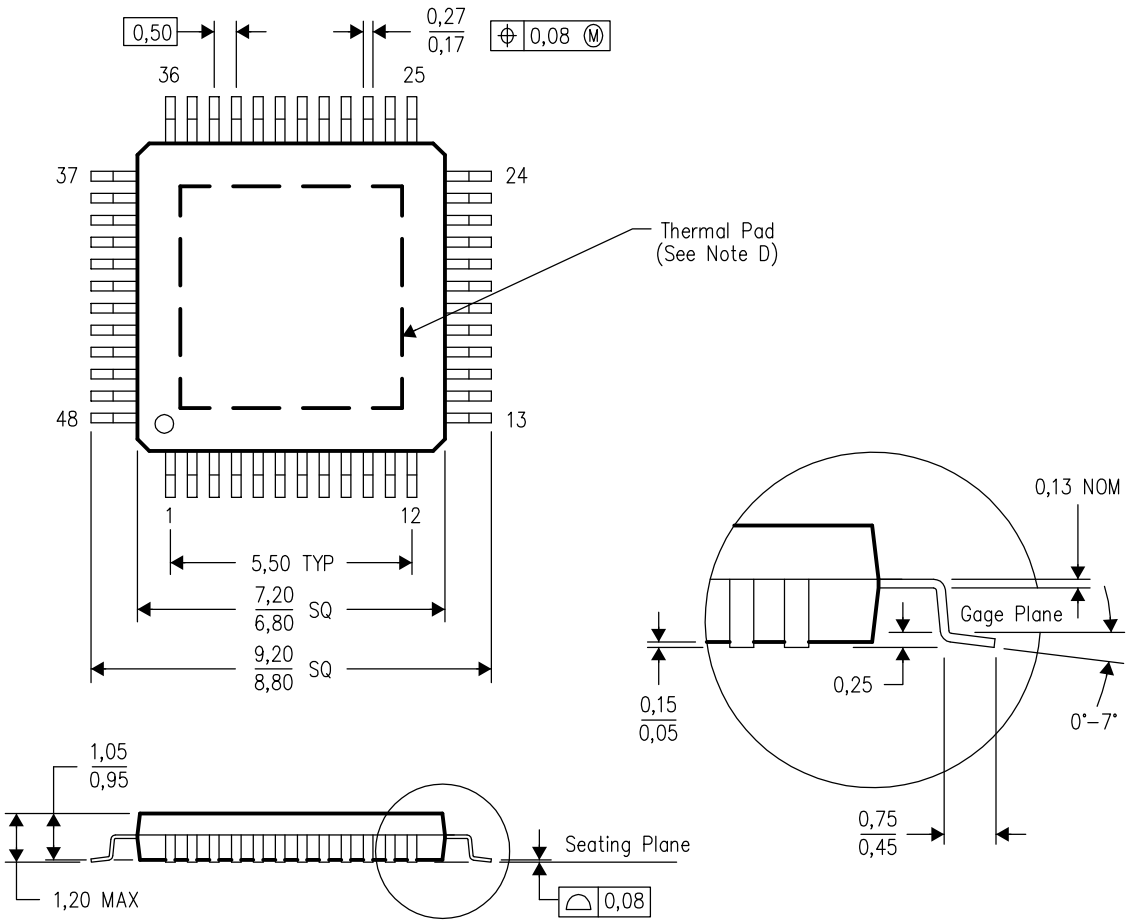
QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4226443/A

PHP (S–PQFP–G48) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

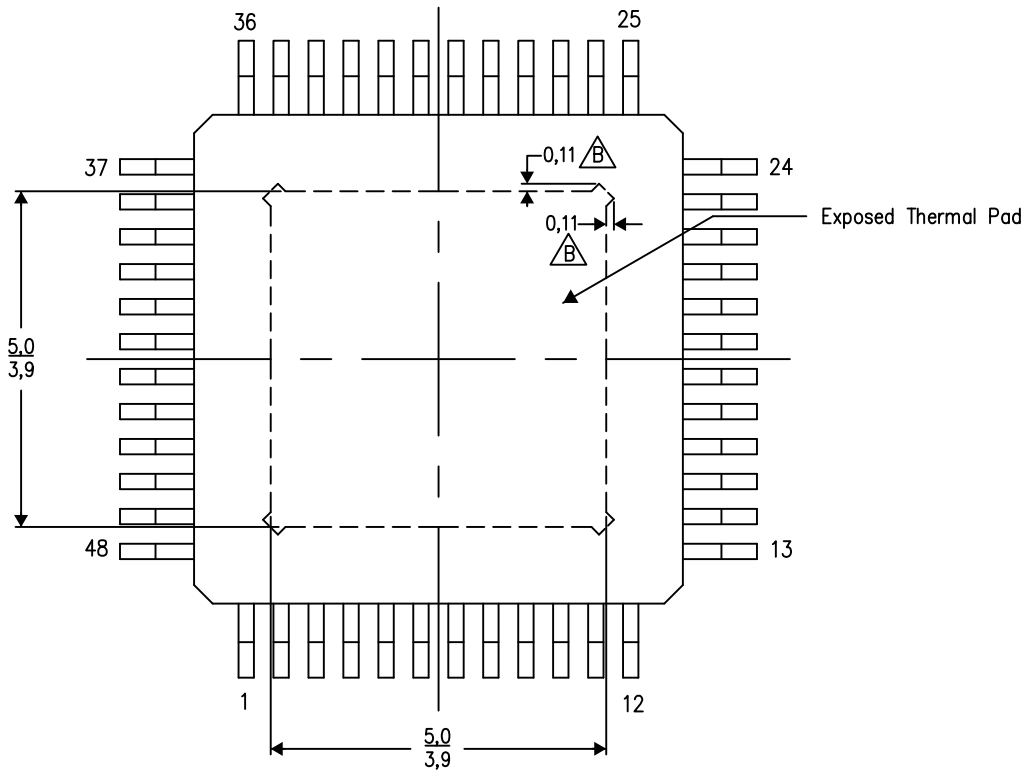
PHP (S–PQFP–G48) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

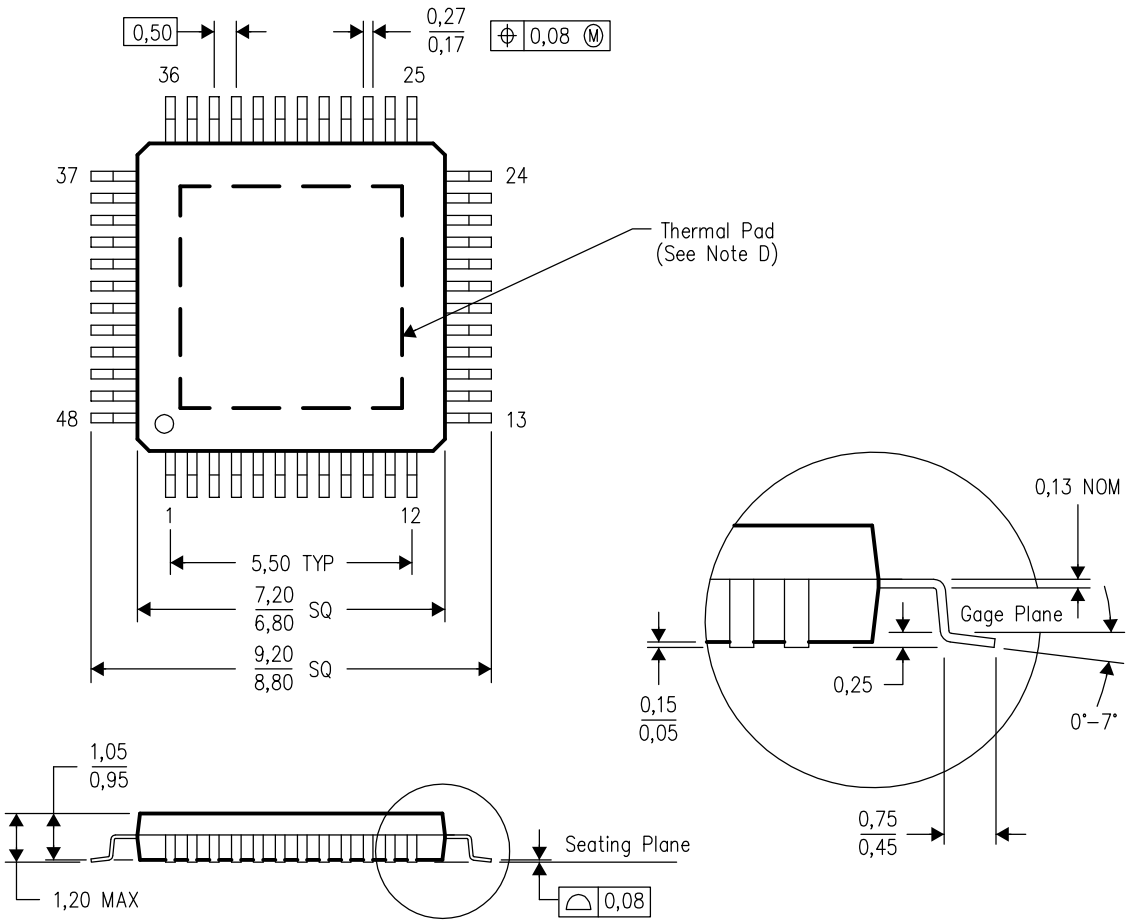
4206329–17/P 03/15

NOTE: A. All linear dimensions are in millimeters

B Tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PHP (S–PQFP–G48) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
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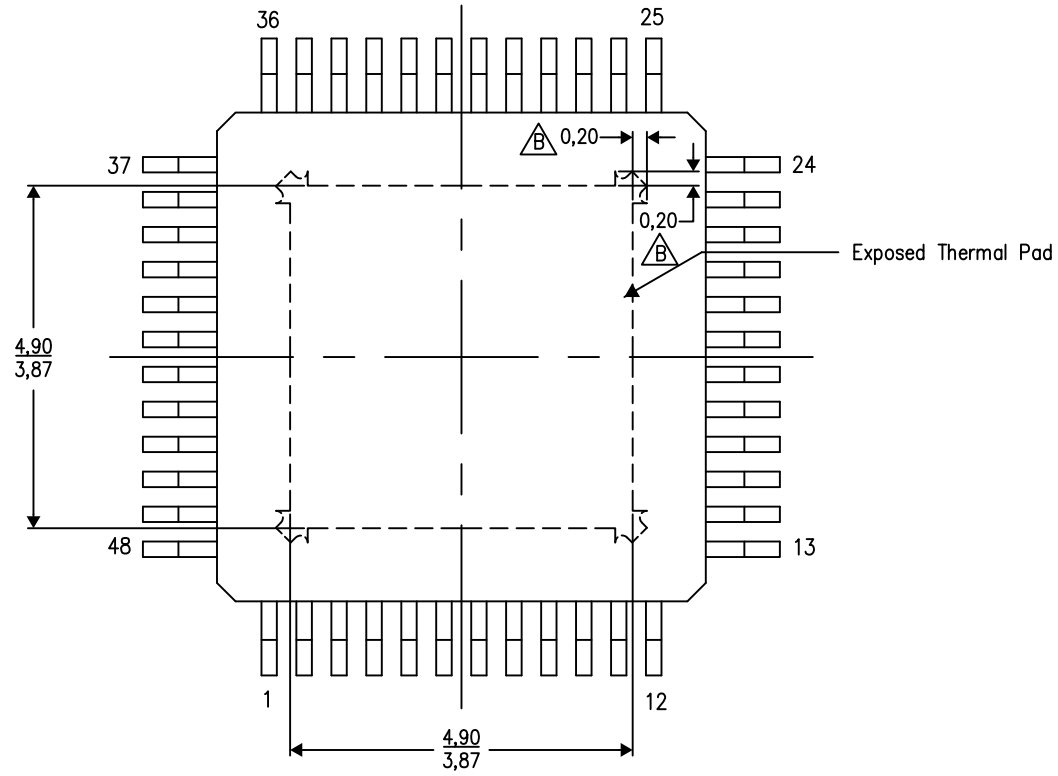
The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

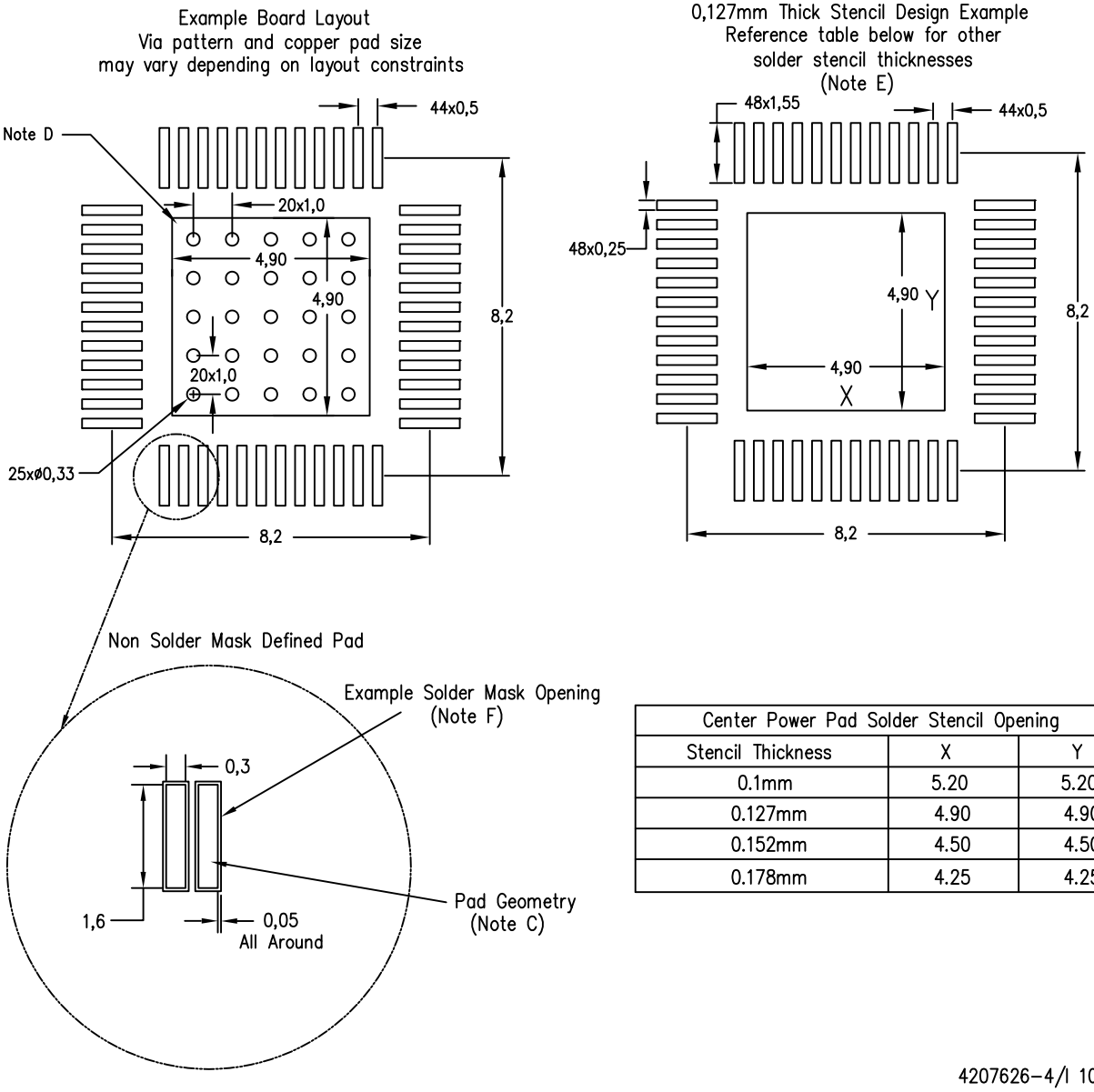
4206329–4/P 03/15

NOTE: A. All linear dimensions are in millimeters

B Tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PHP (S–PQFP–G48) PowerPAD™ PLASTIC QUAD FLATPACK



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	5.20	5.20
0.127mm	4.90	4.90
0.152mm	4.50	4.50
0.178mm	4.25	4.25

4207626–4/I 10/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting options for vias placed in the thermal pad.

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