

## 3.3V TO 18V MUX with Overcurrent Limit

Check for Samples: TPS22980

## **FEATURES**

- Powered From 3.3V
- 4.5V to 19.8V High Voltage Switch
- 3V to 3.6V Switch
- Adjustable Current Limit
- Thermal Shutdown
- Make Before Break Switch
- High Voltage Discharge Before Low Voltage Make
- Reverse Current Blocking

### **APPLICATIONS**

- Notebook Computers
- Desktop Computers
- Power Management Systems

## **DESCRIPTION**

The TPS22980 is a current-limited power mux providing a connection to a peripheral device from either a low voltage supply (3.0V up to 3.6V) or a high voltage supply (5V up to 18V). The desired output is selected by digital control signals.

The high voltage (VHV) and low voltage (V3P3) switch current limits are set with external resistance. Once the current limit is reached, the TPS22980 will control the switch to maintain the current at the limit.

When the high voltage supply is not present, the TPS22980 will maintain the connection to the output from the low voltage supply. When a high voltage line and high voltage enable signal is detected by the device, the high voltage switch will be turned on in conjunction with the low voltage switch until a reverse current is detected by the low voltage switch. The low voltage switch is then disabled allowing a seamless transition from a low voltage to a high voltage supply with minimal drop and shoot-through current.

To prevent current backflow during a transition from a VHV connection to a V3P3 connection, the TPS22980 will break the VHV connection and discharge the output to approximately 3.3V. Once the output reaches 3.3V the device will connect V3P3 switch. If a load is present, the output will transition to 0V before returning to 3.3V.

The TPS22980 is available in a 4mm x 4mm x 1mm QFN package.

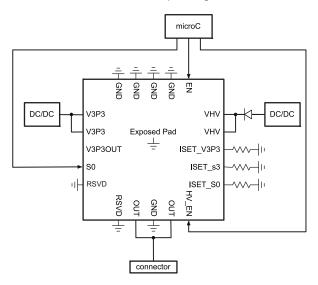


Figure 1. Typical Application

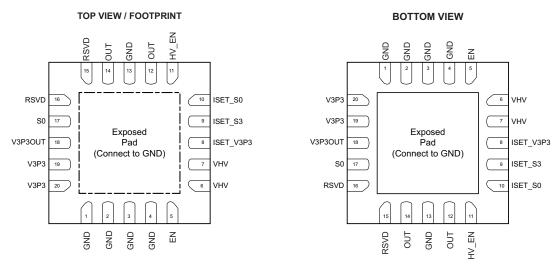


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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



Package Size: 4mm x 4mm x 1mm height, Pad Pitch: 0.5mm

## **PIN FUNCTIONS**

	PIN	PERCENTION						
NO. NAME		DESCRIPTION						
1								
2	GND	Davideo manual						
3	GND	Device ground						
4								
5	EN	Device Enable.						
6	VHV	High voltage newer gunnly input. Place a minimum of 0.1 uE conscitut as class to this nin as possible						
7	VHV	High voltage power supply input. Place a minimum of 0.1µF capacitor as close to this pin as possible.						
8	ISET_V3P3	Sets the current limit for V3P3. Place resistor between this pin and GND. See Equation 1 to calculate resistor value.						
9	ISET_S3	Sets the current limit for VHV in S3 mode. Place resistor between this pin and GND. See Equation 1 to calculate resistor value.						
10	ISET_S0	Sets the current limit for VHV in S0 mode. Place resistor between this pin and GND. See Equation 1 to calculate resistor value.						
11	HV_EN	High voltage output enable.						
12, 14	OUT	Power output. Place a minimum of 1µF capacitor as close to this pin as possible.						
13	GND	Device ground.						
15	D0) (D	Decreed Mark Tarks OND						
16	RSVD	Reserved. Must Tie to GND.						
17	S0	When this pin is asserted, the device is put in S0 mode. Otherwise the device operates in S3 mode.						
18	V3P3OUT	3.3V bypass output. Place a minimum of 0.1µF capacitor as close to this pin as possible.						
19	V3P3	2.2\/ power gupply input. Place a minimum of 0.1\(\text{UE}\) consolitor as along to this pin as possible						
20	vsPs	3.3V power supply input. Place a minimum of 0.1µF capacitor as close to this pin as possible.						
EP	GND							

Product Folder Links : TPS22980

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### ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1) (2)

		VALUE	UNIT
	Input voltage range on V3P3 (VDD) <sup>(3)</sup>	-0.3 to 3.6	
	Input voltage range on EN, HVEN, ISET_V3P3, ISET_S0, ISET_S3, S0 (3)	-0.3 to V3P3+0.3	·
VI	Input voltage range on VHV <sup>(3)</sup>	-0.3 to 20	V
	Output voltage range at OUT <sup>(3)</sup>	-0.3 to 20	
	Output voltage range at V3P3OUT <sup>(3)</sup>	-0.3 to V3P3+0.3	
T <sub>A</sub>	Operating ambient temperature range	-40 to 85	°C
T <sub>J (MAX)</sub>	Maximum operating junction temperature	110	°C
T <sub>stg</sub>	Storage temperature range	-65 to 150	°C
ECD Dating	Charge Device Model (JESD 22 C101)	500	V
ESD Rating	Human Body Model (JESD 22 A114)	2	kV

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be de-rated. Maximum ambient temperature [T<sub>A(max)</sub>] is dependent on the maximum operating junction temperature [T<sub>J(max)</sub>], the maximum power dissipation of the device in the application [P<sub>D(max)</sub>], and the junction-to-ambient thermal resistance of the part/package in the application (θ<sub>JA</sub>), as given by the following equation: T<sub>A(max)</sub> = T<sub>J(max)</sub> – (θ<sub>JA</sub> × P<sub>D(max)</sub>)
   All voltage values are with respect to network ground terminal.

#### THERMAL INFORMATION

		TPS22980	
	THERMAL METRIC <sup>(1)</sup>	RGP	UNITS
		16 PINS	
$\theta_{JA}$	Junction-to-ambient thermal resistance	38.9	
$\theta_{JCtop}$	Junction-to-case (top) thermal resistance	30.7	
$\theta_{JB}$	Junction-to-board thermal resistance	11.5	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	0.4	*C/VV
ΨЈВ	Junction-to-board characterization parameter	11.4	
$\theta_{JCbot}$	Junction-to-case (bottom) thermal resistance	2.2	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.



## RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
$V_{3P3}$	Supply voltage re	3.0	3.6	V	
$V_{HV}$	Supply voltage range		4.5	19.8	V
I <sub>LIM3P3OUT</sub>	V3P3OUT Switch	V3P3OUT Switch current range			
V <sub>IH</sub>	Input logic high	EN, HV_EN, S0	V3P3-0.6	V3P3	V
$V_{IL}$	Input logic low	EN, HV_EN, S0	0	0.6	V
R <sub>SET_V3P3</sub>	3.3V switch curre	3.3V switch current limit set resistance			
R <sub>SET_S0</sub>	VHV switch curre	25.3	402	kΩ	
RS <sub>ET_S3</sub>	VHV switch curre	nt limit in S3 mode set resistance	25.3	402	kΩ

## **ELECTRICAL CHARACTERISTICS**

Unless otherwise noted the specification applies over the  $V_{DD}$  range and operating junction temp  $-40^{\circ}\text{C} \leq T_{J} \leq 85^{\circ}\text{C}$ . Typical values are for  $V_{3P3} = 3.3\text{V}$ ,  $V_{HV} = 15\text{V}$ , and  $T_{J} = 25^{\circ}\text{C}$ .

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SI	JPPLIES AND CURRENTS					
V <sub>3P3</sub>	V3P3 Input voltage range		3	3.3	3.6	V
V <sub>HV</sub>	VHV Input voltage range		4.5		19.8	V
I <sub>VHVACT</sub>	Active quiescent current from VHV	HV_EN = 1, EN = 1			150	μA
I <sub>VHVSD</sub>	Shutdown leakage current from VHV	HV_EN = 0, EN = 0 or 1			30	μA
I <sub>DDACT</sub>	Active quiescent current from V3P3	EN = 1, HV_EN = 0			200	μA
I <sub>DDACTHV</sub>	Active quiescent current from V3P3	EN = 1, HV_EN = 1			150	μA
I <sub>DDSD</sub>	Shutdown Quiescent Current from V3P3	EN = 0, OUT = 0V			10	μA
I <sub>DIS</sub>	OUT Discharge Current	$EN = 1, V_{HV} = 5V$ HV_EN = 1 \to 0	5		10	mA
	LIV EN EN OO OO leest vie leeke ve	V = 0 V			1	μA
I <sub>IN</sub>	HV_EN, EN, S0, S3 Input pin leakage	V = V3P3			1	μΑ
SWITCH A	ND RESISTANCE CHARACTERISTICS					
R <sub>SHV</sub>	VHV Switch resistance	V <sub>HV</sub> = 5 V to 18V, I <sub>VHV</sub> = 1.5 A			250	mΩ
R <sub>S3P3</sub>	V3P3 Switch resistance	V <sub>3P3</sub> = 3.3 V, I <sub>V3P3</sub> = 1.5 A			250	mΩ
R <sub>S3P3BYP</sub>	V3P3 Bypass switch resistance	V <sub>3P3</sub> = 3.3 V, I <sub>V3P3</sub> = 500 mA			500	mΩ
R <sub>OUTDIS</sub>	OUT Pulldown resistance when disabled	EN = 0	1.5	2.5	4	kΩ
VOLTAGE	THESHOLDS	•			•	
1.7	VIIVIII dan valla va la al aut	VHV Input Falling	3.6	4		
$V_{HVUVLO}$	VHV Under voltage lockout	VHV Input Rising		4	4.3	V
	VoDe II I I I I	V3P3 Input Falling	1.8	2.25		.,
V <sub>3P3UVLO</sub>	V3P3 Under voltage lockout	V3P3 Input Rising		2.25	2.5	V
THERMAL	SHUTDOWN					
T <sub>SD</sub>	Shutdown Temperature		110	120	130	°C
T <sub>SDHYST</sub>	Shutdown Hysteresis			10		°C

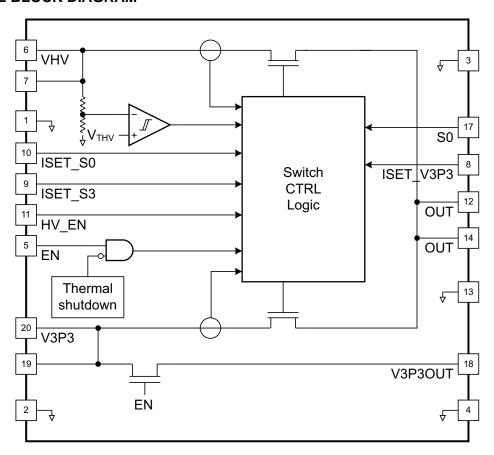


## **ELECTRICAL CHARACTERISTICS (continued)**

Unless otherwise noted the specification applies over the  $V_{DD}$  range and operating junction temp  $-40^{\circ}\text{C} \leq T_{J} \leq 85^{\circ}\text{C}$ . Typical values are for  $V_{3P3} = 3.3\text{V}$ ,  $V_{HV} = 15\text{V}$ , and  $T_{J} = 25^{\circ}\text{C}$ .

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$						
		$R_{SET\_S0, 3} = 402 \text{ k}\Omega$	100	110	150	
I <sub>LIMHV</sub>	VHV Switch current limit state S0 or S3	$R_{SET\_S0, 3} = 80.6 \text{ k}\Omega$	495	525	555	mA
		$R_{SET\_S0, 3} = 26.7 \text{ k}\Omega$	1515	1575	1635	
		$R_{SET_V3P3} = 402 \text{ k}\Omega$	100	110	150	
I <sub>LIM3P3</sub>	V3P3 Switch current limit	$R_{SET_V3P3} = 80.6 \text{ k}\Omega$	495	525	555	mA
		$R_{SET\_V3P3} = 26.7 \text{ k}\Omega$	1515	1575	1635	
I <sub>REV3P3</sub>	V3P3 Switch Reverse Current Limit		10	27	45	mA
T <sub>V3P3RC</sub>	•	$V_{OUT} = V_{3P3} \rightarrow V_{3P3} + 20mV$			100	μS
T <sub>VHVSC</sub>	VHV Switch short circuit response time	C <sub>OUT</sub> = 20 pF		8		μs
T <sub>V3P3SC</sub>	V3P3 Switch short circuit response time	C <sub>OUT</sub> = 20 pF		8		μs
TRANSITIO	ON DELAYS					
T <sub>3P3OFF</sub>	VHV to V3P3 off time	$C_{OUT} = 1.1 \mu F$ , EN = 1, HV_EN = 1 $\rightarrow$ 0			6	ms
T <sub>0-3.3V</sub>	0V to 3.3V ramp time	C <sub>OUT</sub> ≤ 20 pF			6	ms
T <sub>3.3V-VHV</sub>	3.3V to VHV ramp time	C <sub>OUT</sub> ≤ 20 pF			6	ms
T <sub>VHV-3.3V</sub>	VHV to 3.3V ramp time	C <sub>OUT</sub> ≤ 20 pF			23	ms
T <sub>LIM</sub>	Overcurrent response time	C <sub>OUT</sub> ≤ 20 pF			0.5	ms

## **FUNCTIONAL BLOCK DIAGRAM**



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#### **APPLICATION INFORMATION**

#### **CURRENT LIMIT**

The TPS22980 provides current limiting in the power switches. Both the VHV supply current limit and the V3P3 supply current limit are adjustable by external resistors.

Figure 2 shows a simplified view of the TPS22980 current limit function. Both the VHV supply current limit and the V3P3 supply current limit are adjustable by external resistors.

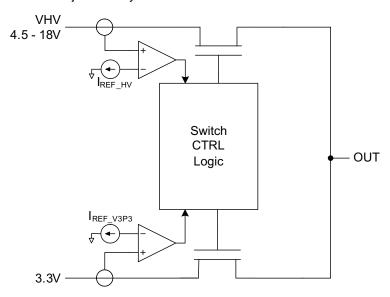


Figure 2. Simplified Current Limit Diagram

The current limit thresholds,  $I_{REF\_HV}$  and  $I_{REF\_V3P3}$ , are set with three external resistors as shown in Figure 3. When the TPS22980 is passes the V3P3 voltage, the current limit is set by  $R_{ISET\_V3P3}$ . The VHV path has two modes that support two different current limits which are selected by the S0 pin. When S0 is asserted high,  $R_{ISET\_S0}$  sets the current limit. When S0 is low,  $R_{ISET\_S3}$  sets the current limit. This allows the system to have two separate VHV current limits for different modes such as active and sleep.

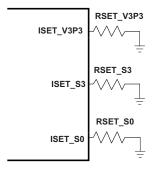
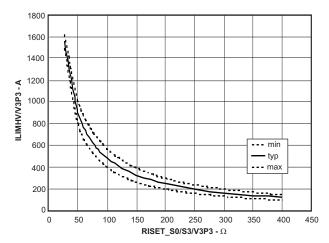


Figure 3. External R<sub>SET</sub> Resistances to Set Current Limits

## **CURRENT LIMIT THRESHOLD**





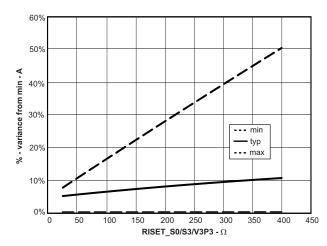


Figure 4. I<sub>LIM</sub> vs R<sub>SET</sub> for VHV and V3P3

Figure 5. Percent Variance from min I<sub>LIM</sub> vs R<sub>SET</sub>

Figure 4 shows the minimum, typical, and maximum current limit for either supply versus its corresponding  $R_{\text{ISET}}$  value. Equation 1 is used to determine the  $R_{\text{ISET}}$  needed to set a minimum ILIM for a given supply and mode. Figure 5 shows the approximate variation from the set minimum  $I_{\text{LIM}}$  value to the typical and maximum  $I_{\text{LIM}}$  values.

$$RISET = \frac{40 \text{ k}\Omega \times Amps}{ILIMmin}$$
 (1)

where:

 $R_{ISET}$  = external resistor used to set the current limit for V3P3, VHV (S0), or VHV (S3), and  $I_{LIMmin}$  = current limit for V3P3, VHV (S0), or VHV (S3) set by the external  $R_{ISET}$  resistor.

Each resistor is placed between the corresponding ISET pin and GND, as shown in Figure 3, providing a minimum current limit between 100mA and 1.5A.

#### TRANSITION DELAYS

Output transitions of the TPS22980 voltages are shown in Figure 6. When the device transitions from VHV to V3P3 at the output, the power switches both turn off until the output falls to near the V3P3 voltage. During this time, a discharge current (IDIS) pulls OUT down. If a load on the line is also pulling OUT down, the output can drop to 0V due to the switch off time of T3P3OFF. Figure 7 shows the voltage drop on the output during this transition with no output capacitance.



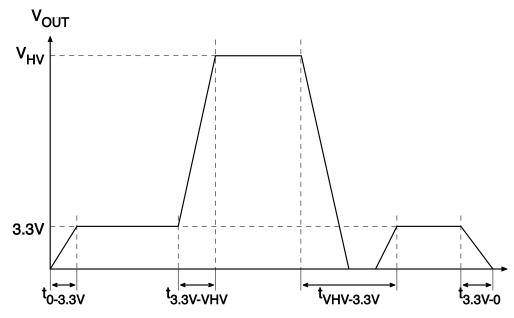


Figure 6. Allowable Voltage Transitions

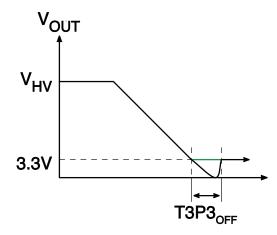


Figure 7. Voltage Drop During Transitions from VHV

## **DIGITAL CONTROL SIGNALS**

The voltage at OUT is controlled by two digital logic input signals, EN and HV\_EN. HV\_EN controls the state of the VHV switch and EN controls the state of V3P3 switch. Table 1 lists the possible output states given the conditions of the digital logic signals. State PD indicates a pulldown resistance of R<sub>OUTDIS</sub> to GND.

Table 1. Output State of OUT Given the States EN and HV\_EN

EN	HV_EN	OUT
0	0	PD
0	1	PD
1	0	V3P3
1	1	VHV

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Figure 8 shows possible combinations of EN and HV\_EN controlling OUT of the TPS22980.

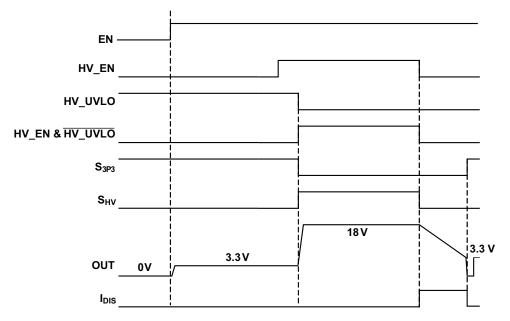


Figure 8. Logic Waveforms Displaying the Transition Between VHV and V3P3

## **OVER-CURRENT LIMIT AND SHORT CIRCUIT PROTECTION**

When the load at OUT attempts to draw more current than the limit set by the external RISET resistors for the V3P3 switch and VHV switch (for both S0 and S3 modes), the device will operate in a constant current mode while lowering the output voltage. Figure 9 shows the delay, t<sub>LIM</sub>, which occurs when an over-current fault is detected until the output current is lowered to ILIMHV tolerances for VHV or ILIM3V3 tolerances for V3P3 as shown in Figure 4.

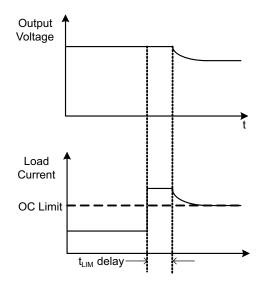


Figure 9. Overcurrent Output Response

All short circuit conditions are treated as over-current conditions. In the event of a short circuit, the device will limit the output current to the corresponding  $R_{\text{SET}}$  value and continue to do so until thermal shutdown is encountered or the short circuit condition is removed.



#### **Reverse Current Protection**

Reverse current protection for the V3P3 supply to OUT triggers at I<sub>REV3P3</sub> causing the V3P3 supply switch to open. When the HV\_EN signal is not asserted and reverse current protection is triggered, a discharge current source is turned on to bring the output voltage to 3.3V nominal.

#### **Thermal Shutdown**

The device enters thermal shutdown when junction temperature reaches T<sub>SD</sub>. The device will resume the previous state on power up once the junction temperature has dropped by 10°C. Connect thermal vias to the exposed GND pad underneath the device package for improved thermal diffusion.

#### **UVLO**

When the VHV rail reaches the under-voltage lockout threshold of  $V_{HVUVLO}$  while HV\_EN is high, the device will switch back to V3P3. Once the UVLO condition has cleared, the device will switch to VHV again. When the V3P3 rail reaches the under-voltage lockout threshold of  $V_{3P3UVLO}$ , regardless of the states of any digital logic controls, the device will open all switches and enter a reset condition.

## **Input Inductive Bounce at Short Circuit**

When the TPS22980 is operating at high currents and high input voltage on VHV, a short circuit condition can cause the input to exceed the maximum safe operating condition for VHV. When a significant inductance is present at the VHV input, sudden turn off of current through the device may produce a large enough inductive voltage bounce that exceeds the maximum safe operating condition and may damage the TPS22980. To prevent this, reduce any inductance at the input. Input capacitors, such as 4.7µF, can reduce the supply bounce and are recommended.

## **Single Point Failure Protection**

The TPS22980 current limits are set by the RISET resistances. Shorting one of these resistance would result in a single point failure that removes the current limiter for that particular input and mode. Without current limiting, an excessive current load may damage the TPS22980 and the system. To prevent a single point failure from occurring, the RISET resistances can be divided into two series resistances each as shown in Figure 10. Failure of a single resistance will not result in runaway current and damage.

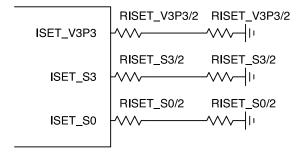


Figure 10. R<sub>ISET</sub> Division to Prevent Single Point Failure

Product Folder Links : TPS22980

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## **REVISION HISTORY**

Changes from Original (December 2011) to Revision A	Page
Changed Typical Application figure.	1
Added bottom view pin out information.	2
Updated Pin Functions Table	
<ul> <li>Added reverse current and thermal shutdown parameters to the ELECTRICAL CHARACTERISTICS table</li> </ul>	4
Updated the APPLICATION INFORMATION section.	6
Changes from Revision A (February 2012) to Revision B	Page
Changed bottom view pin out information.	2
Changes from Revision B (April 2012) to Revision C	Page
Removed ordering information table.	
Added R <sub>OUTDIS</sub> parameter to the Electrical Characteristics table.	
Updated the DIGITAL CONTROL SIGNALS section.	8

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#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	<b>RoHS</b> (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
TPS22980RGPR	Active	Production	QFN (RGP)   20	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS22980
TPS22980RGPR.A	Active	Production	QFN (RGP)   20	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS22980
TPS22980RGPR.B	Active	Production	QFN (RGP)   20	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS22980

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

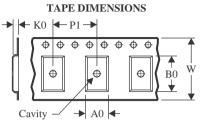
<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

## **PACKAGE MATERIALS INFORMATION**

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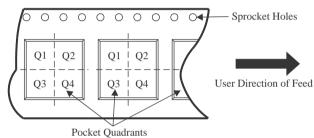
## TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

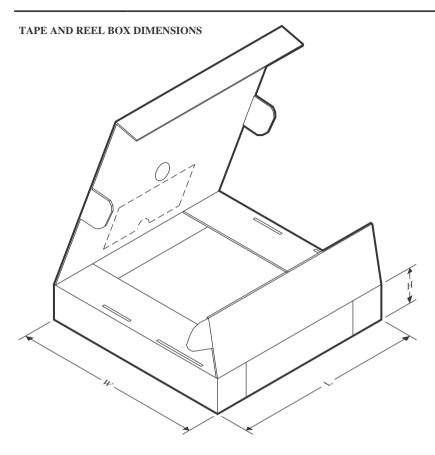


#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22980RGPR	QFN	RGP	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

# PACKAGE MATERIALS INFORMATION

www.ti.com 20-Apr-2023

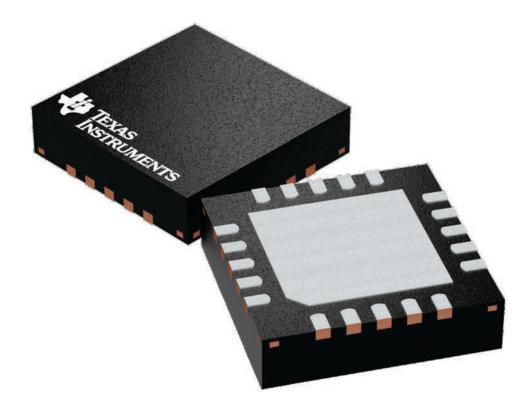


## \*All dimensions are nominal

Device	•	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22980F	RGPR	QFN	RGP	20	3000	346.0	346.0	33.0

4 x 4, 0.5 mm pitch

VERY THIN QUAD FLATPACK

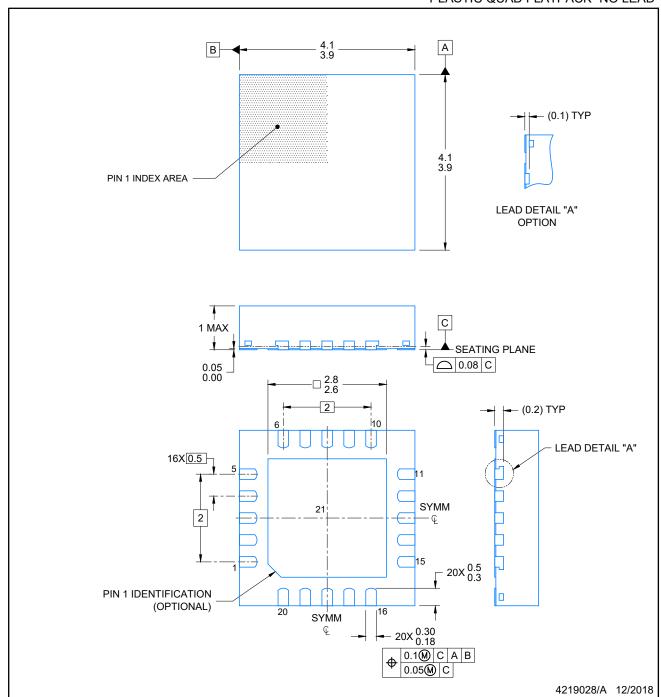


Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.

4224735/A



PLASTIC QUAD FLATPACK- NO LEAD

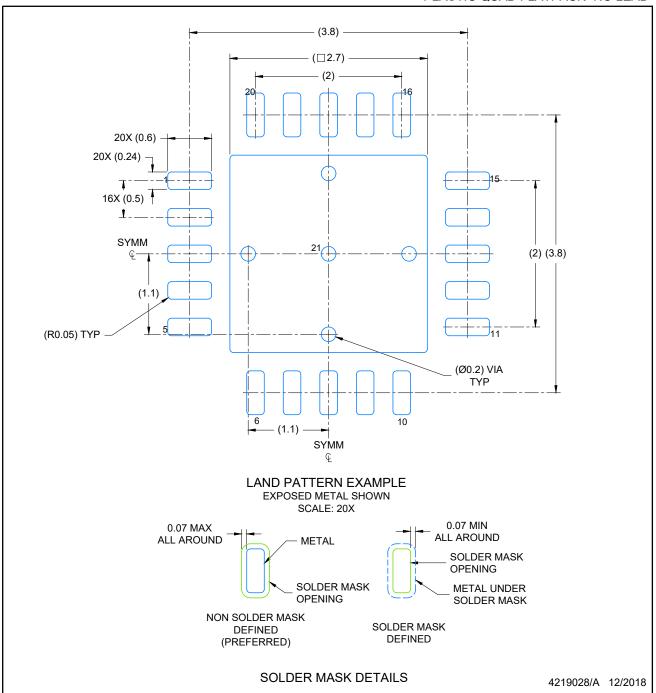


## NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



PLASTIC QUAD FLATPACK- NO LEAD

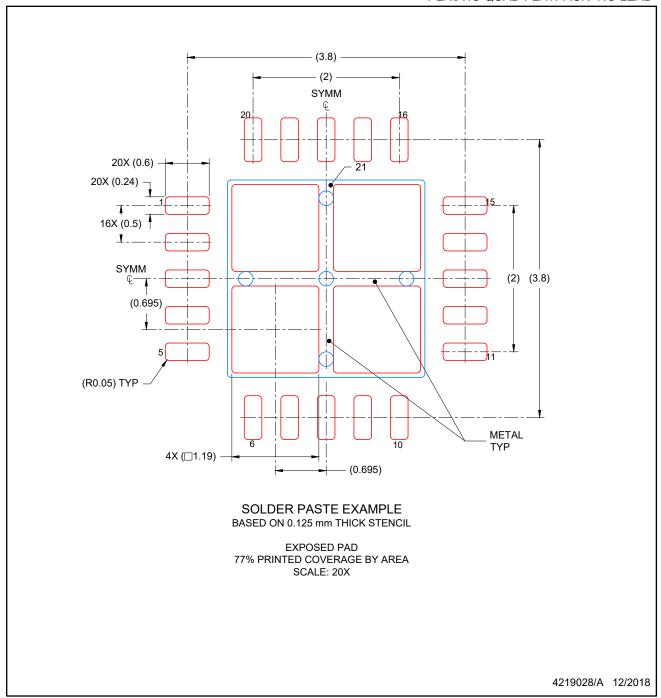


NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC QUAD FLATPACK- NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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