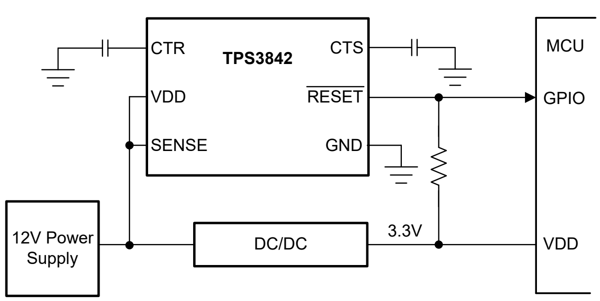
TPS3842 42V Small Size, 850nA Undervoltage or Overvoltage Supervisor With Programmable Delay and De-Glitch

1 Features

- Wide supply voltage range: 1.9V to 42V
- VDD, SENSE, and RESET are rated to 42V
- Low quiescent current: 850nA (typical)
- High threshold accuracy: 0.5% (typical)
- Fixed internal threshold voltages: 2.7V to 9.5V
- Adjustable voltage variant: 0.7V
- Capacitor adjustable delay time with CTR pin
- Capacitor adjustable de-glitch time with CTS pin
- Undervoltage open-drain, active-low output
- Overvoltage open-drain, active-low and active-high output
- Temperature range: –40°C to 125°C
- Small size: SOT5X3 (DRL)

2 Applications

- Factory automation
- Motor drives
- Power delivery
- Enterprise systems
- Grid infrastructure



Typical Application Circuit

3 Description

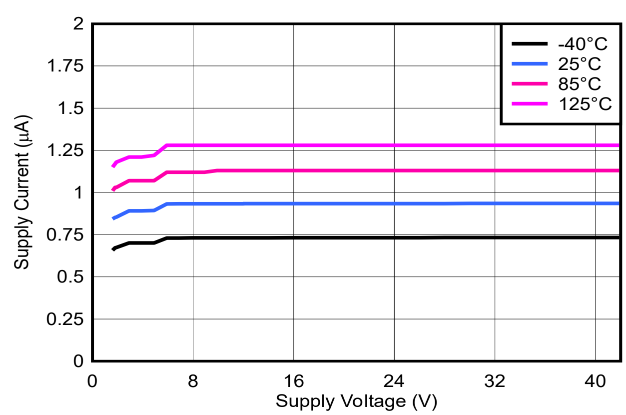
The TPS3842 is a 42V voltage supervisor with 850nA I_{DD}, 0.5% accuracy, and a fast detection time. This device directly connects to 12V / 24V voltage rail for continuous monitoring of undervoltage (UV) or overvoltage (OV) conditions. The TPS3842 comes in a small DRL package for size constrained applications. Built-in hysteresis on the SENSE pin prevents false reset signals when monitoring a supply voltage rail. 1%, 5%, and 10% hysteresis voltage options are available to offer design flexibility to support voltage transients.

SENSE is decoupled from VDD and can monitor higher and lower voltages than VDD. Fixed threshold variants provide accurate low-Iq voltage monitoring. Adjustable threshold variants offer flexible undervoltage threshold setting with external resistors. TPS3842 offers capacitor programmable de-glitch on the SENSE with the CTS pin and capacitor programmable reset delay timing with the CTR pin.

Package Information

PART NUMBER	PACKAGE (1)	PACKAGE SIZE(2)
TPS3842	DRL (SOT5X3, 6)	1.20mm × 1.60mm

(1) For all available packages, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Supply Voltage versus Supply Current

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4 Device Comparison

Device Naming Convention shows some of the device naming nomenclature of the TPS3842. Contact TI sales representatives or on TI's E2E forum for detail and availability.

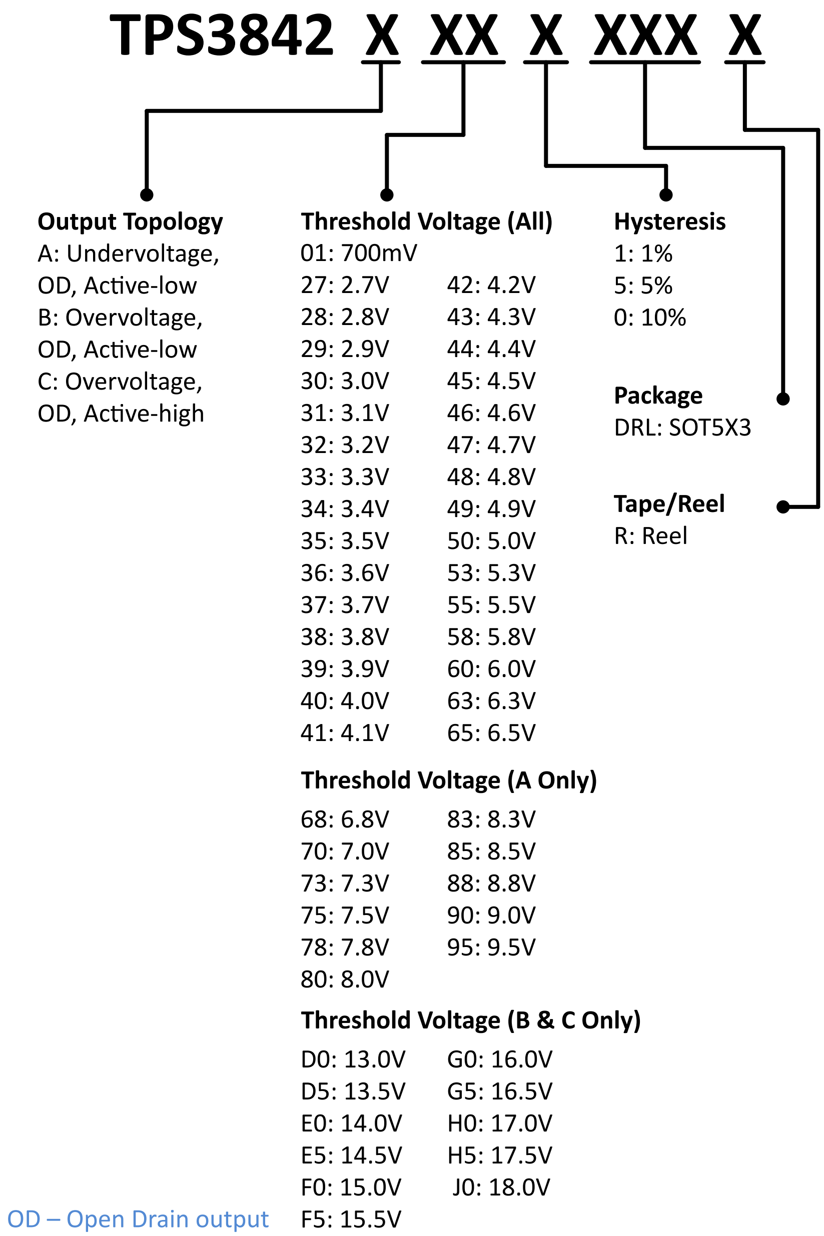

Figure 4-1. Device Naming Convention

1. Suffix 01 with V_{ITN} of 700mV corresponds to the adjustable variant, does not have internal voltage divider resistor ladder.

5 Pin Configuration and Functions

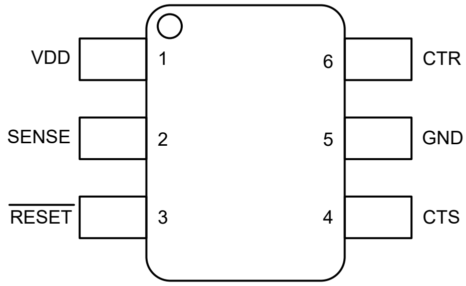

Figure 5-1. TPS3842A, TPS3842B DRL Package 6-Pin SOT5X3 Top View

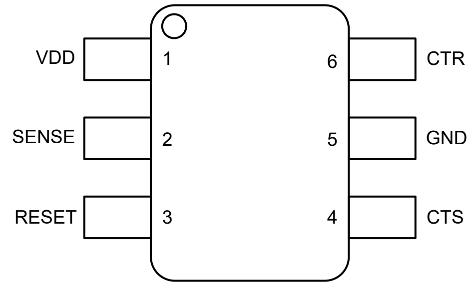

Figure 5-2. TPS3842C DRL Package 6-Pin SOT5X3 Top View

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	**SOT5X3**		
VDD	1	I	Supply voltage pin.
SENSE	2	I	Sense input. Monitors input voltage based on internal voltage threshold. See Section 7.3.1 for more details.
$\overline{RESET}$	3	O	Output reset signal for active-low variants. Connect $\overline{RESET}$ to pull up voltage using a pull up resistance. See Section 7.3.4 for more details.
RESET	3	O	Output reset signal for active-high variants. Connect RESET to pull up voltage using a pull up resistance. See Section 7.3.4 for more details.
CTS	4	I	Sense time delay: Capacitor programmable sense delay: CTS pin offers a user adjustable sense delay time when asserting a reset condition. See Section 7.3.2 for more details.
GND	5	—	Ground pin.
CTR	6	I	Reset time delay: User-programmable reset time delay for $\overline{RESET}$ pin. Connect an external capacitor for adjustable time delay or leave the pin floating for the shortest delay. See Section 7.3.3 for more details.

6 Specification

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Voltage	V_{DD}, V_{SENSE}, $V_{\overline{RESET}}$, V_{RESET}	–0.3	50	V
Voltage	V_{CTR}, V_{CTS}	–0.3	5.5	V
Current	$I_{\overline{RESET}}$, I_{RESET}		±40	mA
Temperature [2]	Operating junction temperature, T_J	-55	150	°C
	Operating free-air temperature, T_A	-55	150	°C
	Storage temperature, T_{stg}	-65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) As a result of the low dissipated power in this device, the operating temperature is assumed that $T_J = T_A$.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 [1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 [2]	±750	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Voltage	V_{DD}	1.9		42	V
Voltage	V_{SENSE}, $V_{\overline{RESET}}$, V_{RESET}	0		42	V
Voltage	V_{CTS} , V_{CTR}	0		5	V
Current	$I_{\overline{RESET}}$, I_{RESET}	0		10	mA
T_A	Junction temperature (free-air temperature)	-40		125	℃

6.4 Thermal Information

THERMAL METRIC[1]		TPS3842	UNIT
		DRL	
		6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	153.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	86.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	42.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	41.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

6.5 Electrical Characteristics

At 1.9V ≤ V_{DD} ≤ 42V, CTS = CTR = Open, $\overline{RESET}$ Voltage ($V_{\overline{RESET}}$) = 100kΩ to V_{DD}, $\overline{RESET}$ load = 50pF, and over the operating free-air temperature range of –40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Supply Voltage		1.9		42	V
V_{POR}	Power on reset voltage[1] (Undervoltage variants)	V_{OL}(max) = 0.25V, $I_{\overline{RESET}\ (Sink)}$ = 15µA			1.3	V
	Power on reset voltage[1] (Overvoltage variants)	V_{OL}(max) = 0.25V, $I_{\overline{RESET}\ (Sink)}$ = 15µA or $I_{RESET\ (Sink)}$ = 15µA			1.7	V
V_{ITN}	Negative-going threshold accuracy (Undervoltage variants)	Fixed internal threshold, V_{ITN} = 2.7V to 9.5V	-1.5	±0.5	1.5	%
		Adjustable internal threshold, V_{ITP} = 700mV	-1.5	±0.5	1.5	%
V_{ITP}	Positive-going threshold accuracy (Overvoltage variants)	Fixed internal threshold, V_{ITP} = 2.7V to 6.5V, 13V to 18V	-1.5	±0.5	1.5	%
		Adjustable internal threshold, V_{ITP} = 700mV	-1.5	±0.5	1.5	%
V_{HYS}	Hysteresis Voltage[2]	1% Variant	0.5	1	1.5	%
V_{HYS}	Hysteresis Voltage[2]	5% Variant	4.5	5	5.5	%
V_{HYS}	Hysteresis Voltage[2]	10% Variant	9.5	10	10.5	%
I_{DD}	Supply current	VDD = 12V, $\overline{RESET}$ or RESET = Not asserted		0.85	1.9	µA
I_{SENSE}	Input current, SENSE pin	V_{SENSE} = V_{IT}, Adjustable version			25	nA
I_{SENSE}	Input current, SENSE pin	V_{SENSE} = 12V, Fixed versions		1.35	2.5	µA
V_{OL}	Low level output voltage	1.9V ≤ V_{DD} < 42V, $I_{\overline{RESET}\ (Sink)}$ = 0.5mA or $I_{RESET\ (Sink)}$ = 0.5mA			300	mV
I_{LKG}	Open drain output leakage current	V_{DD} = $V_{\overline{RESET}}$ = V_{RESET} =12V			300	nA

(1) V_{POR} is the minimum V_{DD} voltage level for a controlled output state.
(2) Hysteresis is with respect of the tripoint V_{ITP}.

6.6 Timing Requirements

At 1.9V ≤ V_{DD} ≤ 42V, CTS = CTR = Open, $\overline{RESET}$ Voltage ($V_{\overline{RESET}}$) = 100kΩ to V_{DD}, $\overline{RESET}$ load = 50pF, and over the operating free-air temperature range of –40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C.

			MIN	NOM	MAX	UNIT
$t_{GI\ (VIT)}$	Glitch Immunity undervoltage $V_{ITN(UV)}$, 20% Overdrive[1]	CTS = Open		5		µs
	Glitch Immunity overvoltage $V_{ITP(OV)}$, 20% Overdrive[1]	CTS = Open		5		µs

(1) 20% Overdrive from threshold. Overdrive % = [V_{SENSE} + V_{ITP}] / V_{ITP}

6.7 Switching Characteristics

At 1.9V ≤ V_{DD} ≤ 42V, CTS = CTR = Open, $\overline{RESET}$ Voltage ($V_{\overline{RESET}}$) = 100kΩ to V_{DD}, $\overline{RESET}$ load = 50pF, and over the operating free-air temperature range of –40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C.

			MIN	NOM	MAX	UNIT
t_{CTR}	Reset time delay	CTR = Open		250		µs
t_{CTR}	Reset time delay	CTR = 0.1uF		285.8		ms
t_{CTR}	Reset time delay	CTR = 3.3uF		9.43		s
t_{PD}	Propagation detect delay[1] [2]	CTS = Open, ADJ Vth		7		µs
t_{PD}	Propagation detect delay[1] [2]	CTS = Open, Fixed Vth		9		µs
t_{CTS}	Sense time delay	CTS = 0.1uF		300		ms

6.7 Switching Characteristics (continued)

At 1.9V ≤ V_{DD} ≤ 42V, CTS = CTR = Open, $\overline{RESET}$ Voltage ($V_{\overline{RESET}}$) = 100kΩ to V_{DD}, $\overline{RESET}$ load = 50pF, and over the operating free-air temperature range of –40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C.

			MIN	NOM	MAX	UNIT
t_{SD}	Startup delay[3]			300		µs

(1) 20% Overdrive from threshold. Overdrive % = [V_{SENSE} + V_{ITP}] / V_{ITP}
(2) t_{PD} measured from threshold trip point (V_{ITP}) to $\overline{RESET}$ V_{OL} voltage for active-low devices and to $\overline{RESET}$ V_{OH} for active-high devices
(3) During the power-on sequence, V_{DD} must be at or above $V_{DD\,(MIN)}$ for at least t_{SD} + t_{CTR} before the output is in the correct state.

6.8 Timing Diagram

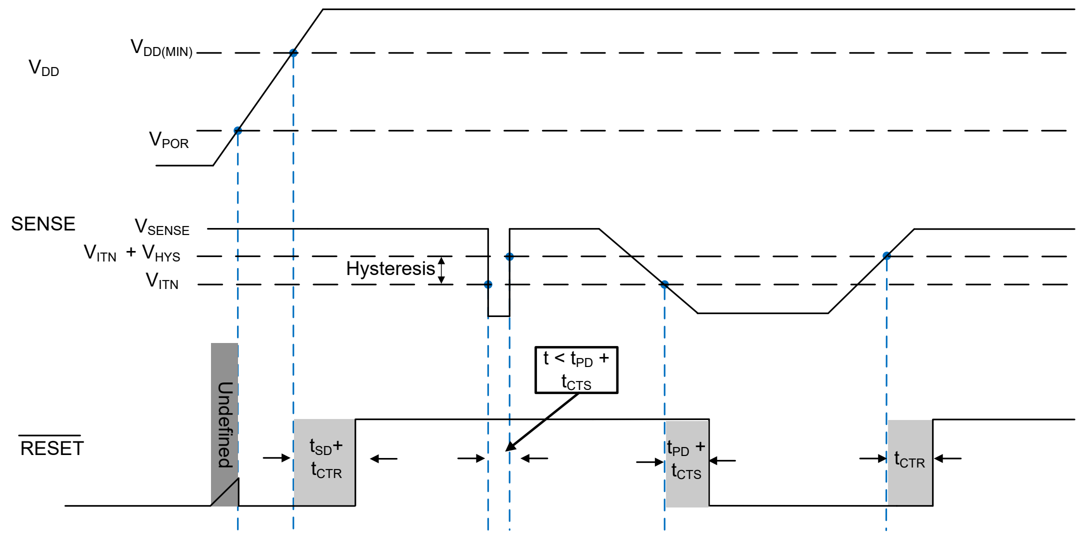

Figure 6-1. Undervoltage Timing Diagram

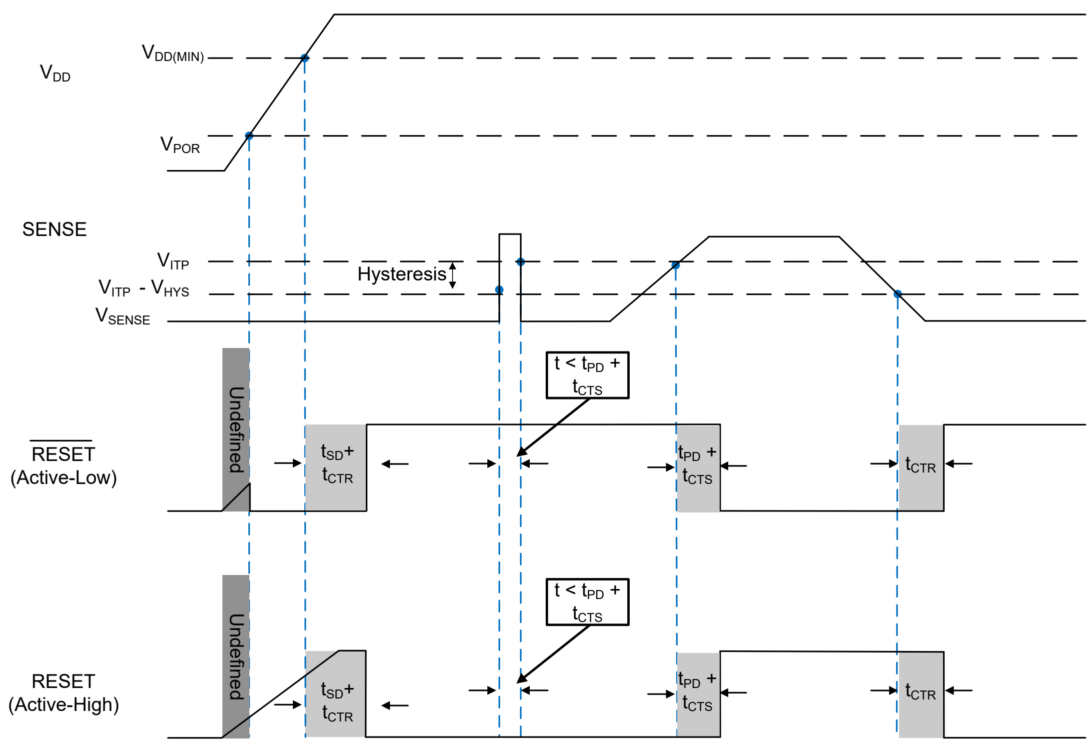

Figure 6-2. Overvoltage Timing Diagram

6.9 Typical Characteristics

At T_A = 25°C, V_{DD} = 3.3V, R_{RESET} = 100kΩ, and C_{LRESET} = 50pF, unless otherwise noted.

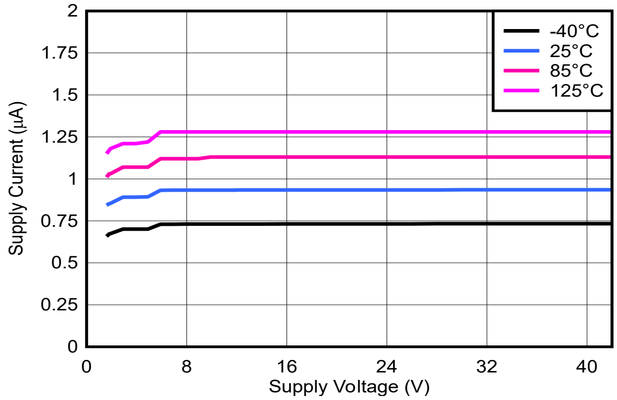

Figure 6-3. Supply Current vs Supply Voltage

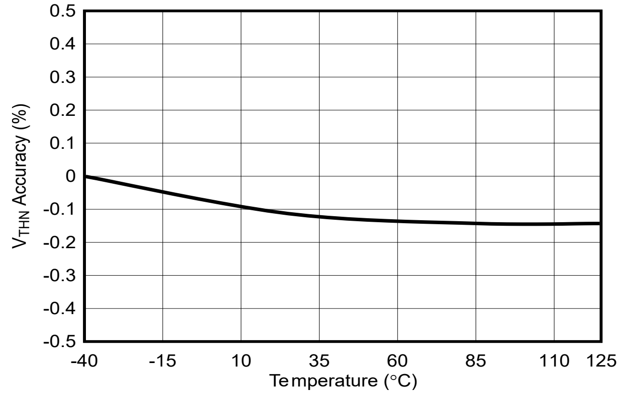

Figure 6-4. V_{THN} Accuracy vs Temperature

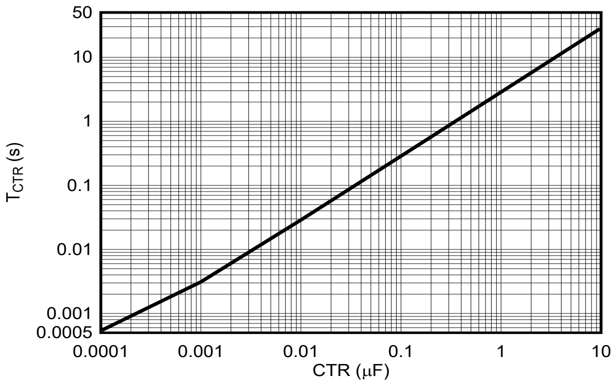

Figure 6-5. T_{CTR} vs CTR

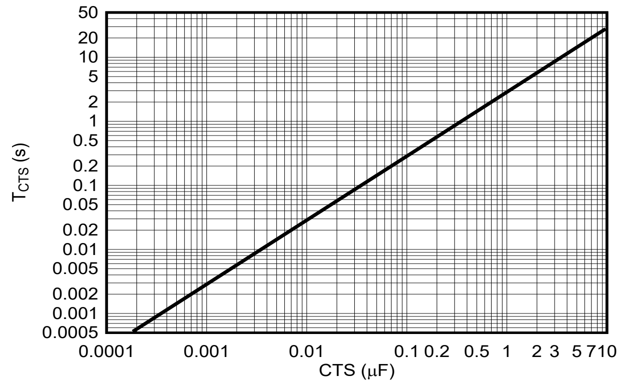

Figure 6-6. T_{CTS} vs CTS

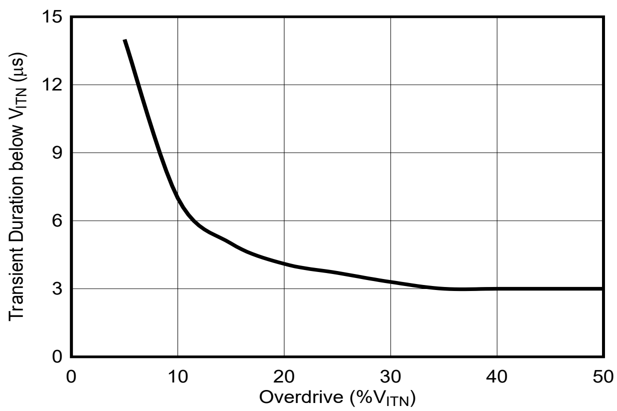

Figure 6-7. Transient Duration at Sense vs Sense Threshold Overdrive Voltage (CTS = Open)

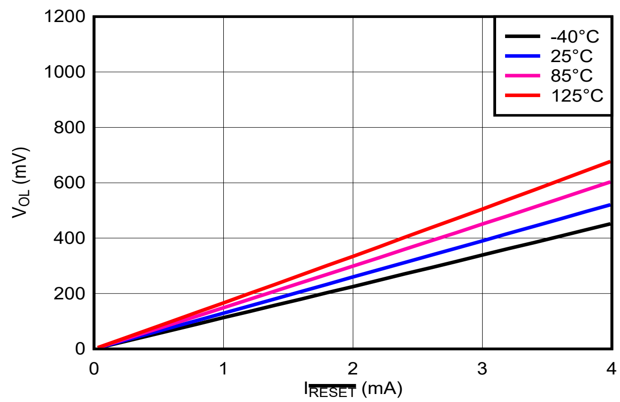

Figure 6-8. RESET Current (Sink) vs V_{OL} (V_{DD} = 3.3V)

6.9 Typical Characteristics (continued)

At T_A = 25°C, V_{DD} = 3.3V, R_{RESET} = 100kΩ, and C_{LRESET} = 50pF, unless otherwise noted.

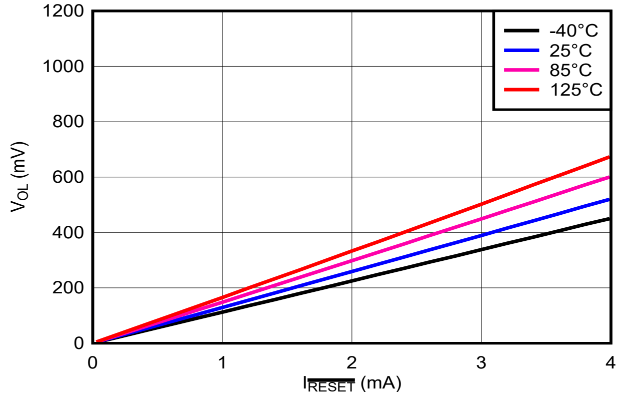

Figure 6-9. RESET Current (Sink) vs V_{OL} (V_{DD} = 12V)

7 Detailed Description

7.1 Overview

The TPS3842 high voltage supervisor product family is designed to assert a $\overline{RESET}$/RESET signal when the SENSE pin voltage crosses V_{IT} and stays beyond V_{IT} for user defined time. The $\overline{RESET}$/RESET output remains asserted for a user-adjustable time until after SENSE voltages returns above the respective threshold and hysteresis.

VDD, SENSE, and $\overline{RESET}$/RESET pins support 42V continuous operation. VDD, SENSE, and $\overline{RESET}$/RESET voltage levels can be independent of each other. The TPS3842 features capacitor programmable sense time delay (CTS) to set a minimum duration of a undervoltage event before $\overline{RESET}$/RESET is asserted. CTS feature also functions as a programmable de-glitch to avoid false resets. The TPS3842 also features a capacitor programmable reset time delay (CTR) to set a minimum duration of $\overline{RESET}$/RESET assertion after a undervoltage event recovers.

7.2 Functional Block Diagrams

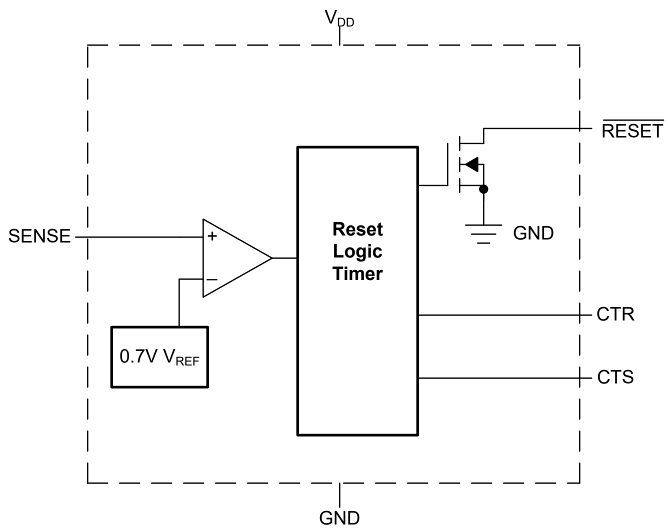

Figure 7-1. Undervoltage Adjustable-Voltage Diagram

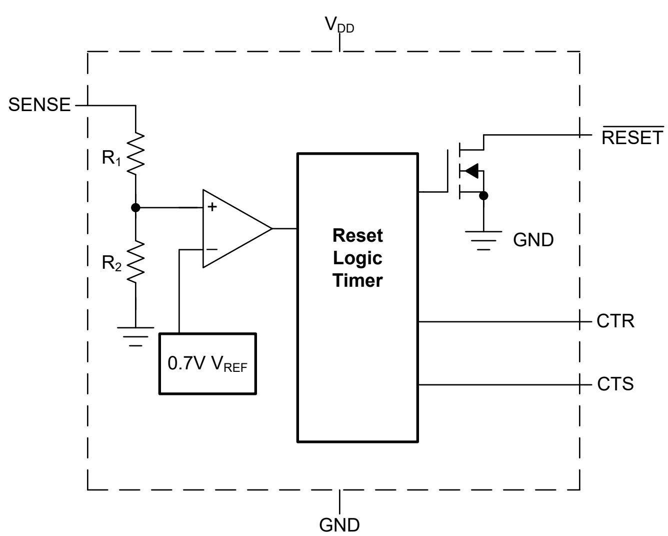

Figure 7-2. Undervoltage Fixed-Voltage Diagram

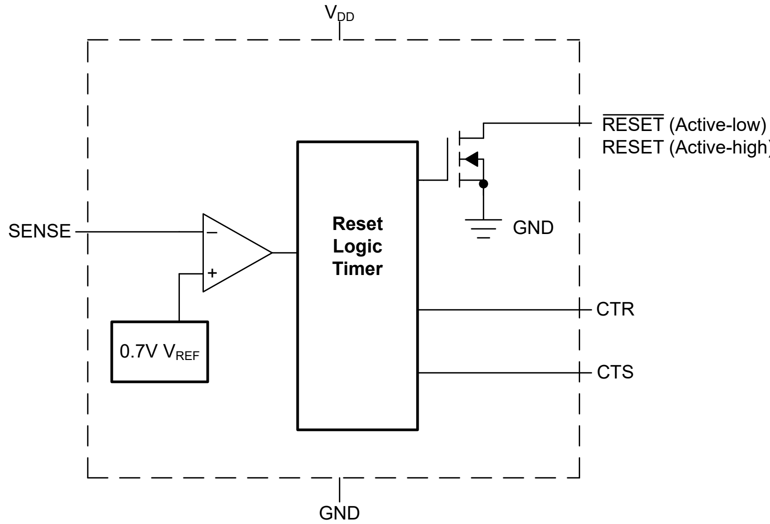

Figure 7-3. Overvoltage Adjustable-Voltage Diagram

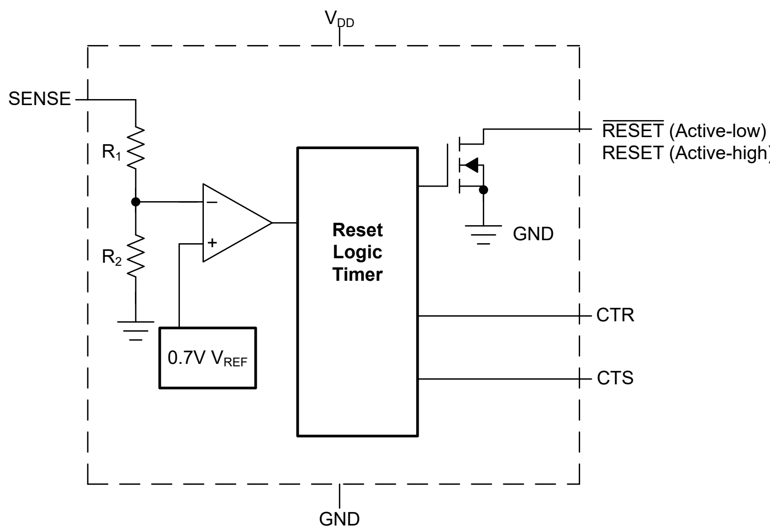

Figure 7-4. Overvoltage Fixed-Voltage Diagram

7.3 Feature Description

A broad range of voltage threshold and hysteresis options are available for the TPS3842, allowing this device to be used in a wide array of applications. Reset threshold voltages can be factory-set from adjustable 0.7V or fixed from 2.7V to 18V. Set the adjustable variant to any voltage above 0.7V using an external resistor divider. Connecting a capacitor between CTR and GND allows the user to select any reset delay period up to 10µF. Connecting a capacitor between CTS and GND allows the user to select any sense delay period up to 10µF.

7.3.1 SENSE Input

The SENSE input provides a pin at which any system voltage can be monitored. If the voltage on this pin drops below V_{ITN} for a t_{PD}+t_{CTS} time interval, then $\overline{\text{RESET}}$/RESET is asserted. The comparator has a built-in hysteresis to suppress unintended $\overline{\text{RESET}}$/RESET assertions and de-assertions. For noisy environments, good analog design practice is to put a 1nF bypass capacitor on the SENSE input to reduce sensitivity to transients and layout parasitics or leverage the CTS feature to set a minimum fault time interval before $\overline{\text{RESET}}$/RESET is asserted.

Figure 7-5 illustrates an example of how to adjust the voltage threshold with external resistor dividers. The resistors can be calculated depending on the desired voltage threshold and device part number. TI recommends using the 700mV threshold option when using an external resistor divider. The variant bypasses the internal resistor ladder for higher accuracy when using external resistors.

For example, consider a 12V rail, V_{MON}, being monitored for undervoltage (UV) using of the TPS3842A011DRLR variant, as shown in Figure 7-5. The monitored UV threshold, denoted as V_{MON-}, is the desired voltage where the device asserts the reset. For this example V_{MON-} = 5.8V. To assert an undervoltage reset the voltage at the sense pin, V_{SENSE}, needs to be equal to the input threshold negative, V_{ITN}. For this example variant V_{SENSE} = V_{ITN} = 0.7V. Using R_1 and R_2 the correlation between V_{MON-} and V_{SENSE} can be seen in Equation 1. Assuming R_1 = 100kΩ, and R_2 can be calculated as R_2 = 13.7kΩ.

$$V_{SENSE} = V_{MON-} \times (R_2 \div (R_1 + R_2)) \quad (1)$$

The TPS3842 hysteresis depends on the configuration selected. For the reset signal to become deasserted, V_{MON} must go above V_{ITN} + V_{HYS}. For this example variant a 1% voltage threshold hysteresis was selected. Therefore, V_{MON} equals 5.858V when the reset signal becomes deasserted. If a 10% hysteresis option was instead used, V_{MON} equals 6.38V when the reset signal becomes deasserted.

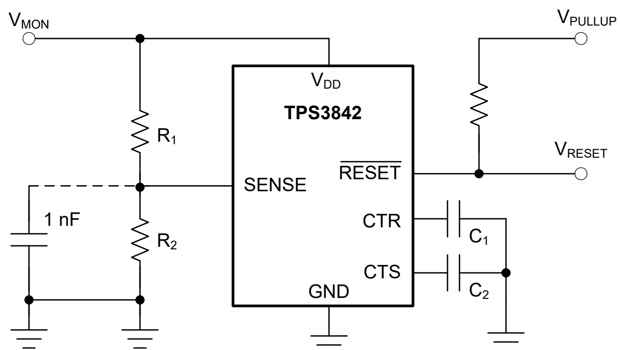

Figure 7-5. Using the TPS3842A011DRLR to Monitor a User-Defined Threshold Voltage

7.3.1.1 SENSE Hysteresis

TPS3842 device offers built-in hysteresis around the V_{IT} threshold to avoid erroneous $\overline{\text{RESET}}$/RESET. The hysteresis (V_{HYS}) is added to the negative thresholds (V_{ITN}) and subtracted for positive thresholds (V_{ITP}).

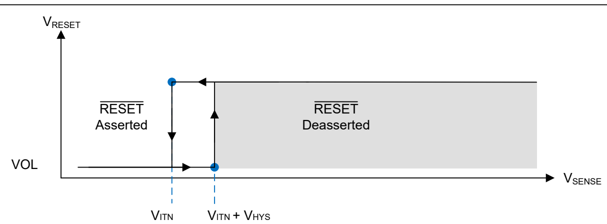

Figure 7-6. Hysteresis (Undervoltage Active-Low)

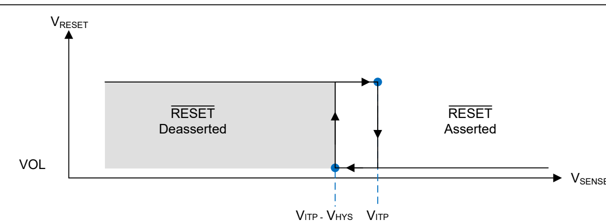

Figure 7-7. Hysteresis (Overvoltage Active-Low)

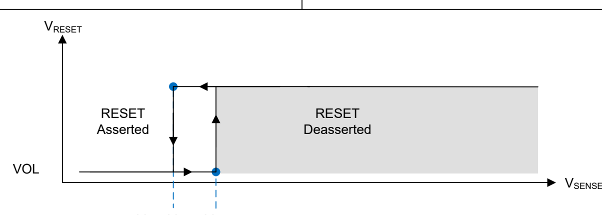

Figure 7-8. Hysteresis (Overvoltage Active-High)

Table 7-1. Common Adjustable Hysteresis Lookup Table

Part Number	DEVICE HYSTERESIS OPTION
TPS3842xxx**1**DRLR	1%

Table 7-1. Common Adjustable Hysteresis Lookup Table (continued)

Part Number	DEVICE HYSTERESIS OPTION
TPS3842xxx**5**DRLR	5%
TPS3842xxx**0**DRLR	10%

Hysteresis is dependent on the device V_{IT} including V_{IT} accuracy and deviations.

Undervoltage (UV):

- V_{ITN} = 700mV
- Voltage Hysteresis (V_{HYS}) = 1% = V_{ITN} × 1% = 7mV (2)
- Release Voltage = V_{ITN} + V_{HYS} = 707mV (3)

Overvoltage (OV):

- V_{ITP} = 700mV
- Voltage Hysteresis (V_{HYS}) = 1% = V_{ITN} × 1% = 7mV (4)
- Release Voltage = V_{ITP} − V_{HYS} = 693mV (5)

7.3.2 Selecting the SENSE Delay Time

TPS3842 has adjustable sense time delay with external capacitors.

- A capacitor on CTS programs the minimum fault time interval before $\overline{\text{RESET}}$ is asserted.
- No capacitor on this pin gives the fastest sense delay time indicated by t_{PD} in Section 6.7.
- Parasitic capacitance on the CTS pin counts as CTS capacitance and increases t_{CTS}.

The time delay (t_{CTS}) can be programmed by connecting a capacitor between CTS pin and GND.

The relationship between external capacitor $C_{CTS\_EXT\ (typ)}$ and the time delay $t_{CTS\ (typ)}$ is given by Equation 6.

$$t_{CTS\ (typ)} = 2.858 \times C_{CTS\_EXT\ (typ)} \tag{6}$$

where:

- $t_{CTS\ (typ)}$ is in seconds (s)
- $C_{CTS\_EXT\ (typ)}$ is in microfarads (µF)

The sense delay varies according to the external capacitor (C_{CTS_EXT}). The minimum and maximum variance due to the constant is show in Equation 7 and Equation 8:

$$t_{CTS\ (max)} = 3.715 \times C_{CTS\_EXT\ (max)} \tag{7}$$

$$t_{CTS\ (min)} = 2 \times C_{CTS\_EXT\ (min)} \tag{8}$$

Make sure there is enough time for the capacitor to fully discharge when a voltage fault occurs to prevent the CTS capacitor from having charge before the next fault. Also, having a too large of a capacitor value can cause very slow charge up (rise times) and system noise can cause the internal circuit to trip earlier or later near the threshold.

Note

Leakages on the capacitor can effect accuracy of sense time delay.

7.3.3 Selecting the RESET Delay Time

TPS3842 has adjustable reset release time delay with external capacitors.

- A capacitor on CTR programs the reset time delay of the output.
- No capacitor on this pin gives the fastest reset delay time.
- Parasitic capacitance on the CTR pin counts as CTR capacitance and increases t_{CTR}.

The time delay (t_{CTR}) can be programmed by connecting a capacitor between CTR pin and GND.

The relationship between external capacitor $C_{CTR\_EXT\ (typ)}$ and the time delay $t_{CTR\ (typ)}$ is given by Equation 9.

$$t_{CTR\ (typ)} = 2.858 \times C_{CTR\_EXT\ (typ)} \quad (9)$$

where:

- $t_{CTR\ (typ)}$ is in seconds (s)
- $C_{CTR\_EXT\ (typ)}$ is in microfarads (μF)

The reset delay varies according to the external capacitor (C_{CTR_EXT}). The minimum and maximum variance due to the constant is show in Equation 10 and Equation 11:

$$t_{CTR\ (max)} = 3.715 \times C_{CTR\_EXT\ (max)} \quad (10)$$

$$t_{CTR\ (min)} = 2 \times C_{CTR\_EXT\ (min)} \quad (11)$$

Having a too large of a capacitor value (> 10μF) can cause very slow charge up (rise times) due to capacitor leakage and system noise can cause the internal circuit to hold $\overline{RESET}$ active.

Note

Leakages on the capacitor can effect accuracy of sense time delay.

7.3.4 RESET Output

$\overline{RESET}$ (active low) denoted with a bar above the pin label. $\overline{RESET}$ remains high voltage (V_{OH}, deasserted) (open-drain variant V_{OH} is measured against the pullup voltage) as long as sense voltage is in normal operation above the threshold boundary and VDD voltage is above VDD(min). If SENSE falls below V_{ITN} for a time period longer than t_{CTS}, $\overline{RESET}$ is asserted, driving the $\overline{RESET}$ pin to a low impedance.

Once SENSE is above V_{ITN} + V_{HYS}, a delay circuit (CTR) is enabled that holds $\overline{RESET}$ low for a specified reset delay period. Once the reset delay has expired, the $\overline{RESET}$ pin goes to a high impedance state.

For overvoltage active low variants, $\overline{RESET}$ asserts when SENSE goes above V_{ITP} for a time period longer than t_{CTS}. Once SENSE is below V_{ITP} - V_{HYS}, a delay circuit (CTR) is enabled that holds $\overline{RESET}$ low for a specified reset delay period. Once the reset delay has expired, the $\overline{RESET}$ pin goes to a high impedance state.

For overvoltage active high variants, RESET deasserts when SENSE goes above V_{ITP} for a time period longer than t_{CTS}. Once SENSE is below V_{ITP} - V_{HYS}, a delay circuit (CTR) is enabled that keeps RESET deasserted for a specified reset delay period. Once the reset delay has expired, the RESET pin asserts.

Open-drain output requires an external pull-up resistor to hold the voltage high to the required voltage logic. Connect the pull-up resistor to the proper voltage rail to enable the output to be connected to other devices at the correct interface voltage levels. $\overline{RESET}$/RESET supports pull-up voltages up to 42V and is independent of VDD and SENSE voltages.

To select the right pull-up resistor, consider system V_{OH} and the Open-Drain Leakage Current (I_{LKG}) provided in the electrical characteristics to set the maximum pull-up resistor value. Low pull-up resistor values increase the amount of current through the internal open-drain output. The current through the open-drain output must be lower than the $I_{\overline{RESET}}$ of the device.

7.4 Device Functional Modes

Table 7-2. Undervoltage Truth Table

SENSE > V_{ITN}	$\overline{RESET}$	VDD
0	L	VDD > VDD(min)
1	H	VDD > VDD(min)
0 or 1	L	VDD(min) > VDD > V_{POR}

Table 7-3. Overvoltage Truth Table

SENSE < V_{ITP}	$\overline{RESET}$	RESET	VDD
0	L	H	VDD > VDD(min)
1	H	L	VDD > VDD(min)
0 or 1	L	H	VDD(min) > VDD > V_{POR}

7.4.1 Normal Operation (V_{DD} > $V_{DD(min)}$)

When V_{DD} is greater than $V_{DD(min)}$, the $\overline{RESET}$/RESET signal is determined by the voltage on the SENSE pin.

- The $\overline{RESET}$/RESET signal corresponds to the voltage on SENSE relative to V_{ITN} or V_{ITP}.

7.4.2 Above Power-On Reset but Less Than $V_{DD(min)}$ (V_{POR} < V_{DD} < $V_{DD(min)}$)

When the voltage on V_{DD} is less than the device $V_{DD(min)}$ voltage, and greater than the power-on reset voltage (V_{POR}), the $\overline{RESET}$ signal is asserted and low impedance regardless of the voltage on the SENSE pin. RESET (active high) signal is deasserted regardless of the voltage on the SENSE pin.

7.4.3 Below Power-On Reset (V_{DD} < V_{POR})

When the voltage on V_{DD} is lower than the required voltage (V_{POR}) $\overline{RESET}$/RESET is undefined.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The following sections describe in detail proper device implementation, depending on the final application requirements.

8.2 Typical Application

A typical application of the TPS3842 used to monitor a 12V power rail is shown in Figure 8-1. The open-drain $\overline{\text{RESET}}$ output is typically connected to the $\overline{\text{RESET}}$ input of a microprocessor. A pullup resistor must be used to hold this line high when $\overline{\text{RESET}}$ is not asserted. The $\overline{\text{RESET}}$ output is undefined for voltage below V_{POR}, but this characteristic is normally not a problem because most microprocessors do not function below this voltage.

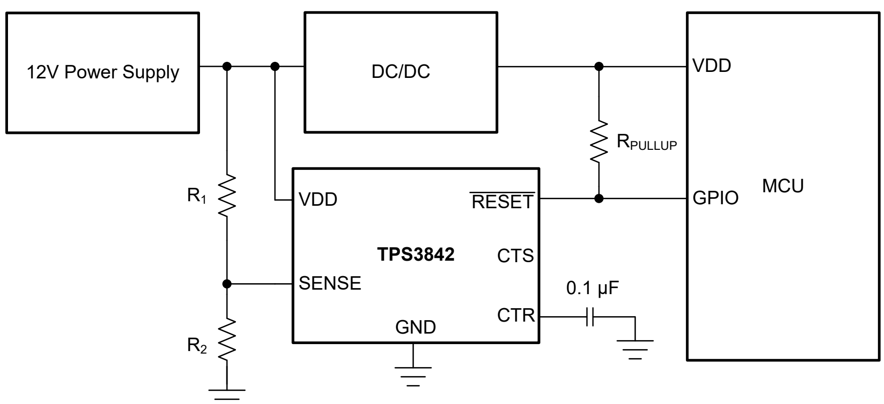

Figure 8-1. Typical Application of the TPS3842 Monitoring a 12V Power Supply

8.2.1 Design Requirements

Table 8-1. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Voltage Threshold	Typical UV voltage threshold 9.5V
Output logic	Open-Drain
SENSE delay	< 0.2ms
$\overline{\text{RESET}}$ delay	300ms

8.2.2 Detailed Design Procedure

The TPS3842 uses high-voltage SENSE and V_{DD} inputs to monitor a 12V power supply for undervoltage. In this design example TPS3842A011DRLR is used.

The negative-going threshold voltage, V_{ITN}, is set by the device variant. In this example, the nominal supply voltage from the power supply is 12V. Setting a undervoltage threshold of 9.5V (approximately 20% under 12V) makes sure that the device resets before supply voltage violates the allowed boundary. The adjustable voltage variant is chosen and R_1 and R_2 are adjusted to meet the threshold. Assuming R_2 equal to 10kΩ and R_1 is calculated as 125kΩ. For additional information on selecting resistor values see Section 7.3.1. TPS3842 also supports fixed voltage threshold variants. Threshold voltage decoding can be found in Device Decoder.

8.2.2.1 Meeting the Sense and Reset Delay

The TPS3842 features both reset assertion (sense) delay, t_{CTS}, and reset deassertion (reset) delay, t_{CTR}. Section 7.3.2 and Section 7.3.3 show how to set the timings for the capacitor-programmable delays. The application requires less than 0.2ms sense delay, thus no capacitor is used and CTS is left open. The application requires greater than 300ms reset delay, thus a 0.1µF capacitor is used.

8.2.3 Application Curve

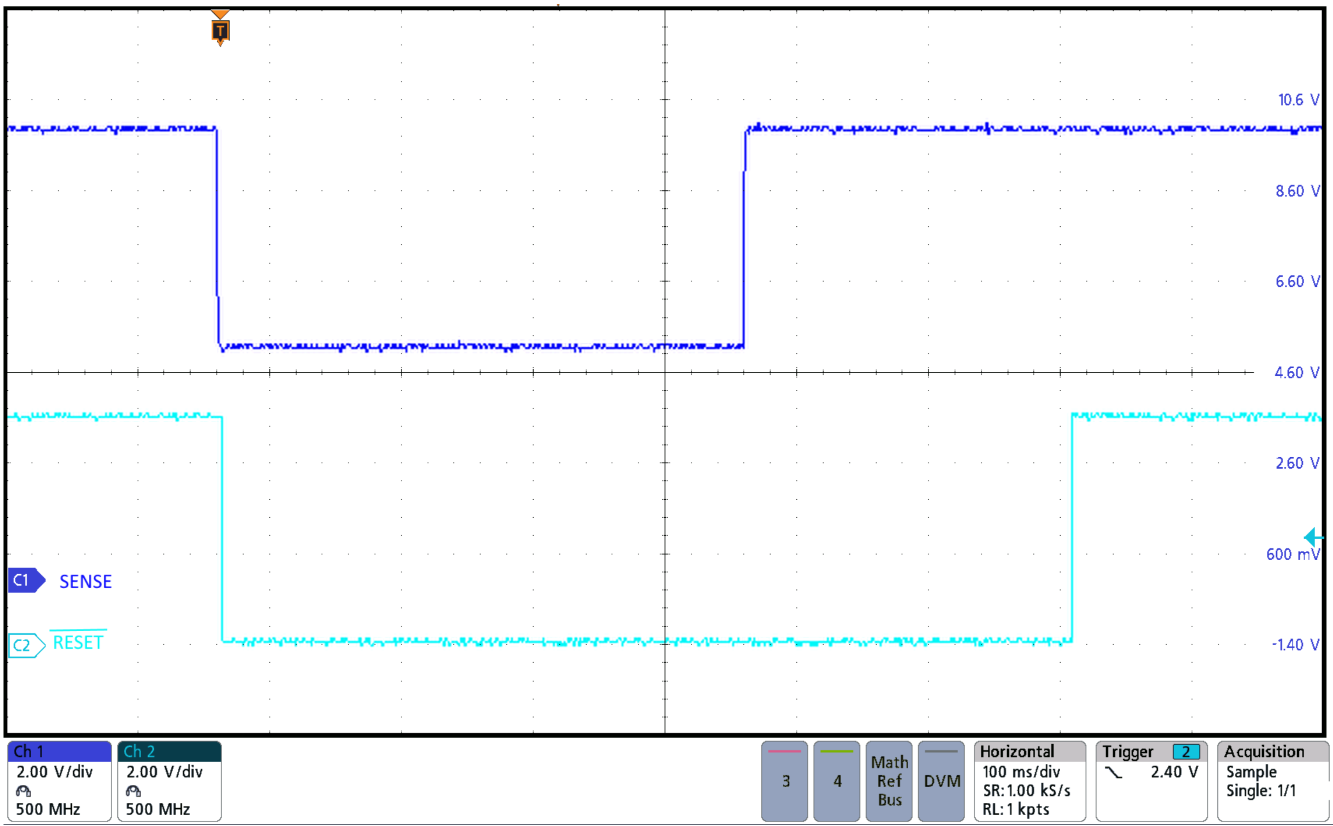

Figure 8-2. TPS3842 Detecting Undervoltage Fault and $\overline{\text{RESET}}$ Recovery

8.2.4 Power Supply Recommendations

TPS3842 is designed to operate from an input supply with a V_{DD} voltage between 1.9V (minimum operation) to 42V (maximum operation). Good analog design practice recommends placing a minimum 0.1µF ceramic capacitor as near as possible to the V_{DD} pin.

8.2.5 Layout

8.2.5.1 Layout Guidelines

- Make sure that the connection to the VDD pin is low impedance. Good analog design practice is to place a greater than 0.1µF ceramic capacitor as near as possible to the VDD pin.
- For noisy environments and to improve noise immunity on the SENSE pins, an optional 1nF capacitor between the SENSE pin and GND can reduce the sensitivity to transient voltages on the monitored signal. An alternative to improve noise immunity is to use the CTS feature.
- If a capacitor is used on CTS or CTR, place these components as close as possible to the respective pins. If the capacitor adjustable pins are left unconnected, make sure to minimize the amount of parasitic capacitance to not affect the t_{PD} or t_{CTR}.
- Place the pull-up resistors on $\overline{\text{RESET}}$/RESET as close to the pin as possible.
- When laying out metal traces, separate high voltage traces from low voltage traces as much as possible.

- Do not have high voltage metal pads or traces closer than 20mils (0.5mm) to the low voltage metal pads or traces.

8.2.5.2 Layout Example

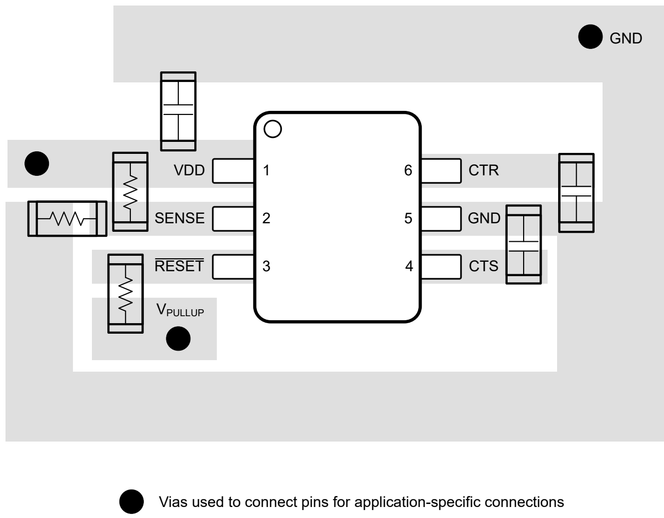

Figure 8-3. TPS3842 Recommended Layout

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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9.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.5 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (August 2024) to Revision B (October 2025) **Page**

- Updated title to include Overvoltage........ 1
- Added overvoltage option throughout the document........ 1
- Updated the numbering format for tables, figures, equations, and cross-references throughout the document 1
- Updated *Features* list........ 1
- Added overvoltage option to the *Description* 1
- Removed nomenclature table........ 3
- Updated device naming convention table........ 3
- Updated the *Pin Configuration and Functions* 4
- Updated *Recommended Operating Conditions, Electrical Characteristics, Timing Requirements, Switching Characteristics* to include Overvoltage variant electrical specifications........ 5
- Added Overvoltage Timing Diagram........ 7
- Added overvoltage description to the *Overview* 10
- Updated the *Functional Block Diagrams* 10
- Updated from: 9.5V to: 18V in the *Feature Description* 11
- Added overvoltage RESET to the *SENSE Input* 11
- Added Overvoltage hysteresis diagrams and equations to the *SENSE Hysteresis* 12
- Added RESET functionality to the *RESET Output* 14
- Added overvoltage truth table........ 15
- Added RESET to description to the *Device Functional Modes* 15
- Added RESET description to the Layout Guidelines........ 17

Changes from Revision * (April 2024) to Revision A (August 2024)	Page
• Production Data Release	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS3842A010DRLR	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	A010
TPS3842A010DRLR.A	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	A010
TPS3842A011DRLR	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	A011
TPS3842A011DRLR.A	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	A011
TPS3842B010DRLR	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	-	SN	Level-1-260C-UNLIM	-40 to 125	B010C

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS3842 :

- Automotive : TPS3842-Q1

NOTE: Qualified Version Definitions:

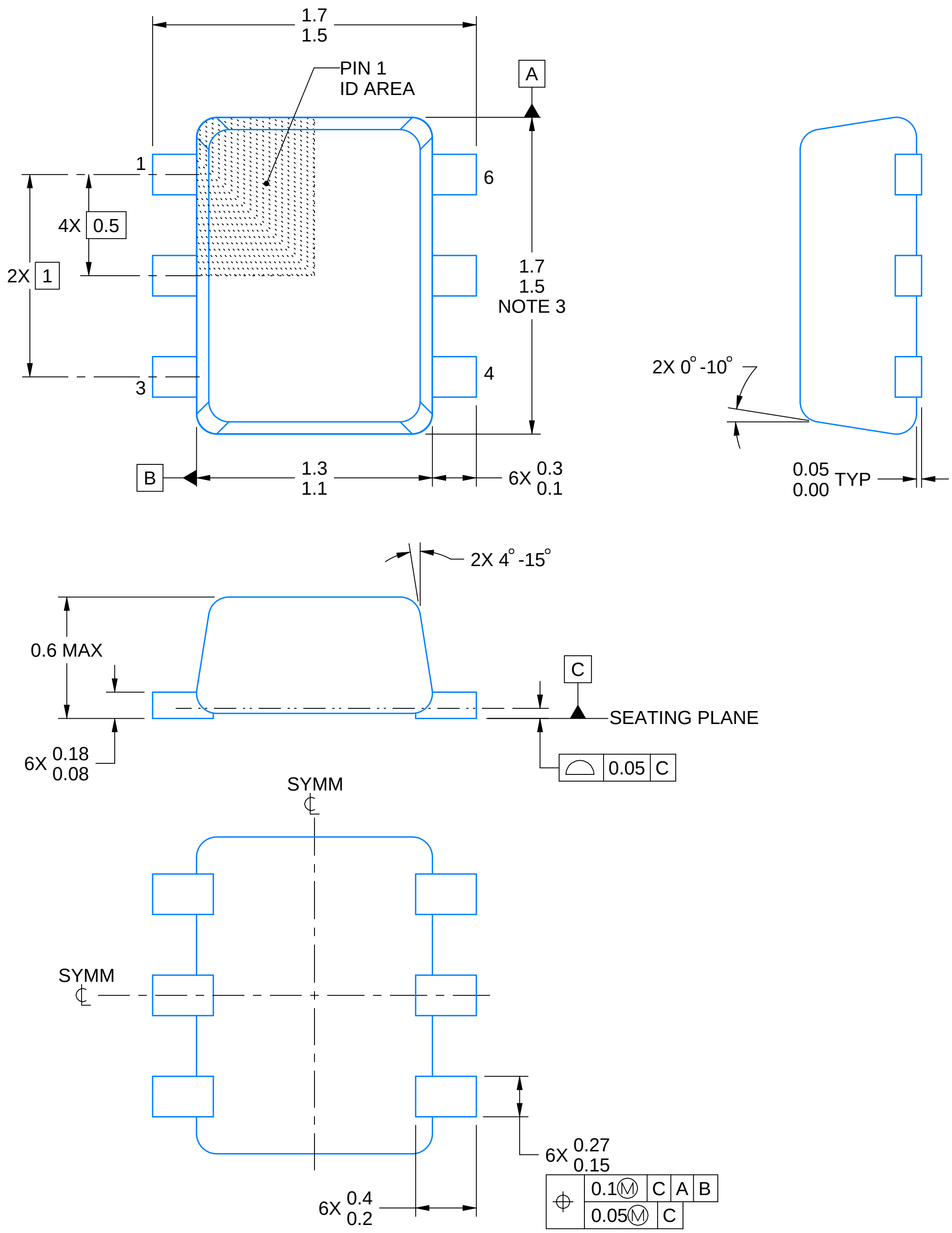
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

PACKAGE OUTLINE

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



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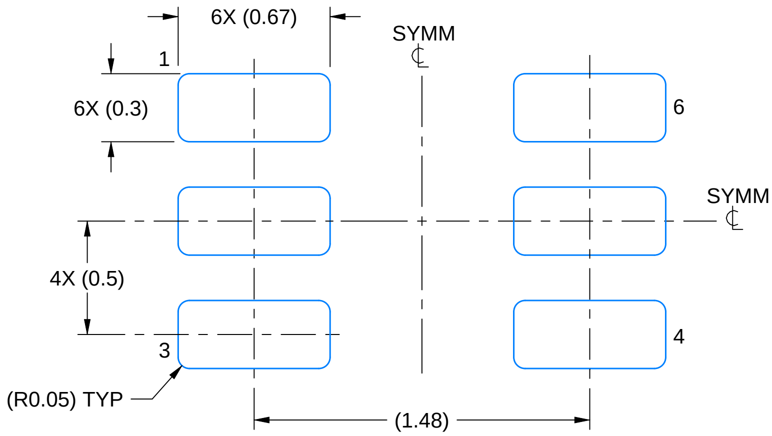
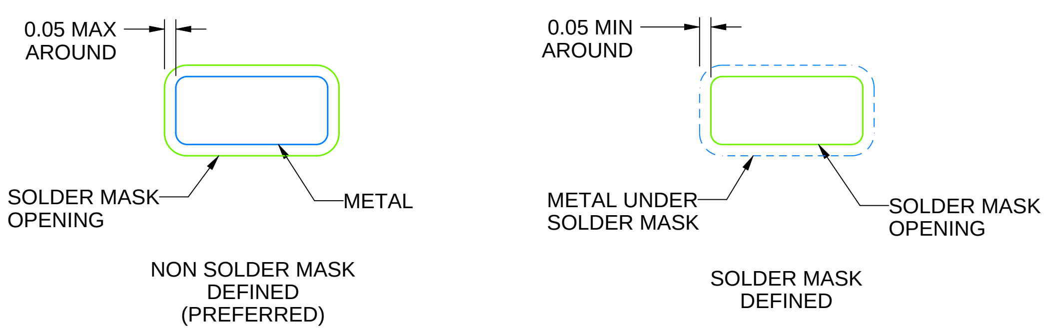
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

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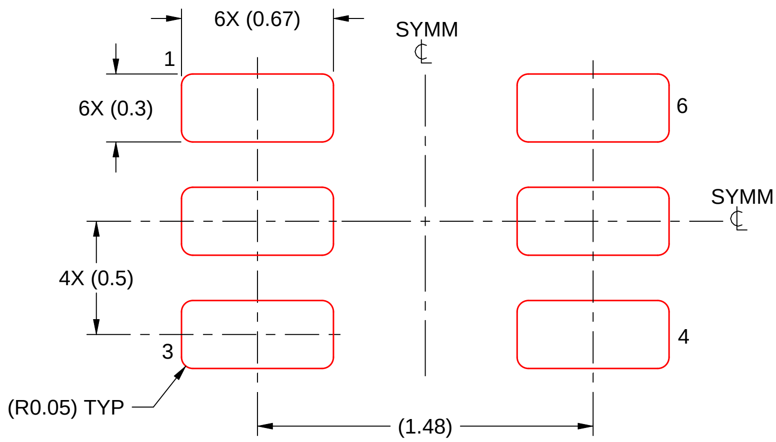
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.