1.6-A, 1.25-MHz BUCK CONVERTER IN A 3 mm × 3 mm SON PACKAGE

FEATURES

- **Input Voltage Range 4.5 V_{DC} to 8 V_{DC}**
- **Output Voltage (0.8 V to 90% V_{IN})**
- **0 A to 1.6 A Current Capability**
- **Fixed 1.25-MHz Switching Frequency**
- **Reference 0.8 V ±1%**
- **Internal 250 mΩ N-Channel MOSFET Switch**
- **Current Mode Control with Internal Slope Compensation**
- **Internal Soft-Start**
- **Internal Loop Compensation**
- **Short Circuit Protection**
- **Thermal Shutdown**
- **High Efficiency Up to 92%**
- **Small 3 mm × 3 mm SON Package**

APPLICATIONS

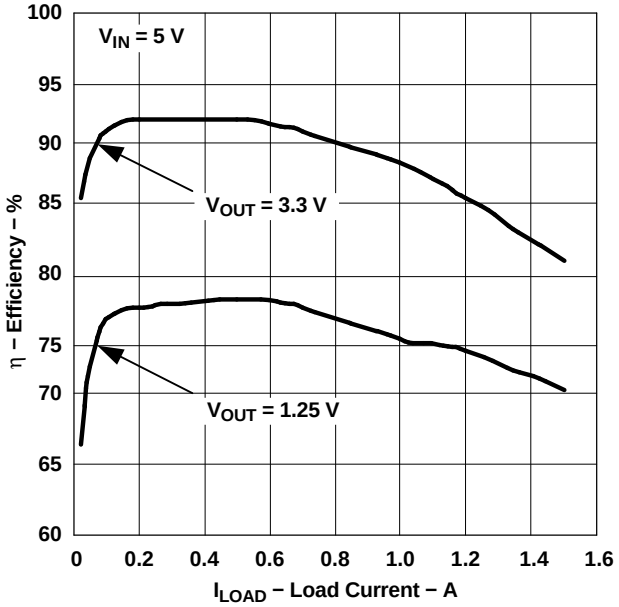
- **Disk Drives**
- **Set Top Box**
- **Point of Load Power**
- **ASIC Power Supplies**

DESCRIPTION

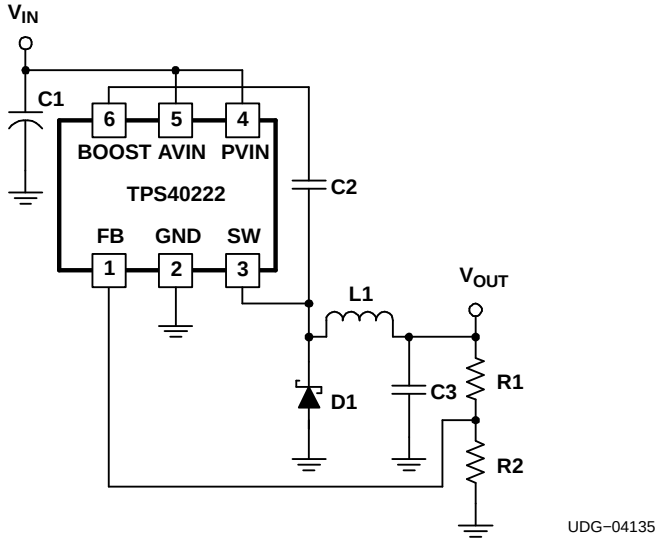
The TPS40222 is a fixed-frequency, current-mode, non-synchronous buck converter optimized for applications powered by a 5-V distributed source. With internally determined operating frequency, soft-start time, and control loop compensation, the TPS40222 provides many features with a minimum of external components.

The TPS40222 operates at 1.25 MHz and supports up to 1.6-A output loads. The output voltage can be programmed to as low as 0.8 V. The TPS40222 utilizes pulse-by-pulse current limit as well as frequency foldback to protect the converter during a catastrophic short circuited output condition.

TYPICAL EFFICIENCY vs LOAD CURRENT



SIMPLIFIED APPLICATION DIAGRAM



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_J	OUTPUT VOLTAGE	PACKAGE	PART NUMBER	MEDIUM	QTY
-40°C to 125°C	Adjustable	Plastic SON (DRP)	TPS40222DRPT	Small tape and reel	250
			TPS40222DRPR	Large tape and reel	3000

ABSOLUTE MAXIMUM RATINGS

over free-air temperature range unless otherwise noted(1)

			TPS40222	UNIT
V_{IN}	Input voltage range	BOOST	19	V
		SW (50 ns maximum)	–5	
		SW	–2 to 16	
		AVIN, PVIN	10	
		FB	-0.3 to 2	
I_{OUT}	Output current source	SW	3.5	A
T_J	Operating junction temperature range		–40 to 160	°C
T_{stg}	Storage temperature		–65 to 165	
	Case temperature for 10 seconds per JSTD-020C		260	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	4.5		8.0	V
I_{OUT}	SW node output current	0		1.6	A
T_J	Operating junction temperature	-40		125	°C

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

	MIN	MAX	UNIT
Human body model		2500	V
CDM		1500	

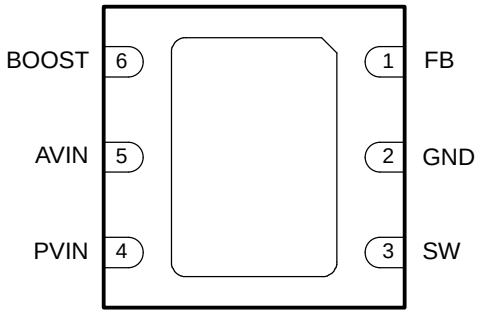
ELECTRICAL CHARACTERISTICS

T_J = -40°C to 125°C, 4.5 ≤ V_{AVIN} = V_{PVIN} ≤ 5.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FEEDBACK VOLTAGE						
V_{FB}	Feedback voltage	T_J = 25°C, No load	792	800	808	mV
		-40°C ≤ T_J ≤ 125°C, No load, 4.5V ≤ V_{DD} ≤ 7 V	788		812	
I_{FB}	Feedback input bias current	V_{FB} = 0.9 V, V_{AVIN} = V_{PVIN} = 5 V		30	100	nA
SOFT-START						
t_{SS}	Soft-start time	V_{AVIN} = V_{PVIN} = 5 V	300	550	850	µs
Gm AMPLIFIER						
Gm	Transconductance(1)			10		µS
GBW	Gain bandwidth product(1)			12		MHz
OSCILLATOR						
f_{SW}	Switching frequency	V_{FB} > 0.7 V	1.00	1.25	1.50	MHz
f_{SWFB}	Minimum foldback frequency	Startup/Overcurrent, V_{FB} = 0 V	75	140		kHz
	Foldback frequency slope(1)	0 V < V_{FB} < 0.4 V		2200		Hz/mV
V_{FFB}	Frequency foldback V_{FB} threshold voltage(1)		0.4		0.6	V
OVERCURRENT DETECTION						
I_{CL}	Overcurrent threshold	V_{AVIN} = V_{PVIN} = 5 V	2.1	2.6	3.1	A
t_{ON}	Minimum on-time in overcurrent(1)			90	200	ns
HIGH SIDE MOSFET AND DRIVER						
$R_{DS(on)}$	Drain-to-source on-resistance	T_J = 25°C		250		mΩ
		-40°C ≤ T_J ≤ 125°C		250	550	
D_{MAX}	Maximum duty cycle		90%	97%		
I_{SWL}	MOSFET SW leakage current	V_{PVIN} = 10 V		-10	-30	µA
I_{BOOST}	Boost current	I_{SW} = 100 mA, V_{AVIN} = V_{PVIN} = 5 V		0.5	1.0	mA
	Boost diode voltage drop	I_{DIODE} ≤ 5 mA		0.9		V
UNDERVOLTAGE LOCKOUT (UVLO)						
V_{ON}	Turn-on voltage		3.6	3.8	4.0	V
V_{HYST}	Hysteresis voltage			0.4		
I_Q	AVIN quiescent current			1.0	1.5	mA
THERMAL SHUTDOWN						
	Thermal shutdown voltage(1)			150		°C
	Thermal hysteresis(1)			-10		

(1) Ensured by design. Not production tested.

DRP PACKAGE
(BOTTOM VIEW)



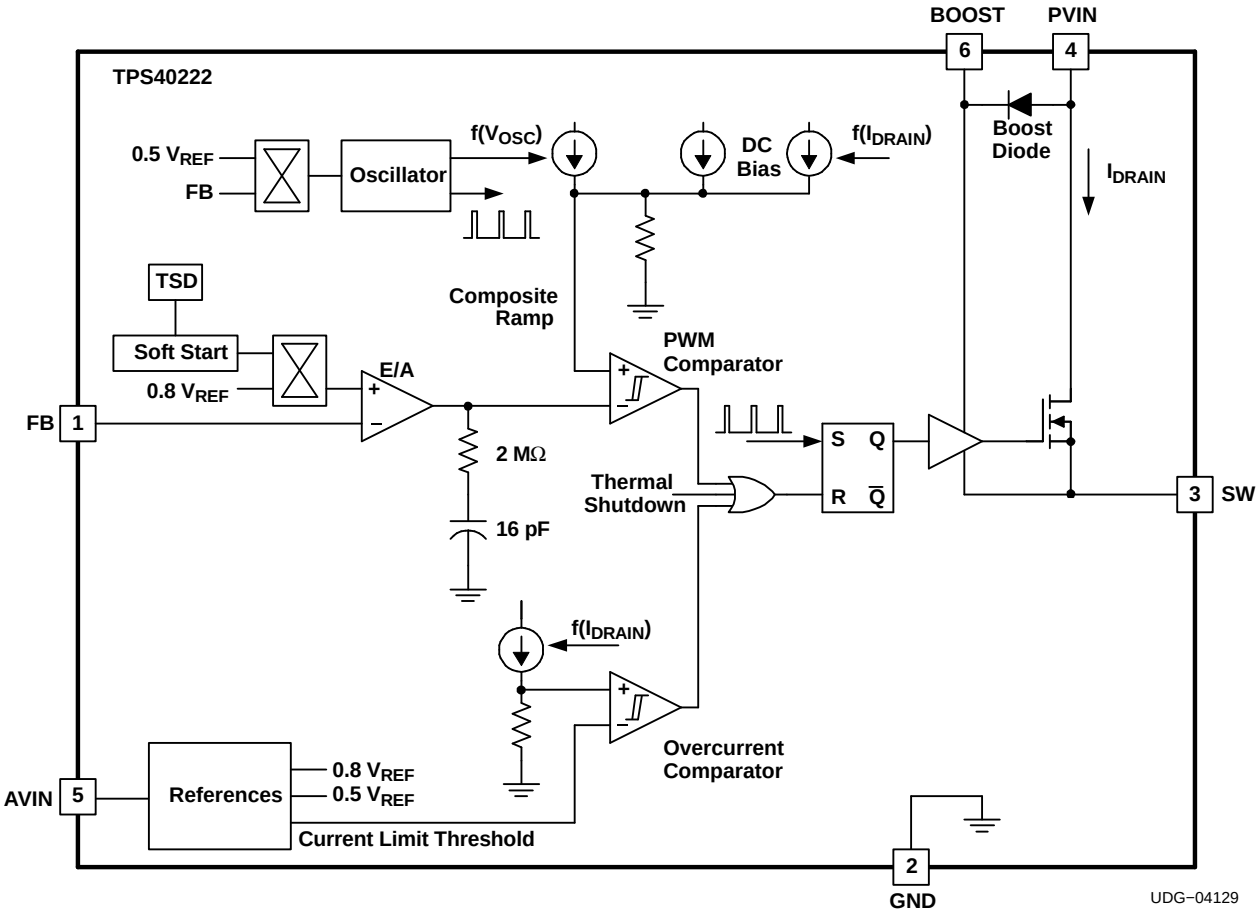
A. Exposed pad provides a low thermal resistance of θ_{JC}= 2°C/W

B. Connect exposed pad to GND.

Table 1. TERMINAL FUNCTIONS

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AVIN	5	I	Input power to the control section of the device. Closely bypass this pin to GND with a low ESR ceramic capacitor of 1-µF or greater.
BOOST	6	I/O	This pin provides a bootstrapped supply for the high-side MOSFET driver for PWM, enabling the gate of the high-side MOSFET to be driven above the input supply rail. Connect a 33-nF capacitor from this pin to SW pin and (optionally) a Schottky diode from this pin to the PVIN pin.
FB	1	I	Inverting input of the error amplifier. In closed-loop operation, the voltage at this pin is the internal reference level of 800 mV. During startup or fault conditions, the voltage on this pin also affects the operating frequency of the converter. With 0 V on the pin, the operating frequency is approximately 140 kHz.The frequency increases linearly to approximately 1.25 MHz as the voltage on the pin is raised to 0.6 V. Above 0.6 V, the operating frequency remains at approximately 1.25 MHz.
GND	2	-	Ground connection to the device.
PVIN	4	I	Input to the power section of the device. Bypass this pin to GND with a low ESR capacitor of 10-µF or greater.
SW	3	I/O	The source connection of the internal switching MOSFET. Connect this pin to the output inductor and an external catch diode to form the converter's switch node.

SIMPLIFIED BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

FEEDBACK VOLTAGE
vs
INPUT VOLTAGE (NO LOAD)

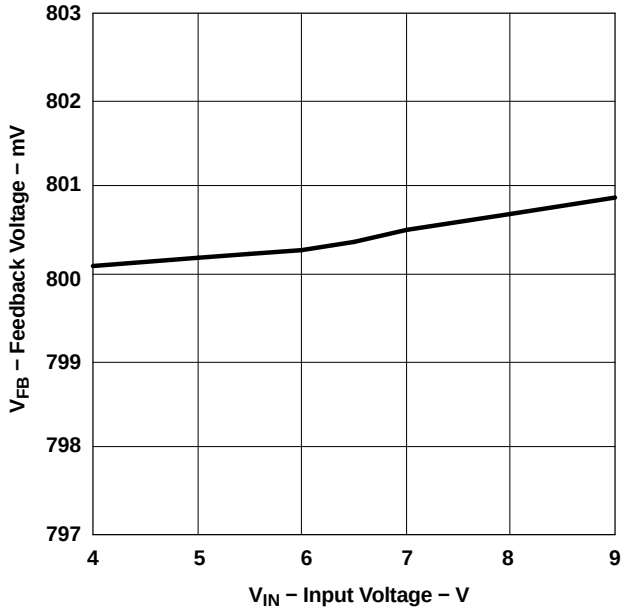


Figure 1.

FEEDBACK VOLTAGE
vs
JUNCTION TEMPERATURE

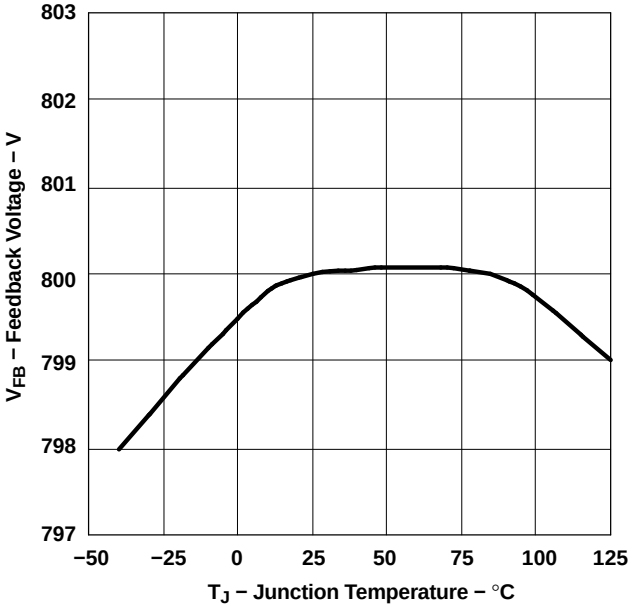


Figure 2.

OSCILLATOR FREQUENCY
vs
FEEDBACK VOLTAGE

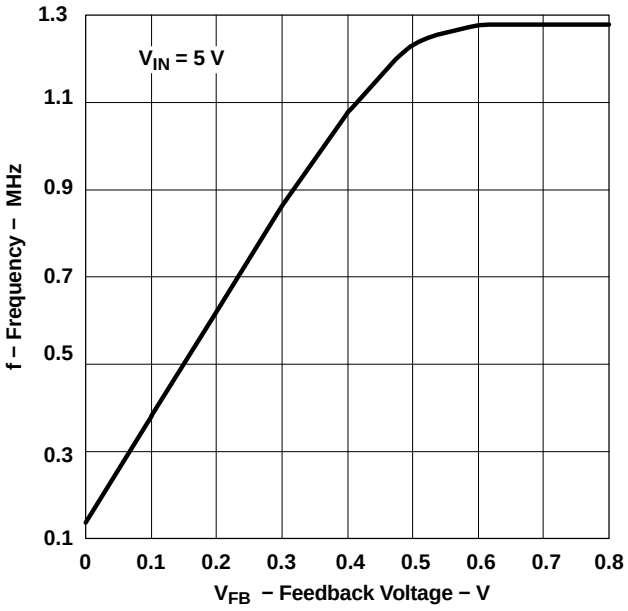


Figure 3.

OSCILLATOR FREQUENCY
vs
INPUT VOLTAGE

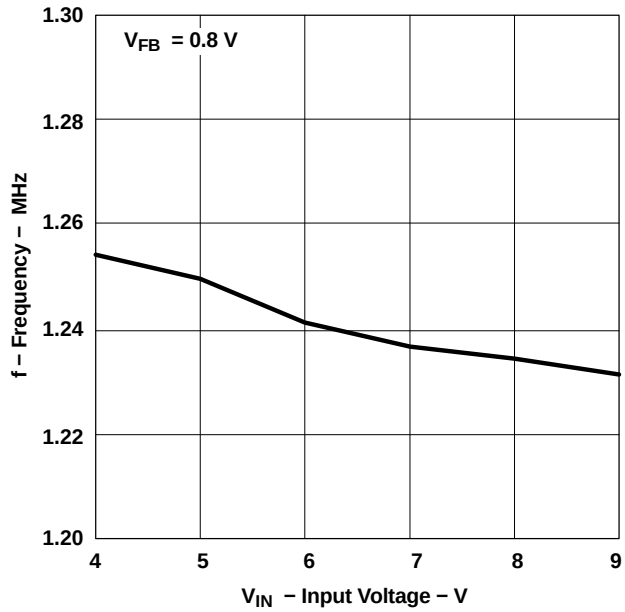


Figure 4.

TYPICAL CHARACTERISTICS (continued)

OVERCURRENT vs INPUT VOLTAGE

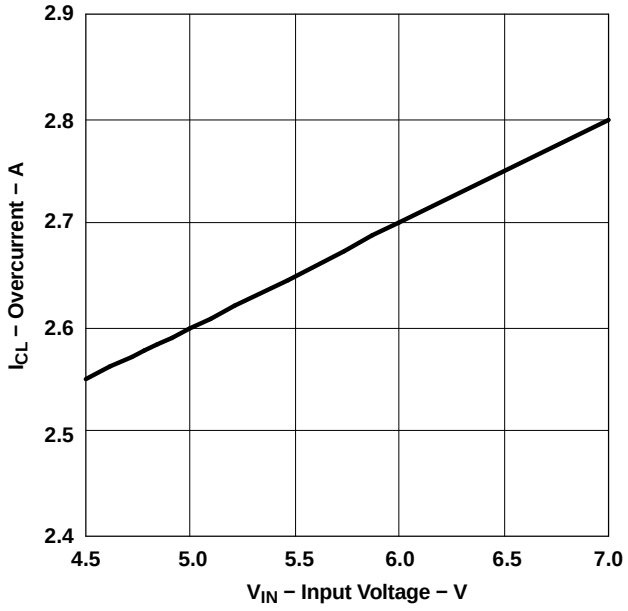


Figure 5.

OVERCURRENT vs JUNCTION TEMPERATURE (V_{IN}=5V)

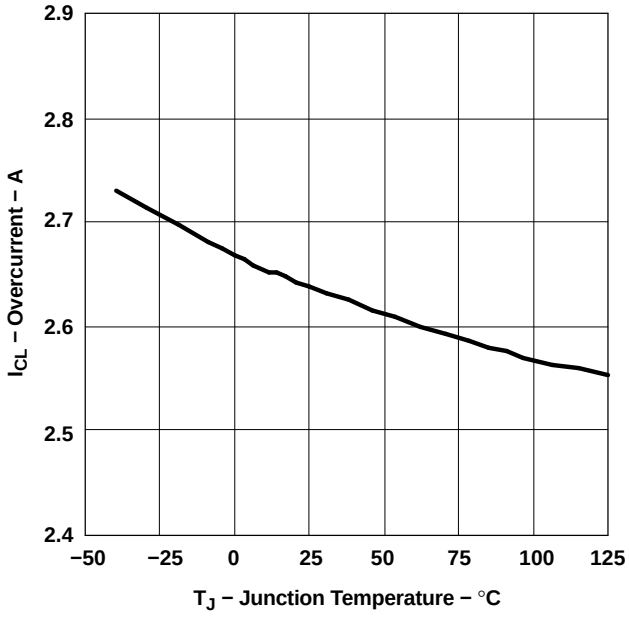


Figure 6.

SWITCHING MOSFET ON-RESISTANCE vs JUNCTION TEMPERATURE

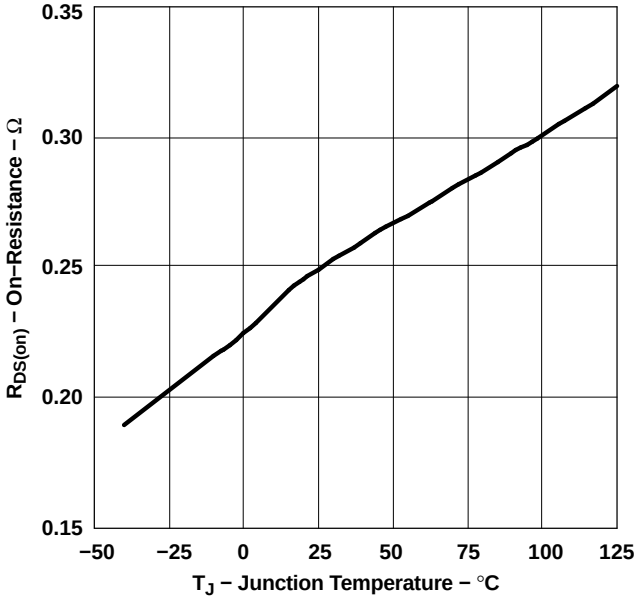


Figure 7.

SOFT-START TIME vs JUNCTION TEMPERATURE

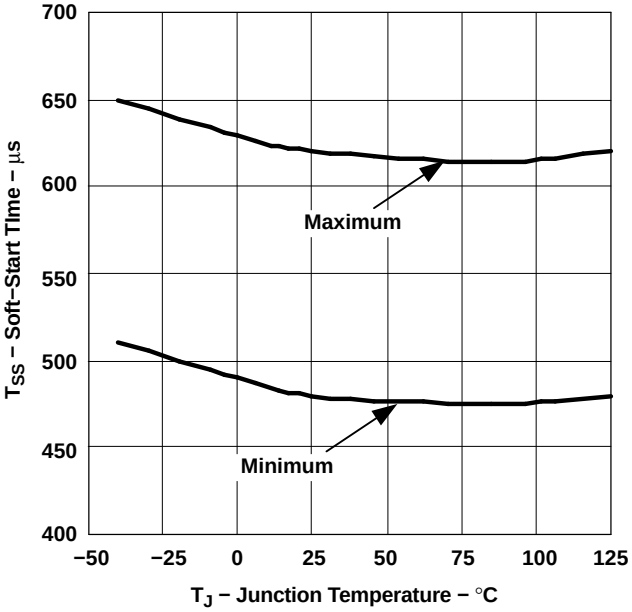


Figure 8.

DETAILED DESCRIPTION

The TPS40222 is a fixed frequency PWM controller incorporating an internal high-side MOSFET switch and is intended for non-synchronous converter applications requiring load current of up to 1.6 A.

Feedback Control

To maintain output voltage regulation, a fixed-frequency, current-mode-control architecture is employed. A transconductance error amplifier with internal compensation senses the output voltage through a resistive divider and compares the result with an internal 0.8-V precision reference voltage. The result of this comparison is fed to the inverting input of a PWM comparator. A composite sawtooth voltage waveform is fed in to the non-inverting input resulting at a PWM signal at the comparator output.

To generate the sawtooth ramp signal, the load current is sensed through the high-side MOSFET during the ON portion of the switching cycle. The sensed current is then split and fed into two trimmed resistor banks that are used to generate the ramps for the PWM control and the pulse-by-pulse current limit. This method of sensing does not require a sense resistor in the high-current path. The portion of the load current for PWM control is then summed with a signal proportional to the oscillator sawtooth, plus a small portion of DC bias to create the composite ramp signal.

UVLO

An internal circuit will turn on the converter when the AVIN voltage rises above approximately 3.8 V. At voltages below this level, the internal oscillator is disabled and the internal MOSFET is biased off.

Reference

The precision bandgap reference of 0.8 V is trimmed to 1%.

Voltage Error Amplifier

The internal transconductance amplifier is used to control the output voltage. A series R-C circuit (2 MΩ, 16 pF) from the output of the amplifier to ground serves as the compensation circuit for the converter.

Oscillator

During normal operation, the internal oscillator runs at a nominal 1.25 MHz. During startup, the oscillator starts at a slower frequency, then as the output voltage rises, the frequency is increased to the nominal operating frequency. The switch-over point occurs when the FB pin voltage exceeds 0.6 V. Above 0.6 V, the oscillator remains at a nominal 1.25 MHz.

A signal derived from the oscillator ramp is used to develop slope compensation for PWM control.

DETAILED DESCRIPTION (continued)

Soft-Start

During power-on, the TPS40222 slowly increases the voltage to the non-inverting input to the error amplifier. In this way, the TPS40222 slowly ramps up the output voltage until the voltage on the non-inverting input to the error amplifier reaches 0.8 V. At that time, the voltage at the non-inverting input to the error amplifier remains at 0.8 V.

Upon startup, the time for the voltage on the non-inverting input of the error amplifier to reach 0.8 V is approximately 550 µs. The rate of rise of the voltage on the output of a TPS40222 is determined by the resistive divider network that sets the converter output voltage.

For example, the rate of rise of the internal soft-start is:

$$\frac{V_{REF}}{t_{SS}} = \frac{0.8\ V}{550\ \mu s} \quad (1)$$

where

- t_{SS} in the example is the typical soft-start time of 550 µs

For a 1.2-V output converter, the rate of rise observed at the output is:

$$\frac{V_{OUT}}{t_{SS}} = \frac{1.2\ V}{550\ \mu s} \quad (2)$$

Output Short-Circuit Protection

Current fault (short-circuit) protection is provided by sensing the current through the switching MOSFET while it is in the ON state and comparing with a preset internal level. If the current exceeds this level, the switching pulse width is limited causing the output voltage to decay. As the output voltage decays, the operating frequency is also decreased, thereby reducing power dissipation.

If the fault condition persists, and the output voltage continues to decay, then a watchdog circuit discharges the internal soft-start capacitor, effectively shutting off the converter. When this interval is completed, the converter then attempts to restart.

Bootstrap

To drive the internal N-channel MOSFET, a bootstrap, or boost circuit, is added to provide a voltage source higher than the input voltage of sufficient energy to fully enhance the MOSFET each switching cycle. During the freewheeling portion of the switching cycle (refer to Figure 9), the internal MOSFET is off, and the voltage at the SW node is clamped to just below ground by D1. At this time the input voltage (less the drop of the internal BOOST diode) is impressed upon C2, allowing it to charge. When the internal MOSFET is commanded to turn ON, the SW node rises towards V_{IN}, and the voltage on the BOOST pin rises to approximately $2 \times V_{IN}$. This voltage is used to further turn on the internal MOSFET for the remainder of the switching cycle.

APPLICATION INFORMATION

Typical Application

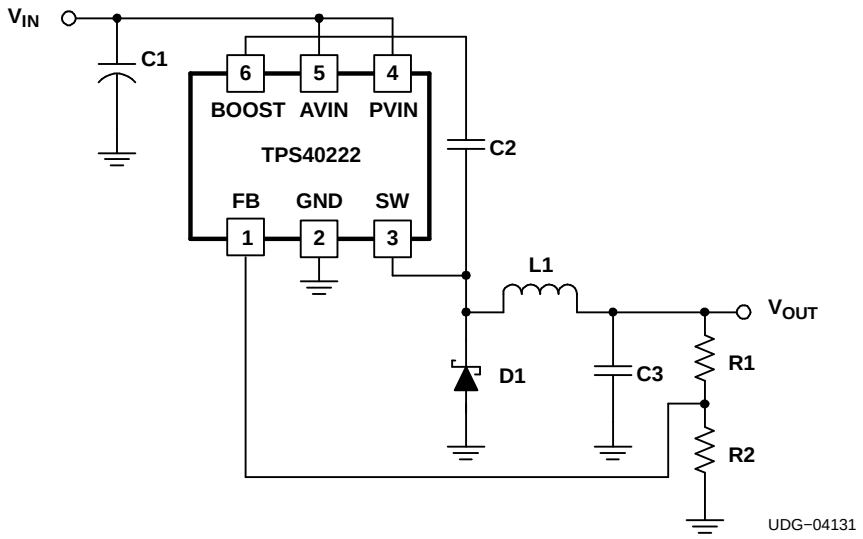


Figure 9. Typical Application

Voltage Setting

The output voltage may be set by knowing that the feedback voltage is 0.8 V and using Equation 3. To determine an output voltage, choose a convenient resistor value for R2 and calculate R1.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) \quad (3)$$

Output Filter (L1 and C3)

Since the loop compensation is internally fixed and cannot be changed, loop stability can only be controlled by the proper choice of output inductance and capacitance. Table 2 provides a shortcut guide to this selection and recommended capacitance to maintain a safe 50 degrees of phase margin for various inductors and output voltages. The table also shows the minimum capacitance for 50 degress of phase margin at three temperatures, with the worst case for stability at -40°C. The granularity of the table is sufficient so the user can interpolate between values to find a specific operating condition. The table values assume a full load, which is also the worst case for phase compensation. As an example of using the table, consider a 2.5-V output converter with a 2.2-µH inductor. The table shows that a minimum of 15-µF of output capacitance is required to guarantee greater than 50 degress of phase margin at the worst case temperature of -40°C. With a lead capacitor (C_{LEAD}) added to the feedback as shown in Figure 10, this minimum capacitance increases to 26-µF and the closed-loop frequency increases by about 20%.

APPLICATION INFORMATION (continued)

Table 2. Capacitor Selection(1)

INDUCTOR VALUE (µH)	5-V_{IN} RIPPLE CURRENT (mA)	C_{MIN} (µF) (PM > 50° at -40°C)	f_C (kHz) T_J = -40°C	f_C(kHz) T_J = 25°C	f_C(kHz) T_J = 125°C	C_{LEAD} VALUE (pF)
OUTPUT VOLTAGE V_{OUT} = 3.3 V						
1.8	Not Recommended(2)					
2.2	340	9	125	101	68	omitted
		21	285	247	92	270
3.3	230	12	98	77	52	omitted
		28	144	112	67	330
4.7	160	15	80	62	41	omitted
		38	111	85	52	470
5.6	140	16	74	58	38	omitted
		40	103	79	47	470
OUTPUT VOLTAGE V_{OUT} = 2.5 V						
1.8	550	13	116	93	63	omitted
		23	169	133	81	330
2.2	370	15	102	81	54	omitted
		26	147	114	65	330
3.3	300	17	91	71	48	omitted
		28	134	102	56	270
4.7	210	20	78	61	41	omitted
		38	106	81	47	470
5.6	180	23	68	53	35	omitted
		34	106	79	43	330
OUTPUT VOLTAGE V_{OUT} = 1.8 V						
1.8	580	20	105	84	56	omitted
		30	137	109	68	470
2.2	470	21	100	80	54	omitted
		32	129	101	62	470
3.3	320	25	86	67	45	omitted
		35	115	88	53	470
4.7	220	30	72	56	37	omitted
		39	99	75	44	470
5.6	190	33	65	51	34	omitted
		40	94	71	41	470
OUTPUT VOLTAGE V_{OUT} = 0.8 V						
1.8	470	50	94	75	50	n/a
2.2	390	52	91	72	48	
3.3	260	60	79	62	42	
4.7	180	70	68	53	36	
5.6	150	75	63	49	33	

(1) See Figure 10.
(2) For V_{OUT} > 3.3 V use an inductor with a value greater than or equal to 2.2 µH.

Output Stage Component Selection

In most applications, the user starts with a known output voltage and current load requirement as shown in Figure 10.

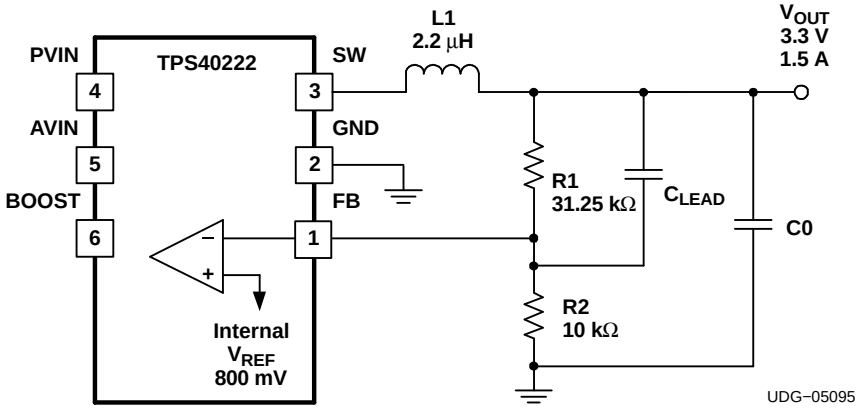


Figure 10. Output Stage

As shown in Figure 10, the trimmed reference voltage is internally connected to the error amplifier. Since the input bias current to this error amplifier is negligible. The feedback resistors R1 and R2 can be selected over a broad range limited by the low bias current into the error amplifier. With this restriction in mind, R2 was selected at 10 kΩ, so its current is 80 µA and large relative to the bias current of the error amplifier. The output voltage is then given by Equation 4.

$$V_{OUT} = 0.8 \times \left(1 + \frac{R1}{R2}\right) = 3.3\ V \tag{4}$$

where

- R1 = 31.25 kΩ
- R2 = 10 kΩ

Inductor Selection

This device's high-frequency internal clock enables the use of smaller, less expensive inductors. Ferrite, with its good high frequency properties, is the material of choice. Several manufacturers provide catalogs with inductor saturation currents, inductance values, and LSRs (internal resistance) for their various sized ferrites. For a 3.3-V, 1.5 A application, the inductor's saturation current must be higher than the maximum output current plus ½ the ripple current. The inductor value sets the ripple current. A small inductor provides better transient response and is a smaller, less expensive part. Too low an inductor value, however, causes high ripple currents that cause high ripple voltage across the ESR of the output capacitance. A rule of thumb is to set high ripple current to be less than 30% of the output current. A first order calculation then gives:

$$L = \frac{\Delta V \times t_{ON}}{\Delta I} \tag{5}$$

where

- ΔV is the input voltage -(IR drops in the inductor and FET) - V_{OUT}
- ΔI is 30% of 1.5 A
- t_{ON} is the on time given by (V_{OUT} /(V_{IN}× f)) where f = 1.25 MHz

Under these conditions, L = 1.55 µH

Selecting a standard value 2.2-µH inductor, with an internal resistance of 32 mΩ, the peak current developed during the on time is 1.66 A. This value is safely below the device's built in overcurrent limit of 2.1 A.

Capacitor Selection

One constraint on the capacitance is the overshoot allowed by a sudden load change. The worst case for a transient load release occurs at the time when the inductor has just finished a t_{ON} pulse. At this point, the inductor is operating at maximum current. When the output load is suddenly removed, all of the inductor current must be absorbed by the output capacitance. With a typical output voltage overshoot requirement of 2% at 3.3-V, the minimum capacitance required to remain in specification is calculated using Equation 6.

$$\frac{1}{2} \times L_O \times \left(I_O\right)^2 \leq \frac{1}{2} C_O \left(V_{OS}{}^2 - V_O{}^2\right) \tag{6}$$

where

- V_{OS} is the maximum overshoot voltage
- L_O = 2.2 µH
- I_O = 1.5 A
- V_O = 3.3 V

Solving this relationship, the minimum required output capacitance C_O is 11-µF.

The other load transition extreme is from no load to full load that occurs just after a minimum on-time cycle has started. At this point, the controller has to support this load for the remainder of the cycle with a minimum of current available from the inductor. In this example, the minimum on-time with a 3.3-V output is 528 ns and the off-time is 800 ns minus 528 ns = 272 ns. Using the relationship shown in Equation 7;

$$C_{MIN} = \frac{I_O \times \Delta t}{\Delta V_{OUT}} = 6.1\ \mu F \tag{7}$$

where

- ΔV_{OUT} is a 2% specified output voltage droop
- I_O = 1.5 A
- Δt = 272 ns

Ceramic capacitors with a low ESR are used to achieve the lowest voltage ripple. For example, current 1206, 6.3-V capacitors that provide 22 µF and an ESR of 2 mΩ are available.

These component selection decisions influence the phase margin and hence the stability of the system. For example, raising the output capacitance reduces the system crossover frequency and raises phase margin. Figure 11 illustrates this in a curve that shows phase margin as a function of output capacitance for two widely different inductors. The curves show that beyond a certain point, added capacitance has limited benefit. This point can be exploited to avoid the expense of excessive output capacitance. The curves also show the advantage of a lower inductance, where only 20-µF of output capacitance is required to obtain 60 degrees of phase margin.

The output voltage affects the phase margin by changing the equivalent output resistance to deliver full load. With a higher output voltage for example, there is a higher full-load resistance and a lower output capacitance is required for the same phase margin. An idea of this effect is illustrated in Figure 12 which plots the required minimum capacitance to achieve 50 degrees of phase margin at different output voltages. The curves also show the reduction in output capacitance that may be achieved with a lower inductor value.

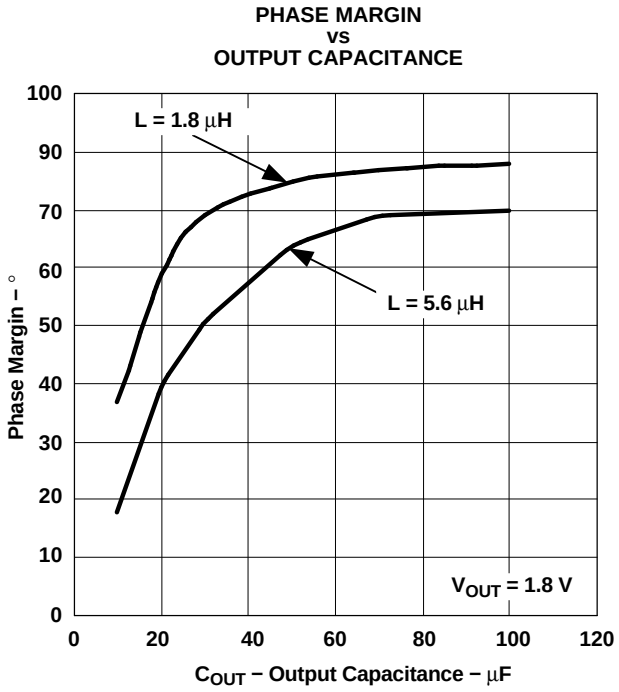


Figure 11.

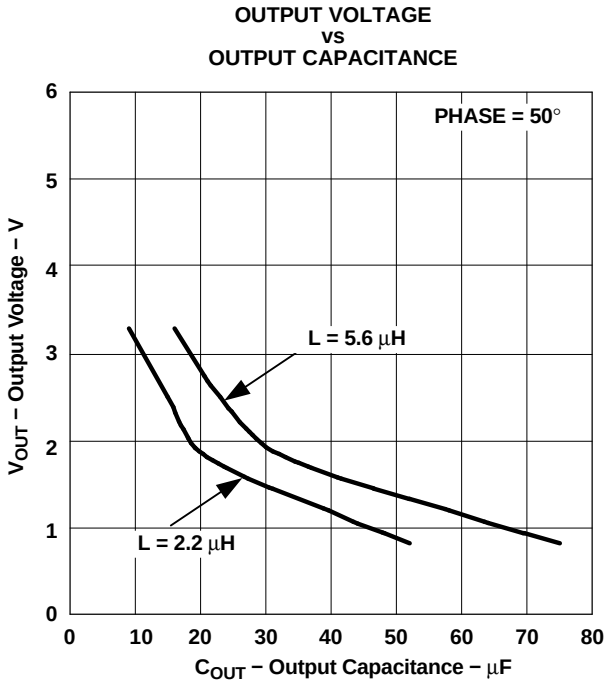


Figure 12.

A further improvement in reducing output capacitance is made by adding a lead capacitor across R1 of the feedback network. This lead capacitor can be determined by making its impedance equal to the resistance of R1 at the resonant frequency of the output L-C network. The lead capacitance is calculated using Equation 8.

$$C_{LEAD} = \frac{1}{2\pi \times f_R \times R} \quad (8)$$

The resonant frequency formed by the inductor and the output load capacitance is calculated in Equation 9.

$$f_R = \frac{1}{2\pi} \times \left(\frac{1}{L \times C_O}\right)^{\frac{1}{2}} \quad (9)$$

Catch Diode (D1)

The selection of the catch diode depends on the application current. Select a diode that has a low forward voltage drop, and a low junction capacitance. A diode with too high of a forward voltage drop or a diode with high junction capacitance result in a converter that has poor efficiency, as well as excessive ringing on the SW node and excessive output voltage noise.

Input Filter Capacitor (C1)

Select a good quality, low ESR ceramic capacitor to bypass the input. For a conservative design, the capacitor should have a ripple current rating equal to the load current of the converter.

Boost Capacitor (C2)

The boost capacitor is sized to ensure there is enough energy available to turn on the internal MOSFET. For most applications, use a ceramic capacitor with a value between 33 nF and 100 nF.

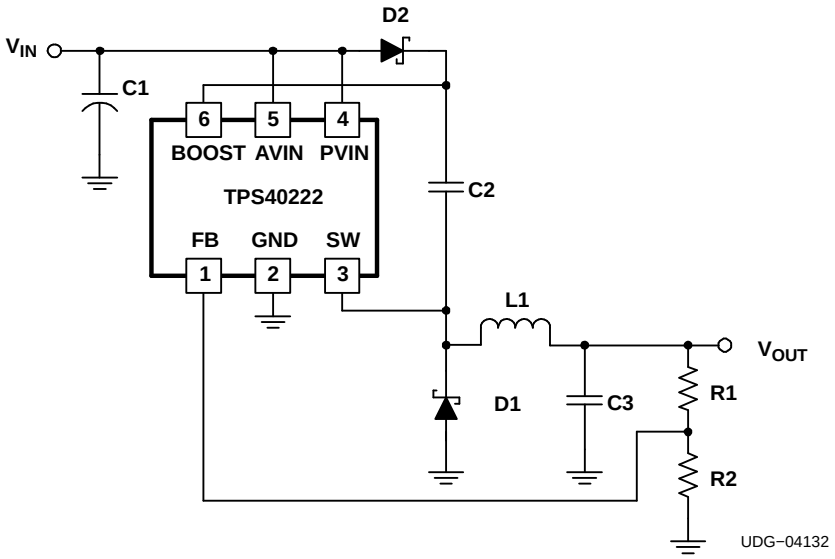


Figure 13. Using a Boost Diode

Boost Diode (D2)

For some applications, the internal bootstrap diode's voltage drop may be too high to sufficiently charge the boost capacitor each switching cycle. For these applications, a Schottky diode, D2 shown in Figure 13, may be added.

Output Preload Requirement

One of the requirements for proper startup of the DC-to-DC converter is that the boost capacitor, C2, has sufficient voltage across it before switching occurs. In some applications, notably those with output voltages of 3.3 V, and those with slowly rising or low input voltages, there is the need to add a small 10 mA, pre-load to the converter to hold the SW node to GND before switching begins. Without a pre-load, the output voltage may not reach regulation. In addition, the pre-load prevents the output from overshooting too much when the load is stepped from a high value to zero.

AVIN Filtering

Some applications may require the addition of an R-C filter on the input of AVIN to filter unwanted noise and improve load regulation. (See Figure 14) Use R4=10 Ω and C5=1 µF. Connect the ground side of C5 as close as possible to the GND pin of the device.

SW Node Snubber

To attenuate excessive ringing at the SW node, an R-C network may be added across D1. (See Figure 14)

Use R3=10 Ω and C4=680 pF as a starting point. Decrease C4 until the minimum capacitance is found for the desired ringing attenuation.

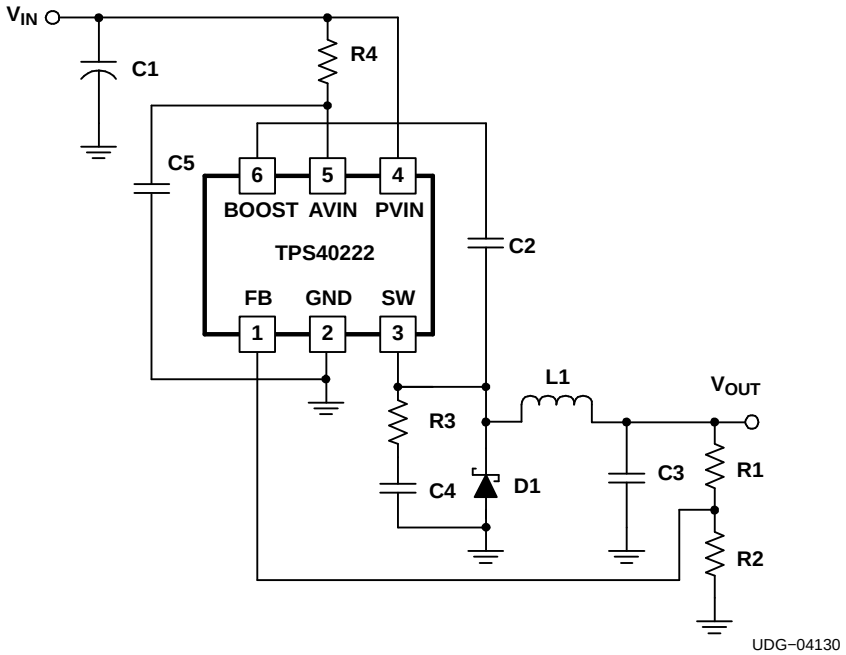


Figure 14. AVIN Filter and SW Node Snubber

Application Circuit Schematic

Figure 15 shows an example of an application incorporating a TPS40222 in a 1.2-V output DC-to-DC converter. Notice the use of parallel capacitors at the input and the output to reduce the effective ESR of the capacitance.

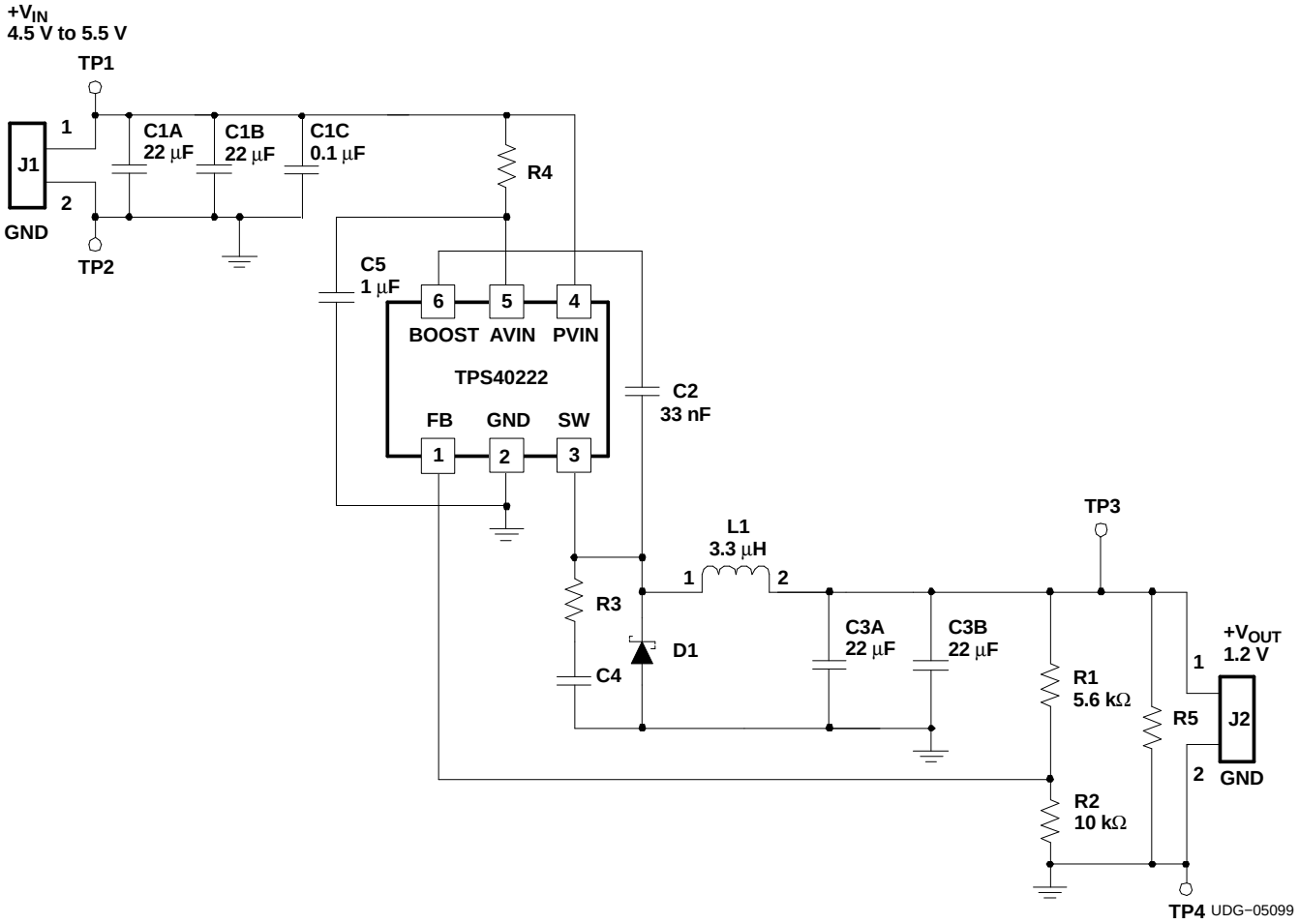


Figure 15. 5-V_{IN}, 1.2 V_{OUT} DC-to-DC Converter

Table 3. List of Materials

REFERENCE DESIGNATOR	QTY	DESCRIPTION	VENDOR PART NUMBER	VENDOR	NOTES
C1A, C1B	2	Capacitor, 22 µF ceramic, 1206			Input bypass
C1D	1	Capacitor, 0.1 µF ceramic, 0805			High-frequency bypass, mount near V_{CC}
C2	1	Capacitor, 33 nF ceramic, 0805			Bootstrap
C3A, C3B	2	Capacitor, 22 µF ceramic, 1206			Output capacitors
C4	1	Capacitor, 680 pF ceramic, 0805			Snubber (optional - open if not used)
C5	1	Capacitor, 1 µF ceramic, 0805			Device input voltage filter capacitor
D1	1	Diode, Schottky, 1 A	RSX501L-20	ROHM	Catch diode
L1	1	Inductor, 3.3 µH	ELL6PV3R3N	Panasonic	Filter inductor
R1	1	Resistor, 5620 Ω, 1%, SMD, 0603			Voltage setting resistor
R2	1	Resistor, 10 kΩ, 1%, SMD, 0603			Voltage setting resistor
R3	1	Resistor, 10 Ω, 10%, SMD, 0805			Snubber (optional - open if not used)
R4	1	Resistor, 10 Ω, 10%, SMD, 0603			Device input voltage filter (optional - short if not used)
R5	1	Resistor, 120 Ω, 10%, SMD, 0805			Output pre-load (optional - open if not used)
U1	1	PWM converter device	TPS40222	Texas Instruments	

APPLICATION CURVES

OUTPUT VOLTAGE vs INPUT VOLTAGE AT LOAD CURRENT

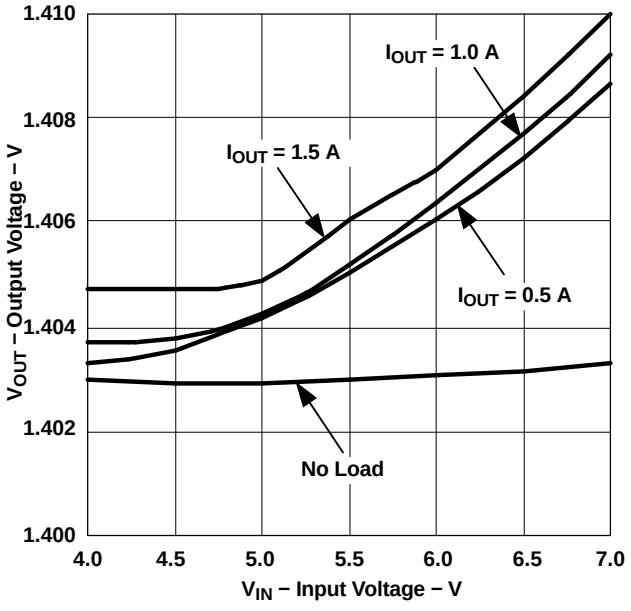


Figure 16.

EFFICIENCY vs LOAD CURRENT

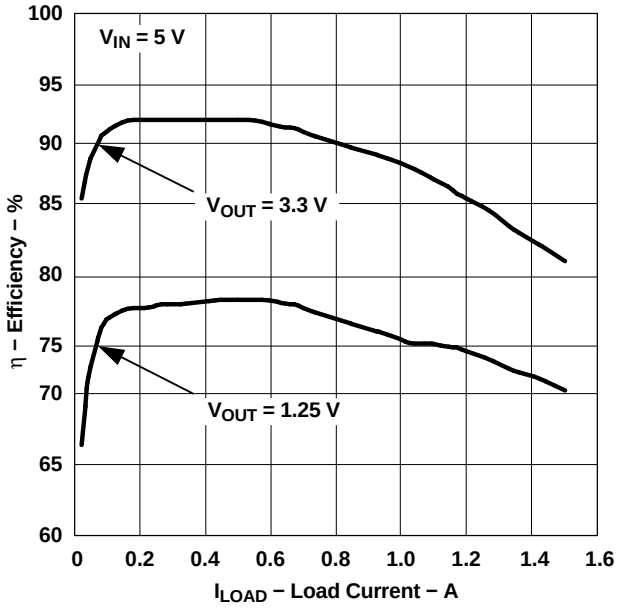


Figure 17.

TYPICAL CHARACTERISTICS

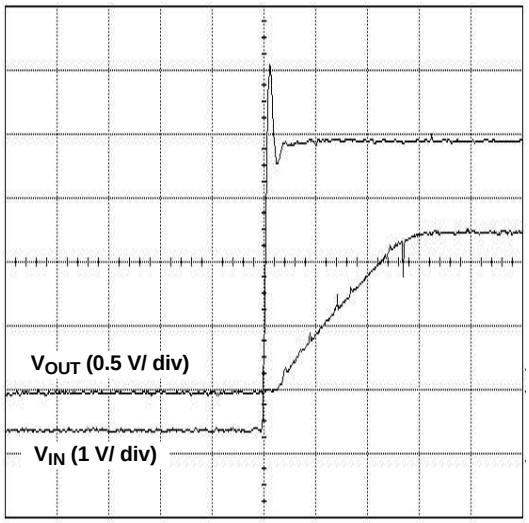


Figure 18. Startup Waveform

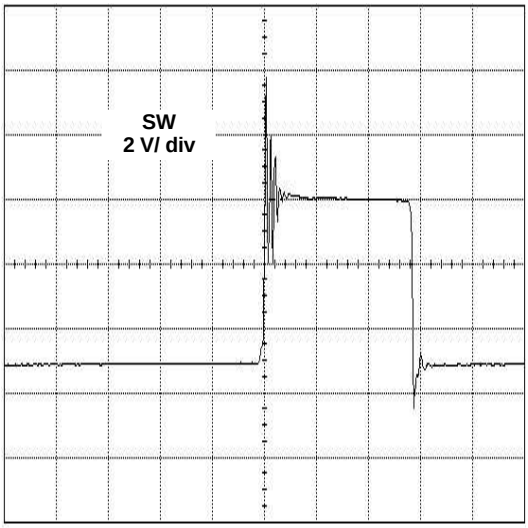


Figure 19. SW Node Waveform

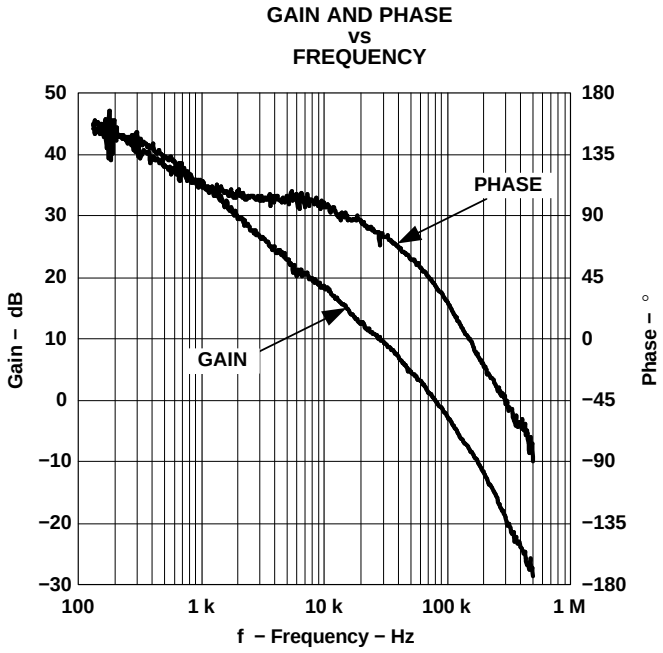


Figure 20.

PC BOARD LAYOUT RECOMMENDATIONS

Device Pad Design

The 6-pin package has an exposed thermal pad intended to help conduct heat out of the package, allowing a higher than otherwise available operating ambient temperature. Place three vias within the pad area, tying them to an analog ground plane.

PCB Layout

When designing a DC-to-DC converter layout, care must be taken to ensure a noise-free design.

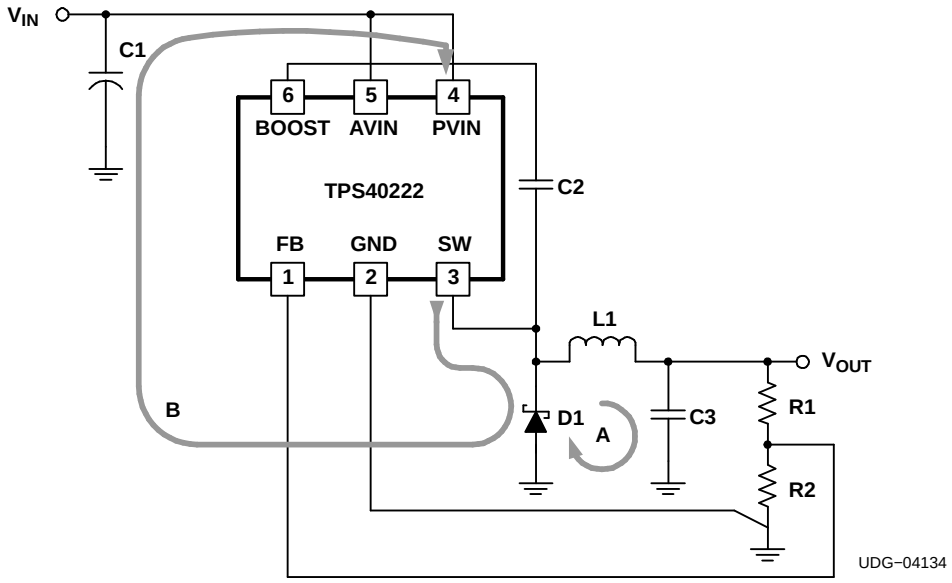


Figure 21. Ensuring a Noise-Free Layout

- AC current loops must be kept as short as possible. The input loop B (C1-U1-D1) in the figure must be kept short to ensure proper filtering by C1 for the device. Excessive high frequency noise on AVIN during switching could degrade overall regulation as the load increases. In order to reduce noise spikes seen by the device, an R-C filter is recommended (see *AVIN Filtering* in the *APPLICATION INFORMATION* section) and a snubber may be added (see *SW Node Snubber* in the *APPLICATION INFORMATION* section).
- The output loop A (D1-L1-C3) should also be kept as small as possible. Noise performance at the output of the converter suffers if the loop area is too large.
- It is recommended that traces carrying large AC currents NOT be connected through a ground plane. Instead, use PCB traces on the top layer to conduct the AC current and use the ground plane as a noise shield. Split the ground plane as necessary to keep noise away from the TPS40222 and noise sensitive areas (R1, R2).
- Keep the SW node as physically small as possible to minimize parasitic capacitance and to minimize radiated emissions
- For good output voltage regulation, R1 should be connected close to the load. The R2-TPS40222 (GND) connection should be tied close to the load as well.
- The trace from the R1-R2 junction to the TPS40222 should be kept away from any noise source, such as the SW node, or the boost circuitry.
- The GND pin and the thermal pad of the TPS40222 should be connected together under the device as indicated in the pad design section. For good thermal conductivity, VIAs directly under the device should connect the thermal pad to a ground plane on the other side of the board.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS40222DRPR	Active	Production	VSON (DRP) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	0222
TPS40222DRPR.A	Active	Production	VSON (DRP) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	0222
TPS40222DRPRG4	Active	Production	VSON (DRP) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	0222
TPS40222DRPT	Active	Production	VSON (DRP) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	0222
TPS40222DRPT.A	Active	Production	VSON (DRP) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	0222
TPS40222DRPTG4	Active	Production	VSON (DRP) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	0222
TPS40222DRPTG4.A	Active	Production	VSON (DRP) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	0222

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

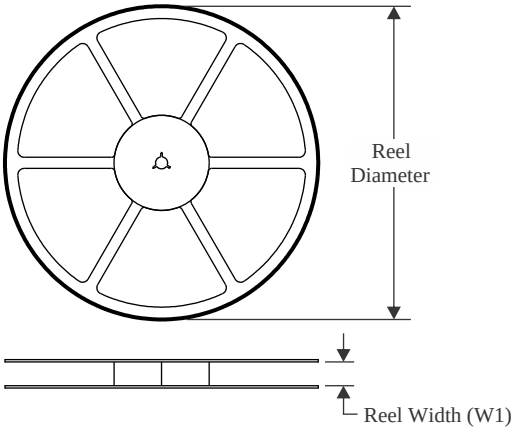
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

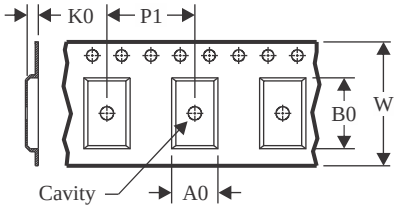
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

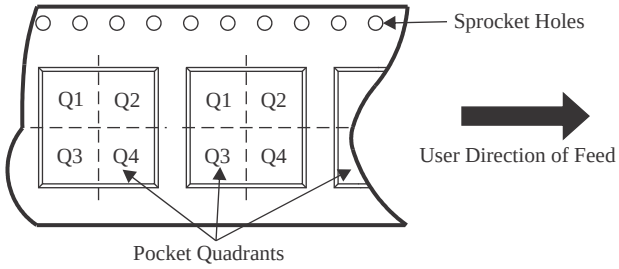


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

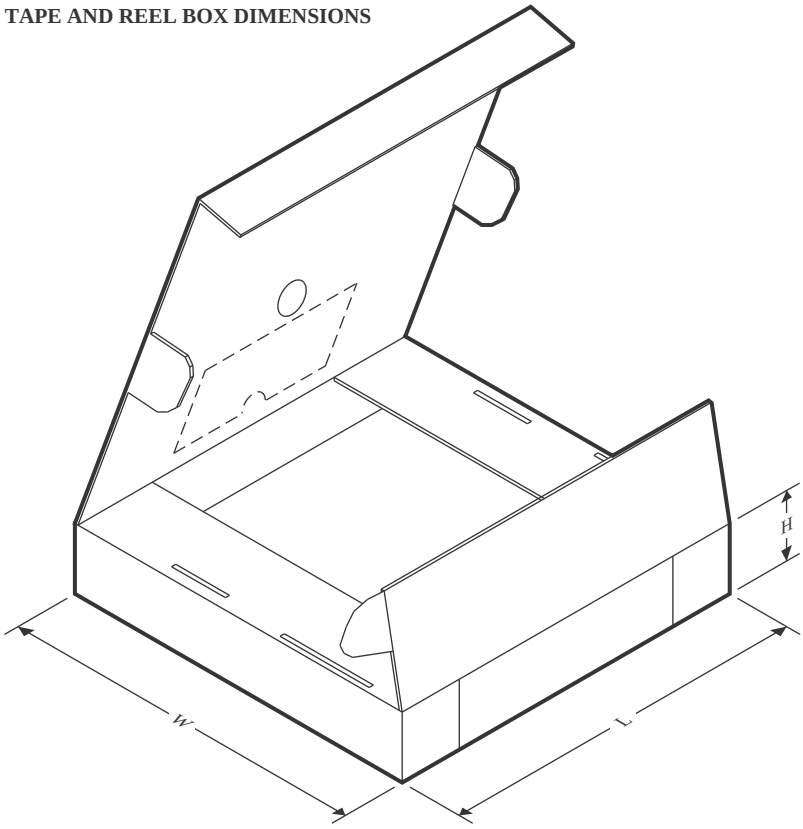
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS40222DRPR	VSON	DRP	6	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS40222DRPT	VSON	DRP	6	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS40222DRPTG4	VSON	DRP	6	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

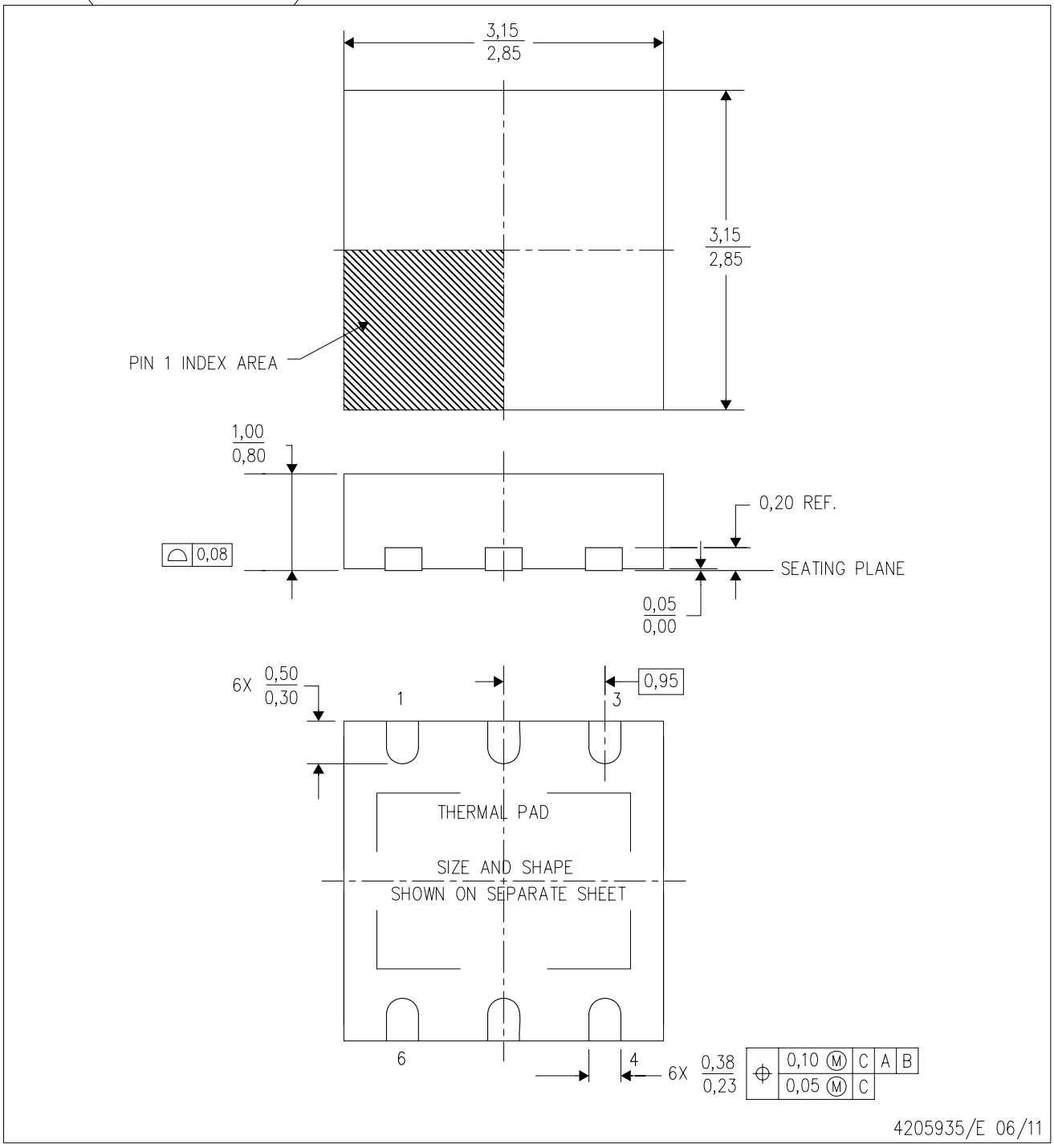
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS40222DRPR	VSON	DRP	6	3000	346.0	346.0	33.0
TPS40222DRPT	VSON	DRP	6	250	210.0	185.0	35.0
TPS40222DRPTG4	VSON	DRP	6	250	210.0	185.0	35.0

DRP (S–PVSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

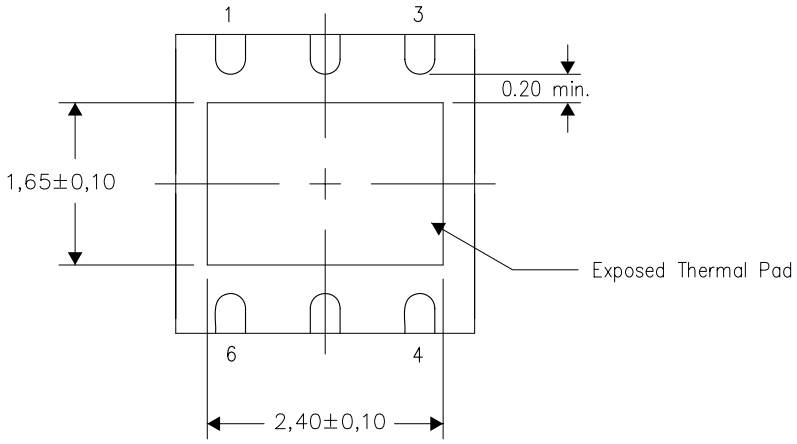
DRP (S–PVSON–N6) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



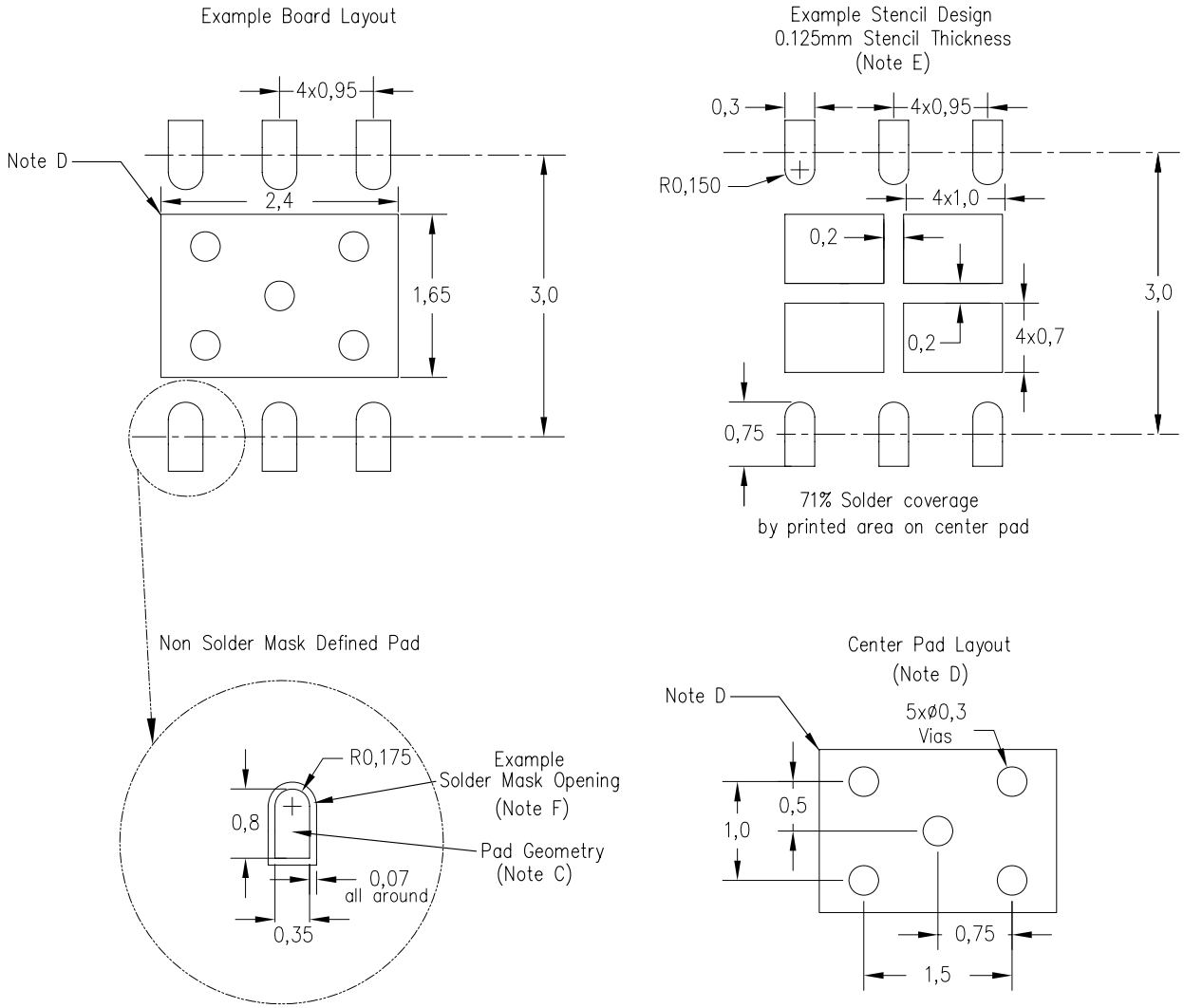
Bottom View

Exposed Thermal Pad Dimensions

4207637/G 06/11

NOTE: All linear dimensions are in millimeters

DRP (S–PVSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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