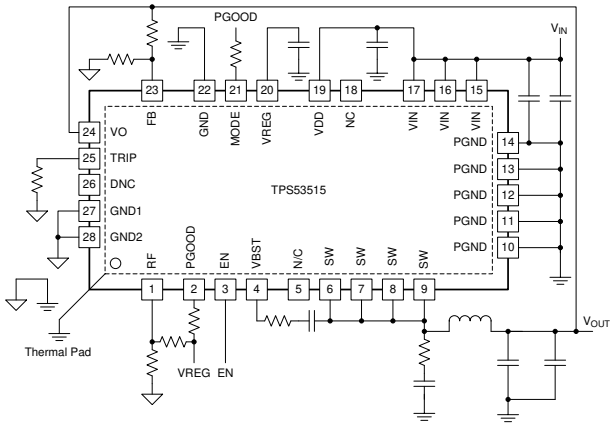
# TPS53515 1.5V to 18V (4.5V to 25V Bias) Input, 12A Single Synchronous Step-Down SWIFT™ Converter

## 1 Features

- Integrated 13.8mΩ and 5.9mΩ MOSFETs with 12A continuous output current
- Supports all ceramic output capacitors
- Reference voltage 600mV ±0.5% tolerance
- Output voltage range: 0.6V to 5.5V
- D-CAP3™ control mode with fast load-step response
- Auto-skipping Eco-mode™ for high light-load efficiency
- FCCM for tight output ripple and voltage requirements
- Eight selectable frequency settings from 250kHz to 1MHz
- Precharged start-up capability
- Built-in output discharge circuit
- Open-drain power-good output
- 3.5mm × 4.5mm, 28-pin, VQFN-CLIP package

## 2 Applications

- Server and cloud-computing POLs
- Broadband, networking, and optical communications infrastructure
- I/O supplies
- Supported at the WEBENCH® Design Center




**Simplified Schematic**

## 3 Description

The TPS53515 device is a small-sized, synchronous buck converter with an adaptive on-time D-CAP3 control mode. The device offers ease-of-use and low external-component count for space-conscious power systems.

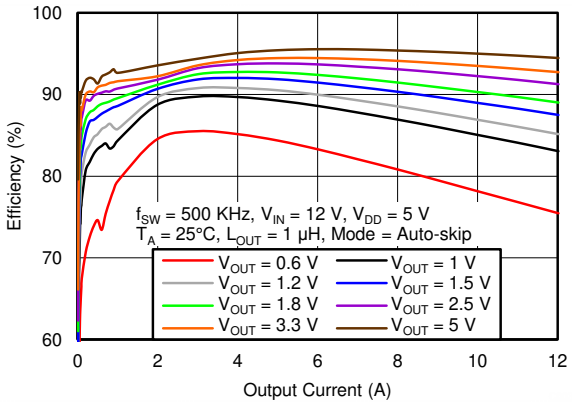
This device features high-performance integrated MOSFETs, accurate 0.5% 0.6V reference, and an integrated boost switch. Competitive features include very low external-component count, fast load-transient response, auto-skip mode operation, internal soft-start control, and no requirement for compensation.

A forced continuous conduction mode helps meet tight voltage regulation accuracy requirements for performance DSPs and FPGAs. The TPS53515 device is available in a 28-pin VQFN-CLIP package and is specified from –40°C to 85°C ambient temperature.

**Package Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) |
|---|---|---|
| TPS53515 | RVE (VQFN-CLIP, 28) | 4.50mm × 3.50mm |

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.




**Efficiency**

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# 4 Pin Configuration and Functions

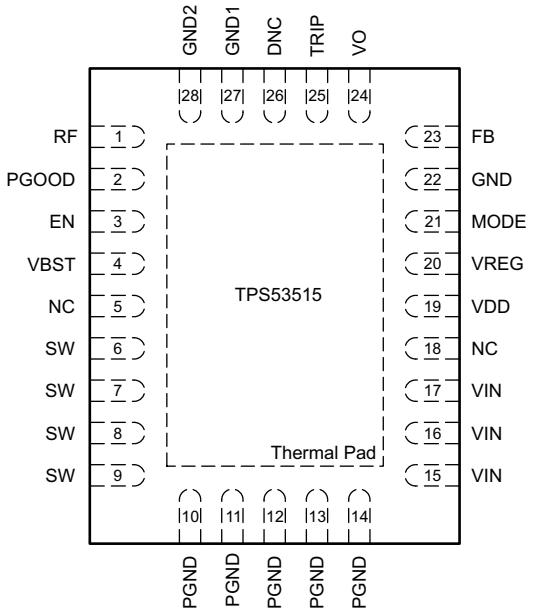



**Figure 4-1. RVE Package 28-Pin VQFN-CLIP Top View**

**Table 4-1. Pin Functions**

| PIN | | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| DNC | 26 | O | Do not connect. This pin is the output of unused internal circuitry and must be floating. |
| EN | 3 | I | The enable pin turns on the DC-DC switching converter. |
| FB | 23 | I | $V_{OUT}$ feedback input. Connect this pin to a resistor divider between the VOUT pin and GND. |
| GND | 22 | G | This pin is the ground of internal analog circuitry and driver circuitry. Connect GND to the PGND plane with a short trace (For example, connect this pin to the thermal pad with a single trace and connect the thermal pad to PGND pins and PGND plane). |
| GND1 | 27 | I | Connect this pin to ground. GND1 is the input of unused internal circuitry and must connect to ground. |
| GND2 | 28 | I | Connect this pin to ground. GND2 is the input of unused internal circuitry and must connect to ground. |
| MODE | 21 | I | The MODE pin sets the forced continuous-conduction mode (FCCM) or Skip-mode operation. The MODE pin also selects the ramp coefficient of D-CAP3 control mode. |
| NC | 5 | — | Not connected. These pins are floating internally. |
| | 18 | | |
| PGND | 10 | G | These ground pins are connected to the return of the internal low-side MOSFET. |
| | 11 | | |
| | 12 | | |
| | 13 | | |
| | 14 | | |
| PGOOD | 2 | O | Open-drain power-good status signal which provides startup delay after the FB voltage falls within the specified limits. After the FB voltage moves outside the specified limits, PGOOD goes low within 2µs. |
| RF | 1 | I | RF is the SW-frequency configuration pin. Connect this pin to a resistor divider between VREG and GND to program different SW frequency settings. |

**Table 4-1. Pin Functions (continued)**

| PIN | | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| SW | 6 | I/O | SW is the output switching terminal of the power converter. Connect this pin to the output inductor. |
| | 7 | | |
| | 8 | | |
| | 9 | | |
| TRIP | 25 | I/O | TRIP is the OCL detection threshold setting pin. $I_{TRIP}$ = 10µA at room temp, 3000ppm/°C current is sourced and sets the OCL trip voltage. See *Current Sense and Overcurrent Protection* for detailed OCP setting. |
| VBST | 4 | P | VBST is the supply rail for the high-side gate driver (boost terminal). Connect the bootstrap capacitor from this pin to the SW node. Internally connected to VREG through the bootstrap PMOS switch. |
| VDD | 19 | P | Power-supply input pin for controller. Input of the VREG LDO. The input range is from 4.5 to 25V. |
| VIN | 15 | P | VIN is the conversion power-supply input pins. |
| | 16 | | |
| | 17 | | |
| VREG | 20 | O | VREG is the 5V LDO output. This voltage supplies the internal circuitry and gate driver. |
| VO | 24 | I | VOUT voltage input to the controller |

(1) I = Input, O = Output, P = Supply, G = Ground

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| Input voltage range(2) | EN | | –0.3 | 7.7 | V |
| | SW | DC | –3 | 30 | |
| | | Transient < 10ns | –5 | 32 | |
| | VBST | | –0.3 | 36 | |
| | VBST(3) | | –0.3 | 6 | |
| | VBST when transient < 10ns | | | 38 | |
| | VDD | | –0.3 | 28 | |
| | VIN | | –0.3 | 30 | |
| | VIN-SW DC | | -3 | 30 | |
| | VIN-SW < 10ns transient | | -5 | 32 | |
| | VO, FB, MODE, RF | | –0.3 | 6 | |
| Output voltage range | PGOOD | | –0.3 | 7.7 | V |
| | VREG, TRIP | | –0.3 | 6 | |
| Junction temperature, $T_J$ | | | –40 | 150 | °C |
| Storage temperature, $T_{stg}$ | | | –55 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommnded Oeprating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground terminal.
(3) Voltage values are with respect to the SW terminal.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2500 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22C101(2) | ±1500 | |

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Input voltage | EN | –0.1 | 7 | V |
| | SW | –3 | 27 | |
| | VBST | –0.1 | 28 | |
| | VBST(1) | –0.1 | 5.5 | |
| | VDD | 4.5 | 25 | |
| | VIN | 1.5 | 18 | |
| | VO, FB, MODE, RF | –0.1 | 5.5 | |
| Output voltage | PGOOD | –0.1 | 7 | V |
| | VREG, TRIP | –0.1 | 5.5 | |
| Operating free-air temperature, $T_A$ | | –40 | 85 | °C |

(1) Voltage values are with respect to the SW pin.

## 5.4 Thermal Information

| THERMAL METRIC[1] | | TPS53515 RVE (VQFN-CLIP) 28 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 37.5 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 34.1 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 18.1 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 1.8 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 18.1 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 2.2 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

## 5.5 Electrical Characteristics

over operating free-air temperature range, VREG = 5V, EN = 5V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY CURRENT** | | | | | | |
| $I_{VDD}$ | VDD bias current | $T_A$ = 25°C, No load<br>Power conversion enabled (no switching) | | 1350 | 1850 | µA |
| $I_{VDDSTBY}$ | VDD standby current | $T_A$ = 25°C, No load<br>Power conversion disabled | | 850 | 1150 | µA |
| $I_{VIN(leak)}$ | VIN leakage current | $V_{EN}$ = 0V | | | 0.5 | µA |
| **VREF OUTPUT** | | | | | | |
| $V_{VREF}$ | Reference voltage | FB w/r/t GND, $T_A$ = 25°C | 597 | 600 | 603 | mV |
| $V_{VREFTOL}$ | Reference voltage tolerance | FB w/r/t GND, 0°C ≤ $T_J$ ≤ 85°C | –0.6% | | 0.5% | |
| | | FB w/r/t GND, =–40°C ≤ $T_J$ ≤ 85°C | –0.7% | | 0.5% | |
| **OUTPUT VOLTAGE** | | | | | | |
| $I_{FB}$ | FB input current | $V_{FB}$ = 600mV | | 50 | 100 | nA |
| $I_{VODIS}$ | VO discharge current | $V_{VO}$ = 0.5V, Power Conversion Disabled | 10 | 12 | 15 | mA |
| **SMPS FREQUENCY** | | | | | | |
| $f_{SW}$ | VO switching frequency(2) | $V_{IN}$ = 12V, $V_{VO}$ = 3.3V, $R_{DR}$ < 0.041 | | 250 | | kHz |
| | | $V_{IN}$ = 12V, $V_{VO}$ = 3.3V, $R_{DR}$ = 0.096 | | 300 | | |
| | | $V_{IN}$ = 12V, $V_{VO}$ = 3.3V, $R_{DR}$ = 0.16 | | 400 | | |
| | | $V_{IN}$ = 12V, $V_{VO}$ = 3.3V, $R_{DR}$ = 0.229 | | 500 | | |
| | | $V_{IN}$ = 12V, $V_{VO}$ = 3.3V, $R_{DR}$ = 0.297 | | 600 | | |
| | | $V_{IN}$ = 12V, $V_{VO}$ = 3.3V, $R_{DR}$ = 0.375 | | 750 | | |
| | | $V_{IN}$ = 12V, $V_{VO}$ = 3.3V, $R_{DR}$ = 0.461 | | 850 | | |
| | | $V_{IN}$ = 12V, $V_{VO}$ = 3.3V, $R_{DR}$ > 0.557 | | 1000 | | |
| $t_{ON(min)}$ | Minimum on-time | $T_A$ = 25°C(1) | | 60 | | ns |
| $t_{OFF(min)}$ | Minimum off-time | $T_A$ = 25°C | 175 | 240 | 310 | ns |
| **INTERNAL BOOTSTRAP SW** | | | | | | |
| $V_F$ | Forward Voltage | $V_{VREG–VBST}$, $T_A$ = 25°C, $I_F$ = 10mA | | 0.15 | 0.25 | V |
| $I_{VBST}$ | VBST leakage current | $T_A$ = 25°C, $V_{VBST}$ = 33V, $V_{SW}$ = 28V | | 0.01 | 1.5 | µA |
| **LOGIC THRESHOLD** | | | | | | |
| $V_{ENH}$ | EN enable threshold voltage | | 1.3 | 1.4 | 1.5 | V |
| $V_{ENL}$ | EN disable threshold voltage | | 1.1 | 1.2 | 1.3 | V |
| $V_{ENHYST}$ | EN hysteresis voltage | | | 0.22 | | V |
| $V_{ENLEAK}$ | EN input leakage current | | –1 | 0 | 1 | µA |
| **SOFT START** | | | | | | |
| $t_{SS}$ | Soft-start time | | | 1 | | ms |
| **PGOOD COMPARATOR** | | | | | | |
| $V_{PGTH}$ | VDDQ PGOOD threshold | PGOOD in from higher | 104% | 108% | 111% | |
| | | PGOOD in from lower | 89% | 92% | 96% | |
| | | PGOOD out to higher | 113% | 116% | 120% | |
| | | PGOOD out to lower | 80% | 84% | 87% | |
| $I_{PG}$ | PGOOD sink current | $V_{PGOOD}$ = 0.5V | 4 | 6 | | mA |
| $t_{PGDLY}$ | PGOOD delay time | Delay for PGOOD going in | 0.8 | 1.0 | 1.2 | ms |
| | | Delay for PGOOD coming out | | 2 | | µs |
| $I_{PGLK}$ | PGOOD leakage current | $V_{PGOOD}$ = 5V | –1 | 0 | 1 | µA |

## 5.5 Electrical Characteristics (continued)

over operating free-air temperature range, VREG = 5V, EN = 5V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **CURRENT DETECTION** | | | | | | |
| $R_{TRIP}$ | TRIP pin resistance range | | 20 | | 70 | kΩ |
| $I_{OCL}$ | Current limit threshold, valley | $R_{TRIP}$ = 52.3kΩ | 10.1 | 12 | 13.9 | A |
| | | $R_{TRIP}$ = 38kΩ | 7.2 | 9.1 | 11.0 | |
| $I_{OCLN}$ | Negative current limit threshold, valley | $R_{TRIP}$ = 52.3kΩ | –15.3 | –11.9 | –8.5 | A |
| | | $R_{TRIP}$ = 38kΩ | –12 | –9 | –6 | |
| $V_{ZC}$ | Zero cross detection offset | | | 0 | | mV |
| **PROTECTIONS** | | | | | | |
| $V_{VREGUVLO}$ | VREG undervoltage-lockout (UVLO) threshold voltage | Wake-up | 3.25 | 3.34 | 3.41 | V |
| | | Shutdown | 3.00 | 3.12 | 3.19 | |
| $V_{VDDUVLO}$ | VDD UVLO threshold voltage | Wake-up (default) | 4.15 | 4.25 | 4.35 | V |
| | | Shutdown | 3.95 | 4.05 | 4.15 | |
| $V_{OVP}$ | Overvoltage-protection (OVP) threshold voltage | OVP detect voltage | 116% | 120% | 124% | |
| $t_{OVPDLY}$ | OVP propagation delay | With 100mV overdrive | | 300 | | ns |
| $V_{UVP}$ | Undervoltage-protection (UVP) threshold voltage | UVP detect voltage | 64% | 68% | 71% | |
| $t_{UVPDLY}$ | UVP delay | UVP filter delay | | 1 | | ms |
| **THERMAL SHUTDOWN** | | | | | | |
| $T_{SDN}$ | Thermal shutdown threshold(1) | Shutdown temperature | | 140 | | °C |
| | | Hysteresis | | 40 | | |
| **LDO VOLTAGE** | | | | | | |
| $V_{REG}$ | LDO output voltage | $V_{IN}$ = 12V, $I_{LOAD}$ = 10mA | 4.65 | 5 | 5.45 | V |
| $V_{DOVREG}$ | LDO low droop drop-out voltage | $V_{IN}$ = 4.5V, $I_{LOAD}$ = 30mA, $T_A$ = 25°C | | | 365 | mV |
| $I_{LDOMAX}$ | LDO overcurrent limit | $V_{IN}$ = 12V, $T_A$ = 25°C | 170 | 200 | | mA |
| **INTERNAL MOSFETS** | | | | | | |
| $R_{DS(on)H}$ | High-side MOSFET on-resistance | $T_A$ = 25°C | | 13.8 | 15.5 | mΩ |
| $R_{DS(on)L}$ | Low-side MOSFET on-resistance | $T_A$ = 25°C | | 5.9 | 7.0 | mΩ |

(1) Specified by design. Not production tested.
(2) Resistor divider ratio ($R_{DR}$) is described in Equation 1.

## 5.6 Typical Characteristics

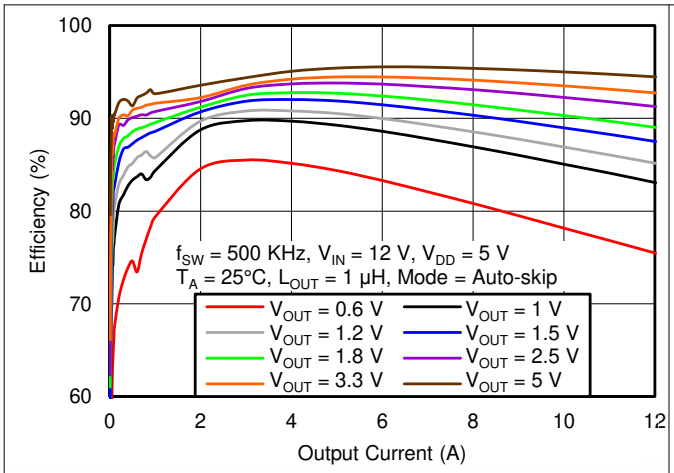



**Figure 5-1. Efficiency vs. Output Current**

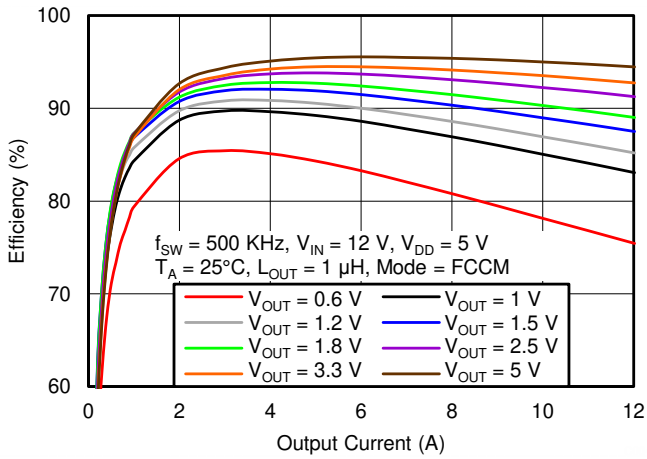



**Figure 5-2. Efficiency vs. Output Current**

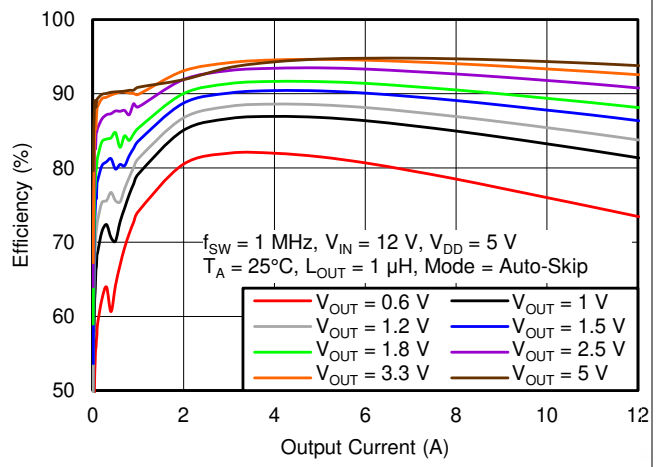



**Figure 5-3. Efficiency vs. Output Current**

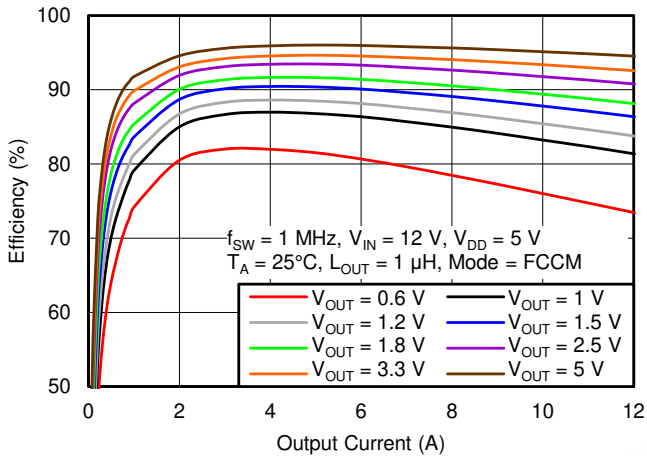



**Figure 5-4. Efficiency vs. Output Current**

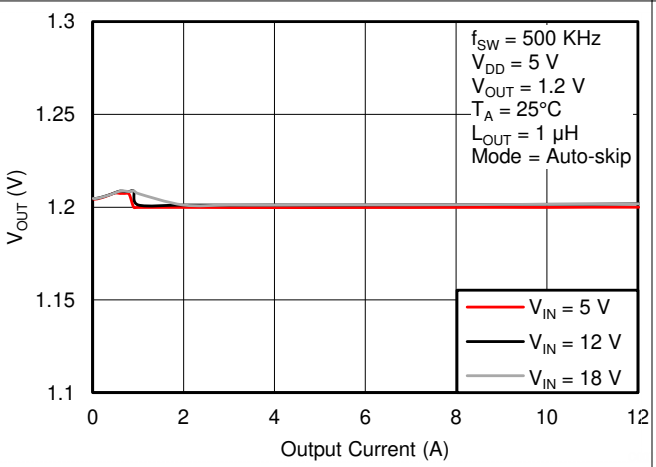



**Figure 5-5. Output Voltage vs. Output Current**

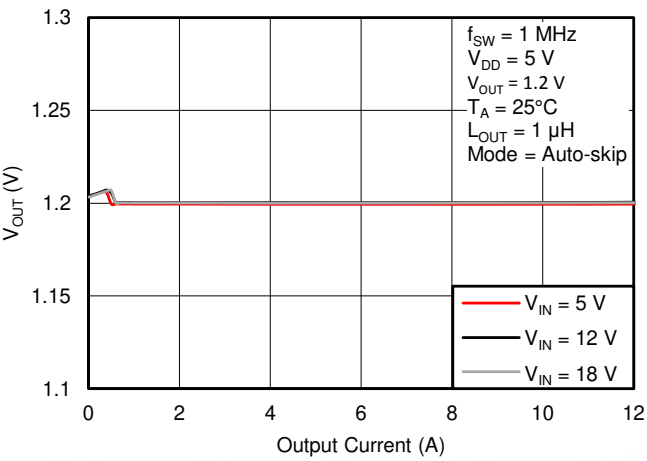



**Figure 5-6. Output Voltage vs. Output Current**

## 5.6 Typical Characteristics (continued)

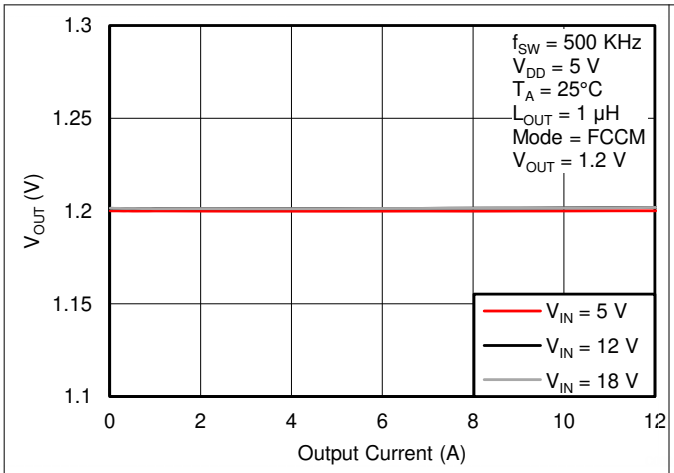



**Figure 5-7. Output Voltage vs. Output Current**

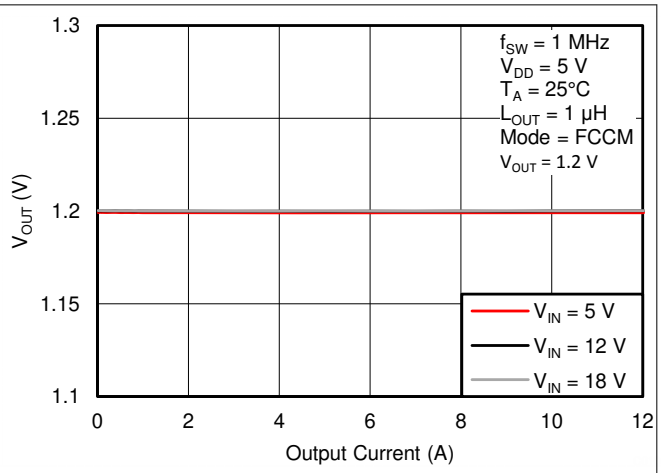



**Figure 5-8. Output Voltage vs. Output Current**

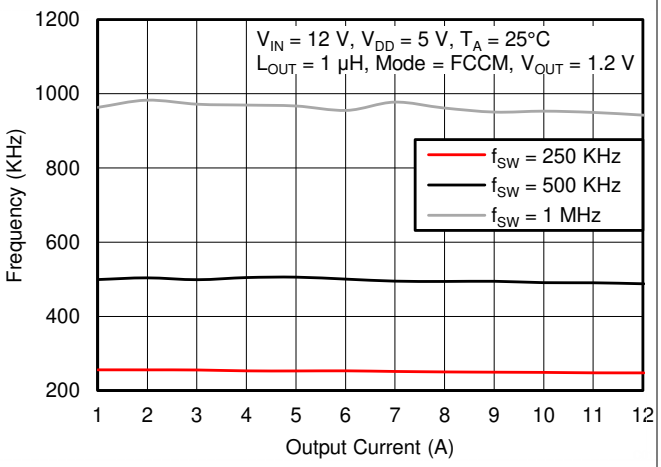



**Figure 5-9. Switching Frequency vs. Output Current**

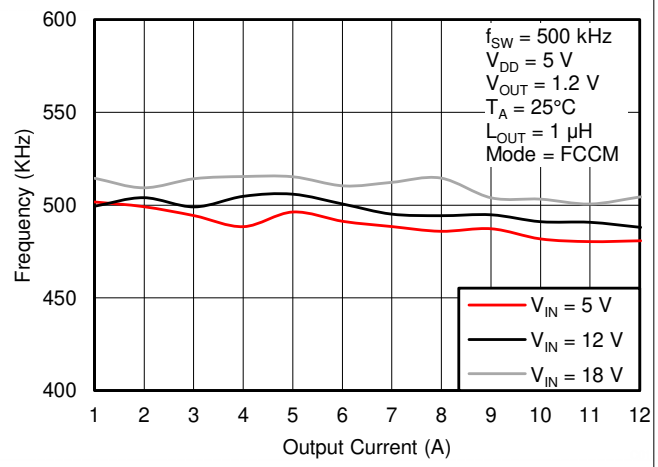



**Figure 5-10. Switching Frequency vs. Output Current**

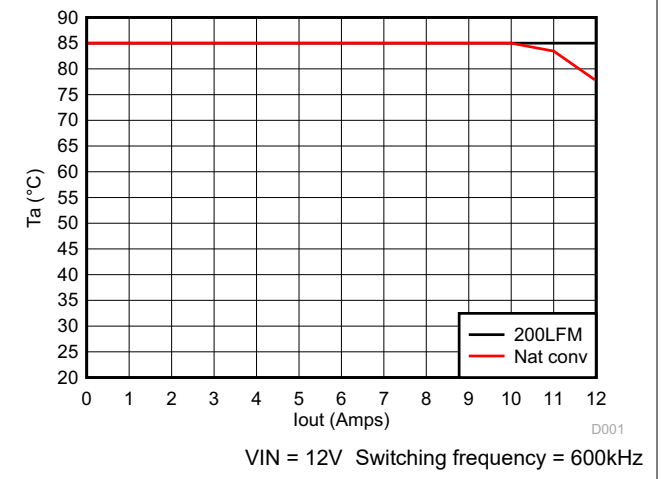



**Figure 5-11. Safe Operating Area, $V_O$ = 1.2V**

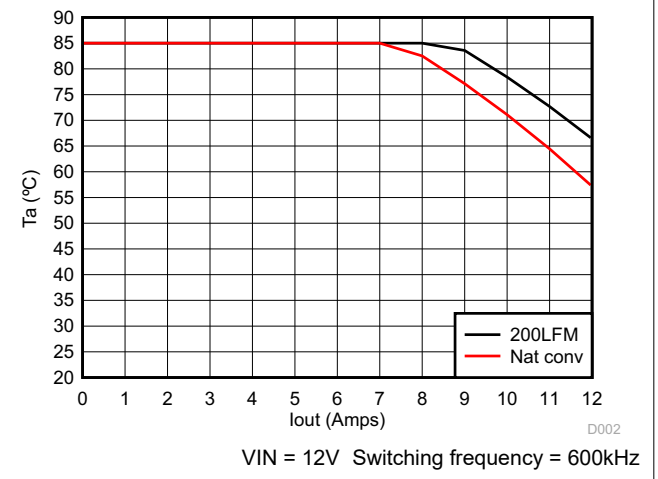



**Figure 5-12. Safe Operating Area, $V_O$ = 5V**

## 5.6 Typical Characteristics (continued)

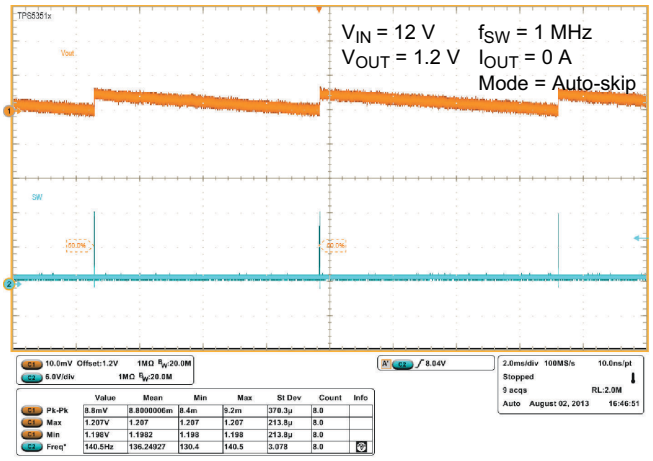



**Figure 5-13. Auto-Skip Mode Steady-State Operation**

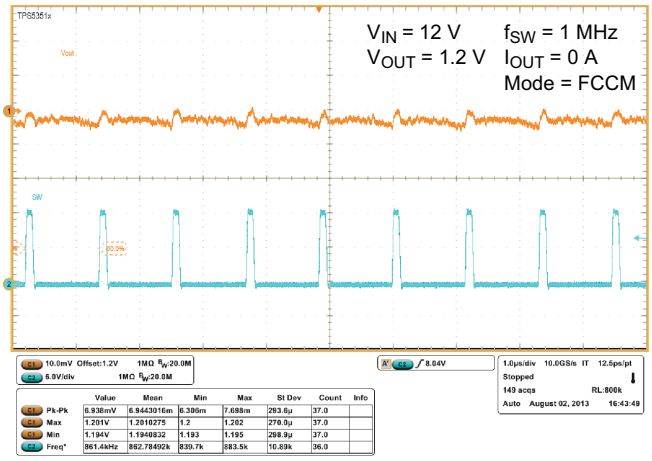



**Figure 5-14. FCCM Steady-State Operation**

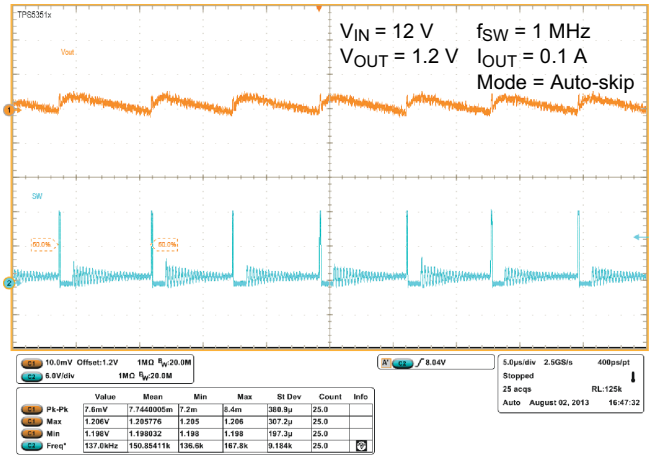



**Figure 5-15. Auto-Skip Mode Steady-State Operation**

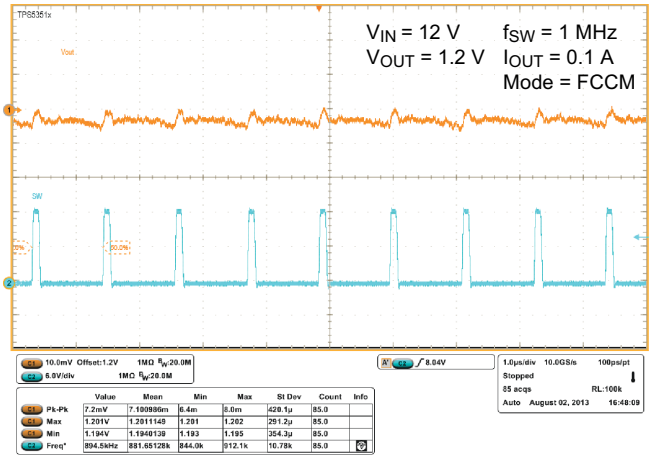



**Figure 5-16. FCCM Steady-State Operation**

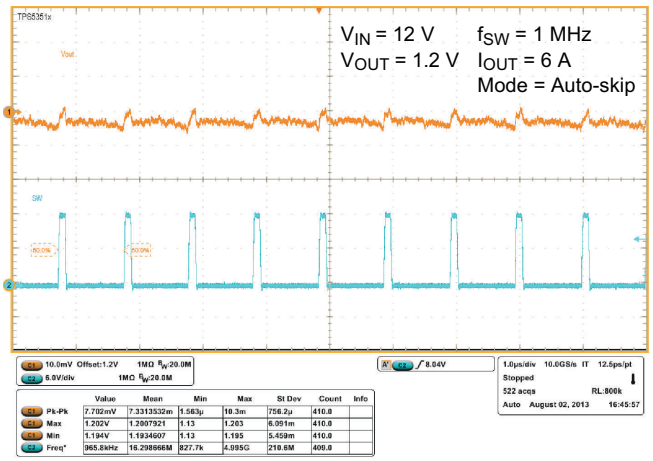



**Figure 5-17. Auto-Skip Mode Steady-State Operation**

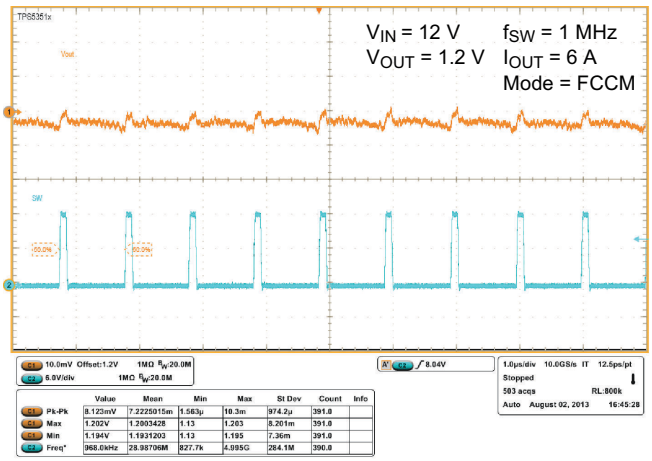



**Figure 5-18. FCCM Steady-State Operation**

## 5.6 Typical Characteristics (continued)

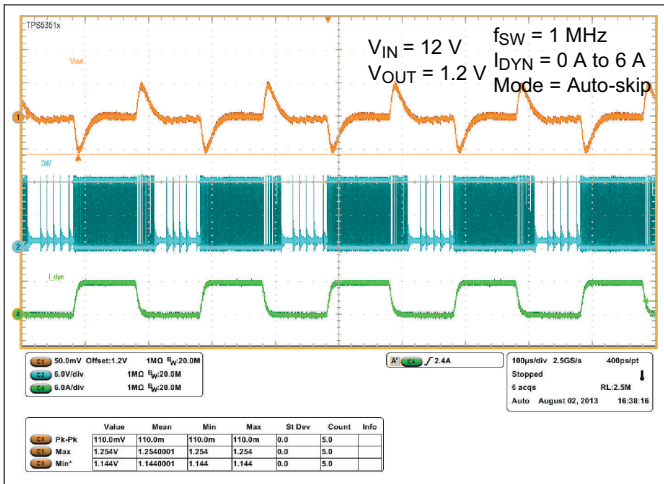



Figure 5-19. Auto-Skip Mode Load Transient

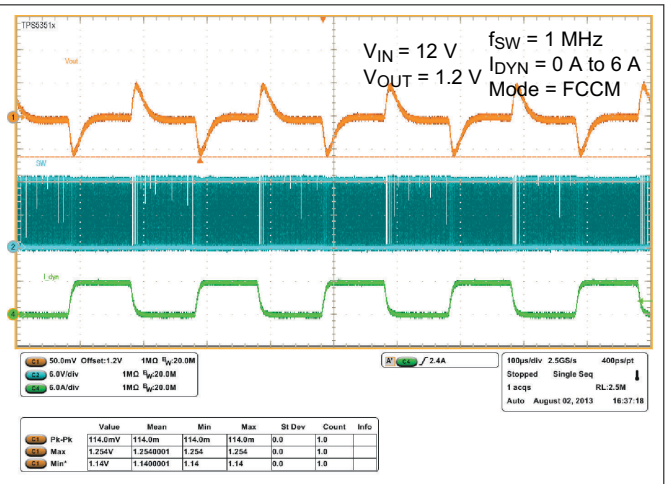



Figure 5-20. FCCM Load Transient

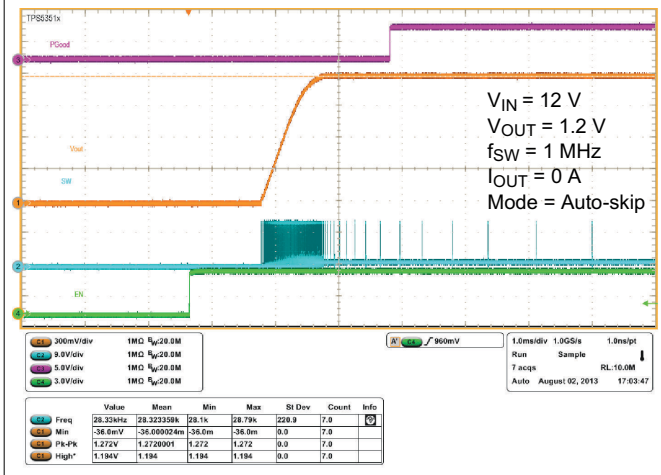



Figure 5-21. Auto-Skip Mode Start-Up

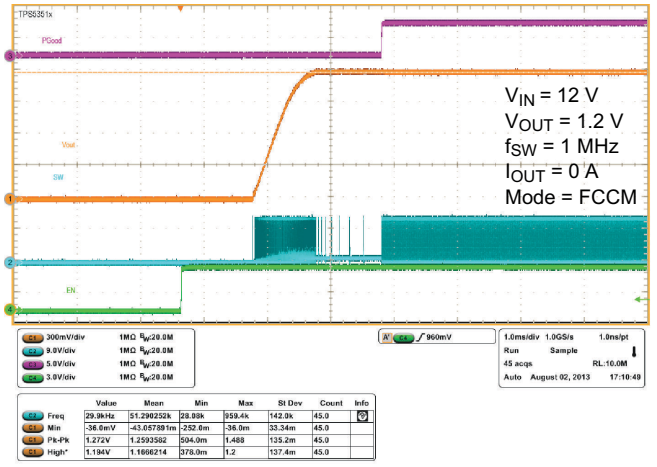



Figure 5-22. FCCM Start-Up

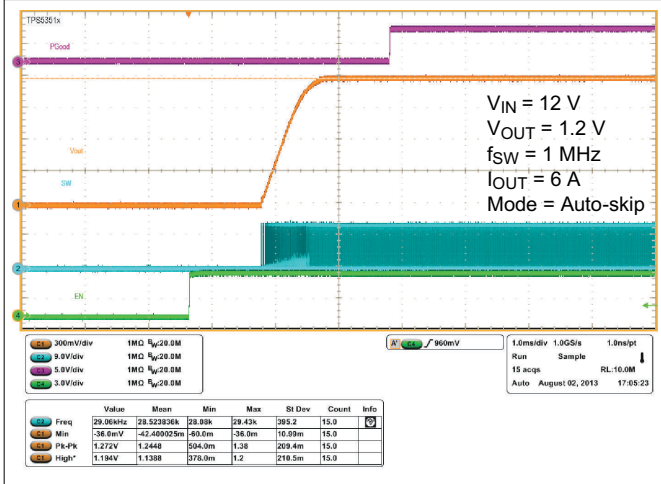



Figure 5-23. Auto-Skip Mode Start-Up

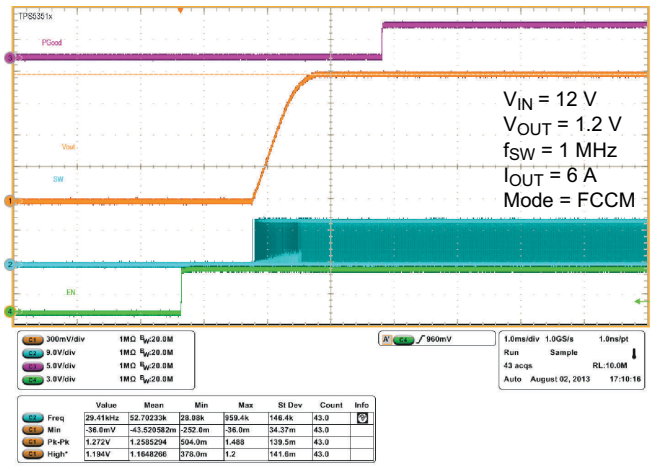



Figure 5-24. FCCM Start-Up

## 5.6 Typical Characteristics (continued)

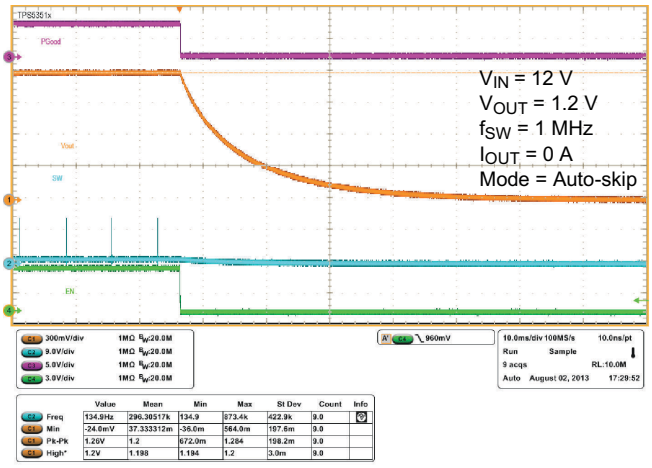



Figure 5-25. Auto-Skip Mode Shutdown Operation

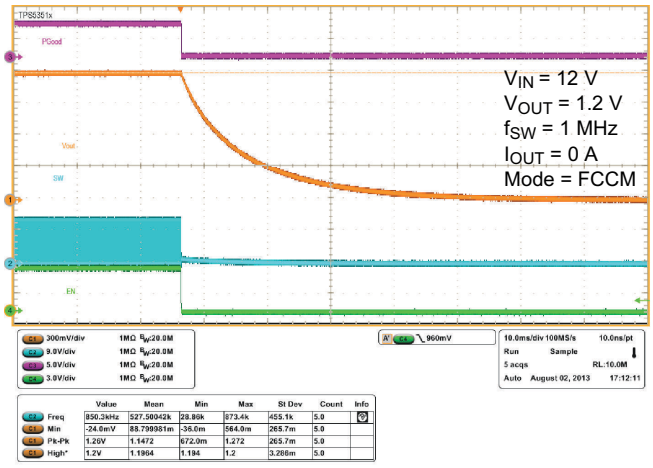



Figure 5-26. FCCM Shutdown Operation

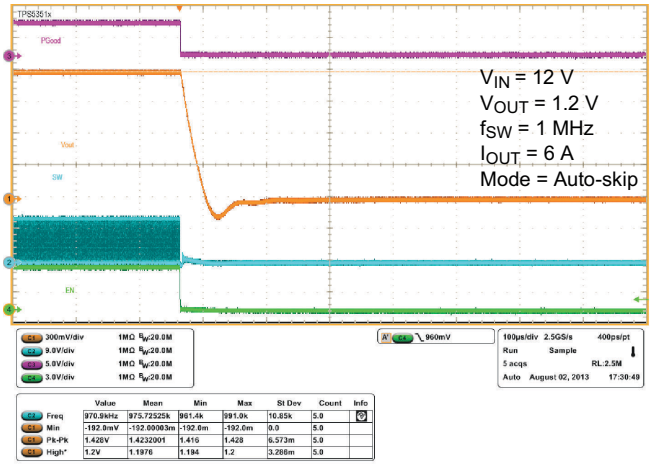



Figure 5-27. Auto-Skip Mode Shutdown Operation

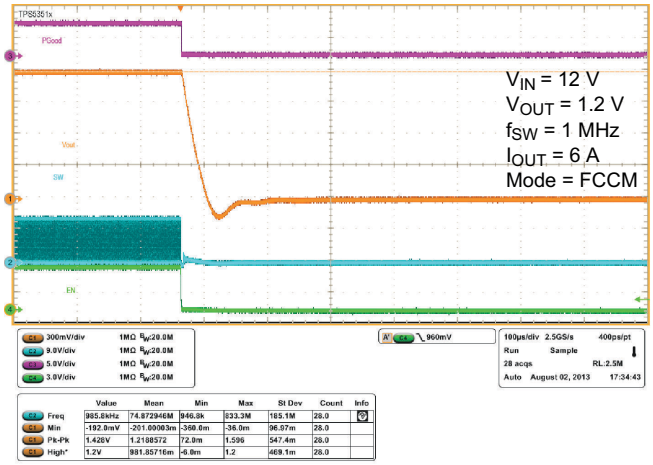



Figure 5-28. FCCM Shutdown Operation

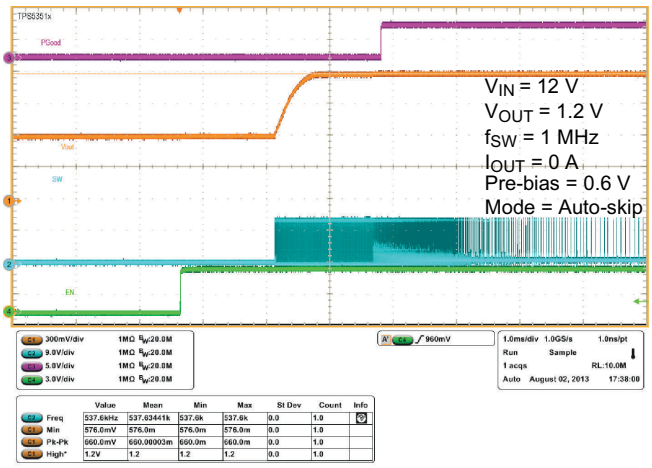



Figure 5-29. Prebias Operation

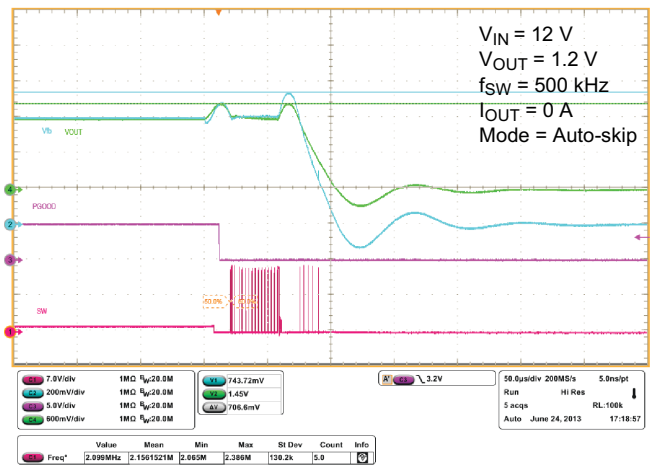



Figure 5-30. Overvoltage Protection

## 5.6 Typical Characteristics (continued)

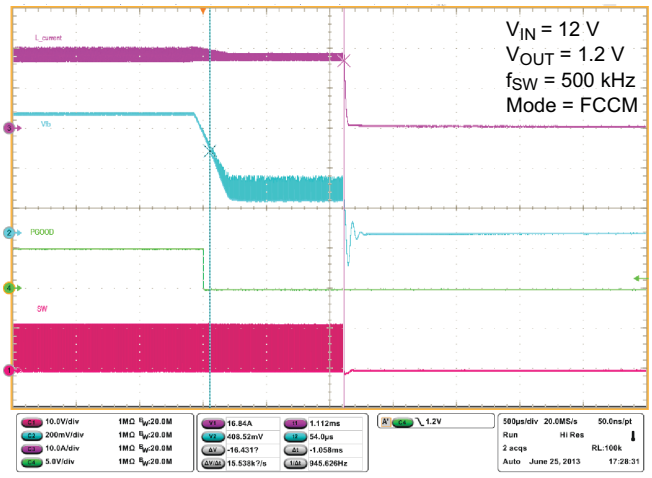
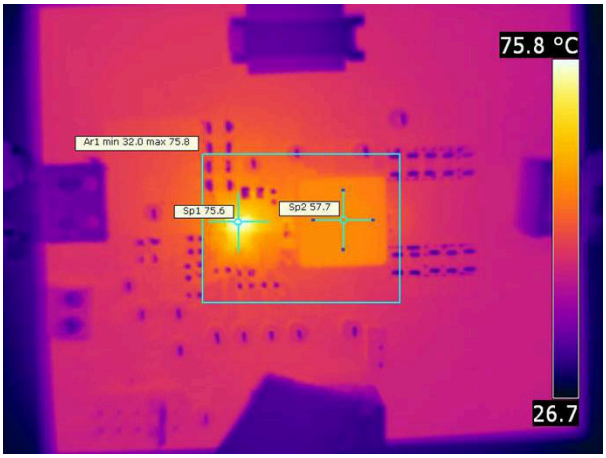



**Figure 5-31. Overcurrent Protection**




| | | |
|---|---|---|
| $f_{SW}$ = 500kHz | $V_I$ = 12V | $V_O$ = 5V |
| $I_O$ = 12A | $C_{OUT}$= 10x 22 µF | ( 1206, 6.3V, X5R) |
| SNB = 3Ω+ 470pF | $R_{BOOT}$= 0Ω | |
| Inductor: | $L_{OUT}$ = 1 µH | 2.1mΩ (typ) |
| PCMC135T-1R0MF | | 12.6mm × 13.8mm × 5mm |

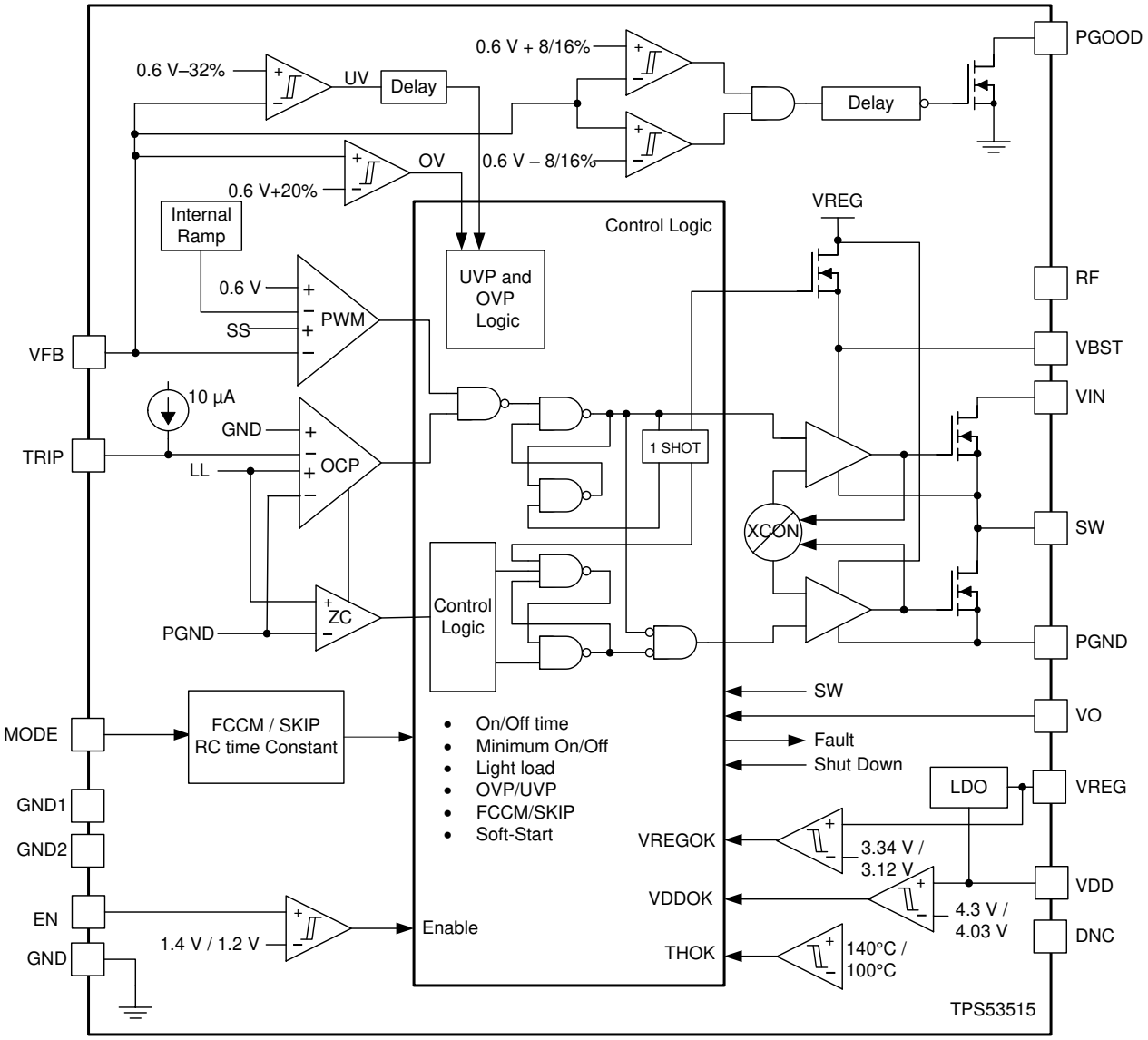
**Figure 5-32. SP1: 75.6℃, SP2: 57.7℃ (Inductor)**

# 6 Detailed Description

## 6.1 Overview

The TPS53515 device is a high-efficiency, single-channel, synchronous-buck converter. The device suits low-output voltage point-of-load applications with 12A or lower output current in computing and similar digital consumer applications. The TPS53515 device features proprietary D-CAP3 control mode combined with adaptive on-time architecture. This combination builds modern low-duty-ratio and ultra-fast load-step-response DC-DC converters in an ideal fashion. The output voltage ranges from 0.6V to 5.5V. The conversion input voltage ranges from 1.5 V to 18V and the VDD input voltage ranges from 4.5V to 25V. The D-CAP3 control mode uses emulated current information to control the modulation. An advantage of this control scheme is that it does not require a phase-compensation network outside which makes the device easy-to-use and also allows low-external component count. Adaptive on-time control tracks the preset switching frequency over a wide range of input and output voltage while increasing switching frequency as needed during load-step transient.

## 6.2 Functional Block Diagram



## 6.3 Feature Description

### 6.3.1 5V LDO and VREG Start-Up

The TPS53515 device has an internal 5V LDO feature using input from VDD and output to VREG. When the VDD voltage rises above 2.8V, the internal LDO is enabled and outputs voltage to the VREG pin. The VREG voltage provides the bias voltage for the internal analog circuitry. The VREG voltage also provides the supply voltage for the gate drives.

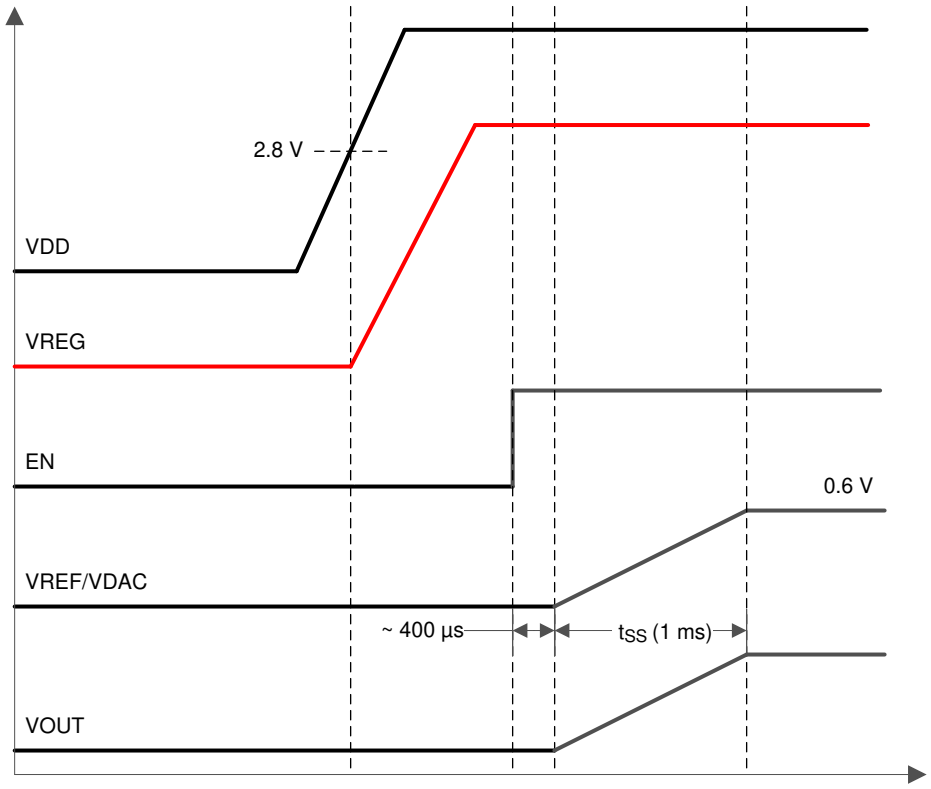



**Figure 6-1. Power-up Sequence Waveforms**

### 6.3.2 Enable, Soft Start, and Mode Selection

The internal LDO regulator starts immediately and regulates to 5V at the VREG pin.

When the EN pin voltage rises above the enable threshold voltage (typically 1.4V), the controller enters the start-up sequence. The controller then uses the first 400 µs to calibrate the switching frequency setting resistance attached to the RF pin and stores the switching frequency code in internal registers. During this period, the MODE pin also senses the resistance attached to this pin to determine the operation mode. In the second phase, an internal DAC starts ramping up the reference voltage from 0V to 0.6V. The ramping up time is 1 ms. The device maintains smooth and constant ramp-up of the output voltage during start-up regardless of load current.

### 6.3.3 Frequency Selection

The TPS53515 device lets users select the switching frequency by using the RF pin. Table 6-1 lists the divider ratio and some example resistor values for the switching frequency selection. The 1% tolerance resistors with a typical temperature coefficient of ±100ppm/°C are recommended. If the design requires a tighter noise margin for more reliable SW-frequency detection, use higher performance resistors.

**Table 6-1. Switching Frequency Selection**

| SWITCHING FREQUENCY ($f_{SW}$) (kHz) | RESISTOR DIVIDER RATIO[1] ($R_{DR}$) | EXAMPLE RF FREQUENCY COMBINATIONS | |
|---|---|---|---|
| | | $R_{RF\_H}$ (kΩ) | $R_{RF\_L}$ (kΩ) |
| 1000 | > 0.557 | 1 | 300 |
| 850 | 0.461 | 180 | 154 |
| 750 | 0.375 | 200 | 120 |
| 600 | 0.297 | 249 | 105 |
| 500 | 0.229 | 240 | 71.5 |
| 400 | 0.16 | 249 | 47.5 |
| 300 | 0.096 | 255 | 27 |
| 250 | < 0.041 | 270 | 11.5 |

(1) Resistor divider ratio ($R_{DR}$) is described in Equation 1.

$$R_{DR} = \frac{R_{RF\_L}}{\left(R_{RF\_L} + R_{RF\_H}\right)} \quad (1)$$

where

- $R_{RF\_L}$ is the low-side resistance of the RF pin resistor divider
- $R_{RF\_H}$ is the high-side resistance of the RF pin resistor divider

### 6.3.4 D-CAP3 Control and Mode Selection

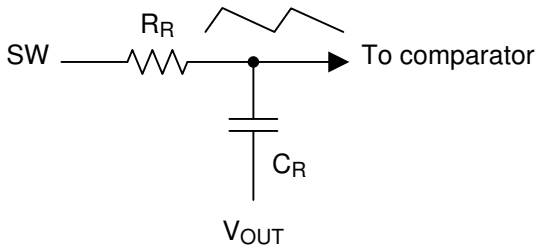



**Figure 6-2. Internal RAMP Generation Circuit**

The TPS53515 device uses D-CAP3 control mode to achieve fast load transient while maintaining the ease-of-use feature. An internal RAMP is generated and fed to the VFB pin to reduce jitter and maintain stability. The amplitude of the ramp is determined by the R-C time-constant as shown in Figure 6-2. At different switching frequencies, ($f_{SW}$) the R-C time-constant varies to maintain relatively constant RAMP amplitude.

#### 6.3.4.1 D-CAP3™ Control Mode

From small-signal loop analysis, a buck converter using the D-CAP3 mode control architecture can be simplified as shown in Figure 6-3.

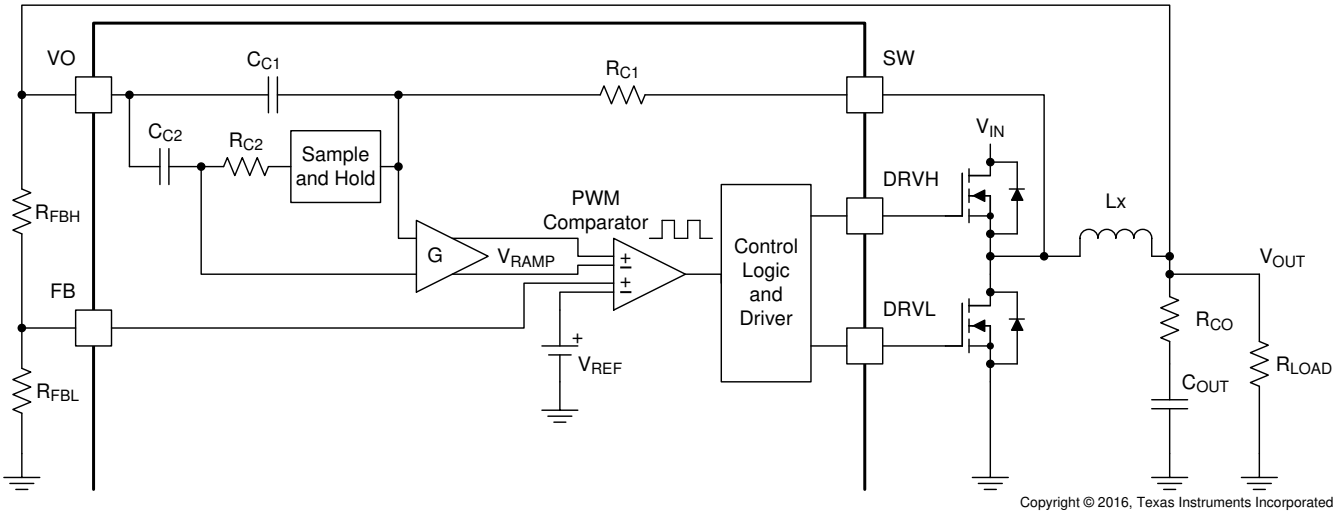



**Figure 6-3. D-CAP3™ Control Mode**

The D-CAP3 control mode architecture includes an internal ripple generation network, enabling the use of very low-ESR output capacitors such as multilayered ceramic capacitors (MLCC). No external current sensing network or voltage compensators are required with D-CAP3 control mode architecture. The role of the internal ripple generation network is to emulate the ripple component of the inductor current information and then combine with the voltage feedback signal to regulate the loop operation. For any control topologies supporting no external compensation design, there is a minimum range, maximum range, or both, of the output filter the control topologies can support. The output filter used with the TPS53515 device is a lowpass L-C circuit. This L-C filter has double pole that is described in Equation 2.

$$f_P = \frac{1}{2 \times \pi \times \sqrt{L_{OUT} \times C_{OUT}}} \quad (2)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the TPS53515 device. The low frequency L-C double pole has a 180 degree in phase. At the output filter frequency, the gain rolls off at a –40dB per decade rate and the phase drops rapidly. The internal ripple generation network introduces a high-frequency zero that reduces the gain roll off from –40dB to –20dB per decade and increases the phase to 90 degree one decade above the zero frequency.

The inductor and capacitor selected for the output filter must be such that the double pole of Equation 2 is located close enough to the high-frequency zero so that the phase boost provided by the high-frequency zero provides adequate phase margin for the stability requirement.

**Table 6-2. Locating the Zero**

| SWITCHING FREQUENCIES ($f_{SW}$) (kHz) | ZERO ($f_Z$) LOCATION (kHz) |
|---|---|
| 250 and 300 | 6 |
| 400 and 500 | 7 |
| 600 and 750 | 9 |
| 850 and 1000 | 12 |

After identifying the application requirements, the output inductance must be designed so that the inductor peak-to-peak ripple current is approximately between 25% and 35% of the $I_{CC(max)}$ (peak current in the application). Use Table 6-2 to help locate the internal zero based on the selected switching frequency. In general, where reasonable (or smaller) output capacitance is desired, Equation 3 can be used to determine the necessary output capacitance for stable operation.

$$f_P = \frac{1}{2 \times \pi \times \sqrt{L_{OUT} \times C_{OUT}}} = f_Z \quad (3)$$

If MLCC is used, consider the derating characteristics to determine the final output capacitance for the design. For example, when using an MLCC with specifications of 10µF, X5R and 6.3V, the deratings by DC bias and AC bias are 80% and 50%, respectively. The effective derating is the product of these two factors, which in this case is 40% and 4µF. Consult with capacitor manufacturers for specific characteristics of the capacitors to be used in the system, applications.

Table 6-3 shows the recommended output filter range for an application design with the following specifications:

- Input voltage, $V_{IN}$ = 12V
- Switching frequency, $f_{SW}$ = 600kHz
- Output current, $I_{OUT}$ = 8A

The minimum output capacitance is verified by the small-signal measurement conducted on the EVM using the following two criteria:

- Loop crossover frequency is less than one-half the switching frequency (300kHz)
- Phase margin at the loop crossover is greater than 50 degrees

For the maximum output capacitance recommendation, simplify the procedure to adopt an unrealistically high output capacitance for this type of converter design, then verify the small-signal response on the EVM using the following one criteria:

- Phase margin at the loop crossover is greater than 50 degrees

As indicated by the phase margin, the actual maximum output capacitance ($C_{OUT(max)}$) can continue to go higher. However, small-signal measurement (bode plot) must be done to confirm the design.

Select a MODE pin configuration as shown in Table 6-4 to in double the R-C time-constant option for the maximum output capacitance design and application. Select a MODE pin configuration to use single R-C time constant option for the normal (or smaller) output capacitance design and application.

The MODE pin also selects skip-mode or FCCM-mode operation.

**Table 6-3. Recommended Component Values**

| $V_{OUT}$ (V) | $R_{LOWER}$ (kΩ) | $R_{UPPER}$ (kΩ) | $L_{OUT}$ (µH) | $C_{OUT(min)}$ (µF) (1) | CROSS-OVER (kHz) | PHASE MARGIN (°) | $C_{OUT(max)}$ (µF) (1) | INTERNAL RC SETTING (µs) | INDUCTOR $\Delta I/I_{CC(max)}$ | $I_{CC(max)}$ (A) |
|---|---|---|---|---|---|---|---|---|---|---|
| 0.6 | 10 | 0 | 0.36 PIMB065T-R36MS | 3 × 100 | 247 | 70 | | 40 | 33% | 8 |
| | | | | | 48 | 62 | 30x 100 | 80 | | |
| 1.2 | | 10 | 0.68 PIMB065T-R68MS | 9 × 22 | 207 | 53 | | 40 | 33% | |
| | | | | | 25 | 84 | 30x 100 | 80 | | |
| 2.5 | | 31.6 | 1.2 PIMB065T-1R2MS | 4 × 22 | 185 | 57 | | 40 | 34% | |
| | | | | | 11 | 63 | 30x 100 | 80 | | |
| 3.3 | | 45.3 | 1.5 PIMB065T-1R5MS | 3 × 22 | 185 | 57 | | 40 | 33% | |
| | | | | | 9 | 59 | 30x 100 | 80 | | |
| 5.5 | | 82.5 | 2.2 PIMB065T-2R2MS | 2 × 22 | 185 | 51 | | 40 | 28% | |
| | | | | | 7 | 58 | 30x 100 | 80 | | |

(1) All $C_{OUT(min)}$ and $C_{OUT(max)}$ capacitor specifications are 1206, X5R, 10V.

For higher output voltage at or above 2.0V, additional phase boost can be required to secure sufficient phase margin due to phase delay/loss for higher output voltage (large on-time ($t_{ON}$)) setting in a fixed on time topology based operation.

A feedforward capacitor placing in parallel with $R_{UPPER}$ is found to be very effective to boost the phase margin at loop crossover. Refer to TI application note SLVA289 for details.

**Table 6-4. Mode Selection and Internal RAMP R-C Time Constant**

| MODE SELECTION | ACTION | $R_{MODE}$ (kΩ) | R-C TIME CONSTANT (µs) | SWITCHING FREQUENCIES $f_{SW}$ (kHz) |
|---|---|---|---|---|
| **Skip Mode** | Pull down to GND | 0 | 60 | 250 and 300 |
| | | | 50 | 400 and 500 |
| | | | 40 | 600 and 750 |
| | | | 30 | 850 and 1000 |
| | | 150 | 120 | 250 and 300 |
| | | | 100 | 400 and 500 |
| | | | 80 | 600 and 750 |
| | | | 60 | 850 and 1000 |
| **FCCM** (1) | Connect to PGOOD | 20 | 60 | 250 and 300 |
| | | | 50 | 400 and 500 |
| | | | 40 | 600 and 750 |
| | | | 30 | 850 and 1000 |
| | | 150 | 120 | 250 and 300 |
| | | | 100 | 400 and 500 |
| | | | 80 | 600 and 750 |
| | | | 60 | 850 and 1000 |
| **FCCM** | Connect to VREG | 0 | 120 | 250 and 300 |
| | | | 100 | 400 and 500 |
| | | | 80 | 600 and 750 |
| | | | 60 | 850 and 1000 |

(1) Device goes into Forced CCM (FCCM) after PGOOD becomes high.

### 6.3.4.2 Sample and Hold Circuitry

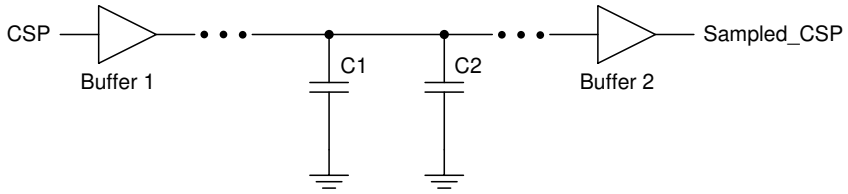



**Figure 6-4. Sample and Hold Logic Circuitry**

The sample and hold circuitry is the difference between D-CAP3 control mode and D-CAP2. The sample and hold circuitry, which is an advance control scheme to boost output voltage accuracy higher on the TPS53515 device, is one of features of the TPS53515 device. The sample and hold circuitry generates a new DC voltage of CSN instead of the voltage which is produced by $R_{C2}$ and $C_{C2}$ which allows for tight output-voltage accuracy and makes the TPS53515 device more competitive.

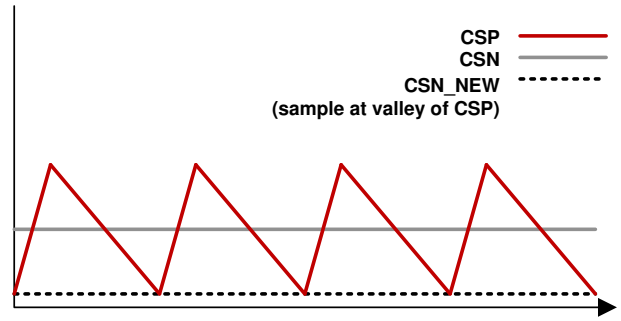



**Figure 6-5. Continuous Conduction Mode (CCM) With Sample and Hold Circuitry**

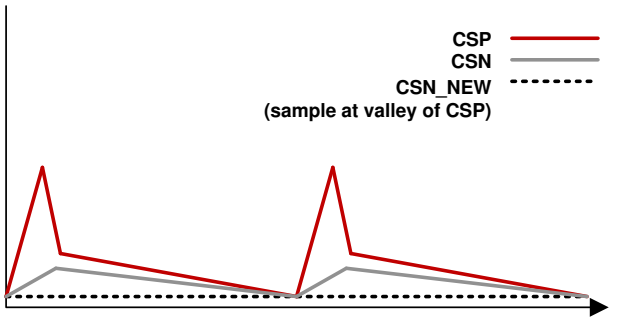



**Figure 6-6. Discontinuous Conduction Mode (DCM) With Sample and Hold Circuitry**

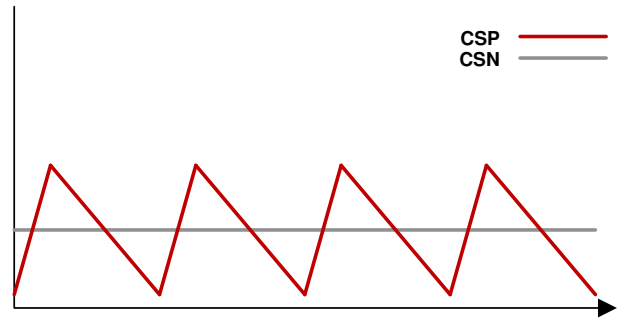



**Figure 6-7. Continuous Conduction Mode (CCM) Without Sample and Hold Circuitry**

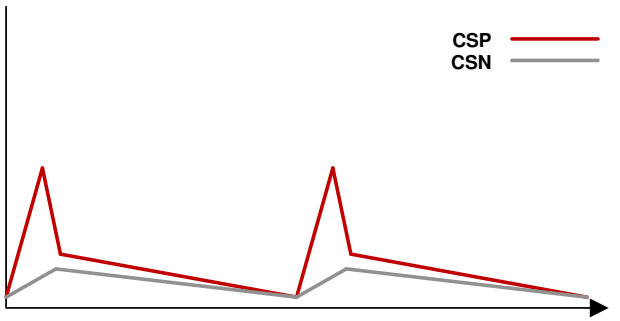



**Figure 6-8. Discontinuous Conduction Mode (DCM) Without Sample and Hold Circuitry**

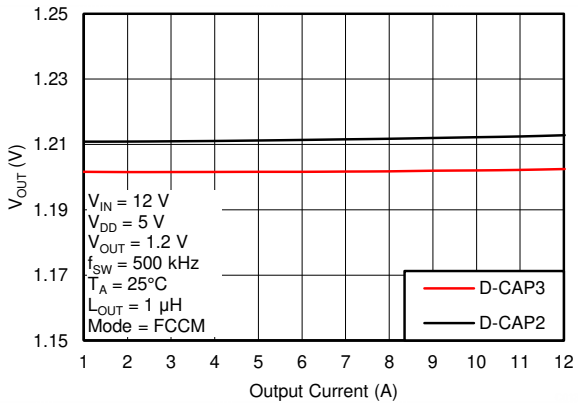



**Figure 6-9. Output Voltage vs Output Current**

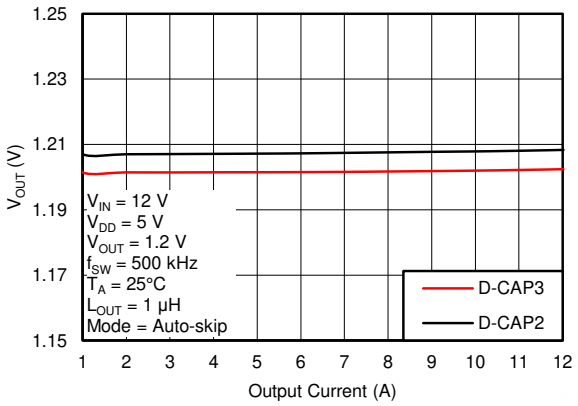



**Figure 6-10. Output Voltage vs Output Current**

#### 6.3.4.3 Adaptive Zero-Crossing

The TPS53515 device uses an adaptive zero-crossing circuit to perform optimization of the zero inductor-current detection during skip-mode operation. This function allows ideal low-side MOSFET turn-off timing. The function also compensates the inherent offset voltage of the Z-C comparator and delay time of the Z-C detection circuit. Adaptive zero-crossing prevents SW-node swing-up caused by too-late detection and minimizes diode conduction period caused by too-early detection. As a result, the device delivers better light-load efficiency.

### *6.3.5 Power-Good*

The TPS53515 device has power-good output that indicates high when switcher output is within the target. The power-good function is activated after the soft-start operation is complete. If the output voltage becomes within ±8% of the target value, internal comparators detect the power-good state and the power-good signal becomes high after a 1-ms internal delay. If the output voltage goes outside of ±16% of the target value, the power-good

signal becomes low after a 2-µs internal delay. The power-good output is an open-drain output and must be pulled-up externally.

### 6.3.6 Current Sense and Overcurrent Protection

s

The TPS53515 device has cycle-by-cycle overcurrent limiting control. The inductor current is monitored during the OFF state and the controller maintains the OFF state during the period that the inductor current is larger than the overcurrent trip level. To provide good accuracy and a cost-effective design, the TPS53515 device supports temperature compensated MOSFET $R_{DS(on)}$ sensing. Connect the TRIP pin to GND through the trip-voltage setting resistor, $R_{TRIP}$. The TRIP pin sources $I_{TRIP}$ current, which is 10µA typically at room temperature, and the trip level is set to the OCL trip voltage $V_{TRIP}$ as shown in Equation 4.

$$V_{TRIP} = R_{TRIP} \times I_{TRIP} \tag{4}$$

where

- $V_{TRIP}$ is in mV
- $R_{TRIP}$ is in kΩ
- $I_{TRIP}$ is in µA

The inductor current is monitored by the voltage between the GND pin and SW pin so that the SW pin is properly connected to the drain pin of the low-side MOSFET. $I_{TRIP}$ has a 3000ppm/°C temperature slope to compensate the temperature dependency of $R_{DS(on)}$. The GND pin acts as the positive current-sensing node. Connect the GND pin to the proper current sensing device, (for example, the source pin of the low-side MOSFET.)

Because the comparison occurs during the OFF state, $V_{TRIP}$ sets the valley level of the inductor current. Thus, the load current at the overcurrent threshold, $I_{OCP}$, is calculated as shown in Equation 5.

$$I_{OCP} = \frac{V_{TRIP}}{\left(8 \times R_{DS(on)}\right)} + \frac{I_{IND(ripple)}}{2} = \frac{V_{TRIP}}{\left(8 \times R_{DS(on)L}\right)} + \frac{1}{2 \times L \times f_{SW}} \times \frac{\left(V_{IN} - V_{OUT}\right) \times V_{OUT}}{V_{IN}} \tag{5}$$

where

- $R_{DS(on)L}$ is the on-resistance of the low-side MOSFET
- $R_{TRIP}$ is in kΩ

Equation 5 calculates the typical DC OCP level (typical low-side on-resistance [$R_{DS(on)}$] of 5.9mΩ must be used); to design for worst case minimum OCP, maximum low-side on-resistance value of 8mΩ must be used.

During an overcurrent condition, the current to the load exceeds the current to the output capacitor thus the output voltage tends to decrease. Eventually, the output voltage crosses the undervoltage-protection threshold and shuts down.

For the TPS53515 device, the overcurrent protection maximum is recommended up to 14A only.

### 6.3.7 Overvoltage and Undervoltage Protection

The TPS53515 device monitors a resistor-divided feedback voltage to detect overvoltage and undervoltage. When the feedback voltage becomes lower than 68% of the target voltage, the UVP comparator output goes high and an internal UVP delay counter begins counting. After 1 ms, the TPS53515 device latches OFF both high-side and low-side MOSFETs drivers. The UVP function enables after soft-start is complete.

When the feedback voltage becomes higher than 120% of the target voltage, the OVP comparator output goes high and the circuit latches OFF the high-side MOSFET driver and turns on the low-side MOSFET until reaching a negative current limit. Upon reaching the negative current limit, the low-side FET is turned off and the high-side FET is turned on again for a minimum on-time. The TPS53515 device operates in this cycle until the output voltage is pulled down under the UVP threshold voltage for 1 ms. After the 1-ms UVP delay time, the high-side

FET is latched off and low-side FET is latched on. The fault is cleared with a reset of VDD or by retoggling the EN pin.

#### 6.3.8 Out-of-Bounds Operation

The TPS53515 device has an out-of-bounds (OOB) overvoltage protection that protects the output load at a much lower overvoltage threshold of 8% above the target voltage. OOB protection does not trigger an overvoltage fault, so the device is not latched off after an OOB event. OOB protection operates as an early no-fault overvoltage-protection mechanism. During the OOB operation, the controller operates in forced PWM mode only by turning on the low-side FET. Turning on the low-side FET beyond the zero inductor current quickly discharges the output capacitor thus causing the output voltage to fall quickly toward the setpoint. During the operation, the cycle-by-cycle negative current limit is also activated to ensure the safe operation of the internal FETs.

#### 6.3.9 UVLO Protection

The TPS53515 device monitors the voltage on the VDD pin. If the VDD pin voltage is lower than the UVLO off-threshold voltage, the switch mode power supply shuts off. If the VDD voltage increases beyond the UVLO on-threshold voltage, the controller turns back on. UVLO is a nonlatch protection.

#### 6.3.10 Thermal Shutdown

The TPS53515 device monitors internal temperature. If the temperature exceeds the threshold value (typically 140°C), TPS53515 device shuts off. When the temperature falls approximately 40°C below the threshold value, the device turns on. Thermal shutdown is a nonlatch protection.

### 6.4 Device Functional Modes

#### 6.4.1 Auto-Skip Eco-mode Light Load Operation

While the MODE pin is pulled to GND directly or through 150kΩ resistor, the TPS53515 device automatically reduces the switching frequency at light-load conditions to maintain high efficiency. This section describes the operation in detail.

As the output current decreases from heavy load condition, the inductor current also decreases until the rippled valley of the inductor current touches zero level. Zero level is the boundary between the continuous-conduction and discontinuous-conduction modes. The synchronous MOSFET turns off when this zero inductor current is detected. As the load current decreases further, the converter runs into discontinuous-conduction mode (DCM). The on-time is maintained to a level approximately the same as during continuous-conduction mode operation so that discharging the output capacitor with a smaller load current to the level of the reference voltage requires more time. The transition point to the light-load operation $I_{O(LL)}$ (for example: the threshold between continuous- and discontinuous-conduction mode) is calculated as shown in Equation 6.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (6)$$

where

- $f_{SW}$ is the PWM switching frequency

Using only ceramic capacitors is recommended for Auto-skip mode.

#### 6.4.2 Forced Continuous-Conduction Mode

When the MODE pin is tied to the PGOOD pin through a resistor, the controller operates in continuous conduction mode (CCM) during light-load conditions. During CCM, the switching frequency maintained to an almost constant level over the entire load range which is suitable for applications requiring tight control of the switching frequency at the cost of lower efficiency.

# 7 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 7.1 Application Information

The TPS53515 device is a high-efficiency, single-channel, synchronous-buck converter. The device suits low-output voltage point-of-load applications with 12A or lower output current in computing and similar digital consumer applications.

## 7.2 Typical Application

This design example describes a D-CAP3 control mode, 8A synchronous buck converter with integrated MOSFETs. The device provides a fixed 1.2V output at up to 8A from a 12V input bus.

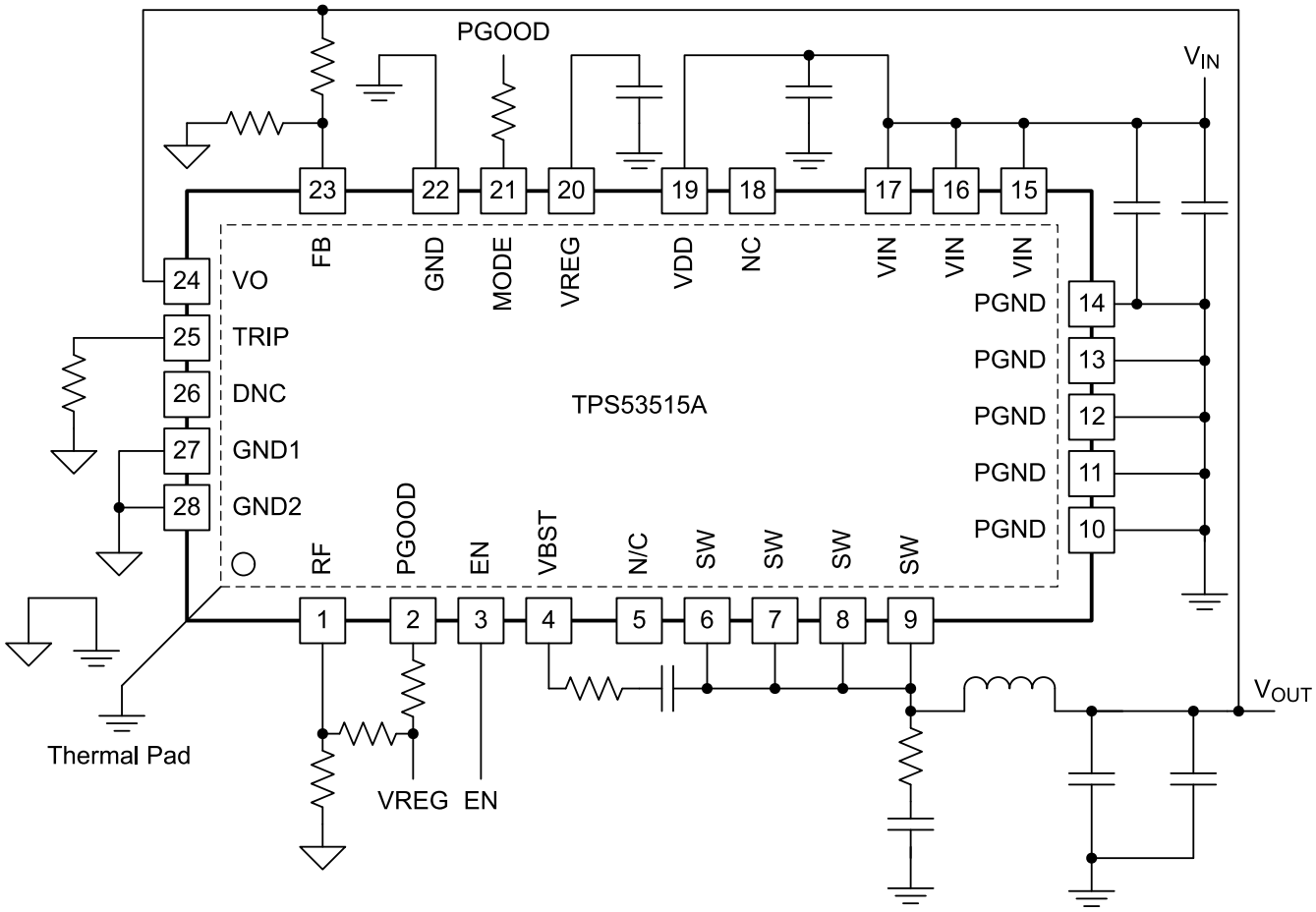



**Figure 7-1. Application Circuit Diagram**

### 7.2.1 Design Requirements

This design uses the parameters listed in Table 7-1.

**Table 7-1. Design Example Specifications**

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **INPUT CHARACTERISTIC** | | | | | | |
| $V_{IN}$ | Voltage range | | 5 | 12 | 18 | V |
| $I_{MAX}$ | Maximum input current | $V_{IN}$ = 5V, $I_{OUT}$ = 8A | | 2.5 | | A |
| | No load input current | $V_{IN}$ = 12V, $I_{OUT}$ = 0A with auto skip mode | | 1 | | mA |
| **OUTPUT CHARACTERISTICS** | | | | | | |
| $V_{OUT}$ | Output voltage | | | 1.2 | | V |
| | Output voltage regulation | Line regulation, 5V ≤ $V_{IN}$ ≤ –14V with FCCM | | 0.2% | | |
| | | Load regulation, $V_{IN}$ = 12V, 0A ≤ $I_{OUT}$ ≤ 8A with FCCM | | 0.5% | | |
| $V_{RIPPLE}$ | Output voltage ripple | $V_{IN}$ = 12V, $I_{OUT}$ = 8A with FCCM | | 10 | | $mV_{PP}$ |
| $I_{LOAD}$ | Output load current | | 0 | | 12 | A |
| $I_{OVER}$ | Output over current | | | 11 | | |
| $t_{SS}$ | Soft-start time | | | 1 | | ms |
| **SYSTEMS CHARACTERISTICS** | | | | | | |
| $f_{SW}$ | Switching frequency | | | 1 | | MHz |
| η | Peak efficiency | $V_{IN}$ = 12V, $V_{OUT}$ = 1.2V, $I_{OUT}$ = 4A | | 88.5% | | |
| η | Full load efficiency | $V_{IN}$ = 12V, $V_{OUT}$ = 1.2V, $I_{OUT}$ = 8A | | 86.9% | | |
| $T_A$ | Operating temperature | | | 25 | | °C |

### 7.2.2 Detailed Design Procedure

The external components selection is a simple process using D-CAP3 control mode. Select the external components using the following steps.

#### 7.2.2.1 Choose the Switching Frequency

The switching frequency is configured by the resistor divider on the RF pin. Select one of eight switching frequencies from 250kHz to 1MHz. Refer to Table 6-1 for the relationship between the switching frequency and resistor-divider configuration.

#### 7.2.2.2 Choose the Operation Mode

Select the operation mode using Table 6-4.

#### 7.2.2.3 Choose the Inductor

Determine the inductance value to set the ripple current at approximately ¼ to ½ of the maximum output current. Larger ripple current increases output ripple voltage, improves signal-to-noise ratio, and helps to stabilize operation.

$$L = \frac{1}{I_{IND(ripple)} \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} = \frac{3}{I_{OUT(max)} \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}}$$
$$= \frac{3}{6 \times 500\,kHz} \times \frac{\left(12\,V - 1.2\,V\right) \times 1.2\,V}{12\,V} = 1.08\,\mu H \quad (7)$$

The inductor requires a low DCR to achieve good efficiency. The inductor also requires enough room above peak inductor current before saturation. The peak inductor current is estimated using Equation 8.

$$I_{IND(peak)} = \frac{V_{TRIP}}{8 \times R_{DS(on)}} + \frac{1}{L \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} = \frac{10\,\mu A \times R_{TRIP}}{8 \times 5.9\,m\Omega} + \frac{1}{1\mu H \times 500\,kHz} \times \frac{(12\,V - 1.2\,V) \times 1.2\,V}{12\,V} \quad (8)$$

#### 7.2.2.4 Choose the Output Capacitor

The output capacitor selection is determined by output ripple and transient requirement. When operating in CCM, the output ripple has two components as shown in Equation 9. Equation 10 and Equation 11 define these components.

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)} \quad (9)$$

$$V_{RIPPLE(C)} = \frac{I_{L(ripple)}}{8 \times C_{OUT} \times f_{SW}} \quad (10)$$

$$V_{RIPPLE(ESR)} = I_{L(ripple)} \times ESR \quad (11)$$

#### 7.2.2.5 Determine the Value of R1 and R2

The output voltage is programmed by the voltage-divider resistors, R1 and R2, shown in Equation 12. Connect R1 between the VFB pin and the output, and connect R2 between the VFB pin and GND. The recommended R2 value is from 1kΩ to 20kΩ. Determine R1 using Equation 12.

$$R1 = \frac{V_{OUT} - 0.6}{0.6} \times R2 = \frac{1.2\,V - 0.6}{0.6} \times 10\,k\Omega = 10\,k\Omega \quad (12)$$

### 7.2.3 Application Curves

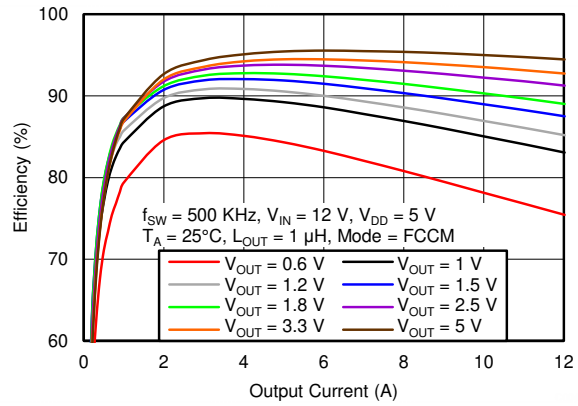



**Figure 7-2. Efficiency vs. Output Current**

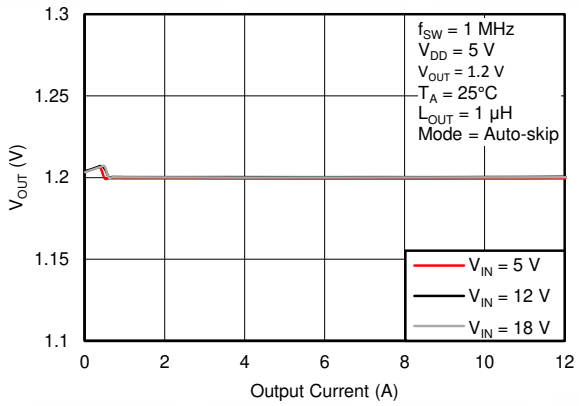



**Figure 7-3. Output Voltage vs. Output Current**

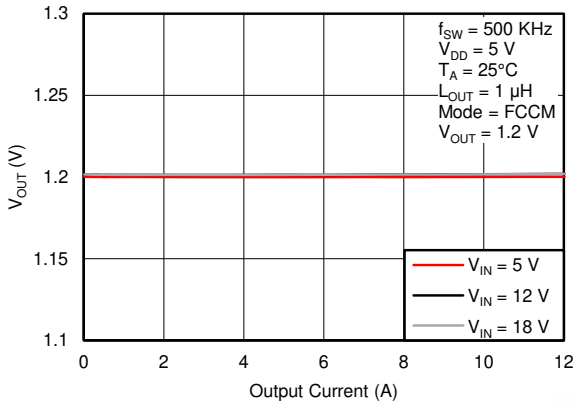



**Figure 7-4. Output Voltage vs. Output Current**

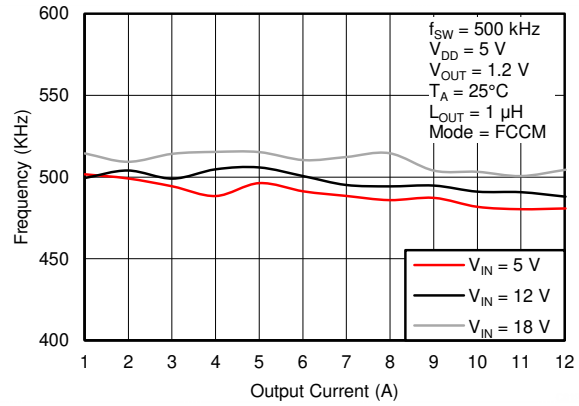
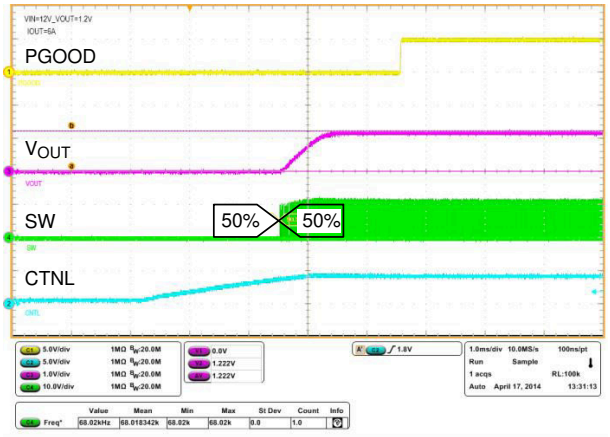
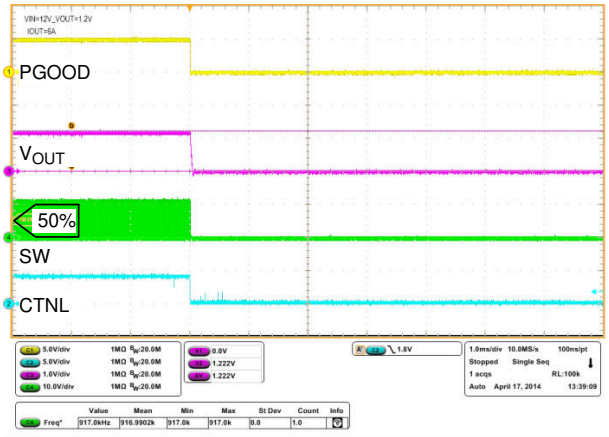



**Figure 7-5. Switching Frequency vs. Output Current**



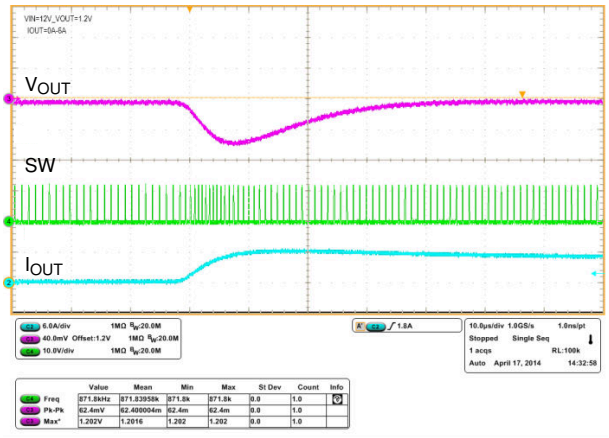

$I_{LOAD}$ = 6 A

**Figure 7-6. Start-Up Sequence**



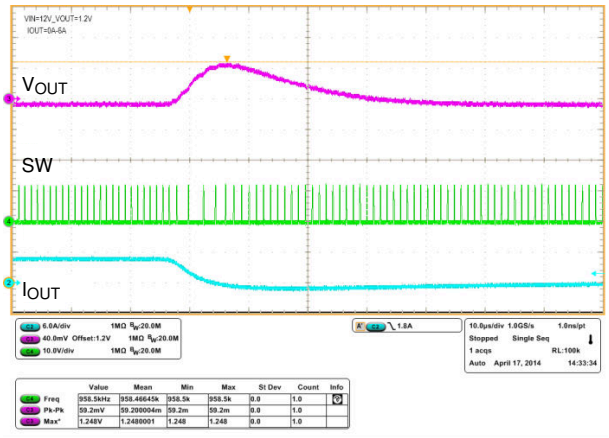

$I_{LOAD}$ = 6 A

**Figure 7-7. Shutdown Sequence**



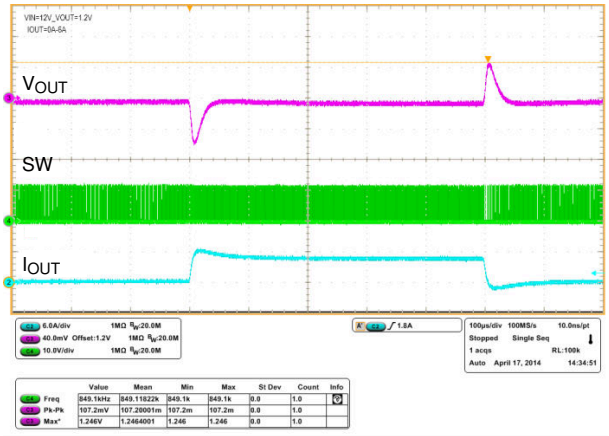

$I_{LOAD}$ from 0A to 6A

**Figure 7-8. Load Transient**



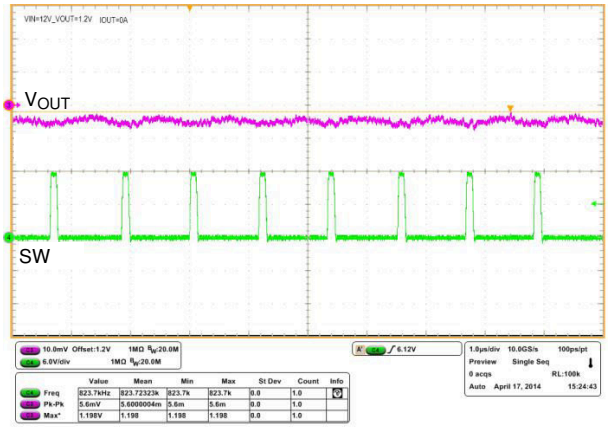

$I_{LOAD}$ from 6A to 0A

**Figure 7-9. Load Transient**



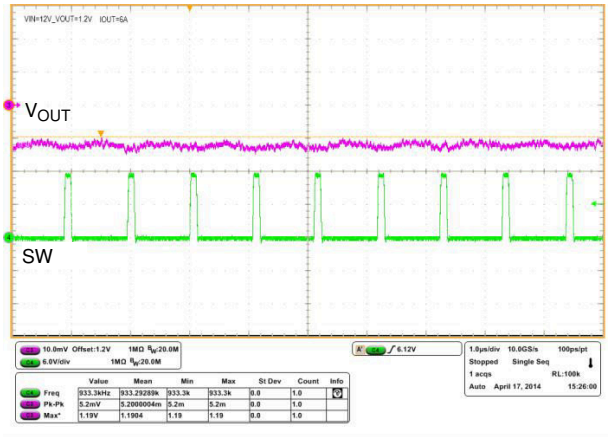

$I_{LOAD}$ from 0A to 6A to 0A

**Figure 7-10. Full Cycle Load Transient**



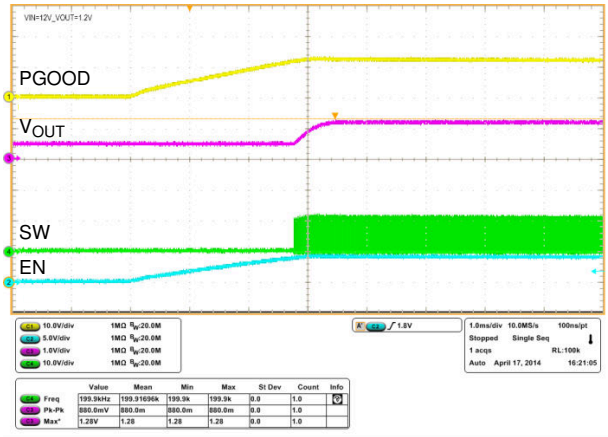

$I_{LOAD}$ = 0 A

**Figure 7-11. Output Voltage Ripple**




$I_{LOAD}$ = 6 A

**Figure 7-12. Output Voltage Ripple**




Preset $V_{OUT}$ = 0.5V

**Figure 7-13. Prebias Start-Up**

## 7.3 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 1.5V and 18V (4.5V to 25V biased). This input supply must be well regulated. Proper bypassing of input supplies and internal regulators is also critical for noise performance, as is PCB layout and grounding scheme. See the recommendations in *Section 7.4*.

## 7.4 Layout

### *7.4.1 Layout Guidelines*

Before beginning a design using the TPS53515 device, consider the following:

- Place the power components (including input and output capacitors, the inductor, and the DPA02259 device) on the solder side of the PCB. To shield and isolate the small signal traces from noisy power lines, insert and connect at least one inner plane to ground.
- All sensitive analog traces and components such as VFB, PGOOD, TRIP, MODE, and RF must be placed away from high-voltage switching nodes such as SW and VBST to avoid coupling. Use internal layers as ground planes and shield the feedback trace from power traces and components.
- GND (pin 22) must be connected directly to the thermal pad. Connect the thermal pad to the PGND terminals and then to the GND plane.
- The GND1 terminal (pin 27) and the GND2 terminal (pin 28) are not actual GND terminals and neither of these terminals must be used for dedicated ground connection. The recommendation is to connect GND1 terminal (pin 27) and the GND2 terminal (pin 28) to the nearby ground.
- Place the VIN decoupling capacitors as close to the VIN and PGND terminals as possible to minimize the input AC-current loop.
- Place the feedback resistor near the device to minimize the VFB trace distance.
- Place the frequency-setting resistor ($R_{RF}$), OCP-setting resistor ($R_{TRIP}$) and mode-setting resistor ($R_{MODE}$) close to the device. Use the common GND via to connect the resistors to the GND plane if applicable.
- Place the VDD and VREG decoupling capacitors as close to the device as possible. Provide GND vias for each decoupling capacitor and ensure the loop is as small as possible.
- This design defines the PCB trace as a switch node, which connects the SW terminals and high-voltage side of the inductor. The switch node must be as short and wide as possible.
- Use separated vias or trace to connect SW node to the snubber, bootstrap capacitor, and ripple-injection resistor. Do not combine these connections.
- Place one more small capacitor (2.2nF, 0402 size) between the VIN and PGND terminals. This capacitor must be placed as close to the device as possible.
- TI recommends placing a snubber between the SW shape and GND shape for effective ringing reduction. The value of snubber design starts at 3Ω + 470pF.
- Consider R-C-$C_C$ network (ripple injection network) component placement and place the AC coupling capacitor, $C_C$, close to the device, and R and C close to the power stage. (Application designs with output capacitance lower than the minimum can require only an R-C-C network. In this case, Bode plot verification is needed to validate the design).
- See Figure 7-14 for the layout recommendation.

### 7.4.2 Layout Example

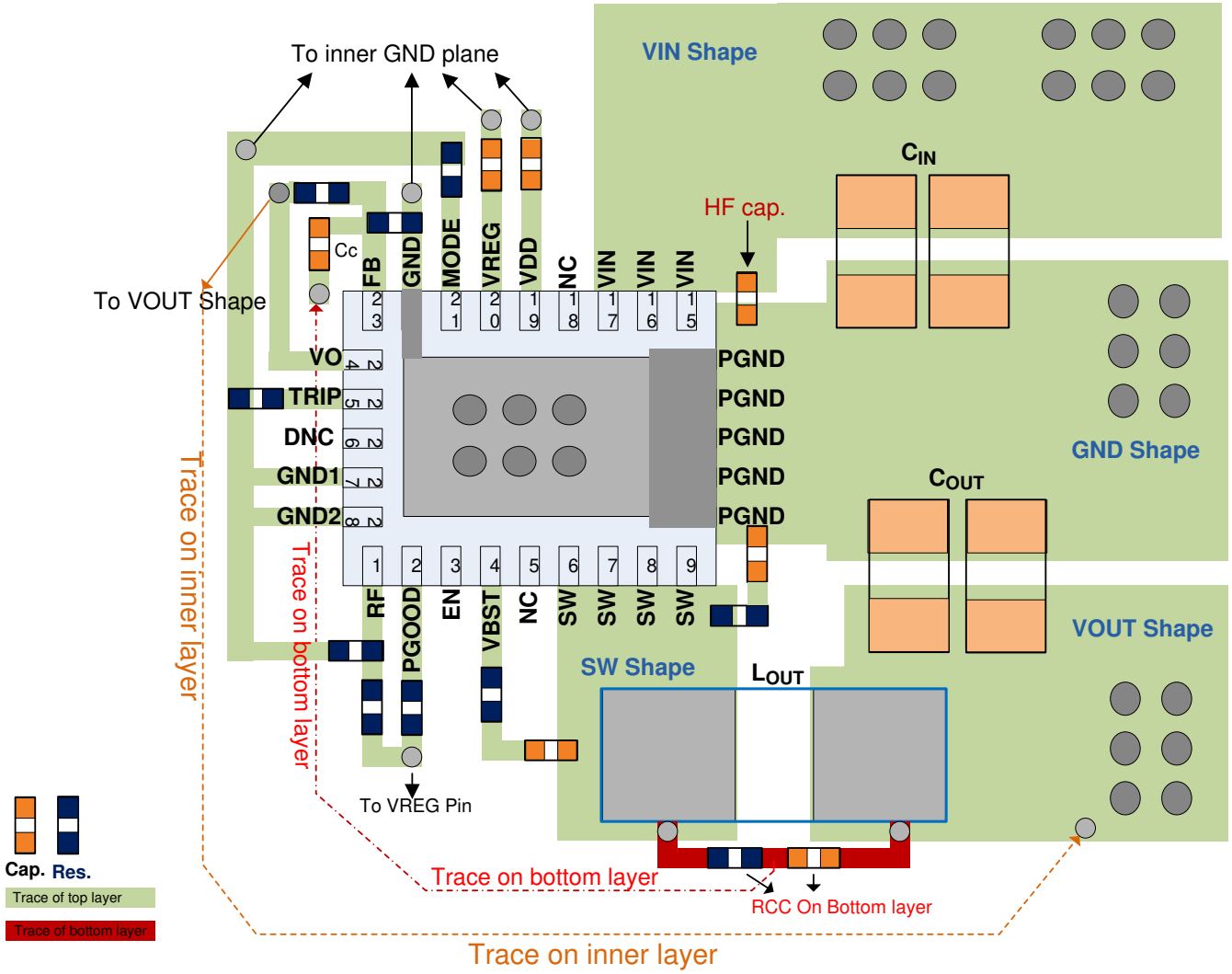
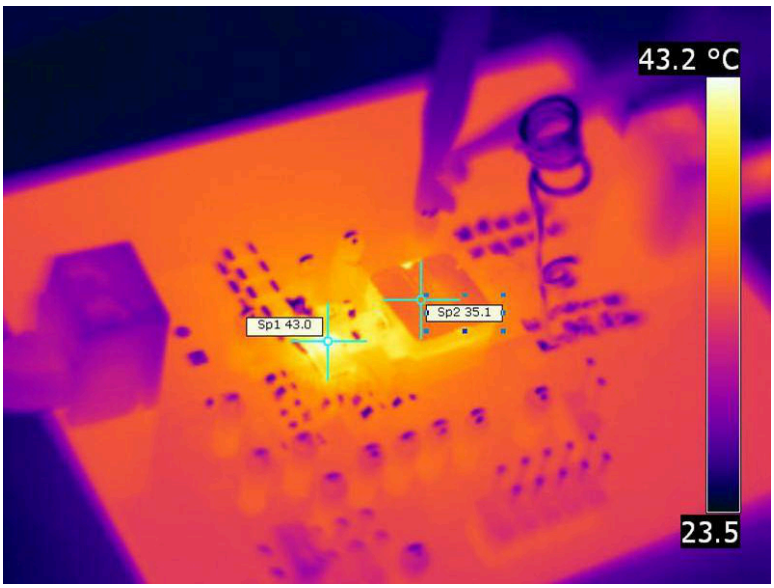



**Figure 7-14. Layout Recommendation**

### 7.4.3 Thermal Performance




$T_A$ = 23°C, $f_{SW}$ = 500kHz, $V_{IN}$ = 12V, $V_{OUT}$ = 1.24V, $I_{OUT}$ = 8A, $R_{BOOT}$= 0Ω, SNB = 3Ω + 470pF
Inductor: $L_{OUT}$ = 1 µH, PIMB103T-1R0MS-63, 10mm × 11.2mm × 3mm, 5.3mΩ

**Figure 7-15. SP1: 43℃ (TPS53515), SP2: 35.1℃ (Inductor)**

# 8 Device and Documentation Support

## 8.1 Documentation Support

### *8.1.1 Related Documentation*

Texas Instruments, *Optimizing Transient Response of Internally Compensated dc-dc Converters With Feedforward Capacitor* application note

## 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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## 8.4 Trademarks

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All trademarks are the property of their respective owners.

## 8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 8.6 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision B (July 2015) to Revision C (February 2026) | Page |
|---|---|
| • Updated the numbering format for tables, figures and cross-references throughout the document | 1 |
| • Added VIN-SW DC and VIN-SW < 10ns transient in the *Absolute Maximum Ratings* table | 5 |
| • Updated Figure 7-1 | 24 |

| Changes from Revision A (December 2013) to Revision B (July 2015 ) | Page |
|---|---|
| • Added *Pin Configuration and Functions* section, *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section | 1 |

| Changes from Revision * (August 2013) to Revision A (December 2013) | Page |
|---|---|
| • Added updates to front page graphics | 1 |
| • Added updates to *Electrical Specifications* section | 7 |

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS53515RVER | Active | Production | VQFN-CLIP (RVE) \| 28 | 3000 \| LARGE T&R | ROHS Exempt | NIPDAU \| SN | Level-2-260C-1 YEAR | -40 to 85 | TPS53515 |
| TPS53515RVER.A | Active | Production | VQFN-CLIP (RVE) \| 28 | 3000 \| LARGE T&R | ROHS Exempt | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TPS53515 |
| TPS53515RVER.B | Active | Production | VQFN-CLIP (RVE) \| 28 | 3000 \| LARGE T&R | - | Call TI | Call TI | -40 to 85 | |
| TPS53515RVET | Active | Production | VQFN-CLIP (RVE) \| 28 | 250 \| SMALL T&R | ROHS Exempt | NIPDAU \| SN | Level-2-260C-1 YEAR | -40 to 85 | TPS53515 |
| TPS53515RVET.A | Active | Production | VQFN-CLIP (RVE) \| 28 | 250 \| SMALL T&R | ROHS Exempt | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TPS53515 |
| TPS53515RVET.B | Active | Production | VQFN-CLIP (RVE) \| 28 | 250 \| SMALL T&R | - | Call TI | Call TI | -40 to 85 | |
| TPS53515RVETG4 | Active | Production | VQFN-CLIP (RVE) \| 28 | 250 \| SMALL T&R | ROHS Exempt | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TPS53515 |
| TPS53515RVETG4.A | Active | Production | VQFN-CLIP (RVE) \| 28 | 250 \| SMALL T&R | ROHS Exempt | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TPS53515 |
| TPS53515RVETG4.B | Active | Production | VQFN-CLIP (RVE) \| 28 | 250 \| SMALL T&R | - | Call TI | Call TI | -40 to 85 | |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

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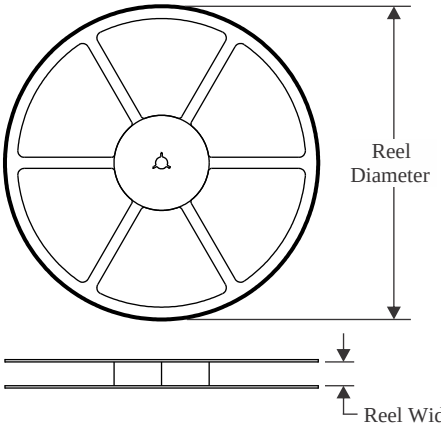
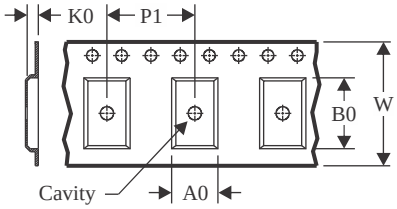
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

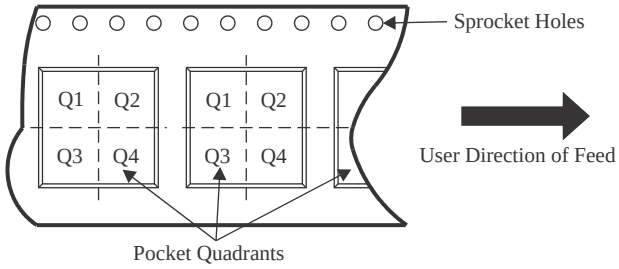



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

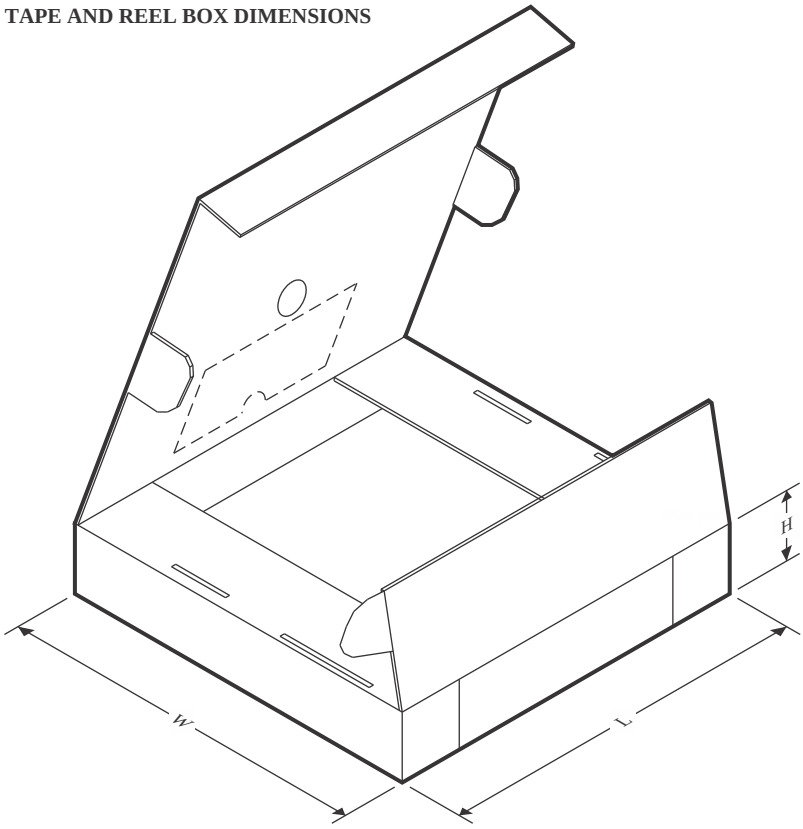
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS53515RVER | VQFN-CLIP | RVE | 28 | 3000 | 330.0 | 12.4 | 3.71 | 4.71 | 1.1 | 8.0 | 12.0 | Q1 |
| TPS53515RVET | VQFN-CLIP | RVE | 28 | 250 | 180.0 | 12.4 | 3.71 | 4.71 | 1.1 | 8.0 | 12.0 | Q1 |
| TPS53515RVETG4 | VQFN-CLIP | RVE | 28 | 250 | 180.0 | 12.4 | 3.71 | 4.71 | 1.1 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

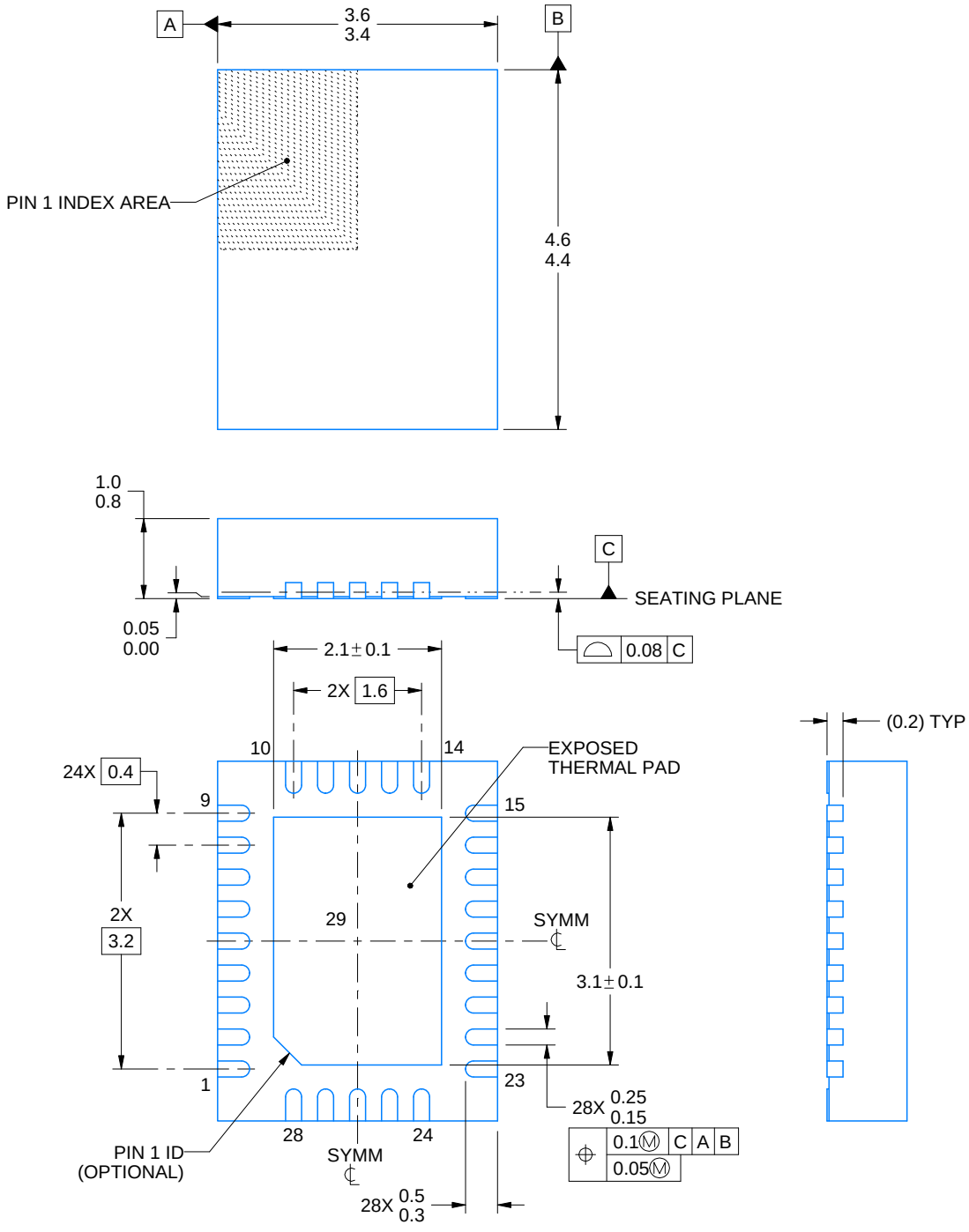
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS53515RVER | VQFN-CLIP | RVE | 28 | 3000 | 346.0 | 346.0 | 33.0 |
| TPS53515RVET | VQFN-CLIP | RVE | 28 | 250 | 210.0 | 185.0 | 35.0 |
| TPS53515RVETG4 | VQFN-CLIP | RVE | 28 | 250 | 210.0 | 185.0 | 35.0 |

# PACKAGE OUTLINE

## RVE0028A

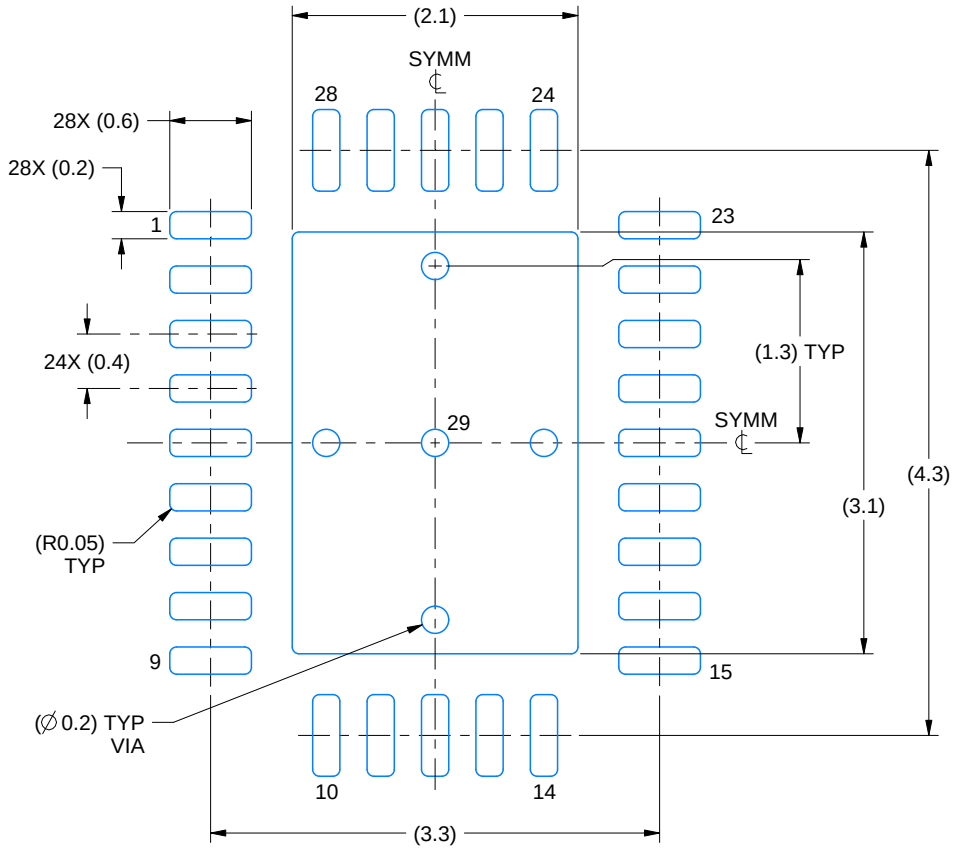
## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

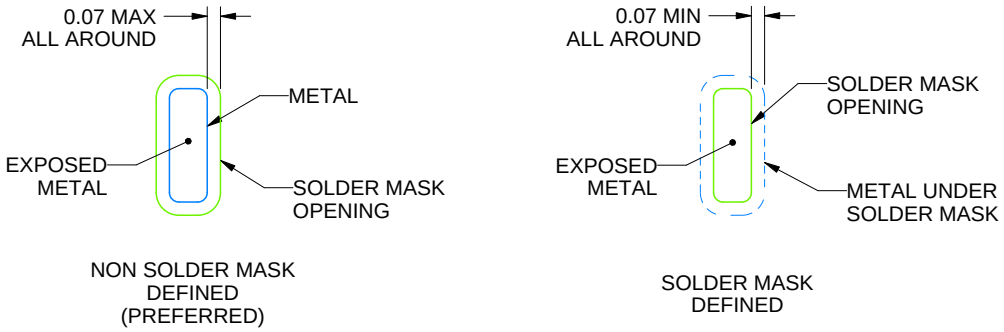



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X




SOLDER MASK DETAILS

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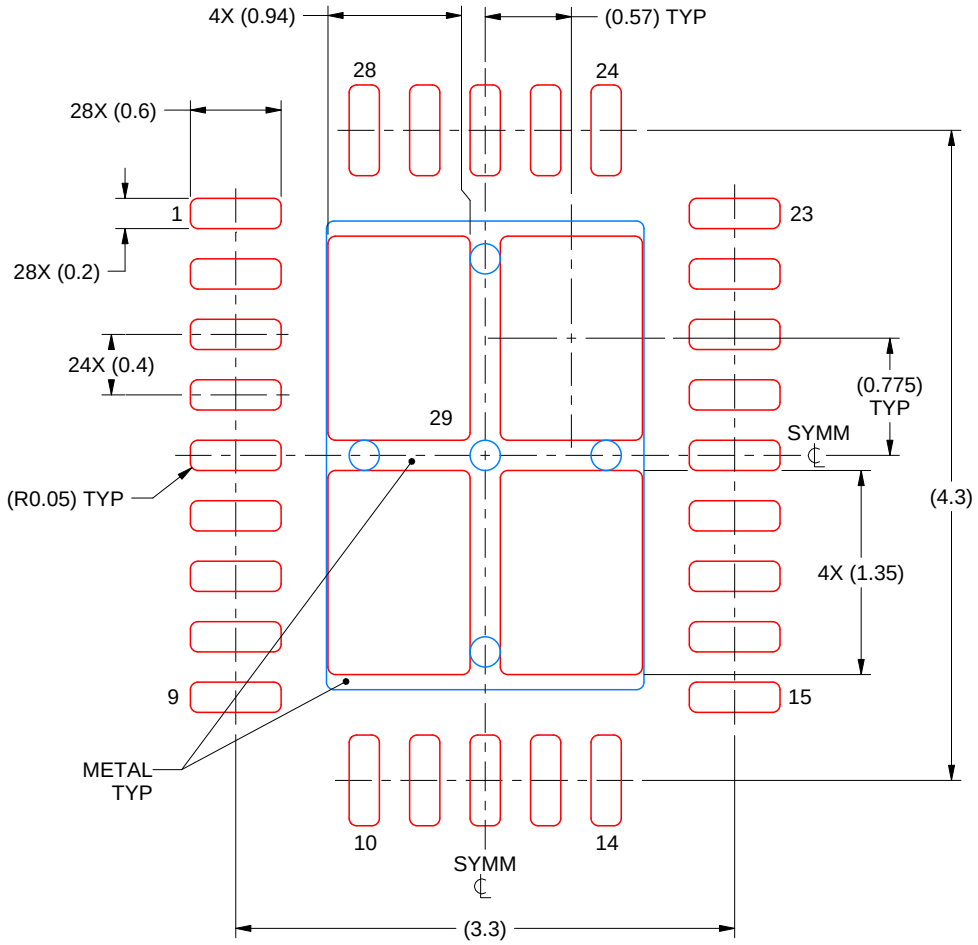
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 29
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

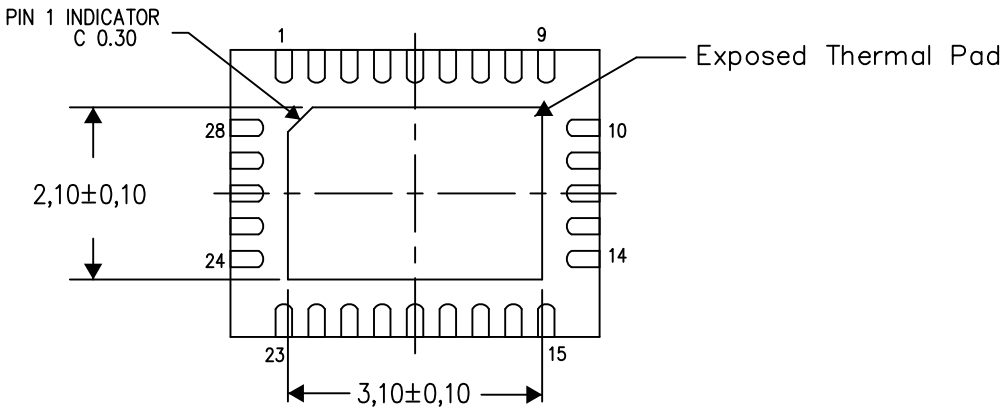
RVE (R–PVQFN–N28) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



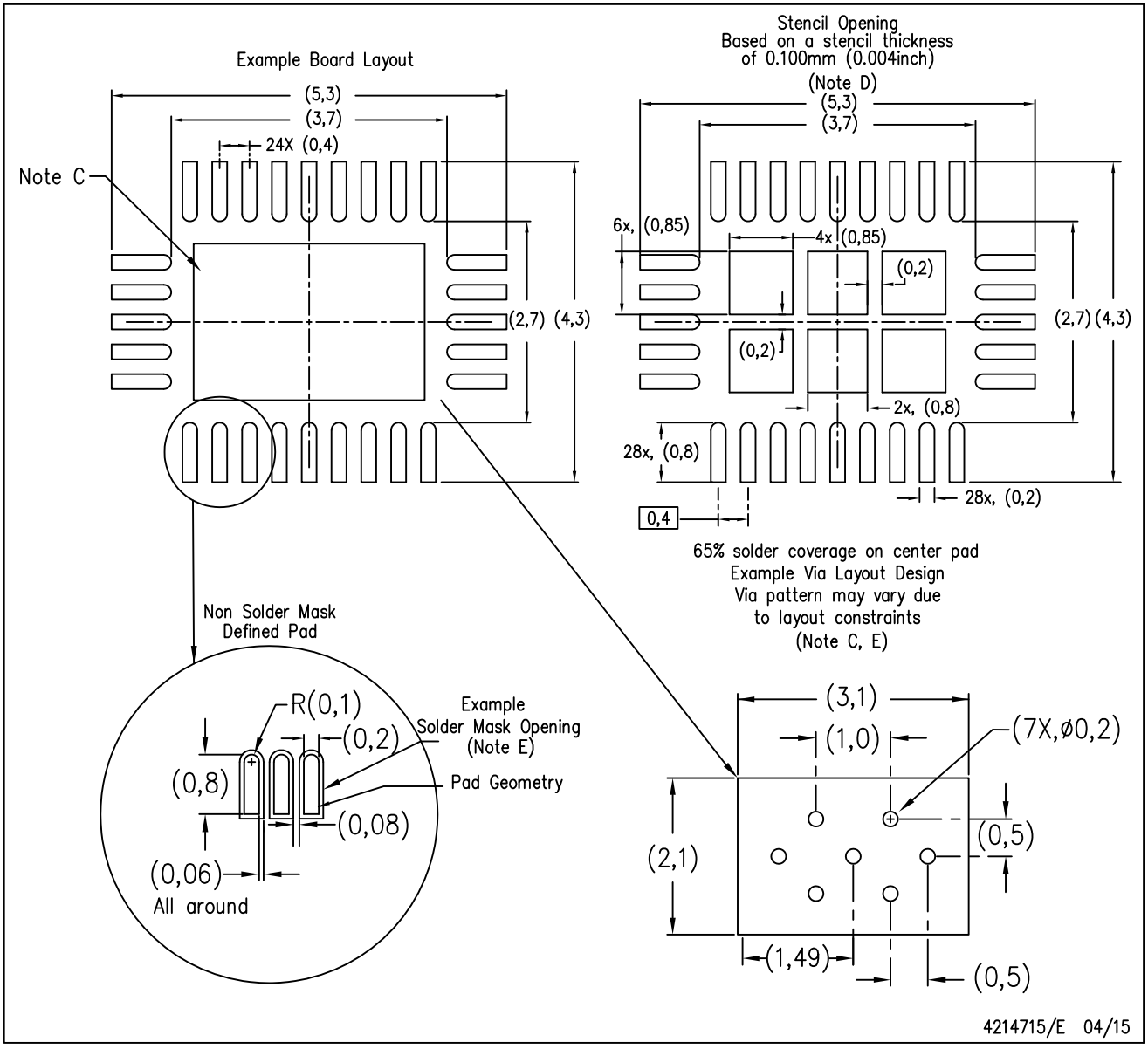

Bottom View

Exposed Thermal Pad Dimensions

4211776/E 04/15

NOTE: All linear dimensions are in millimeters

RVE (R–PWQFN–N28) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Electroformed stencils offer adequate release at thicker values/lower Area Ratios. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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Last updated 10/2025