

TPS536C5 Dual-Channel ($N + M \leq 12$ phase) D-CAP+™, Step-Down, Multiphase Controller with AMD-SVI3 and PMBus Interfaces

1 Features

- Input voltage range: 4.5 V to 17 V
- Output voltage range: 0.25 V to 5.5 V
- Dual output supporting $N+M \leq 12$ phases, $M \leq 6$ phases
- Native trans-inductor voltage regulator (TLVR) topology support
- AMD® SVI3 compliant
- Enhanced D-CAP+™ control to provide superior transient performance with excellent dynamic current sharing
- Programmable loop compensations
- Flexible phase-firing sequencing
- Individual phase current calibrations and reports
- Dynamic phase shedding with programmable current threshold for optimizing efficiency at light and heavy loads
- Fast phase-adding for undershoot reduction
- Driverless configuration for efficient high-frequency switching
- Fully compatible with TI NexFET™ power stages for high-density solutions
- Accurate, adjustable voltage positioning
- Patented AutoBalance™ phase current balancing
- Selectable per-phase current limit
- PMBus™ system interface for telemetry of voltage, current, power, temperature, and fault conditions
- 6.00 × 6.00 mm, 48-pin, 0.4 mm pitch, QFN package

2 Applications

- [Rack server](#)
- [Microserver and tower server](#)
- [High performance computing](#)
- [Baseband unit \(BBU\)](#)

3 Description

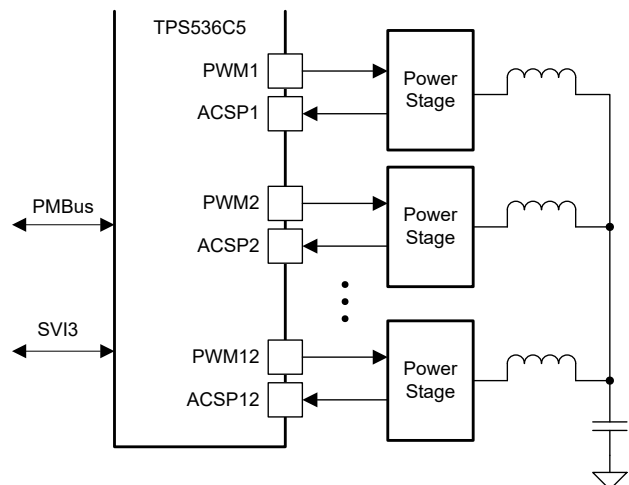
The TPS536C5 is a fully AMD SVI3 compliant step-down controller with dual channels, built-in non-volatile memory (NVM), and PMBus™ interface, and is fully compatible with TI NexFET™ smart power stage. Advanced control features such as D-CAP+™ architecture with undershoot reduction (USR) provide fast transient response, low output capacitance, and good current sharing. The device also provides novel phase interleaving strategy and dynamic phase shedding for efficiency improvement at different loads. Adjustable control of V_{CORE} slew rate and voltage positioning round out the AMD SVI3 features. In addition, the device supports the PMBus communication interface for reporting the telemetry of voltage, current, power, temperature, and fault conditions to the systems. All programmable parameters can be configured by the PMBus interface and can be stored in NVM as the new default values to minimize the external component count.

The TPS536C5 device is offered in a thermally enhanced 48-pin QFN packaged and is rated to operate from -40°C to 125°C .

Device Information

PART NUMBER ⁽¹⁾	PACKAGE	BODY SIZE (NOM)
TPS536C5	QFN (48)	6.00 × 6.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Copyright © 2021, Texas Instruments Incorporated



Table of Contents

1 Features	1	5.3 Support Resources.....	3
2 Applications	1	5.4 Trademarks.....	3
3 Description	1	5.5 Electrostatic Discharge Caution.....	3
4 Revision History	2	5.6 Glossary.....	3
5 Device and Documentation Support	3	6 Mechanical, Packaging, and Orderable Information	4
5.1 Documentation Support.....	3	6.1 Tape and Reel Information.....	4
5.2 Receiving Notification of Documentation Updates.....	3		

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2022	*	Initial Release

5 Device and Documentation Support

5.1 Documentation Support

5.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, Dual channel DCAP+ multiphase controllers: TPS53685, TPS536C5 Technical Reference Manual SLUUCN5

5.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

5.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

5.4 Trademarks

D-CAP+™, NexFET™, AutoBalance™, TI E2E™ are trademarks of Texas Instruments.

PMBus™ is a trademark of SMIF, Inc..

AMD® is a registered trademark of Advanced Micro Devices, Inc..

All trademarks are the property of their respective owners.

5.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

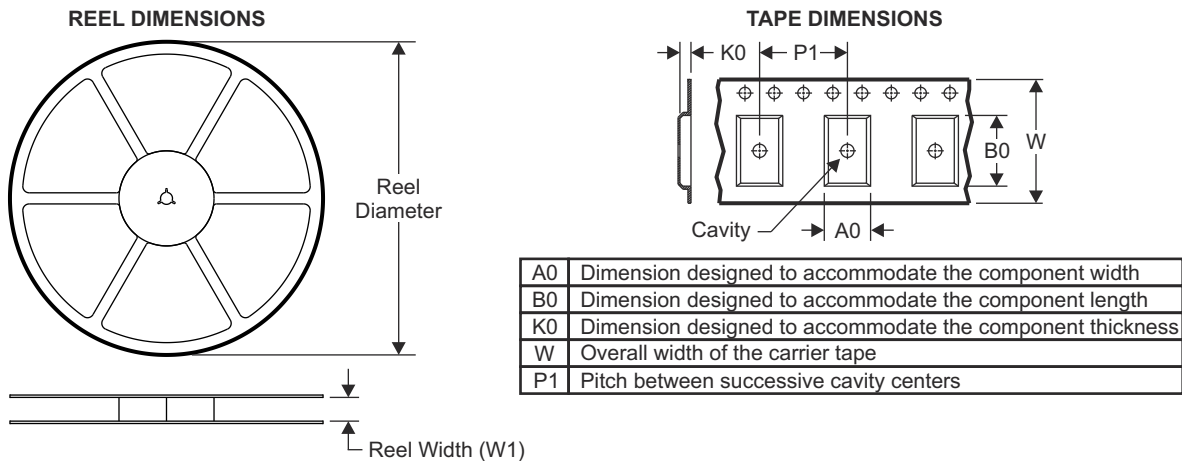
5.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

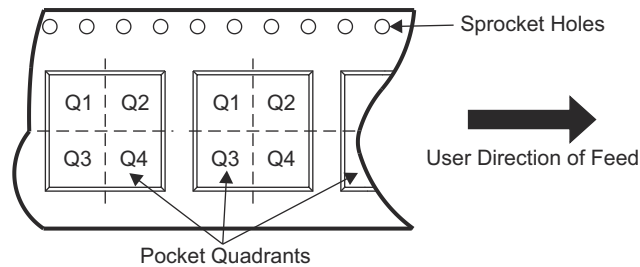
6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

6.1 Tape and Reel Information

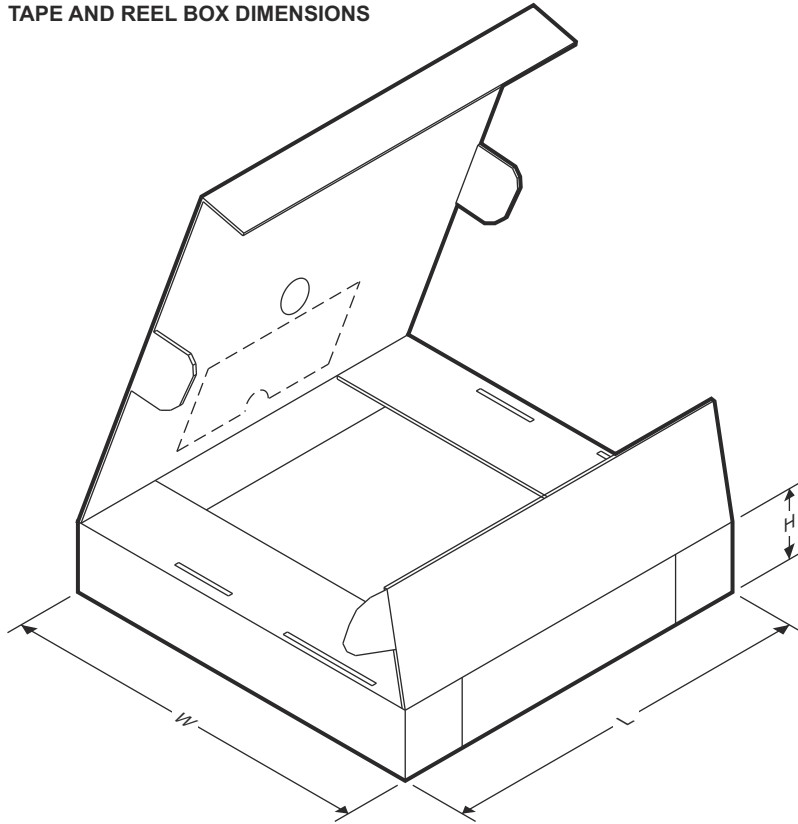


QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS536C5RSLR	VQFN	RSL	48	3000	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS

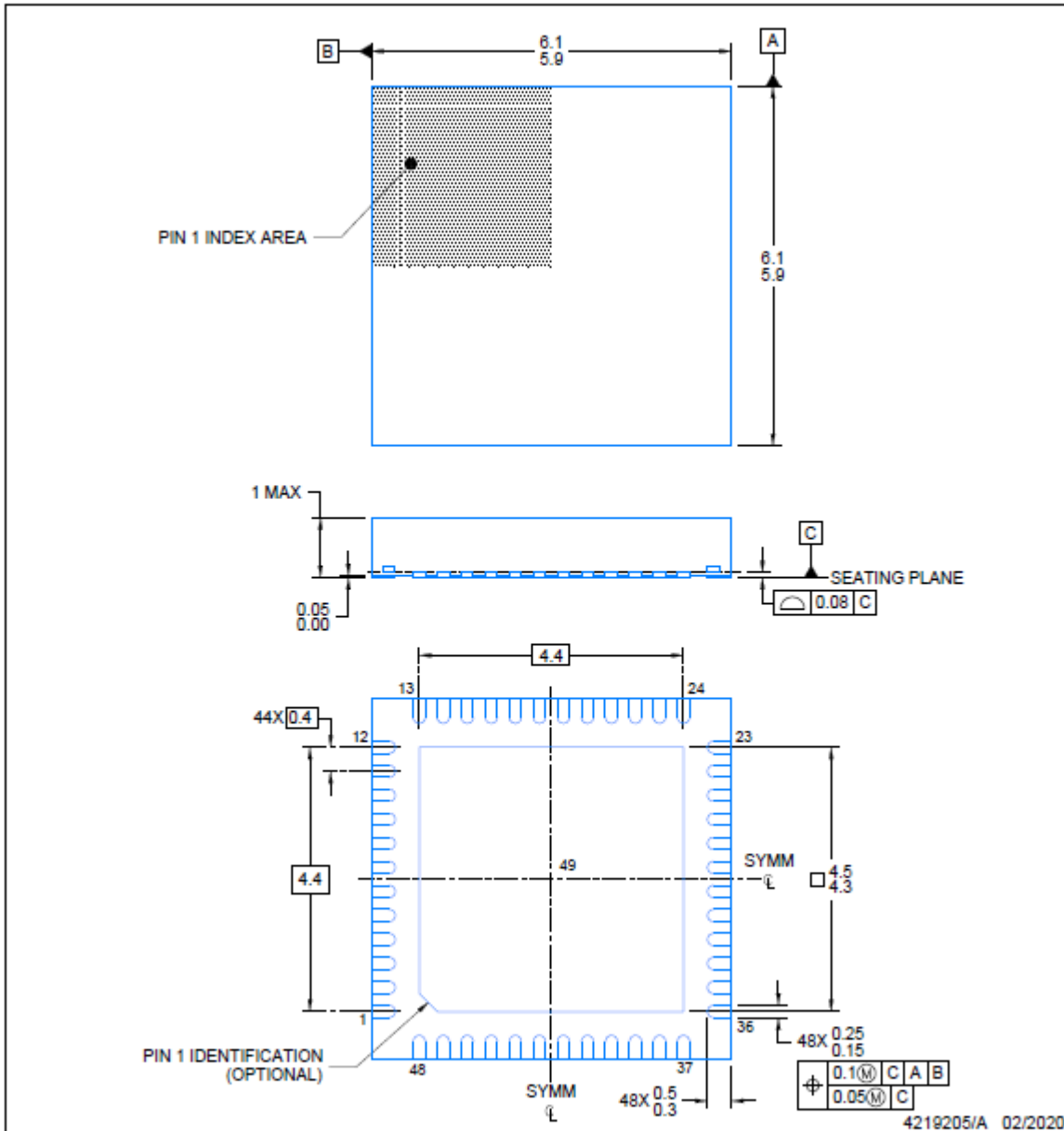


Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS536C5RSLR	VQFN	RSL	48	3000	367.0	367.0	38.0

RSL0048B

PACKAGE OUTLINE
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



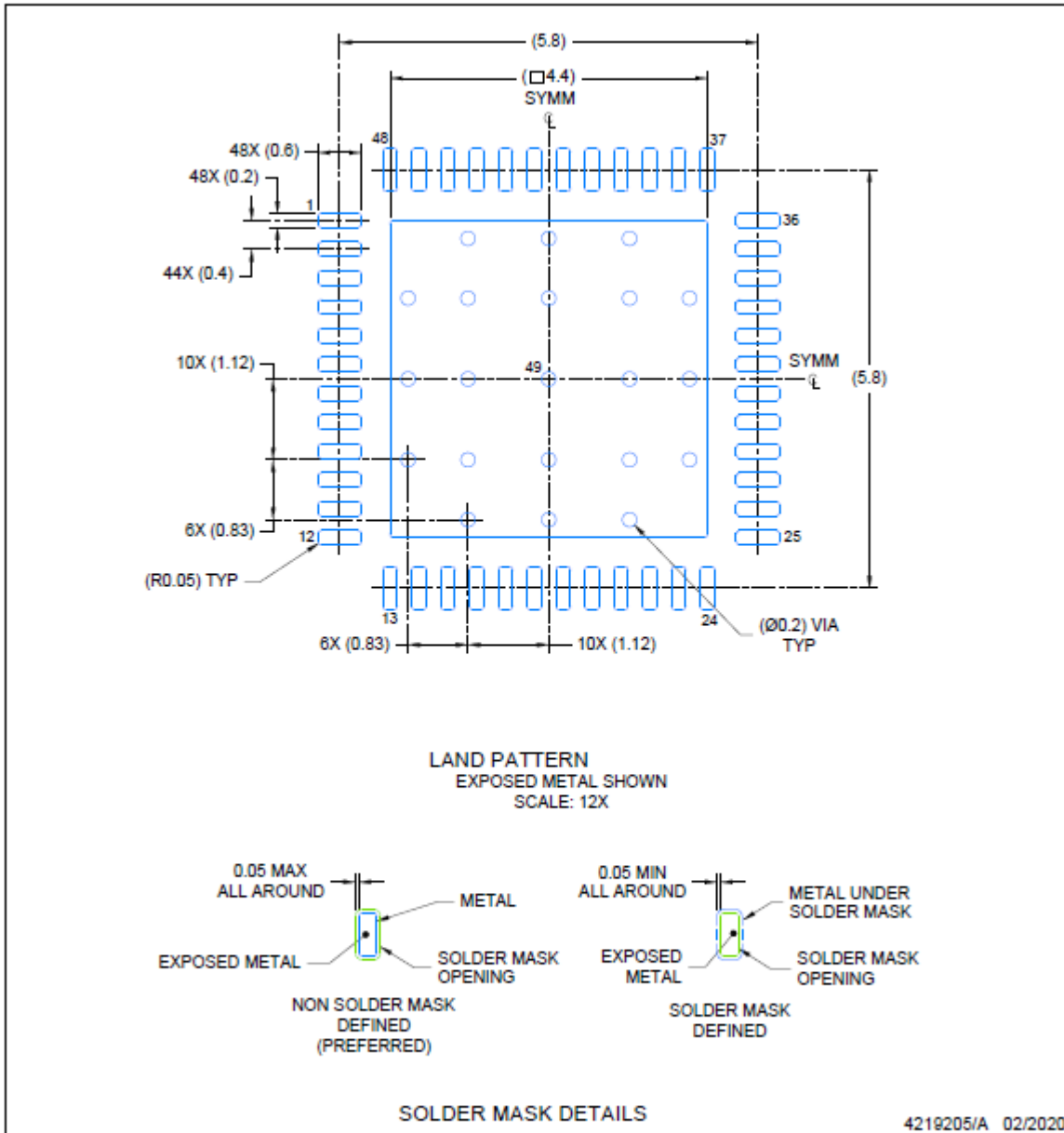
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

RSL0048B

BOARD LAYOUT
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



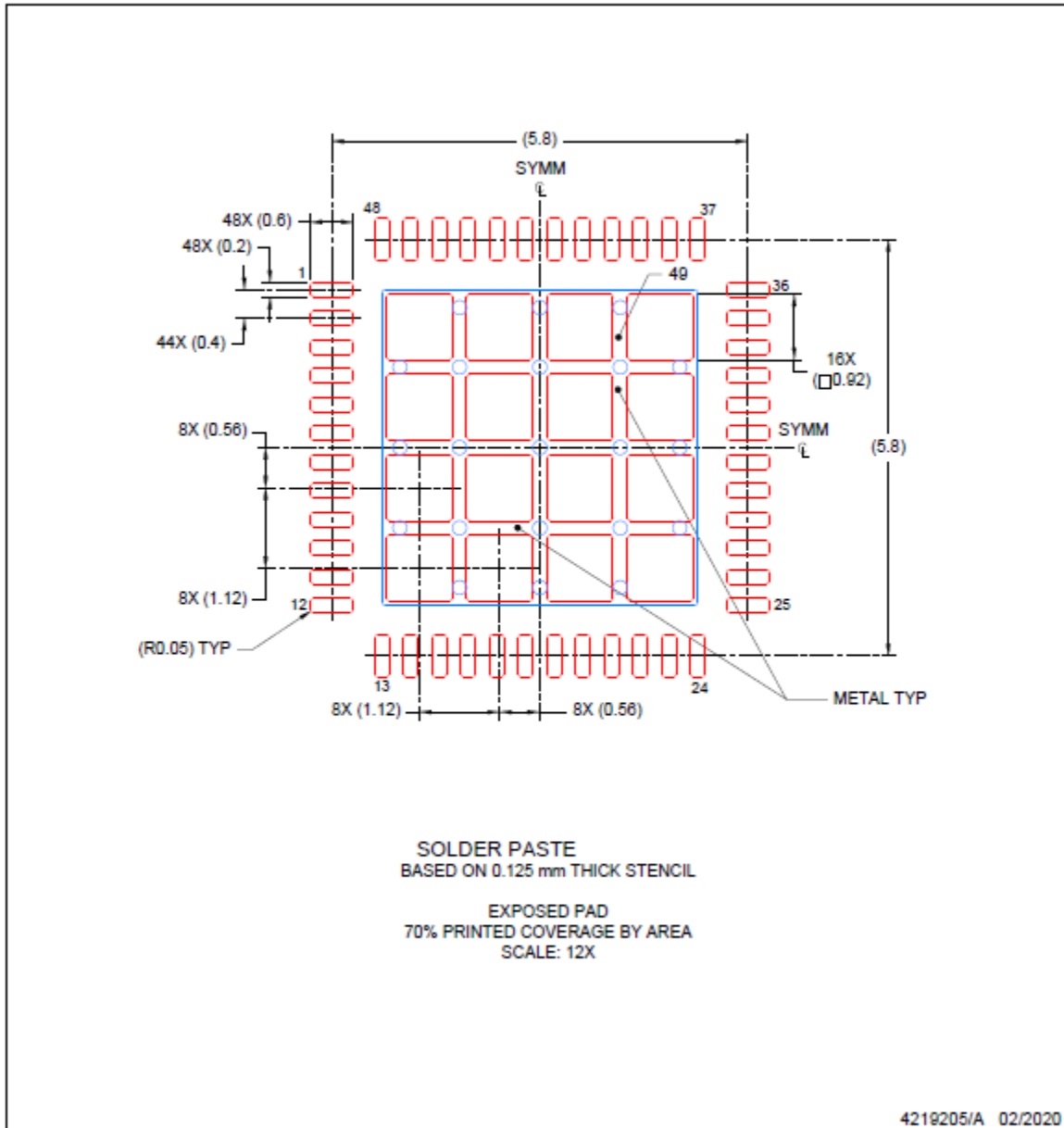
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

RSL0048B

STENCIL DESIGN
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS536C5RSLR	Active	Production	VQFN (RSL) 48	3000 LARGE T&R	Yes	Call TI Nipdauag	Level-3-260C-168 HR	-40 to 105	TPS 536C5
TPS536C5RSLR.A	Active	Production	VQFN (RSL) 48	3000 LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 105	TPS 536C5

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

GENERIC PACKAGE VIEW

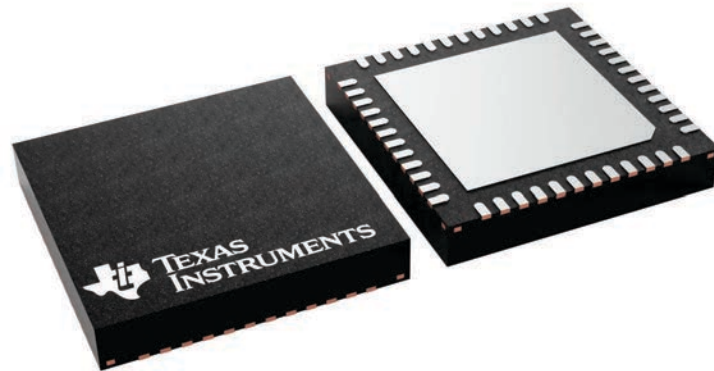
RSL 48

VQFN - 1 mm max height

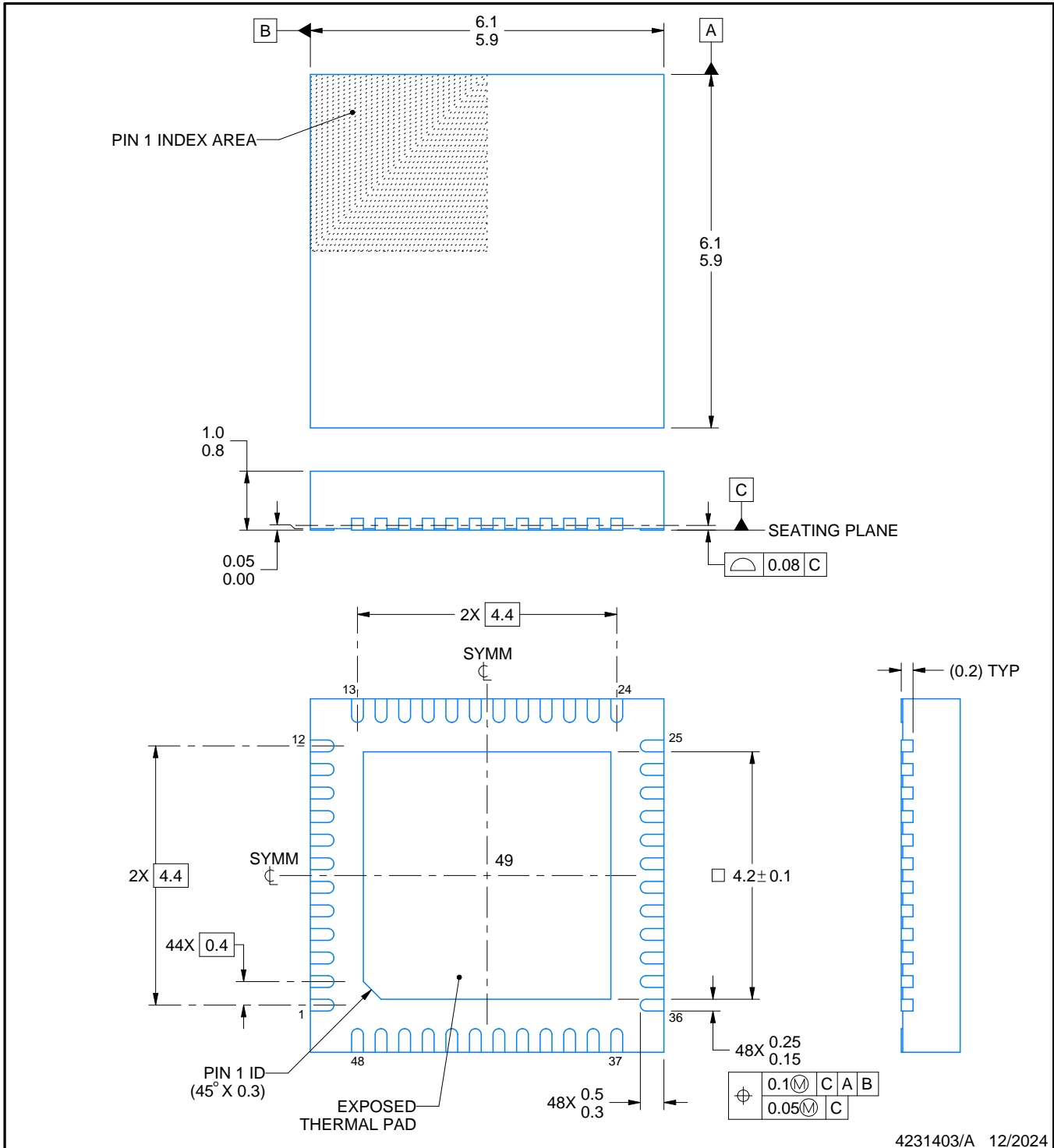
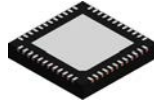
6 x 6, 0.4 mm pitch

QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225749/A



NOTES:

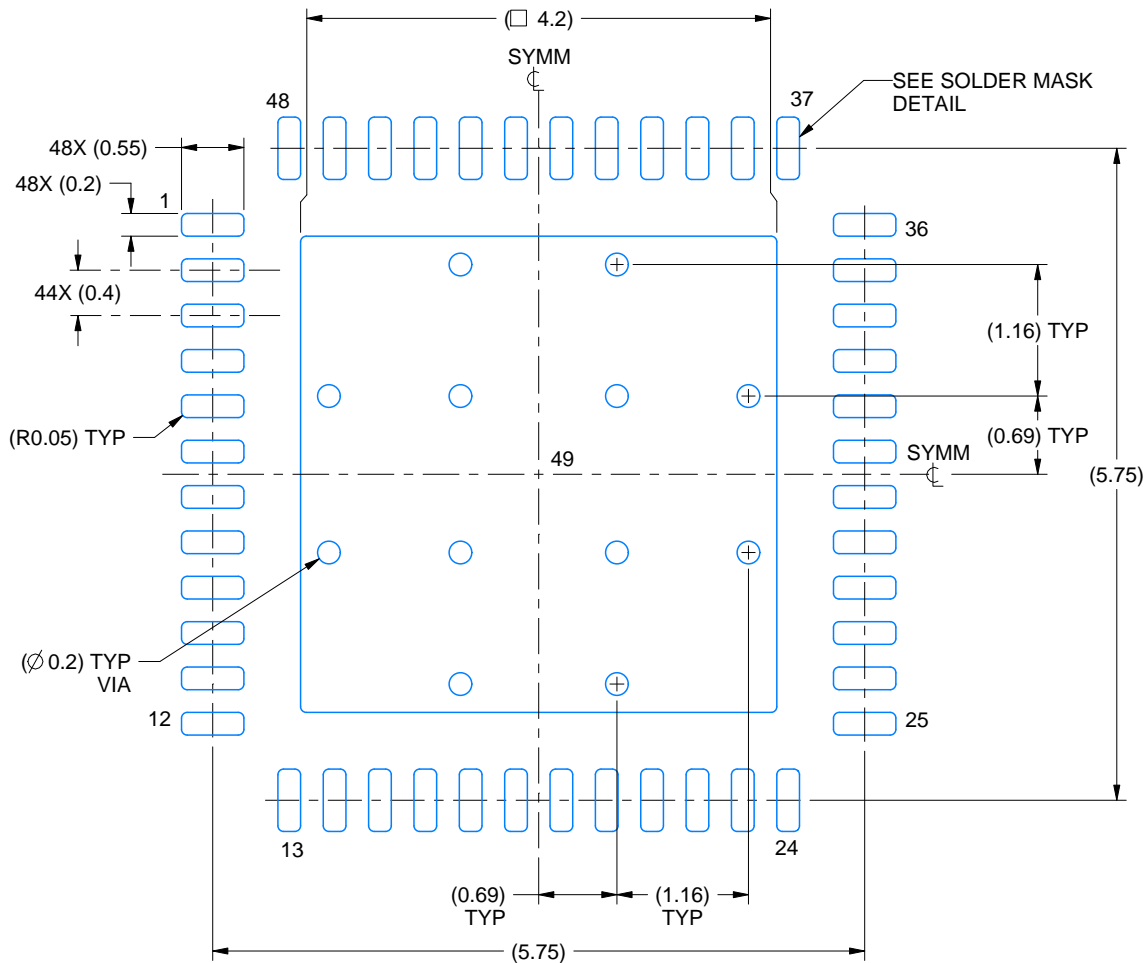
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

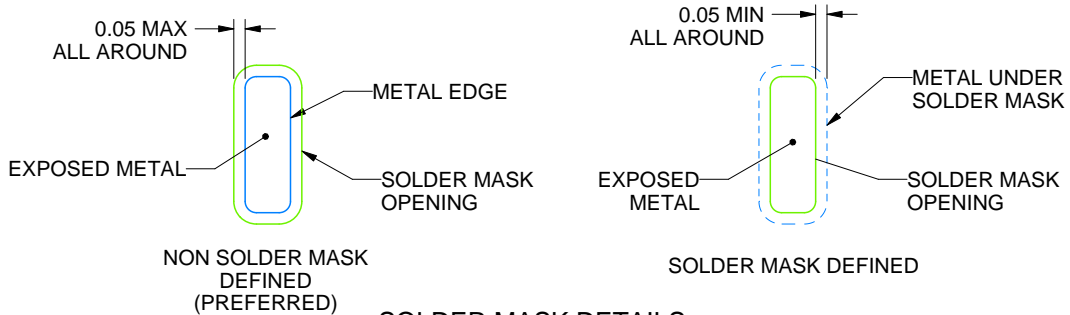
RSL0048G

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4231403/A 12/2024

NOTES: (continued)

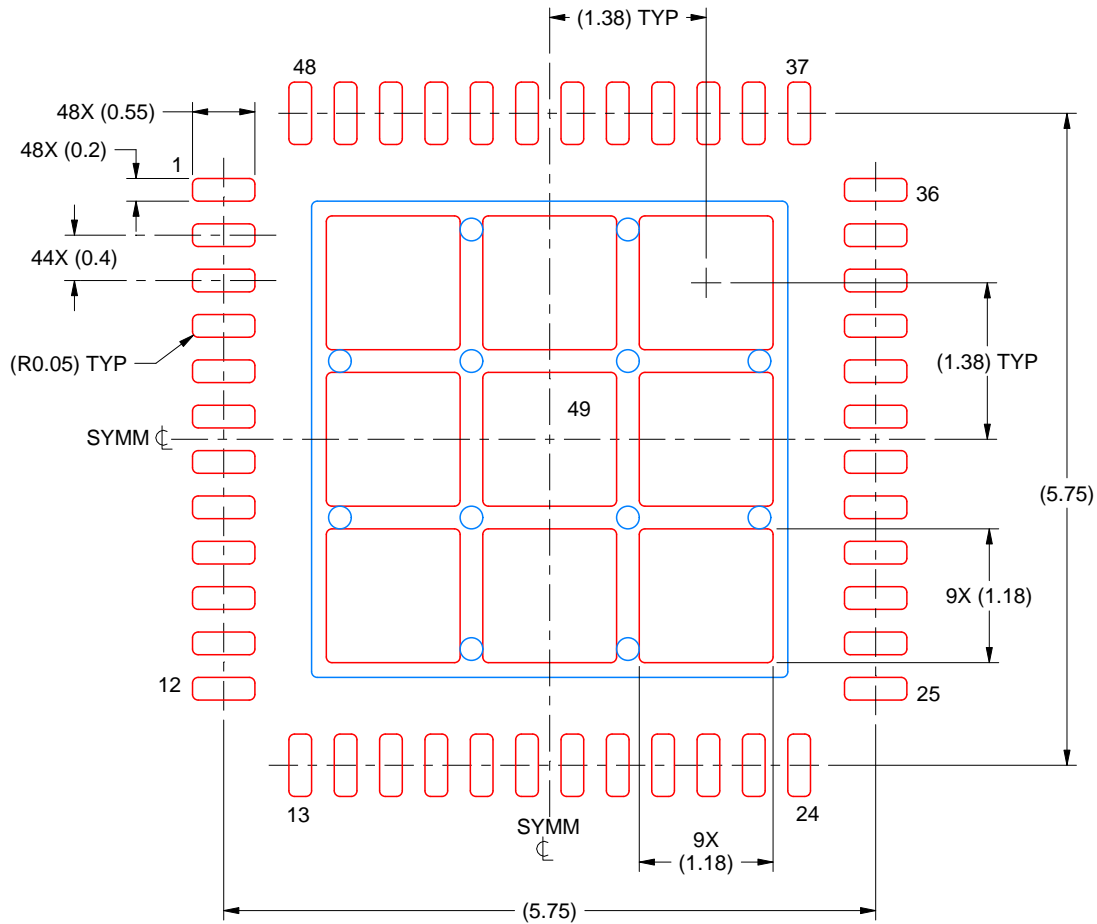
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RSL0048G

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 49
71% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4231403/A 12/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025