TPS6287Cxx 2.8V to 6V Input, up to 50A, Stackable Step-Down Converters With I²C Interface and Telemetry

ADVANCE INFORMATION

1 Features

- Input voltage range: 2.8V to 6V
- Output voltage accuracy: ±0.5%
- Output voltage range from 0.4V to 1.0V
- Internal power MOSFETs: 1.8mΩ and 0.7mΩ
- External compensation
- Optional stacked operation for increased output current capability
- Adjustable switching frequency from 833kHz to 3MHz
- External synchronization
- Forced PWM or power save mode operation
- Optimized load transient operation
- Fixed frequency DCS-Control
- Transient non-synchronous mode
- Adjustable droop compensation
- Optimized for small and low-profile inductors
- I²C-compatible interface with up to 3.4MHz
- Differential remote sense
- Thermal pre-warning and thermal shutdown
- Input and output overvoltage protection
- Output discharge
- Optional spread spectrum clocking
- Telemetry for V_{IN}, Temp, V_{OUT}, and I_{OUT}
- Interrupt output
- Power-good output with window comparator with adjustable thresholds
- Available in 5.0mm × 6.0mm, VQFN package

2 Applications

- FPGA, ASIC, and digital core supply
- Optical networks
- Storage

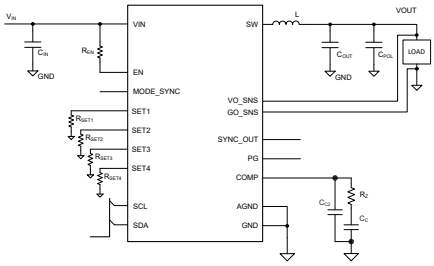
3 Description

The TPS6287Cxx devices are a family of pin-to-pin, up to 50A synchronous step-down DC/DC converters with I²C interface and differential remote sense. Low-resistance power switches allow up to 50A continuous output current at high ambient temperatures. The devices can operate in stacked mode to deliver higher output currents or to spread the power dissipation across multiple devices. In stacked operation, the converters frequencies are synchronized, share a common compensation signal and shift the phases to supply loads with several hundreds of amperes. The TPS6287Cxx family implements a fixed-frequency-DCS-Control scheme with adjustable switching frequency and adjustable loop compensation. The high switching frequency and loop bandwidth is optimized for low-profile- and small-size inductors and low output capacitance. Devices can operate in power-save mode (PSM) for maximum efficiency, or forced-PWM mode for best transient performance and lowest output voltage ripple. The I²C compatible interface offers several control, monitoring, and warning features including telemetry data of input voltage, output voltage, output current, and temperature. Four SET pins can be used to program default settings before start-up.

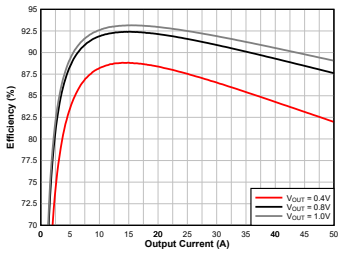
Device Information

PART NUMBER	CURRENT RATING(1)	PACKAGE(2)	PACKAGE SIZE(3)
TPS6287C25(4)	25A	VAA (WQFN-FCRLF, 20)	5mm × 6mm
TPS6287C40(4)	40A		
TPS6287C50	50A		

(1) See the *Device Options* table.
(2) For more information, see Section 7.
(3) The package size (length × width) is a nominal value and includes pins, where applicable.
(4) Preview information (not Advance Information).



TPS6287Cxx Simplified Schematic



Efficiency TPS6287C50 (V_{IN} = 5V; F_{SW} = 833kHz)

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4 Device Options

ORDERABLE PART NUMBER	OUTPUT CURRENT	DEFAULT F_{SW}
TPS6287C25WVAAR(1)	25A	1.0MHz
TPS6287C40WVAAR(1)	40A	0.833MHz
TPS6287C50WVAAR	50A	1.5MHz

(1) Preview information (not Advance Information)

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5 Device and Documentation Support

5.1 Device Support

5.1.1 Third-Party Products Disclaimer

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To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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5.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

5.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

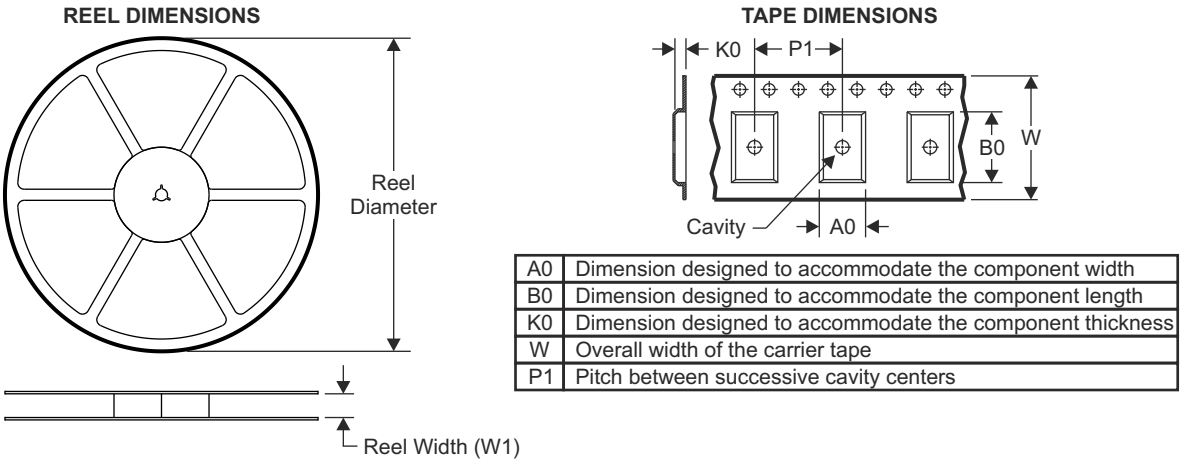
6 Revision History

DATE	REVISION	NOTES
March 2026	*	Initial Release

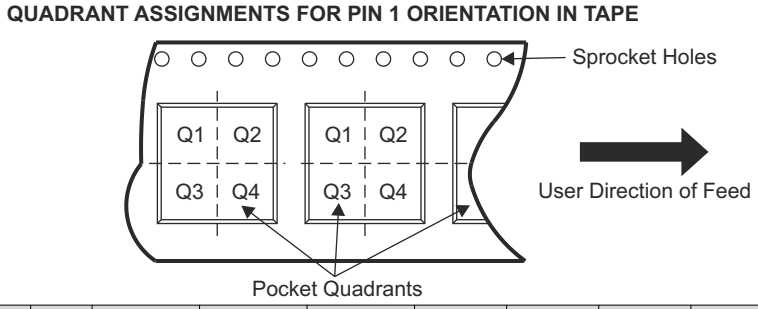
7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Tape and Reel Information



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS6287C50TEWVAAR	WQFN-FCRLF	VAA	20	3000	330.0	12.4	5.25	6.25	0.9	8.0	12.0	Q2
TPS6287C40TAWVAAR	WQFN-FCRLF	VAA	20	3000	330.0	12.4	5.25	6.25	0.9	8.0	12.0	Q2
TPS6287C25TAWVAAR	WQFN-FCRLF	VAA	20	3000	330.0	12.4	5.25	6.25	0.9	8.0	12.0	Q2

ADVANCE INFORMATION

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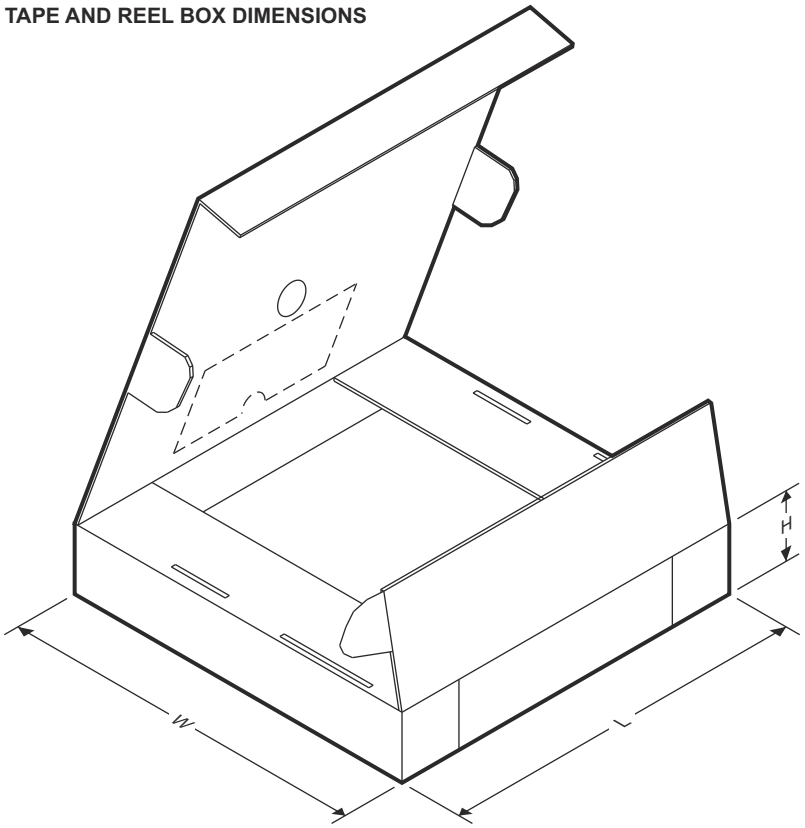
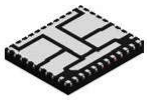
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS6287C50TEWVAAR	WQFN-FCRLF	VAA	20	3000	367	367	35
TPS6287C40TAWVAAR	WQFN-FCRLF	VAA	20	3000	367	367	35
TPS6287C25TAWVAAR	WQFN-FCRLF	VAA	20	3000	367	367	35

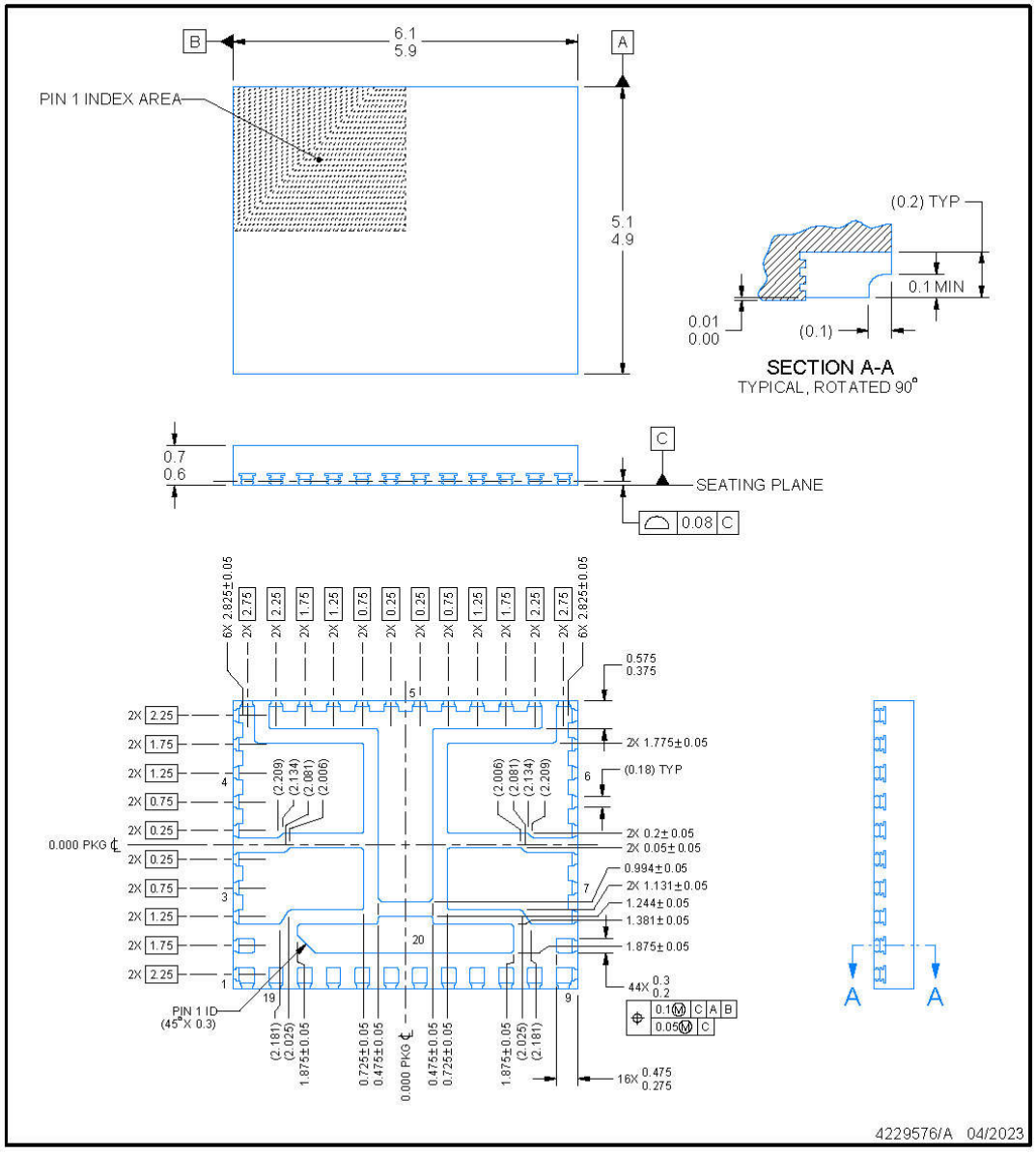
PACKAGE OUTLINE

VAA0020A



WQFN-FCRLF - 0.7 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

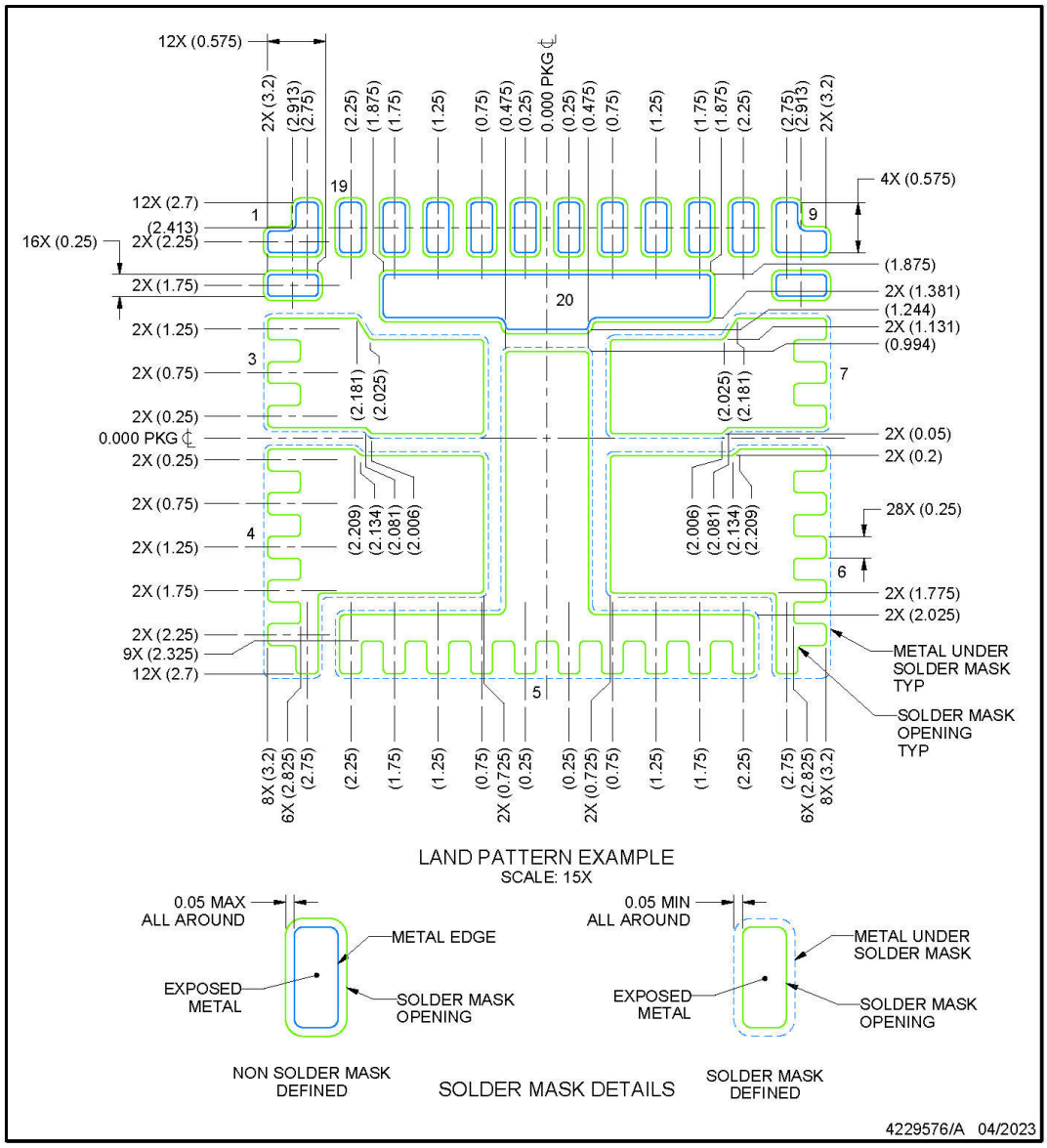
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

VAA0020A — **WQFN-FCRLF - 0.7 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



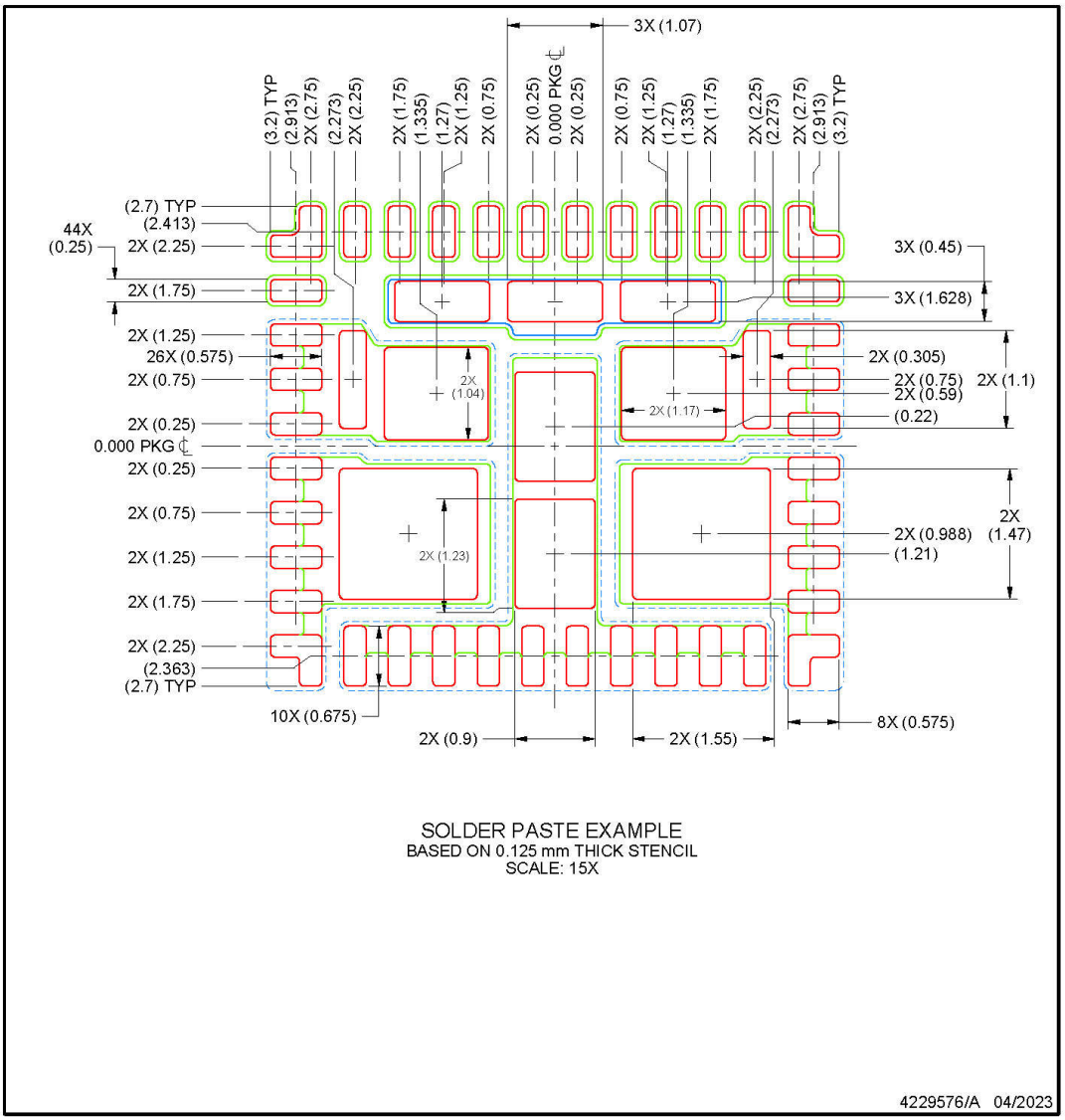
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

VAA0020A — **WQFN-FCRLF - 0.7 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 15X

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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