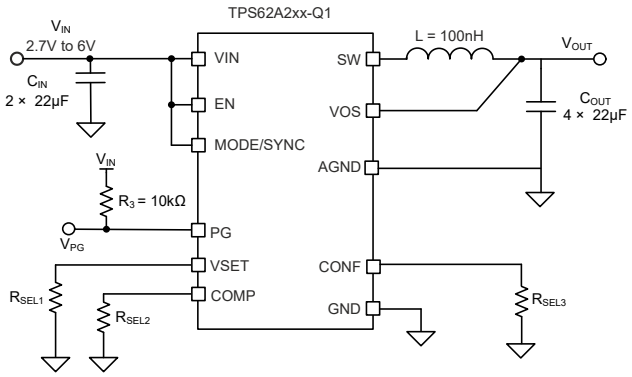
TPS62A2xx-Q1 2.7V to 6V Input, 8A, 10A, 12A Automotive Fast Transient Synchronous Step-Down Converters

1 Features

- AEC-Q100 qualified for automotive applications
  - Temperature grade 1: –40°C to +125°C T_A
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Family of 8A, 10A, and 12A devices
- Input voltage range: 2.7V to 6V
- Output voltage from 0.4V to 3.3V with ±0.8% accuracy in PWM operation
- Switching frequency from 1.5MHz to 4MHz
  - External synchronization through the MODE/SYNC pin
- Fast transient response with COT control
  - Fixed switching frequency during steady-state operation
  - 16 internal compensation settings to reduce output capacitance
- Low $R_{DS(on)}$ MOSFETS: 6.7mΩ and 3.5mΩ
- Minimum on-time of 25ns (maximum) at V_{IN} = 5V
- Selectable FPWM mode through the MODE/SYNC pin
- Programmable spread spectrum clocking
- Precise enable input threshold
- Adjustable soft-start timings
- Active output discharge
- Power-good output with window comparator
- 3mm × 3mm QFN package with wettable flanks

2 Applications

- ADAS domain controller
- Digital cockpit processing unit
- Driver monitoring
- Front camera



Typical Application Schematic for TPS62A2xx-Q1

3 Description

The TPS62A2xx-Q1 series are families of pin-to-pin compatible, high-efficiency, synchronous step-down DC-DC converters capable of delivering continuous output currents of 8A, 10A, and 12A. Using a constant on-time (COT) control topology, these devices provide fast transient response while maintaining fixed switching frequency operation during steady-state conditions.

To enhance loop performance, the devices offer 16 selectable internal compensation settings, enabling higher bandwidth and reducing output capacitance. Integrated low RDS(on) MOSFETs support continuous output up to 12A even at high ambient temperatures.

When R2D is enabled, the switching frequency is selectable through the CONF pin with four discrete options: 1.5MHz, 2.25MHz, 2.5MHz, and 4MHz. The device also supports synchronization to an external clock through the MODE/SYNC pin. In PFM/PWM mode, the device automatically enters power-save mode at light loads to achieve high efficiency across the full load range. The device maintains the output voltage accuracy within ±0.8% in PWM mode. The soft-start feature provides controlled power-up and limits the inrush current.

Device Information

PART NUMBER	OUTPUT CURRENT(3)	PACKAGE(1)	PACKAGE SIZE(2)
TPS62A208-Q1	8A	VAQ (WQFN-FCRLF, 18)	3mm × 3mm
TPS62A210-Q1(4)	10A		
TPS62A212-Q1	12A		

(1) For more information, see Section 7.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) See the *Device Comparison Table*.
(4) Preview information (not Production Data).

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4 Device Comparison Table

DEVICE NUMBER(1)	OUTPUT CURRENT	SPREAD SPECTRUM CLOCKING	SOFT-START TIME	OUTPUT VOLTAGE (V)	FREQUENCY (MHz)	COMPENSATION SETTING	TAM(2)
TPS62A2080QWVAQRQ1	8A	Disabled	0.5ms	Configured through VSET pin	Configured through CONF pin	Configured through COMP pin	Disabled
TPS62A2100QWVAQRQ1 (3)	10A	Disabled	0.5ms	Configured through VSET pin	Configured through CONF pin	Configured through COMP pin	Disabled
TPS62A2120QWVAQRQ1	12A	Disabled	0.5ms	Configured through VSET pin	Configured through CONF pin	Configured through COMP pin	Disabled
TPS62A2121QWVAQRQ1 (3)	12A	Enabled	2ms	Configured through VSET pin	Configured through CONF pin	Configured through COMP pin	Disabled
TPS62A2083QWVAQRQ1 (3)	8A	Enabled	1ms	Configured through VSET pin	Configured through CONF pin	Configured through COMP pin	Disabled
TPS62A2124QWVAQRQ1 (3)	12A	Enabled	0.5ms	1.15 (Fixed)	2.25 (Fixed)	12 (Fixed)	Disabled
TPS62A2106QWVAQRQ1 (3)	10A	Disabled	1ms	0.625 (Fixed)	2 (Fixed)	4 (Fixed)	Disabled
TPS62A2107QWVAQRQ1 (3)	10A	Disabled	1ms	0.94375 (Fixed)	2 (Fixed)	8 (Fixed)	Disabled
TPS62A2125QWVAQRQ1 (3)	12A	Disabled	0.5ms	Configured through VSET pin	Configured through CONF pin	Configured through COMP pin	Enabled

(1) For part numbers with fixed output voltage, frequency, and compensation setting, please connect VSET, CONF, and COMP pins to AGND.
(2) TAM is Transient Non-synchronous mode.
(3) Preview information (not Production Data).

5 Device and Documentation Support

5.1 Device Support

5.1.1 Third-Party Products Disclaimer

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5.2 Documentation Support

5.2.1 Related Documentation

For related documentation, see the following:

Texas Instruments, *TPS62A212-Q1 Buck Converter Evaluation Module* EVM user's guide

5.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

5.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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5.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

5.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

6 Revision History

DATE	REVISION	NOTES
June 2026	*	Initial Release

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS62A2080QWVAQRQ1	Active	Production	WQFN-FCRLF (VAQ) | 18	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A2080Q
TPS62A2120QWVAQRQ1	Active	Production	WQFN-FCRLF (VAQ) | 18	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A2120Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

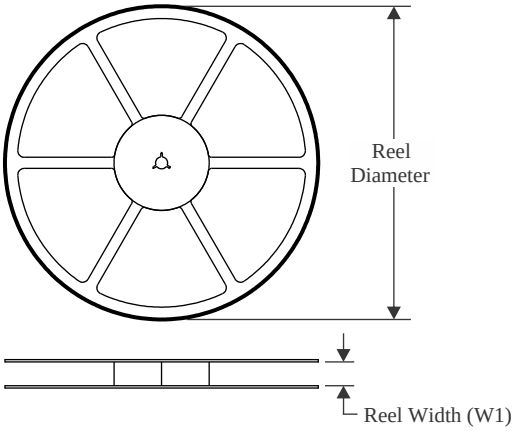
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

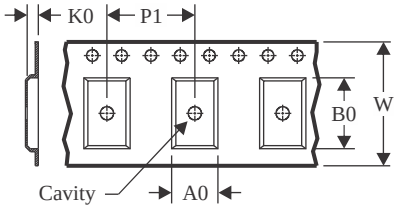
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

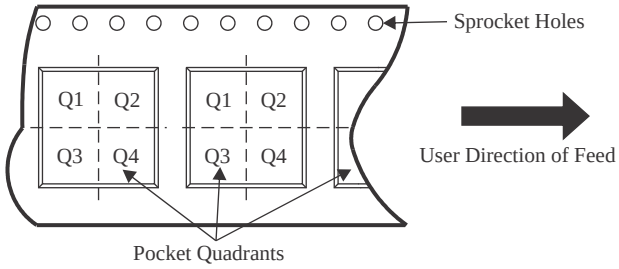


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

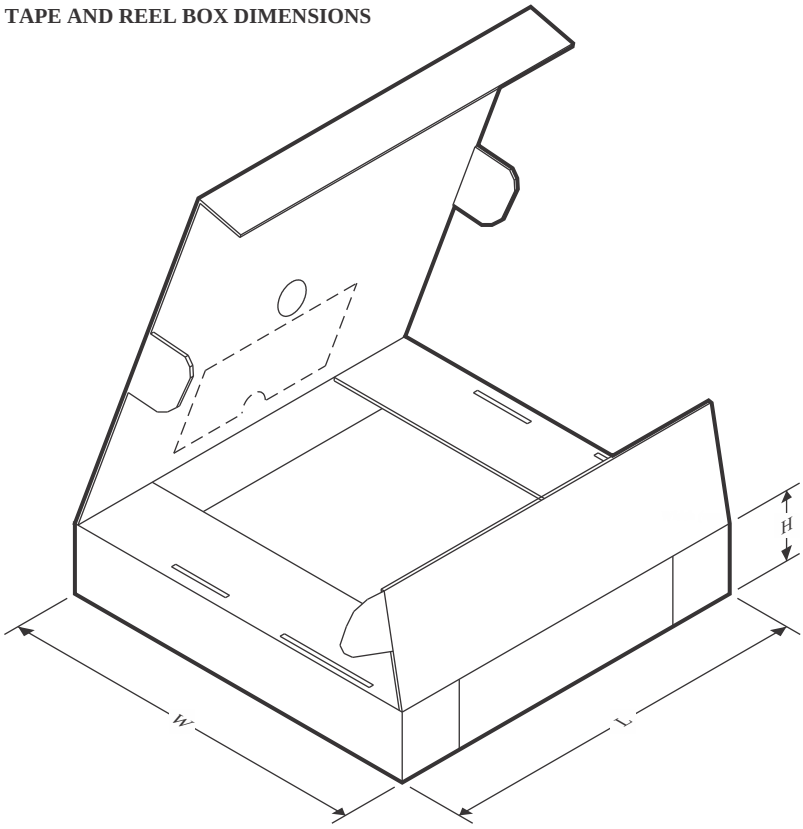
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62A2080QWVAQRQ1	WQFN-FCRLF	VAQ	18	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62A2120QWVAQRQ1	WQFN-FCRLF	VAQ	18	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

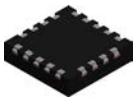


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62A2080QWVAQRQ1	WQFN-FCRLF	VAQ	18	3000	367.0	367.0	35.0
TPS62A2120QWVAQRQ1	WQFN-FCRLF	VAQ	18	3000	367.0	367.0	35.0

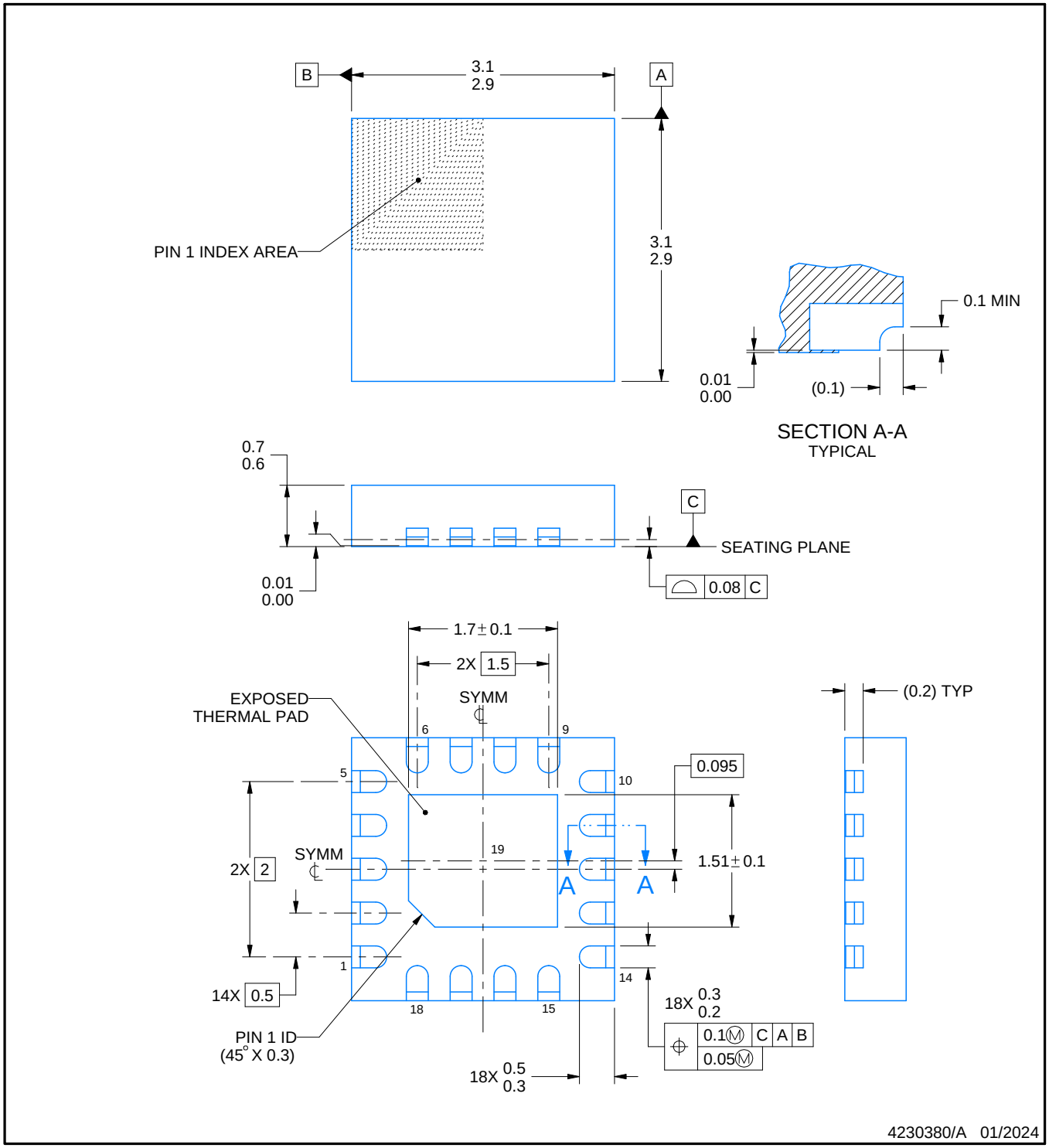
PACKAGE OUTLINE

VAQ0018A



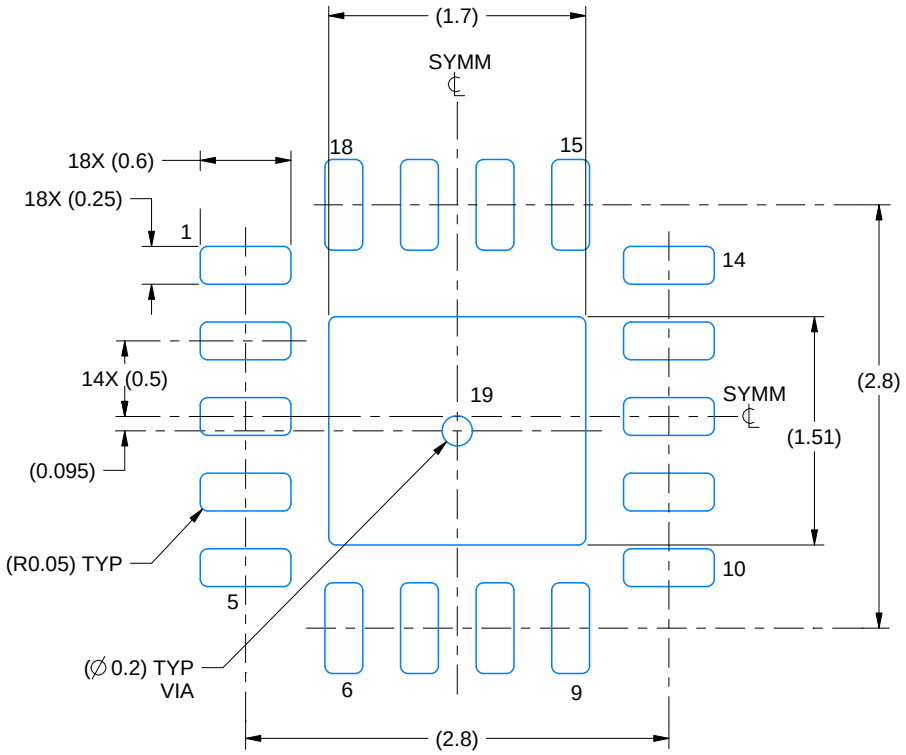
WQFN-FCRLF - 0.7 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

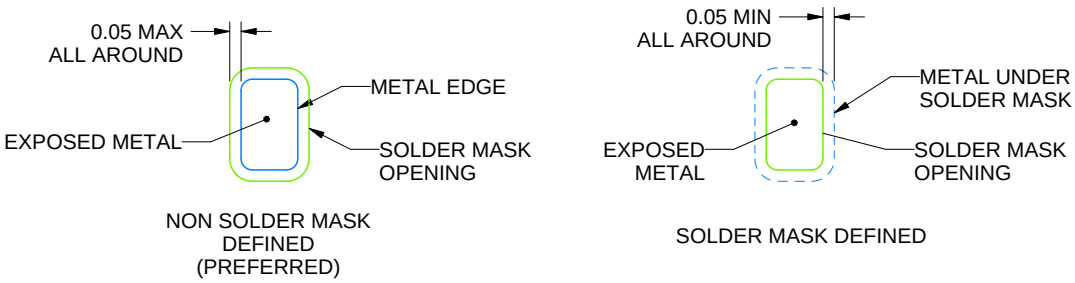


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

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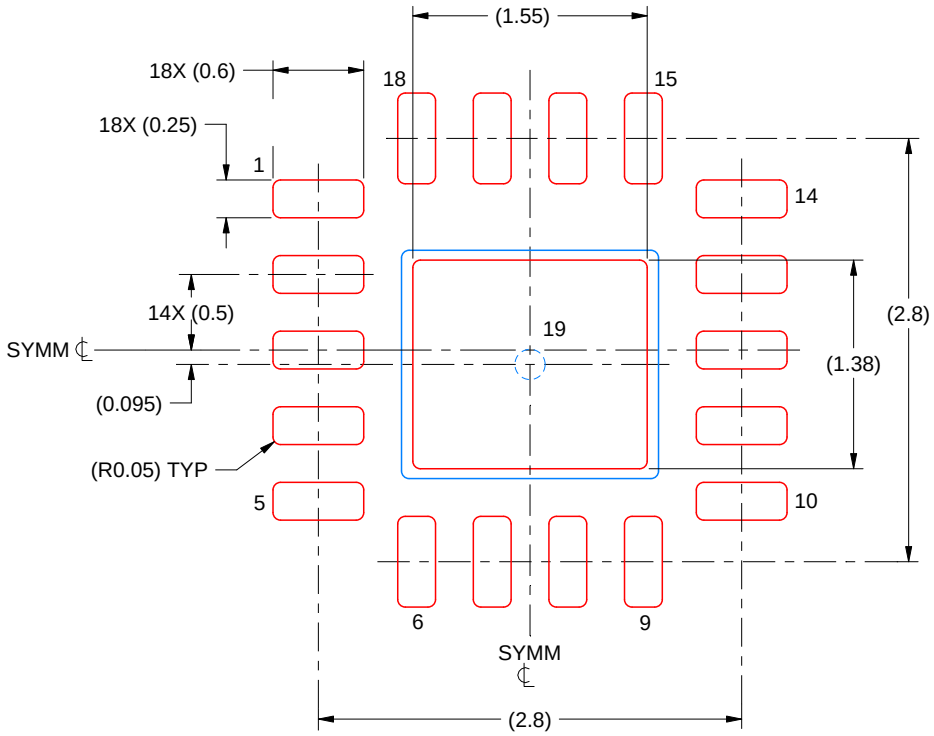
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 19
84% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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