

DUAL-OUTPUT, LOW DROPOUT VOLTAGE REGULATORS WITH INTEGRATED SVS FOR SPLIT VOLTAGE SYSTEMS

 Check for Samples: [TPS70445](#), [TPS70448](#), [TPS70451](#), [TPS70458](#), [TPS70402](#)

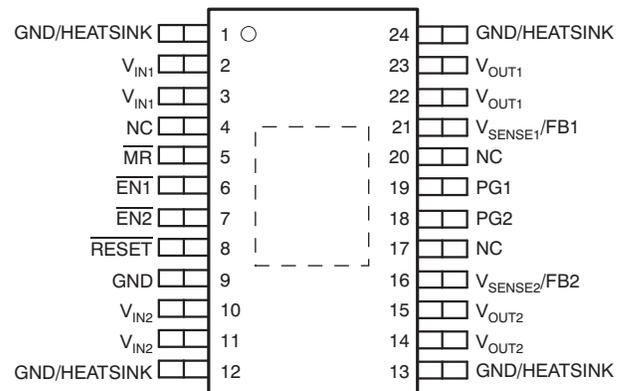
FEATURES

- Dual Output Voltages for Split-Supply Applications
- Independent Enable Functions (See Part Number [TPS703xx](#) for Sequenced Outputs)
- Output Current Range of 1 A on Regulator 1 and 2 A on Regulator 2
- Fast Transient Response
- Voltage Options: 3.3-V/2.5-V, 3.3-V/1.8-V, 3.3-V/1.5-V, 3.3-V/1.2-V, and Dual Adjustable Outputs
- Open Drain Power-On Reset with 120-ms Delay
- Open Drain Power Good for Regulator 1 and Regulator 2
- Ultralow 185 μ A (typ) Quiescent Current
- 2 μ A Input Current During Standby
- Low Noise: 78 μ V_{RMS} Without Bypass Capacitor
- Quick Output Capacitor Discharge Feature
- One Manual Reset Input
- 2% Accuracy Over Load and Temperature
- Undervoltage Lockout (UVLO) Feature
- 24-Pin PowerPAD™ TSSOP Package
- Thermal Shutdown Protection

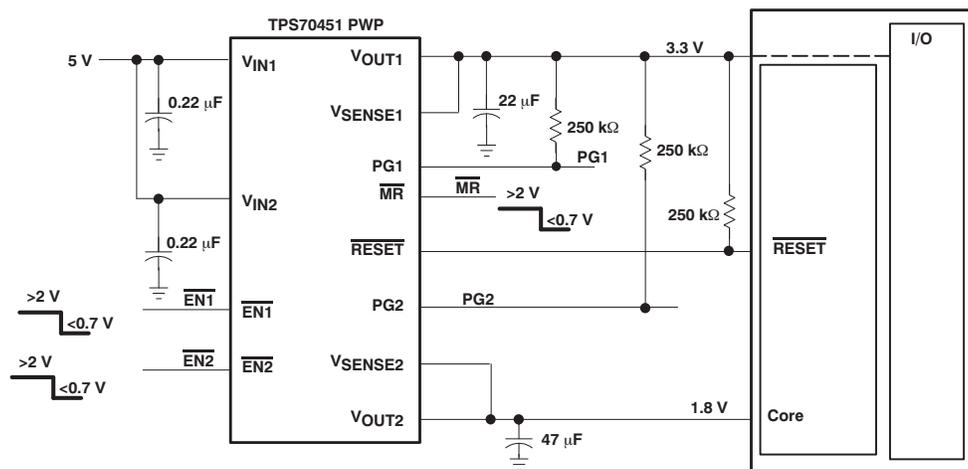
DESCRIPTION

The TPS704xx family of devices consists of dual-output, low-dropout voltage regulators with integrated SVS (RESET, POR, or power on reset) and power good (PG) functions. These devices are capable of supplying 1 A and 2 A by regulator 1 and regulator 2 respectively. Quiescent current is typically 185 μ A at full load. Differentiated features, such as accuracy, fast transient response, SVS supervisory circuit (power on reset), manual reset input, and independent enable functions provide a complete system solution.

PWP PACKAGE
(TOP VIEW)



NC = No internal connection



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The TPS704xx family of voltage regulators offers very low dropout voltage and dual outputs. These devices have extremely low noise output performance without using any added filter bypass capacitors and are designed to have a fast transient response and be stable with 47- μ F low ESR capacitors.

These devices have fixed 3.3-V/2.5-V, 3.3-V/1.8-V, 3.3-V/1.5-V, 3.3-V/1.2-V, and adjustable voltage options. Regulator 1 can support up to 1 A, and regulator 2 can support up to 2 A. Separate voltage inputs allow the designer to configure the source power.

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (typically 160 mV on regulator 1) and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (maximum of 250 μ A over the full range of output current and full range of temperature). This LDO family also features a sleep mode; applying a high signal to EN1 or EN2 (enable) shuts down regulator 1 or regulator 2, respectively. When a high signal is applied to both EN1 and EN2, both regulators enter sleep mode, thereby reducing the input current to 2 μ A at $T_J = +25^\circ\text{C}$.

For each regulator, there is an internal discharge transistor to discharge the output capacitor when the regulator is turned off (disabled).

The PG1 pin reports the voltage condition at V_{OUT1} . The PG1 pin can be used to implement a SVS (RESET, POR, or power on reset) for the circuitry supplied by regulator 1. The PG2 pin reports the voltage conditions at V_{OUT2} . The PG2 pin can be used to implement a SVS (power on reset) for the circuitry supplied by regulator 2.

The TPS704xx features a RESET (SVS, POR, or power on reset). RESET is an active low, open drain output and requires a pull-up resistor for normal operation. When pulled up, RESET goes into a high impedance state (that is, logic high) after a 120-ms delay when both of the following conditions are met. First, V_{IN1} must be above the undervoltage condition. Second, the manual reset (MR) pin must be in a high impedance state. To monitor V_{OUT1} , the PG1 output pin can be connected to MR. To monitor V_{OUT2} , the PG2 output pin can be connected to MR. RESET can be used to drive power on reset or a low-battery indicator. If RESET is not used, it can be left floating.

Internal bias voltages are powered by V_{IN1} and require 2.7 V for full functionality. Each regulator input has an undervoltage lockout circuit that prevents each output from turning on until the respective input reaches 2.5 V.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION⁽¹⁾

| PRODUCT | VOLTAGE (V) ⁽²⁾ | | PACKAGE-LEAD (DESIGNATOR) | SPECIFIED TEMPERATURE RANGE (T _J) | ORDERING NUMBER | TRANSPORT MEDIA, QUANTITY |
|----------|----------------------------|-------------------|------------------------------|---|--------------------|------------------------------|
| | V _{OUT1} | V _{OUT2} | | | | |
| TPS70402 | Adjustable | Adjustable | HTSSOP-24 (PWP) | –40°C to +125°C | TPS70402PWP | Tube, 60 |
| | | | | | TPS70402PWPR | Tape and Reel, 2000 |
| TPS70445 | 3.3 V | 1.2 V | HTSSOP-24 (PWP) | –40°C to +125°C | TPS70445PWP | Tube, 60 |
| | | | | | TPS70445PWPR | Tape and Reel, 2000 |
| TPS70448 | 3.3 V | 1.5 V | HTSSOP-24 (PWP) | –40°C to +125°C | TPS70448PWP | Tube, 60 |
| | | | | | TPS70448PWPR | Tape and Reel, 2000 |
| TPS70451 | 3.3 V | 1.8 V | HTSSOP-24 (PWP) | –40°C to +125°C | TPS70451PWP | Tube, 60 |
| | | | | | TPS70451PWPR | Tape and Reel, 2000 |
| TPS70458 | 3.3 V | 2.5 V | HTSSOP-24 (PWP) | –40°C to +125°C | TPS70458PWP | Tube, 60 |
| | | | | | TPS70458PWPR | Tape and Reel, 2000 |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at ti.com.

(2) For fixed 1.20 V operation, tie FB to OUT.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Over operating free-air temperature range (unless otherwise noted).

| | TPS704xx | UNIT |
|---|---|------|
| Input voltage range: V _{IN1} , V _{IN2} ⁽²⁾ | –0.3 to +7 | V |
| Voltage range at $\overline{EN1}$, $\overline{EN2}$ | –0.3 to +7 | V |
| Output voltage range (V _{OUT1} , V _{SENSE1}) | 5.5 | V |
| Output voltage range (V _{OUT2} , V _{SENSE2}) | 5.5 | V |
| Maximum RESET, PG1, PG2 voltage | 7 | V |
| Maximum MR voltage | V _{IN1} | V |
| Peak output current | Internally limited | — |
| Continuous total power dissipation | See Dissipation Ratings Table | — |
| Operating virtual junction temperature range, T _J | –40 to +150 | °C |
| Storage temperature range, T _{stg} | –65 to +150 | °C |
| ESD rating, HBM | 2 | kV |

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are tied to network ground.

DISSIPATION RATINGS

| PACKAGE | AIR FLOW (CFM) | $T_A \leq +25^\circ\text{C}$ | DERATING FACTOR | $T_A = +70^\circ\text{C}$ | $T_A = +85^\circ\text{C}$ |
|--------------------|----------------|------------------------------|-----------------|---------------------------|---------------------------|
| PWP ⁽¹⁾ | 0 | 3.067W | 30.67mW/°C | 1.687W | 1.227W |
| | 250 | 4.115W | 41.15mW/°C | 2.265W | 1.646W |

(1) This parameter is measured with the recommended copper heat sink pattern on a 4-layer PCB, 1 oz. copper on a 4-in by 4-in ground layer. For more information, refer to TI technical brief [SLMA002](#).

RECOMMENDED OPERATING CONDITIONS

Over operating temperature range (unless otherwise noted).

| | MIN | MAX | UNIT |
|---|------|------|------|
| Input voltage, V_I ⁽¹⁾ (regulator 1 and 2) | 2.7 | 6 | V |
| Output current, I_O (regulator 1) | 0 | 1 | A |
| Output current, I_O (regulator 2) | 0 | 2 | A |
| Output voltage range (for adjustable option) | 1.22 | 5.5 | V |
| Operating virtual junction temperature, T_J | -40 | +125 | °C |

(1) To calculate the minimum input voltage for maximum output current, use the following equation: $V_{I(\min)} = V_{O(\max)} + V_{DO(\max \text{ load})}$.

ELECTRICAL CHARACTERISTICS

Over recommended operating junction temperature range ($T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$), V_{IN1} or $V_{IN2} = V_{OUT(nom)} + 1\text{ V}$, $I_O = 1\text{ mA}$, $\overline{EN} = 0\text{ V}$, $C_{OUT1} = 22\text{ }\mu\text{F}$, and $C_{OUT2} = 47\text{ }\mu\text{F}$ (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT | |
|---|--|---|--|---------------------------------|-------|-------|----------------------------|----|
| V_O | Reference voltage | $2.7\text{ V} < V_{IN} < 6\text{ V}$, $T_J = +25^\circ\text{C}$ | FB connected to V_O | | 1.22 | | V | |
| | | $2.7\text{ V} < V_{IN} < 6\text{ V}$, | FB connected to V_O | 1.196 | | 1.244 | | |
| | 1.2 V Output (V_{OUT2}) | $2.7\text{ V} < V_{IN} < 6\text{ V}$, | $T_J = +25^\circ\text{C}$ | | 1.2 | | | |
| | | $2.7\text{ V} < V_{IN} < 6\text{ V}$, | | 1.176 | | 1.224 | | |
| | 1.5 V Output (V_{OUT2}) | $2.7\text{ V} < V_{IN} < 6\text{ V}$, | $T_J = +25^\circ\text{C}$ | | 1.5 | | | |
| | | $2.7\text{ V} < V_{IN} < 6\text{ V}$, | | 1.47 | | 1.53 | | |
| | 1.8 V Output (V_{OUT2}) | $2.8\text{ V} < V_{IN} < 6\text{ V}$, | $T_J = +25^\circ\text{C}$ | | 1.8 | | | |
| | | $2.8\text{ V} < V_{IN} < 6\text{ V}$, | | 1.764 | | 1.836 | | |
| | 2.5 V Output (V_{OUT2}) | $3.5\text{ V} < V_{IN} < 6\text{ V}$, | $T_J = +25^\circ\text{C}$ | | 2.5 | | | |
| | | $3.5\text{ V} < V_{IN} < 6\text{ V}$, | | 2.45 | | 2.55 | | |
| 3.3 V Output (V_{OUT2}) | $4.3\text{ V} < V_{IN} < 6\text{ V}$, | $T_J = +25^\circ\text{C}$ | | 3.3 | | | | |
| | $4.3\text{ V} < V_{IN} < 6\text{ V}$, | | 3.234 | | 3.366 | | | |
| Quiescent current (GND current) for regulator 1 and regulator 2, $\overline{EN1} = \overline{EN2} = 0\text{ V}^{(1)}$ | | See ⁽²⁾ | $T_J = +25^\circ\text{C}$ | | 185 | | μA | |
| | | See ⁽²⁾ | | | | 250 | | |
| Output voltage line regulation ($\Delta V_O/V_O$) for regulator 1 and regulator 2 ⁽³⁾ | | $V_O + 1\text{ V} < V_{IN} \leq 6\text{ V}$, | $T_J = +25^\circ\text{C}^{(1)}$ | | 0.01 | | %V | |
| | | $V_O + 1\text{ V} < V_{IN} \leq 6\text{ V}$ | ⁽¹⁾ | | | 0.1 | | |
| Load regulation for V_{OUT1} and V_{OUT2} | | $T_J = +25^\circ\text{C}$ | | | 1 | | mV | |
| V_n | Output noise voltage (TPS70451) | Regulator 1 | BW = 300 Hz to 50 kHz, $C_O = 33\text{ }\mu\text{F}$, $T_J = +25^\circ\text{C}$ | | 79 | | μV_{RMS} | |
| | | Regulator 2 | | | 77 | | | |
| Output current limit | | Regulator 1 | $V_{OUT} = 0\text{ V}$ | | 1.75 | 2.2 | A | |
| | | Regulator 2 | | | 3.8 | 4.5 | | |
| Thermal shutdown junction temperature | | | | | +150 | | $^\circ\text{C}$ | |
| I_i | Standby current (standby) | Regulator 1 | $\overline{EN1} = V_{IN}$, $\overline{EN2} = V_{IN}$ | $T_J = +25^\circ\text{C}$ | 1 | 2 | μA | |
| | | Regulator 2 | $\overline{EN1} = V_{IN}$, $\overline{EN2} = V_{IN}$ | | | 10 | | |
| PSRR | Power-supply ripple rejection (TPS70451) | Regulator 1 | $f = 1\text{ kHz}$ | $T_J = +25^\circ\text{C}^{(1)}$ | 65 | | dB | |
| | | Regulator 2 | $f = 1\text{ kHz}$ | $T_J = +25^\circ\text{C}^{(1)}$ | 60 | | | |
| RESET Terminal | | | | | | | | |
| Minimum input voltage for valid $\overline{\text{RESET}}$ | | $I_{\text{RESET}} = 300\text{ }\mu\text{A}$, | $V_{(\text{RESET})} \leq 0.8\text{ V}$ | | 1.0 | 1.3 | V | |
| $t_{(\text{RESET})}$ | | $\overline{\text{RESET}}$ pulse duration | | | 80 | 120 | 160 | ms |
| Output low voltage | | $V_{IN} = 3.5\text{ V}$, | $I_{(\text{RESET})} = 1\text{ mA}$ | | 0.15 | 0.4 | V | |
| Leakage current | | $V_{(\text{RESET})} = 6\text{ V}$ | | | | 1 | μA | |

(1) Minimum input operating voltage is 2.7 V or $V_{O(\text{typ})} + 1\text{ V}$, whichever is greater. Maximum input voltage = 6 V , minimum output current = 1 mA .

(2) $I_O = 1\text{ mA}$ to 1 A for Regulator 1 and 1 mA to 2 A for Regulator 2.

(3) If $V_O < 1.8\text{ V}$ then $V_{\text{Imax}} = 6\text{ V}$, $V_{\text{Imin}} = 2.7\text{ V}$:
 Line regulation (mV) = (%/V) $\times V_O \times \frac{(V_{\text{Imax}} - 2.7)}{100} \times 1000$
 If $V_O > 2.5\text{ V}$ then $V_{\text{Imax}} = 6\text{ V}$, $V_{\text{Imin}} = V_O + 1\text{ V}$:
 Line regulation (mV) = (%/V) $\times V_O \times \frac{[V_{\text{Imax}} - (V_O + 1)]}{100} \times 1000$

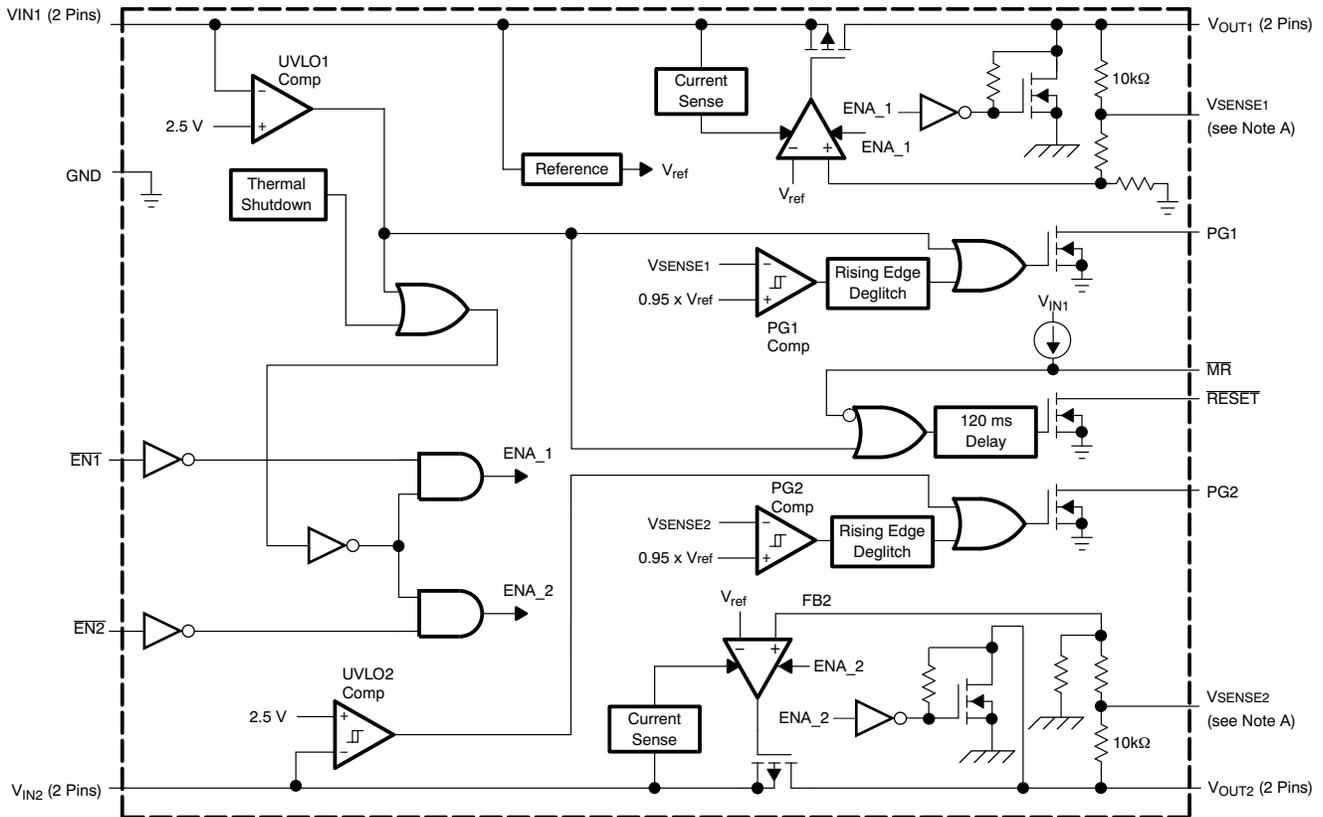
ELECTRICAL CHARACTERISTICS (continued)

Over recommended operating junction temperature range ($T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$), V_{IN1} or $V_{IN2} = V_{OUT(nom)} + 1\text{ V}$,
 $I_O = 1\text{ mA}$,
 $\overline{EN} = 0\text{ V}$, $C_{OUT1} = 22\text{ }\mu\text{F}$, and $C_{OUT2} = 47\text{ }\mu\text{F}$ (unless otherwise noted).

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|-----|------|------|---------------|
| V_{IN1}/V_{IN2} Terminal | | | | | |
| UVLO threshold | | 2.4 | | 2.65 | V |
| UVLO hysteresis | | | 110 | | mV |
| PG1/PG2 Terminal | | | | | |
| Minimum input voltage for valid PGx | $I_{(PGx)} = 300\text{ }\mu\text{A}$, $V_{(PGx)} \leq 0.8\text{ V}$ | | 1.0 | 1.3 | V |
| Trip threshold voltage | V_O decreasing | 92 | 95 | 98 | % V_{OUT} |
| Hysteresis voltage | Measured at V_O | | 0.5 | | % V_{OUT} |
| $t_{r(PGx)}$ | Rising edge deglitch | | 30 | | μs |
| Output low voltage | $V_{IN} = 2.7\text{ V}$, $I_{(PGx)} = 1\text{ mA}$ | | 0.15 | 0.4 | V |
| Leakage current | $V_{(PGx)} = 6\text{ V}$ | | | 1 | μA |
| EN1/EN2 Terminal | | | | | |
| High-level \overline{ENx} input voltage | | 2 | | | V |
| Low-level \overline{ENx} input voltage | | | | 0.7 | V |
| Input current (\overline{ENx}) | | -1 | | 1 | μA |
| MR Terminal | | | | | |
| High-level input voltage | | 2 | | | V |
| Low-level input voltage | | | | 0.7 | V |
| Pull-up current source | | | 6 | | μA |
| V_{OUT1} Terminal | | | | | |
| Dropout voltage ⁽⁴⁾ | $I_O = 1\text{ A}$, $V_{IN1} = 3.2\text{ V}$ $T_J = +25^\circ\text{C}$ | | 160 | | mV |
| | $I_O = 1\text{ A}$, $V_{IN1} = 3.2\text{ V}$ | | | 250 | |
| Peak output current | 2 ms pulse width | | 1.2 | | A |
| Discharge transistor current | $V_{OUT1} = 1.5\text{ V}$ | | 7.5 | | mA |
| V_{OUT2} Terminal | | | | | |
| Peak output current | 2 ms pulse width | | 3 | | A |
| Discharge transistor current | $V_{OUT2} = 1.5\text{ V}$ | | 7.5 | | mA |
| FB Terminal | | | | | |
| Input current: TPS70402 | FB = 1.8 V | | | 1 | μA |

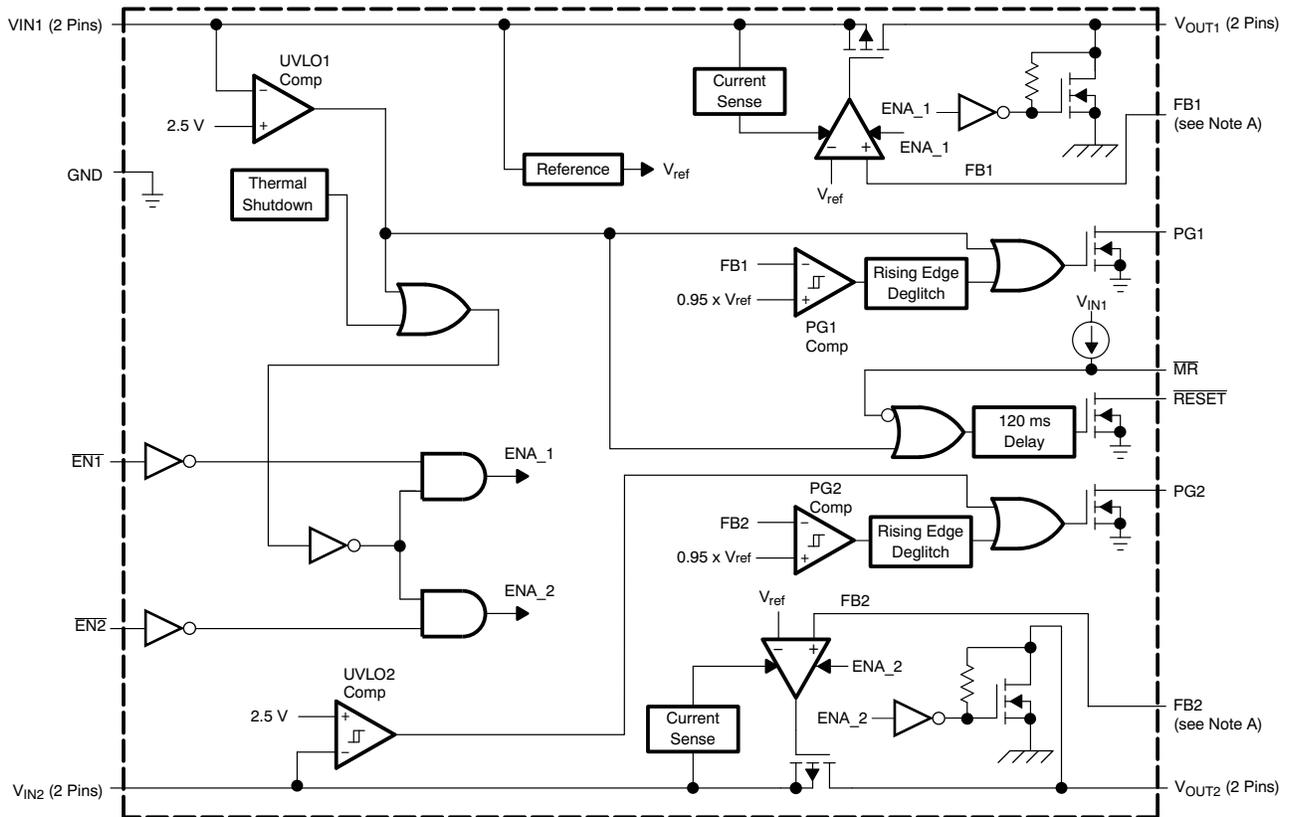
(4) Input voltage (V_{IN1} or V_{IN2}) = $V_{O(typ)} - 100\text{ mV}$. For 1.5-V, 1.8-V, and 2.5-V regulators, the dropout voltage is limited by input voltage range. The 3.3-V regulator input is set to 3.2 V to perform this test.

DEVICE INFORMATION
Fixed Voltage Version



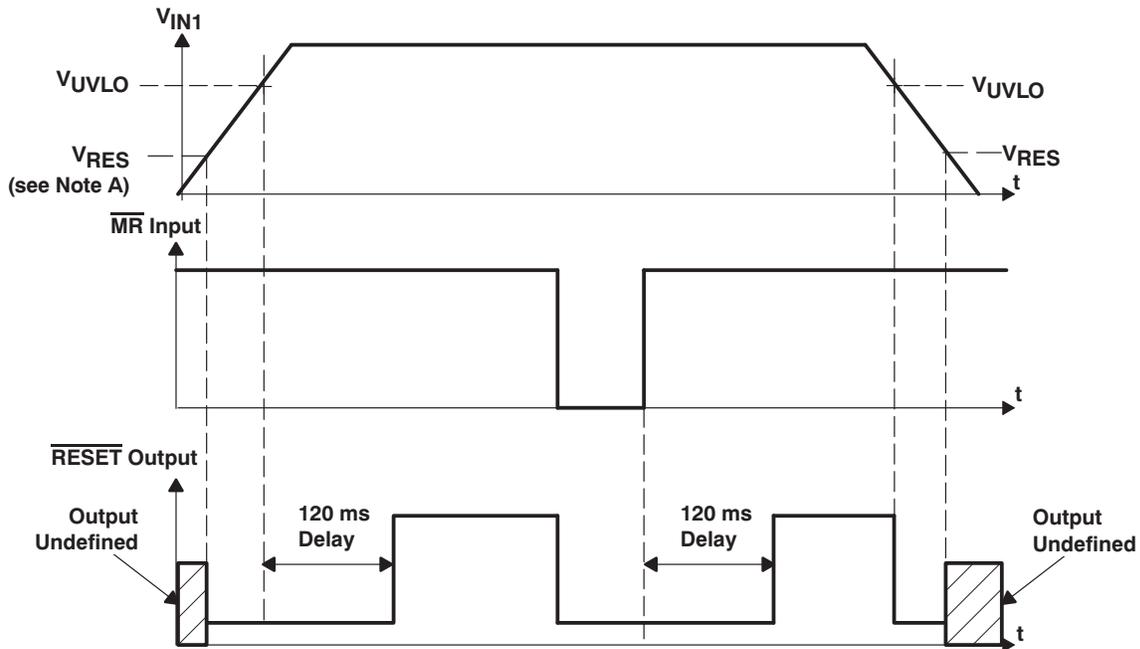
- A. For most applications, V_{SENSE1} and V_{SENSE2} should be externally connected to V_{OUT1} and V_{OUT2} , respectively, as close as possible to the device. For other implementations, refer to SENSE terminal connection discussion in the [Application Information](#) section.

Adjustable Voltage Version



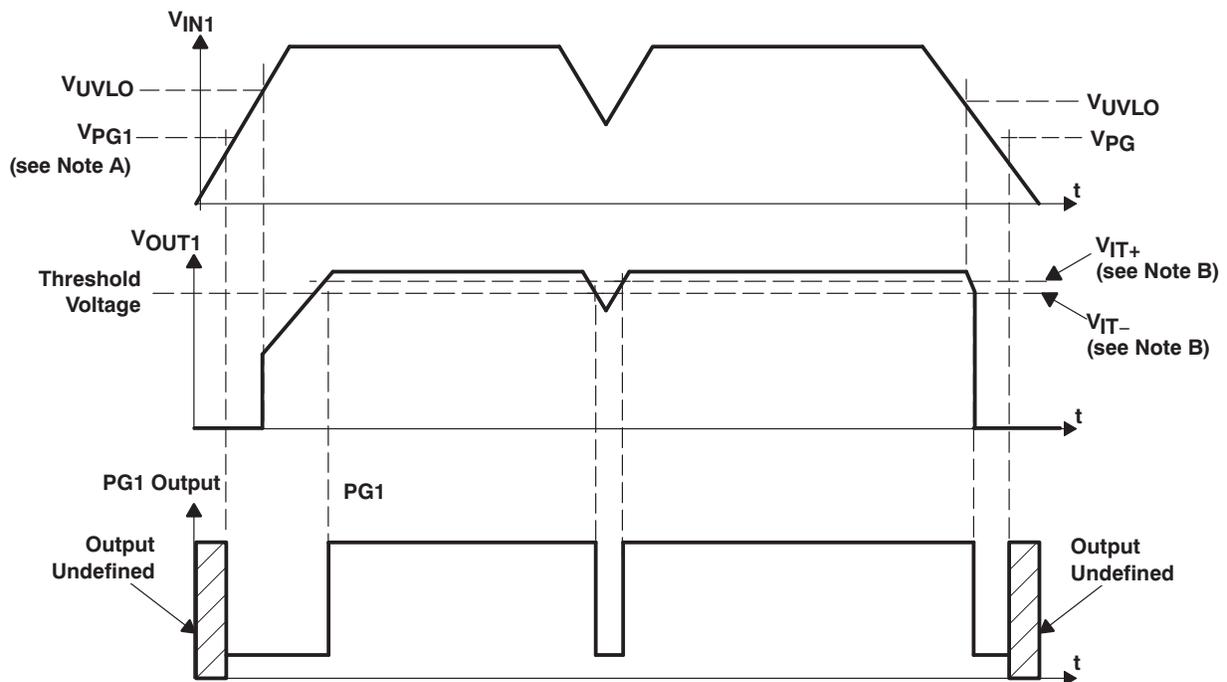
- A. For most applications, FB1 and FB2 should be externally connected to resistor dividers as close as possible to the device. For other implementations, refer to FB terminals connection discussion in the [Application Information](#) section.

RESET Timing Diagram



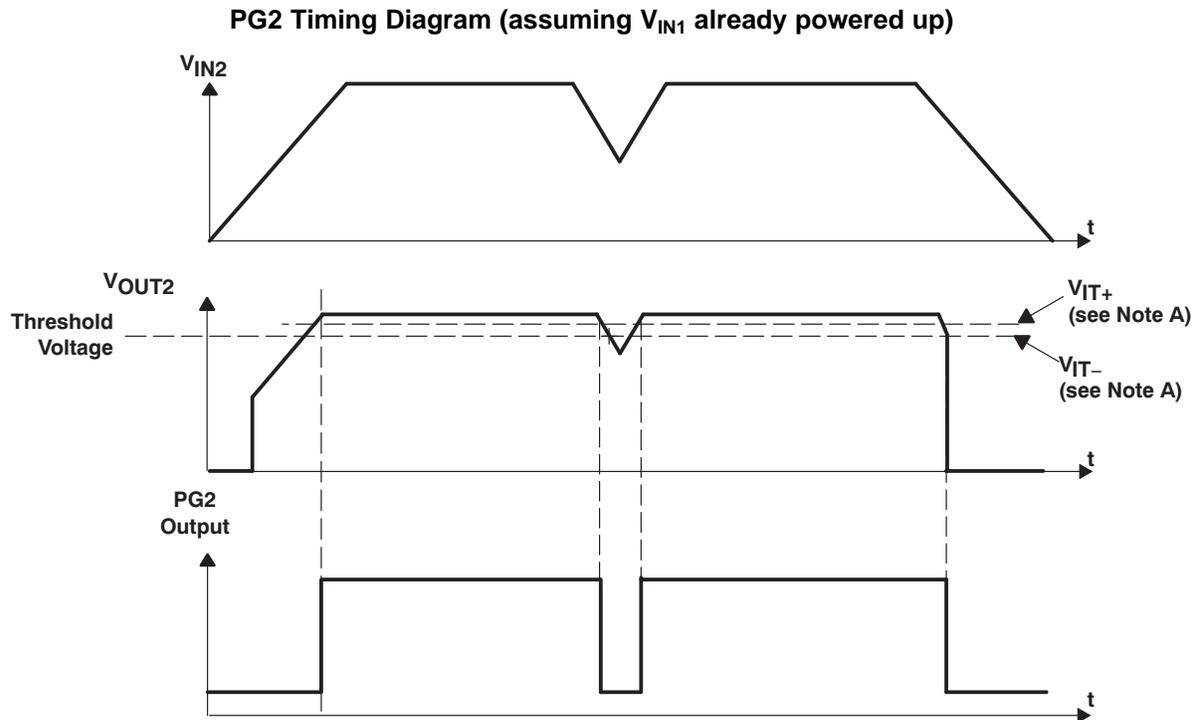
NOTE A: V_{RES} is the minimum input voltage for a valid \overline{RESET} . The symbol V_{RES} is not currently listed within EIA or JEDEC standards for semiconductor symbology.

PG1 Timing Diagram



NOTES A: V_{PG1} is the minimum input voltage for a valid PG. The symbol V_{PG1} is not currently listed within EIA or JEDEC standards for semiconductor symbology.

B: V_{IT-} trip voltage is typically 5% lower than the output voltage ($95\%V_O$). V_{IT-} to V_{IT+} is the hysteresis voltage.



NOTE A: V_{IT-} trip voltage is typically 5% lower than the output voltage ($95\%V_O$). V_{IT-} to V_{IT+} is the hysteresis voltage.

TERMINAL FUNCTIONS

| TERMINAL | | I/O | DESCRIPTION |
|--------------------|---------------|-----|--|
| NAME | NO. | | |
| $\overline{EN1}$ | 6 | I | Active low enable for V_{OUT1} |
| $\overline{EN2}$ | 7 | I | Active low enable for V_{OUT2} |
| GND | 9 | — | Ground |
| GND/HEATSINK | 1, 12, 13, 24 | — | Ground/heatsink |
| \overline{MR} | 5 | I | Manual reset input, active low, pulled up internally |
| NC | 4, 17, 20 | — | No connection |
| PG1 | 19 | O | Open drain output, low when V_{OUT1} voltage is less than 95% of the nominal regulated voltage |
| PG2 | 18 | O | Open drain output, low when V_{OUT2} voltage is less than 95% of the nominal regulated voltage |
| \overline{RESET} | 8 | O | Open drain output, SVS (power-on reset) signal, active low |
| V_{IN1} | 2, 3 | I | Input voltage of regulator 1 |
| V_{IN2} | 10, 11 | I | Input voltage of regulator 2 |
| V_{OUT1} | 22, 23 | O | Output voltage of regulator 1 |
| V_{OUT2} | 14, 15 | O | Output voltage of regulator 2 |
| $V_{SENSE1}/FB1$ | 21 | I | Regulator 1 output voltage sense/regulator 1 feedback for adjustable |
| $V_{SENSE2}/FB2$ | 16 | I | Regulator 2 output voltage sense/regulator 2 feedback for adjustable |

Detailed Description

The TPS704xx low dropout regulator family provides dual regulated output voltages with independent enable functions. These devices provide fast transient response and high accuracy with small output capacitors, while drawing low quiescent current. Other features are integrated SVS (power-on reset, $\overline{\text{RESET}}$) and power good (PG1, PG2) that monitor output voltages and provide logic output to the system. These differentiated features provide a complete power solution.

The TPS704xx, unlike many other LDOs, features very low quiescent current that remains virtually constant even with varying loads. Conventional LDO regulators use a PNP pass element, the base current of which is directly proportional to the load current through the regulator ($I_B = I_C/\beta$). The TPS704xx uses a PMOS transistor to pass current; because the gate of the PMOS is voltage-driven, operating current is low and stable over the full load range.

Pin Functions

Enable ($\overline{\text{EN1}}$, $\overline{\text{EN2}}$)

The $\overline{\text{EN}}$ terminals are inputs that enable or shut down each respective regulator. If $\overline{\text{EN}}$ is at a voltage high signal, the respective regulator is in shutdown mode. When $\overline{\text{EN}}$ goes to voltage low, the respective regulator is enabled.

Power-Good (PG1, PG2)

The PG terminals are open drain, active high output terminals that indicate the status of each respective regulator. When V_{OUT1} reaches 95% of its regulated voltage, PG1 goes to a high impedance state. When V_{OUT2} reaches 95% of its regulated voltage, PG2 goes to a high impedance state. Each PG goes to a low impedance state when its respective output voltage is pulled below 95% (that is, goes to an overload condition) of its regulated voltage. The open drain outputs of the PG terminals require a pull-up resistor.

Manual Reset Pin

$\overline{\text{MR}}$ is an active low input terminal used to trigger a reset condition. When $\overline{\text{MR}}$ is pulled to logic low, a POR ($\overline{\text{RESET}}$) occurs. The terminal has a 6- μA pull-up current to V_{IN1} ; however, it is recommended that the pin be pulled high to V_{IN1} when it is not used.

Sense (V_{SENSE1} , V_{SENSE2})

The sense terminals of fixed-output options must be connected to the regulator outputs, and the connection should be as short as possible. Internally, the sense terminal connects to high-impedance, wide-bandwidth amplifiers through a resistor-divider network and noise pickup feeds through to the regulator output. It is essential to route the sense connection in such a way as to minimize or avoid noise pickup. Adding RC networks between sense terminals and V_{OUT} terminals to filter noise is not recommended because these networks can cause the regulators to oscillate.

FB1 and FB2

FB1 and FB2 are input terminals used for adjustable-output devices and must be connected to the external feedback resistor divider. FB1 and FB2 connections should be as short as possible. It is essential to route them in such a way as to minimize or avoid noise pickup. Adding RC networks between FB terminals and V_{OUT} terminals to filter noise is not recommended because these networks can cause the regulators to oscillate.

RESET Indicator

\overline{RESET} is an active low, open drain output and requires a pullup resistor for normal operation. When pulled up, \overline{RESET} goes into a high impedance state (that is, logic high) after a 120-ms delay when both of the following conditions are met. First, V_{IN1} must be above the undervoltage condition. Second, the manual reset (\overline{MR}) pin must be in a high impedance state. To monitor V_{OUT1} , the PG1 output pin can be connected to \overline{MR} . To monitor V_{OUT2} , the PG2 output pin can be connected to \overline{MR} . If \overline{RESET} is not used, it can be left floating.

V_{IN1} and V_{IN2}

V_{IN1} and V_{IN2} are inputs to each regulator. **Internal bias voltages are powered by V_{IN1} .**

V_{OUT1} and V_{OUT2}

V_{OUT1} and V_{OUT2} are output terminals of each regulator.

TYPICAL CHARACTERISTICS

Table of Graphs

| | | | FIGURE |
|-------|--|------------------------------------|-------------------------|
| V_O | Output voltage | vs Output current | Figure 1 and Figure 2 |
| | | vs Junction temperature | Figure 3 to Figure 4 |
| | Ground current | vs Junction temperature | Figure 5 |
| PSRR | Power-supply rejection ratio | vs Frequency | Figure 6 to Figure 9 |
| | Output spectral noise density | vs Frequency | Figure 10 to Figure 13 |
| Z_O | Output impedance | vs Frequency | Figure 14 to Figure 17 |
| | Dropout voltage | vs Temperature | Figure 18 and Figure 19 |
| | | vs Input voltage | Figure 20 and Figure 21 |
| | Load transient response | | Figure 22 and Figure 23 |
| | Line transient response (V_{OUT1}) | | Figure 24 |
| | Line transient response (V_{OUT2}) | | Figure 25 |
| V_O | Output voltage | vs Time (start-up) | Figure 26 and Figure 27 |
| | | Equivalent series resistance (ESR) | Figure 29 to Figure 32 |

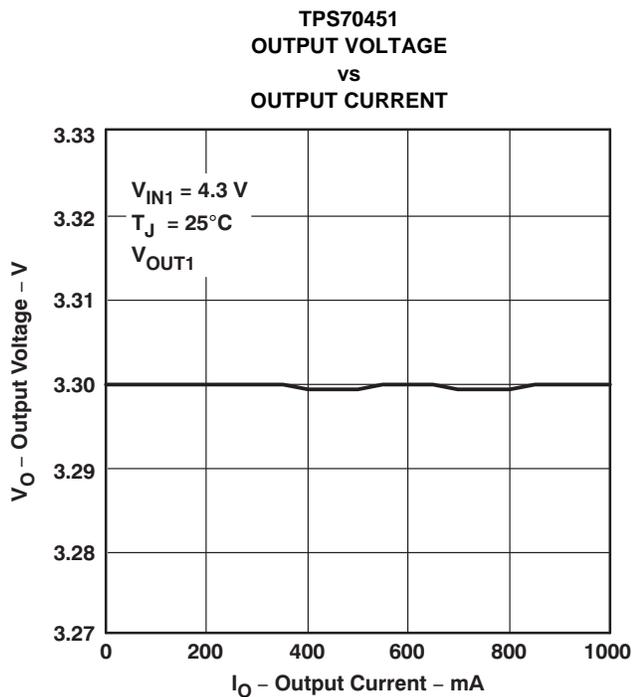


Figure 1.

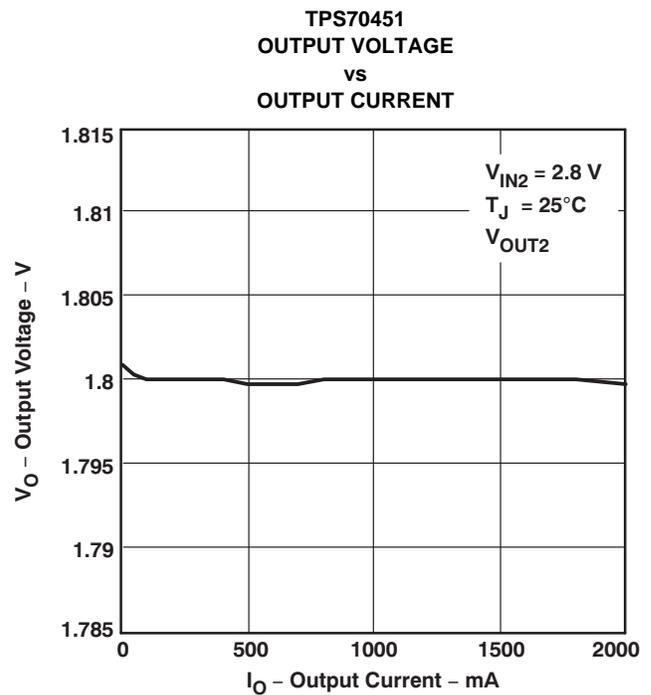


Figure 2.

TYPICAL CHARACTERISTICS (continued)

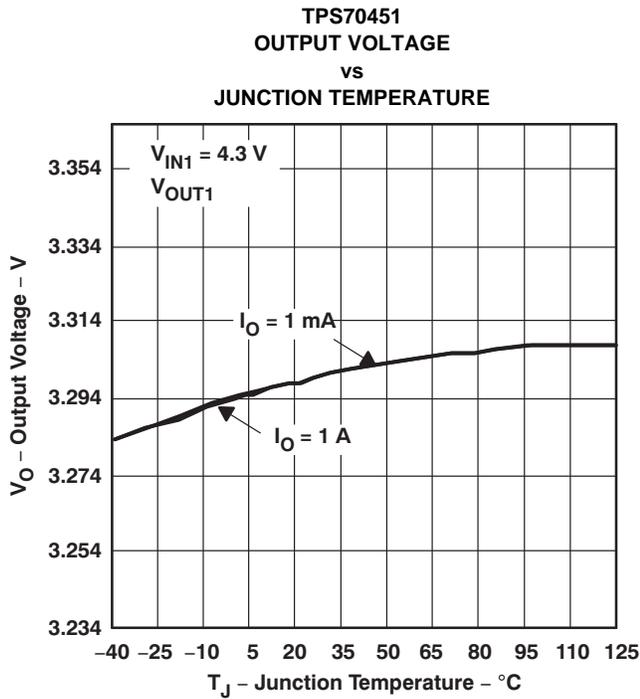


Figure 3.

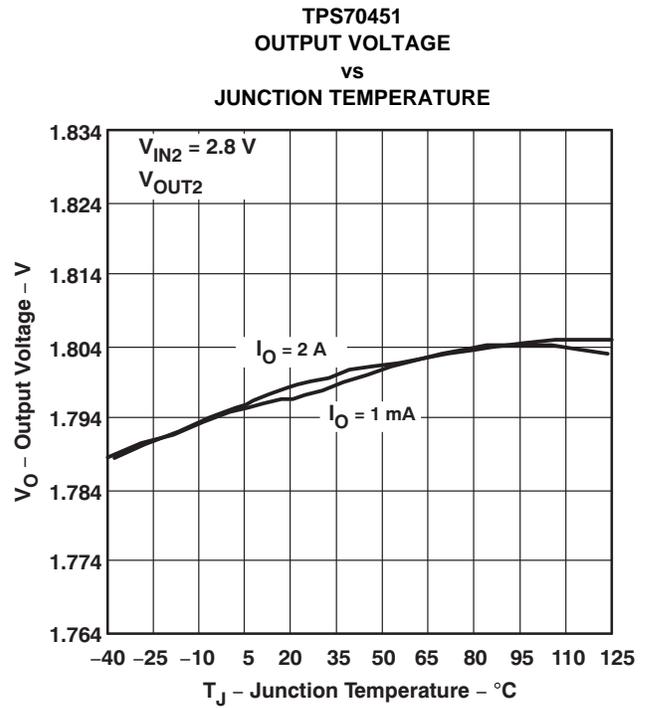


Figure 4.

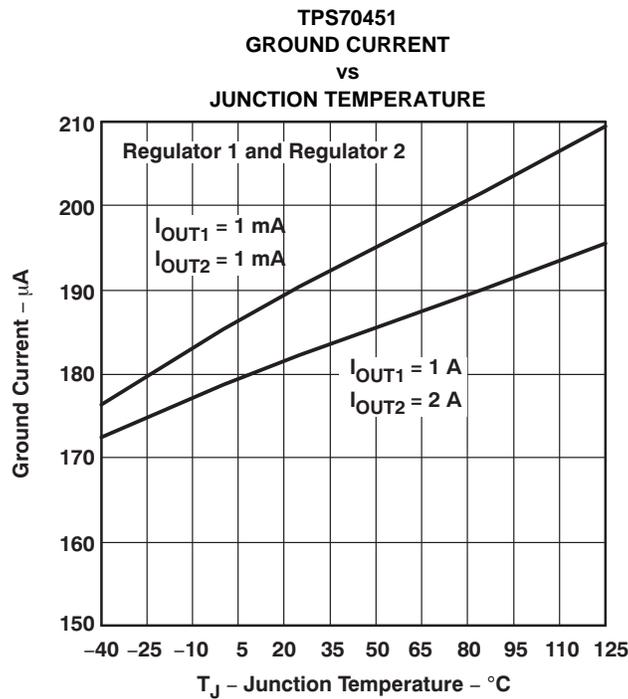


Figure 5.

TYPICAL CHARACTERISTICS (continued)

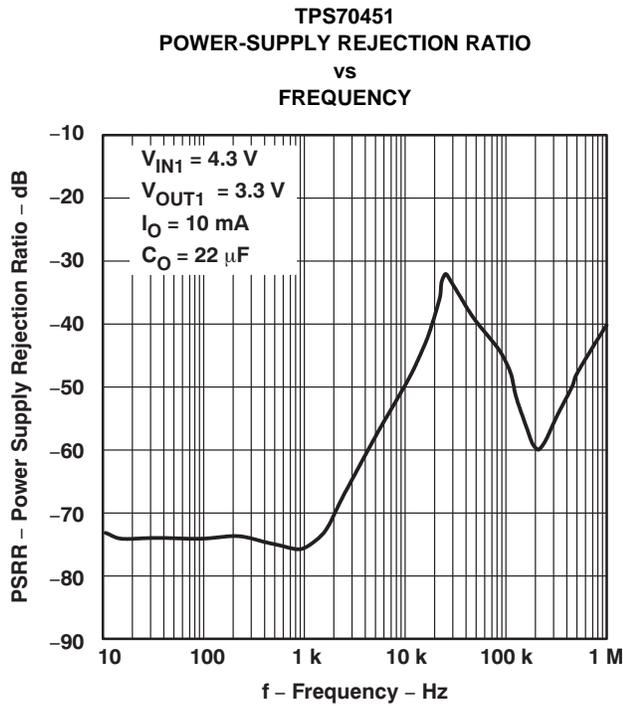


Figure 6.

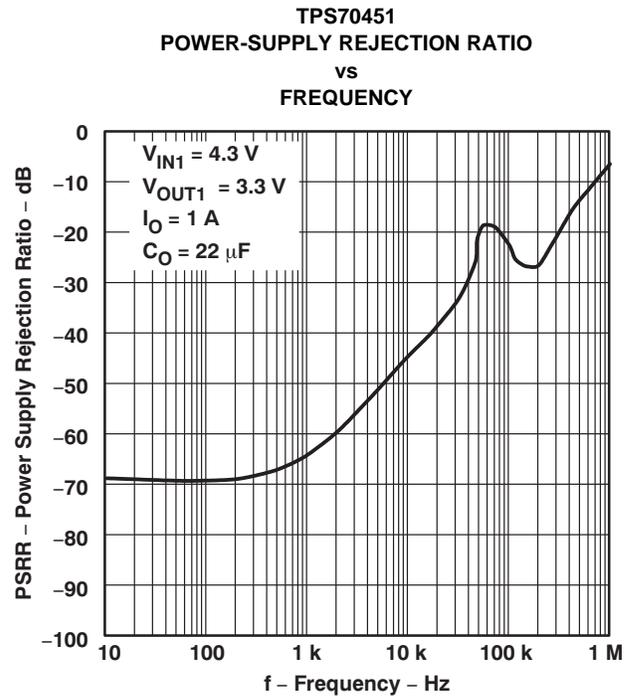


Figure 7.

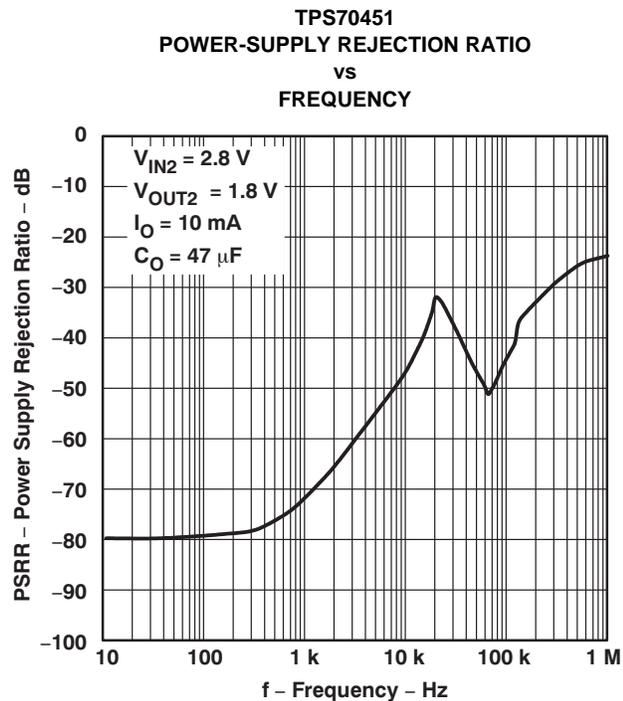


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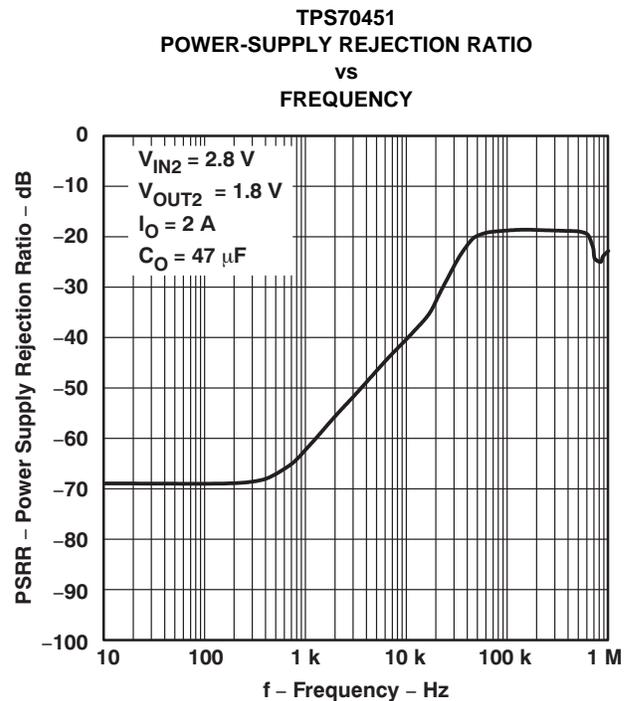


Figure 9.

TYPICAL CHARACTERISTICS (continued)

OUTPUT SPECTRAL NOISE DENSITY
 vs
 FREQUENCY

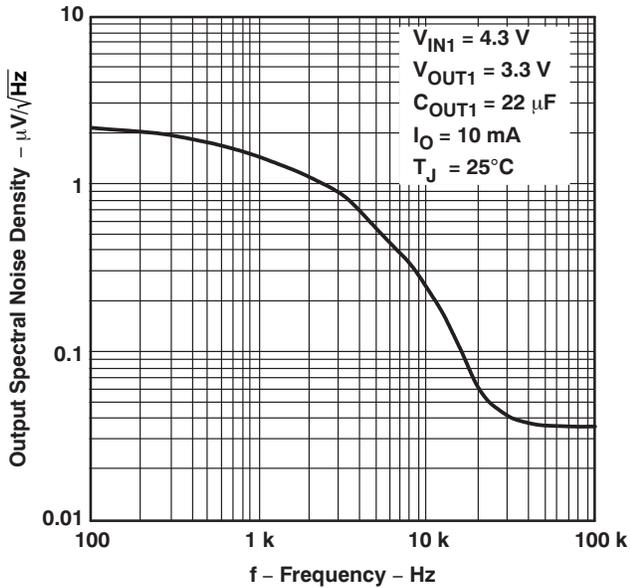


Figure 10.

OUTPUT SPECTRAL NOISE DENSITY
 vs
 FREQUENCY

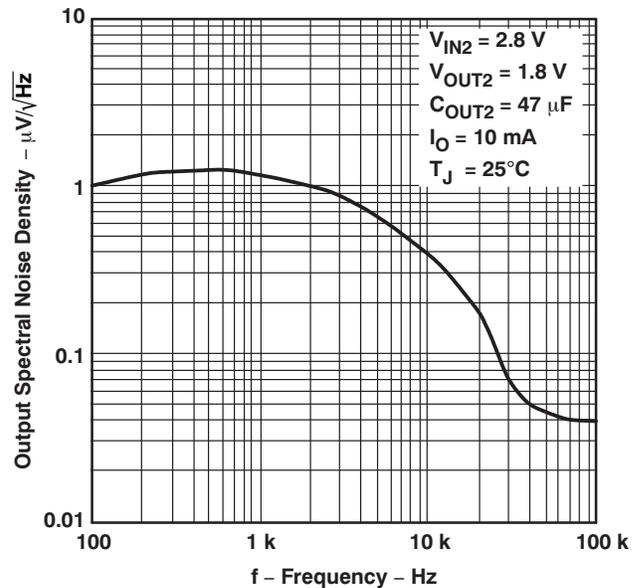


Figure 11.

OUTPUT SPECTRAL NOISE DENSITY
 vs
 FREQUENCY

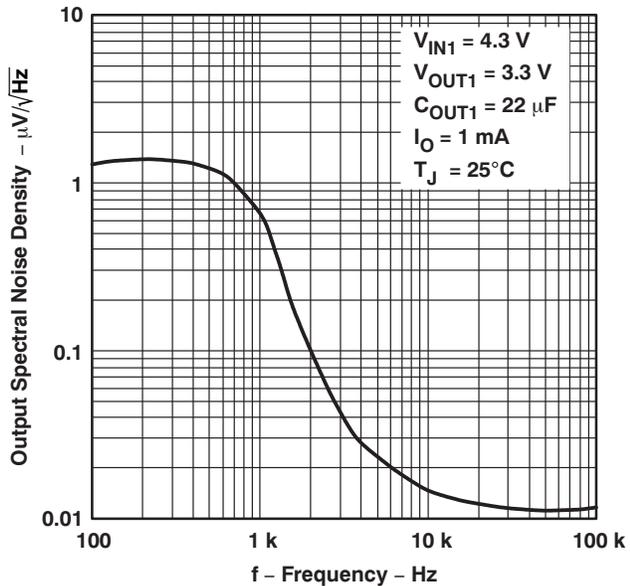


Figure 12.

OUTPUT SPECTRAL NOISE DENSITY
 vs
 FREQUENCY

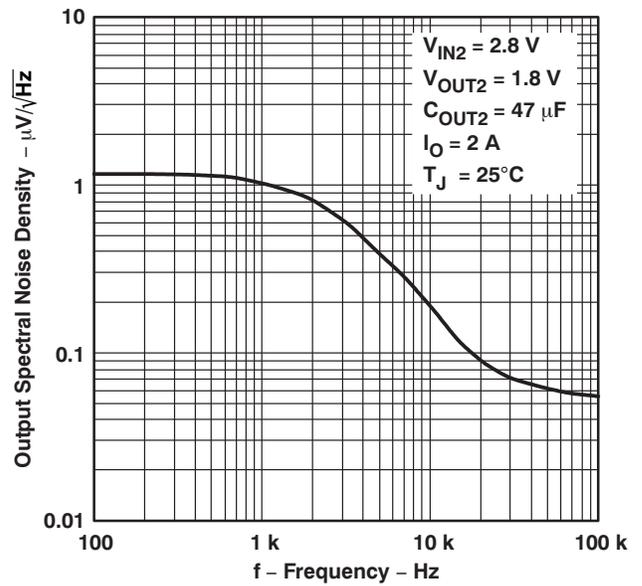


Figure 13.

TYPICAL CHARACTERISTICS (continued)

OUTPUT IMPEDANCE
 vs
 FREQUENCY

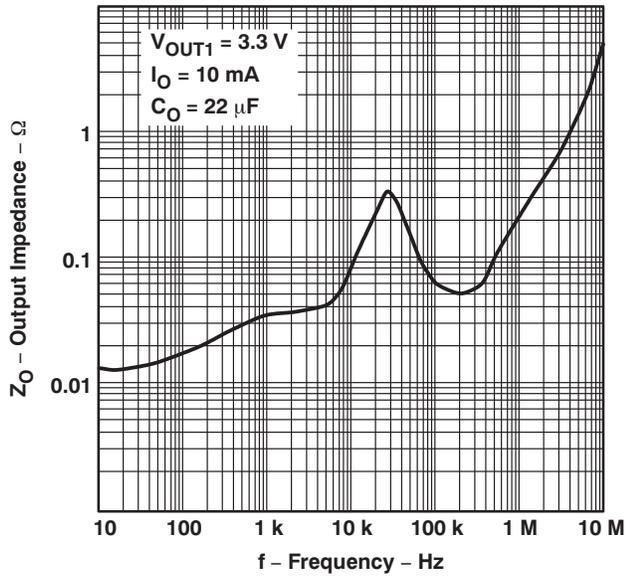


Figure 14.

OUTPUT IMPEDANCE
 vs
 FREQUENCY

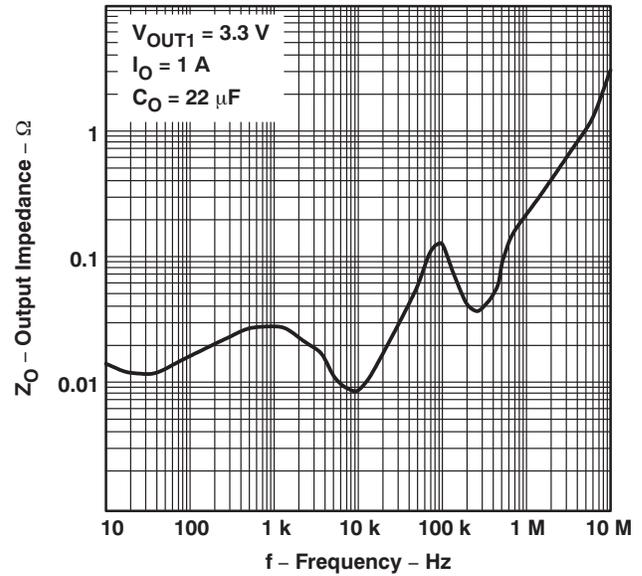


Figure 15.

OUTPUT IMPEDANCE
 vs
 FREQUENCY

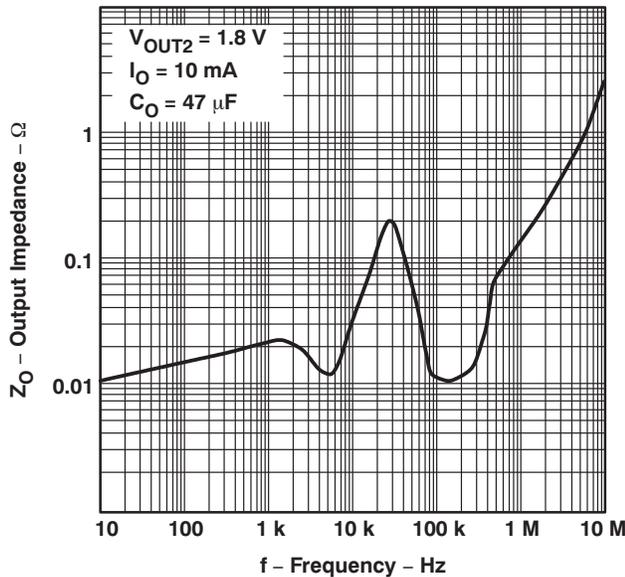


Figure 16.

OUTPUT IMPEDANCE
 vs
 FREQUENCY

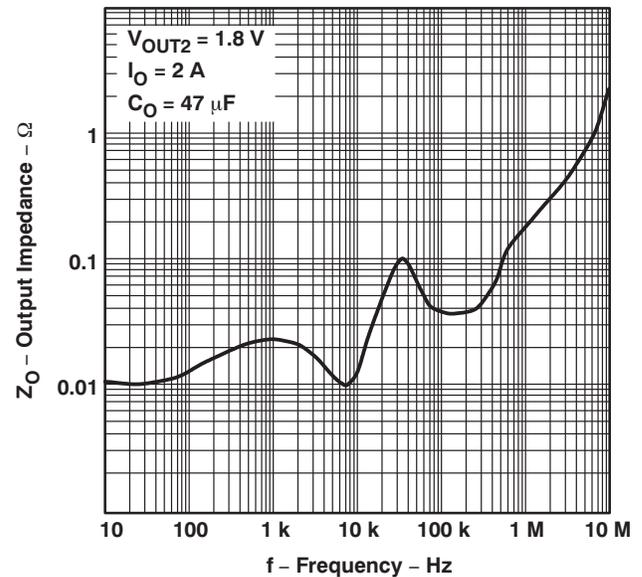
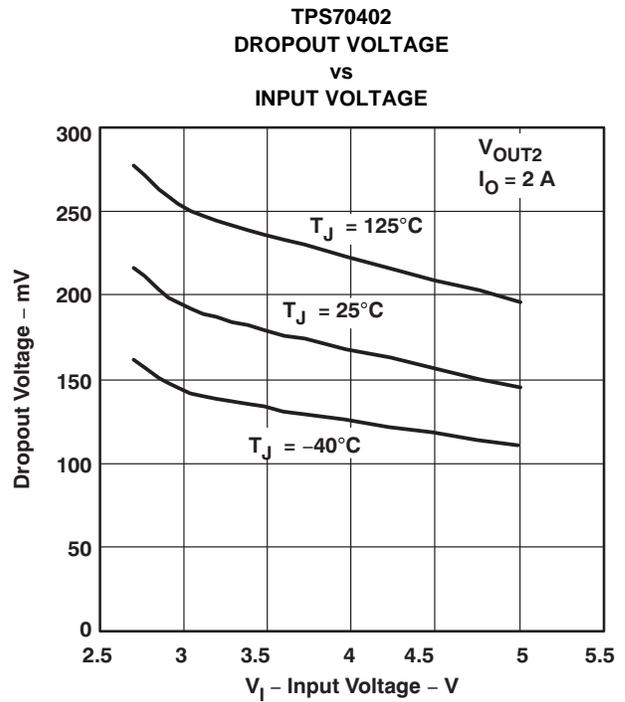
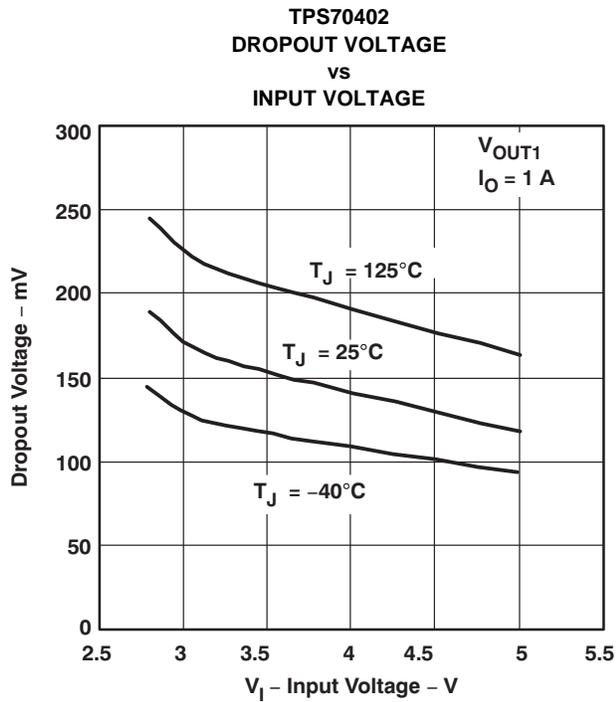
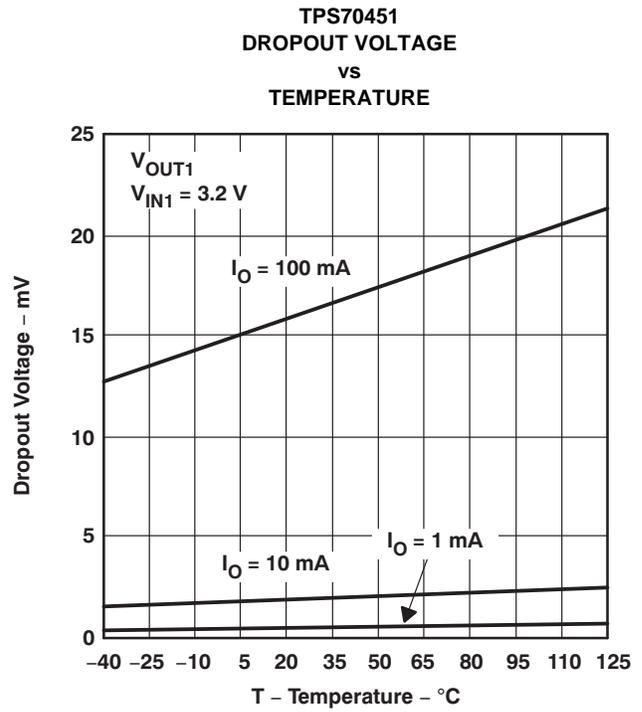
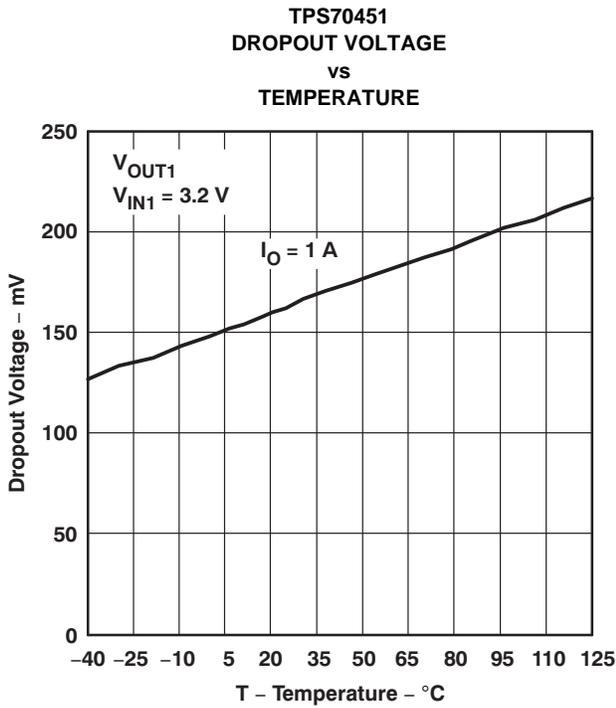


Figure 17.

TYPICAL CHARACTERISTICS (continued)



TYPICAL CHARACTERISTICS (continued)

LOAD TRANSIENT RESPONSE

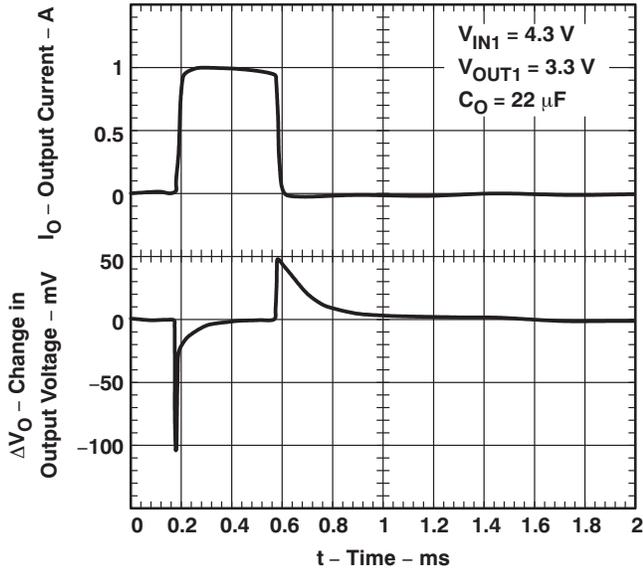


Figure 22.

LOAD TRANSIENT RESPONSE

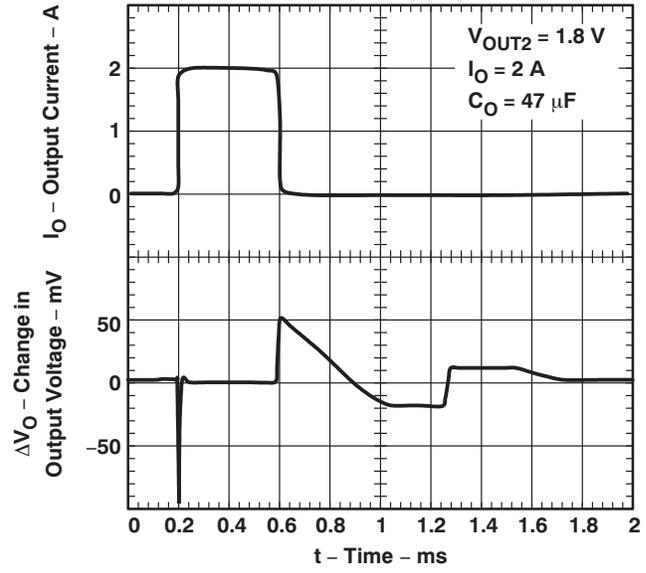


Figure 23.

LINE TRANSIENT RESPONSE

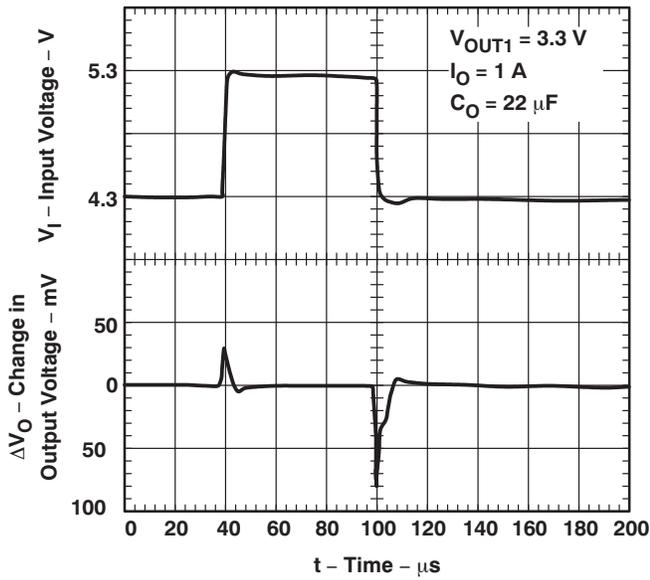


Figure 24.

LINE TRANSIENT RESPONSE

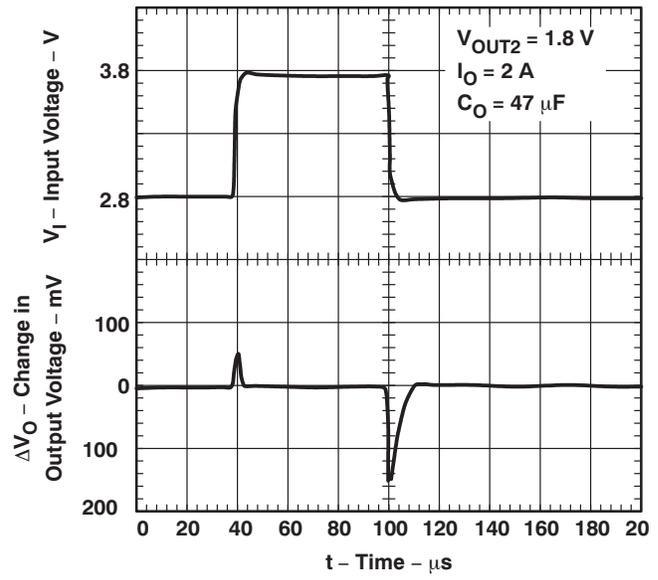


Figure 25.

TYPICAL CHARACTERISTICS (continued)

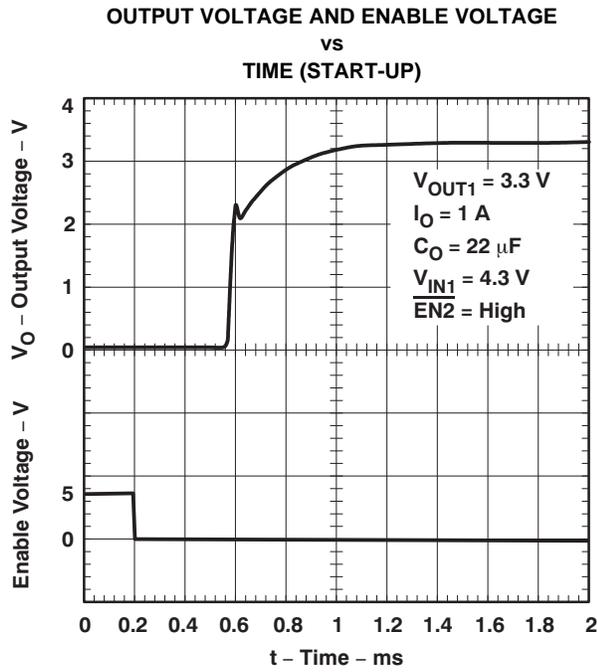


Figure 26.

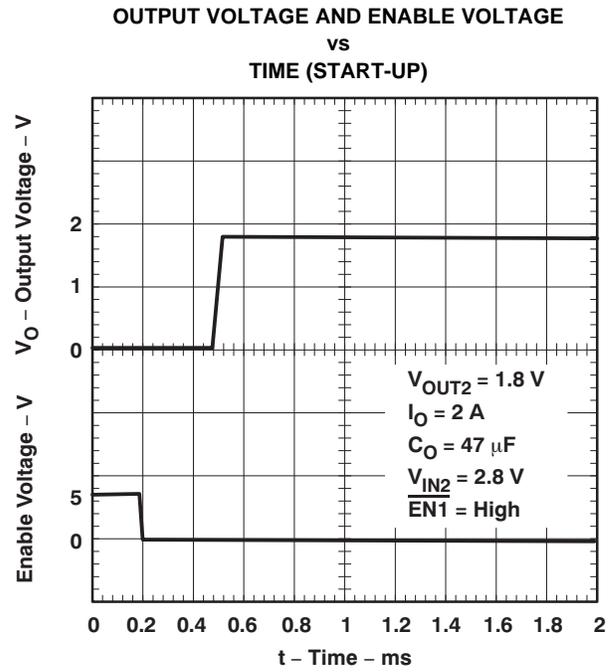


Figure 27.

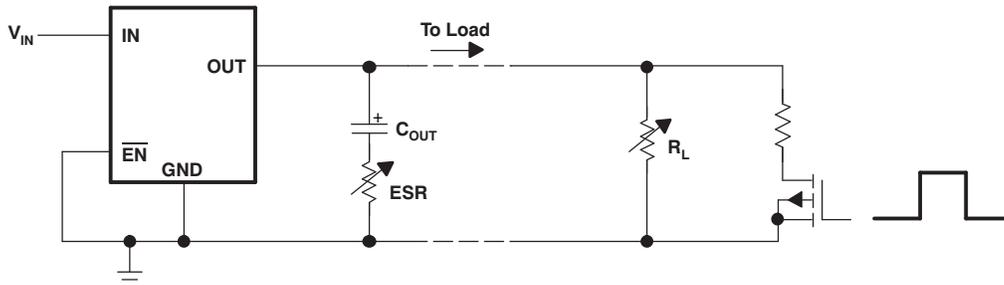


Figure 28. Test Circuit for Typical Regions of Stability

TYPICAL CHARACTERISTICS (continued)

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE⁽¹⁾

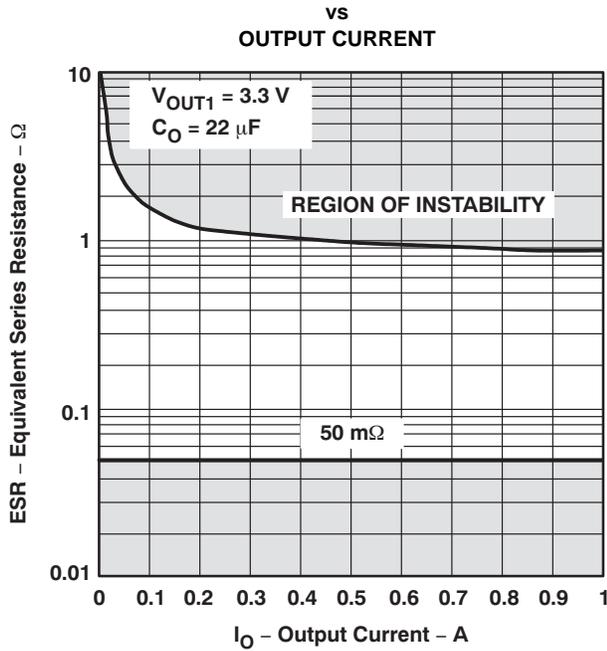


Figure 29.

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE⁽¹⁾

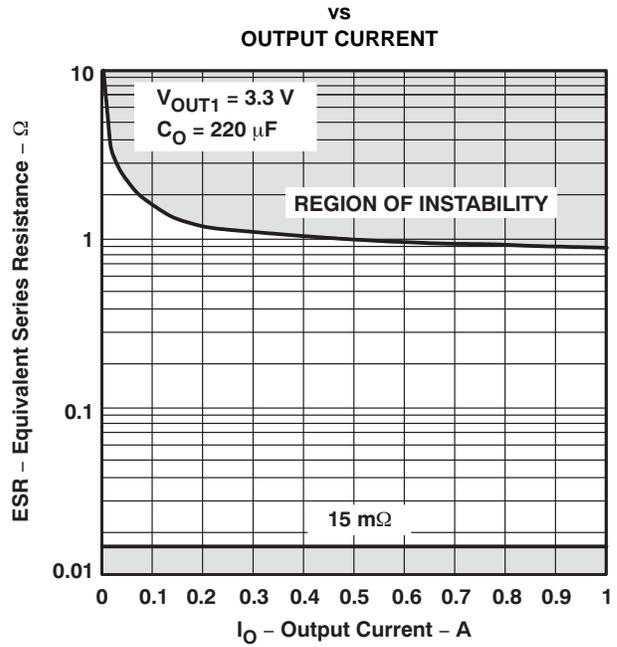


Figure 30.

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE⁽¹⁾

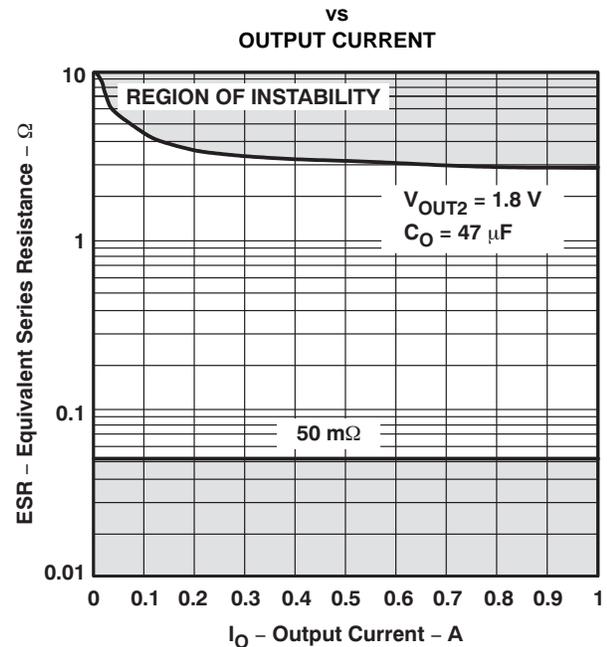


Figure 31.

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE⁽¹⁾

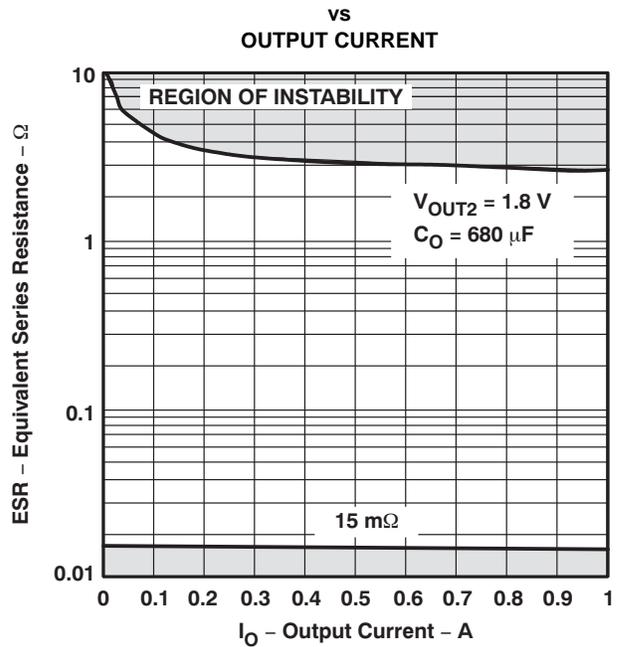


Figure 32.

⁽¹⁾ Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

THERMAL INFORMATION

Thermally-Enhanced TSSOP-24 (PWP— PowerPAD™)

The thermally-enhanced PWP package is based on the 24-pin TSSOP, but includes a thermal pad [see [Figure 33\(c\)](#)] to provide an effective thermal contact between the IC and the printed wiring board (PWB).

Traditionally, surface mount and power have been mutually exclusive terms. A variety of scaled-down TO220-type packages have leads formed as gull wings to make them applicable for surface-mount applications. These packages, however, suffer from several shortcomings: they do not address the very low profile requirements (<2 mm) of many of today's advanced systems, and they do not offer a pin-count high enough to accommodate increasing integration. On the other hand, traditional low-power surface-mount packages require power-dissipation derating that severely limits the usable range of many high-performance analog circuits.

The PWP package (thermally-enhanced TSSOP) combines fine-pitch surface-mount technology with thermal performance comparable to much larger power packages.

The PWP package is designed to optimize the heat transfer to the PWB. Because of the very small size and limited mass of a TSSOP package, thermal enhancement is achieved by improving the thermal conduction paths that remove heat from the component. The thermal pad is formed using a lead-frame design (patent pending) and manufacturing technique to provide the user with direct connection to the heat-generating IC. When this pad is soldered or otherwise coupled to an external heat dissipator, high power dissipation in the ultrathin, fine-pitch, surface-mount package can be reliably achieved.

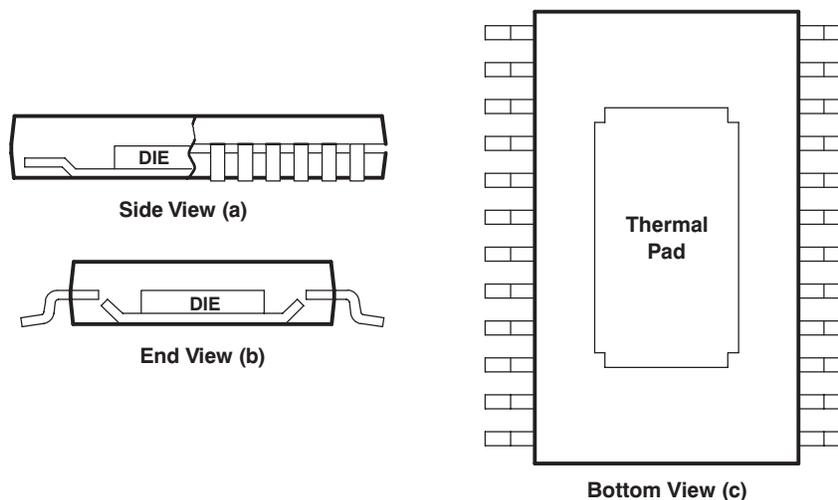


Figure 33. Views of Thermally-Enhanced PWP Package

Because the conduction path has been enhanced, power-dissipation capability is determined by the thermal considerations in the PWB design. For example, simply adding a localized copper plane (heat-sink surface), which is coupled to the thermal pad, enables the PWP package to dissipate 2.5 W in free air (reference [Figure 35\(a\)](#), 8 cm² of copper heat sink and natural convection). Increasing the heat-sink size increases the power dissipation range for the component. The power dissipation limit can be further improved by adding airflow to a PWB/IC assembly (see [Figure 34](#) and [Figure 35](#)). The line drawn at 0.3 cm² in [Figure 34](#) and [Figure 35](#) indicates performance at the minimum recommended heat-sink size, illustrated in [Figure 36](#).

The thermal pad is directly connected to the substrate of the IC, which for the TPS704xx series is a secondary electrical connection to device ground. The heat-sink surface that is added to the PWP can be a ground plane or left electrically isolated. In TO220-type surface-mount packages, the thermal connection is also the primary electrical connection for a given terminal which is not always ground. The PWP package provides up to 24 independent leads that can be used as inputs and outputs (**Note:** leads 1, 12, 13, and 24 are internally connected to the thermal pad and the IC substrate).

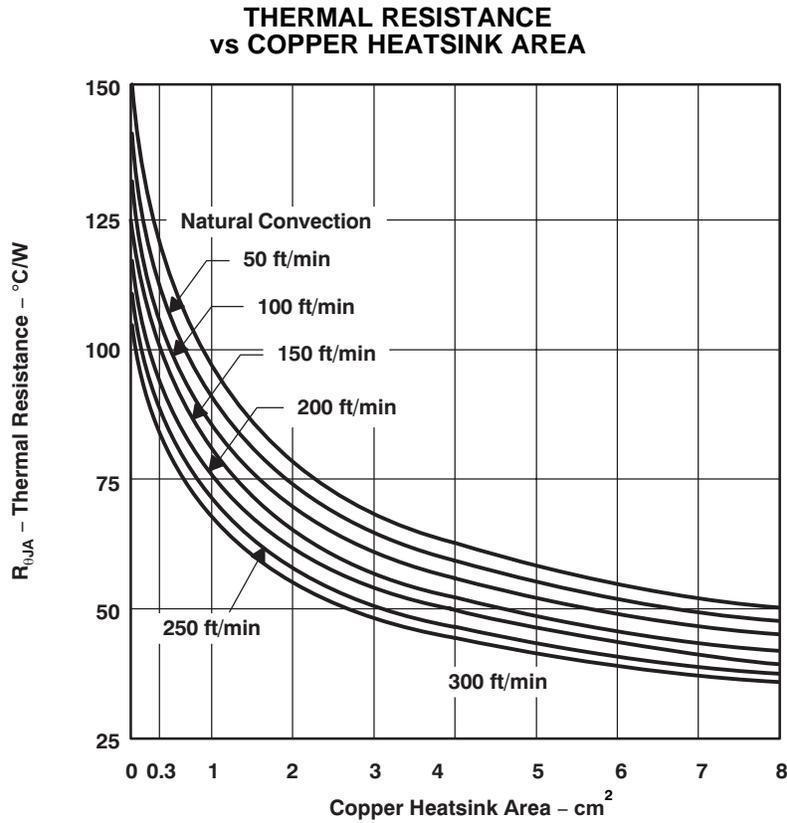
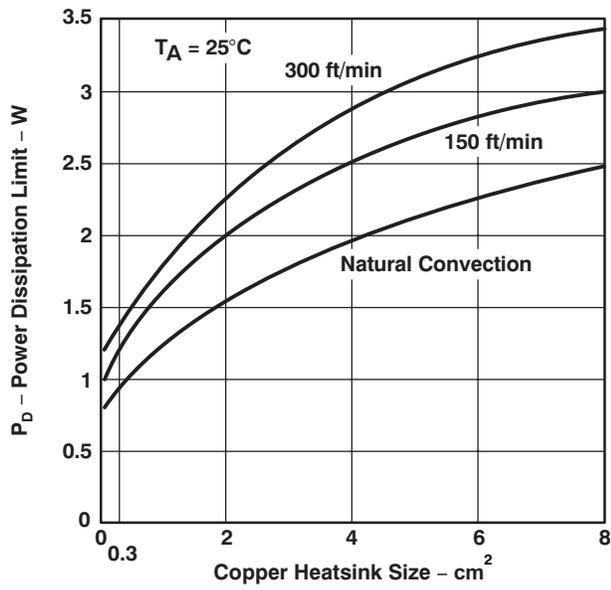
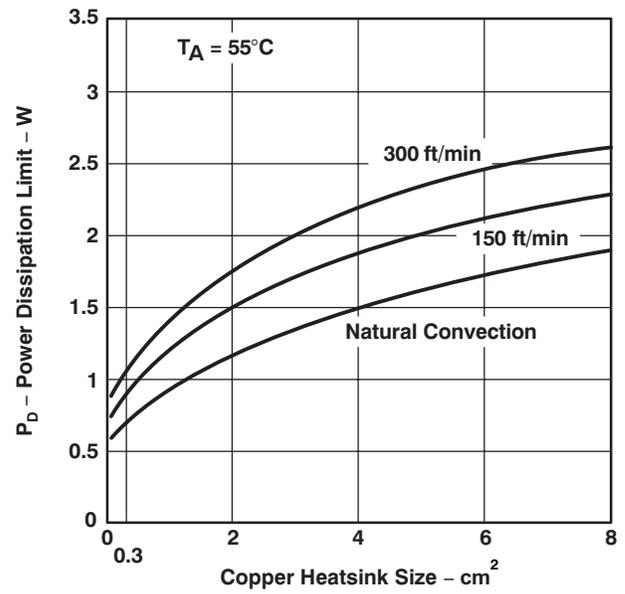


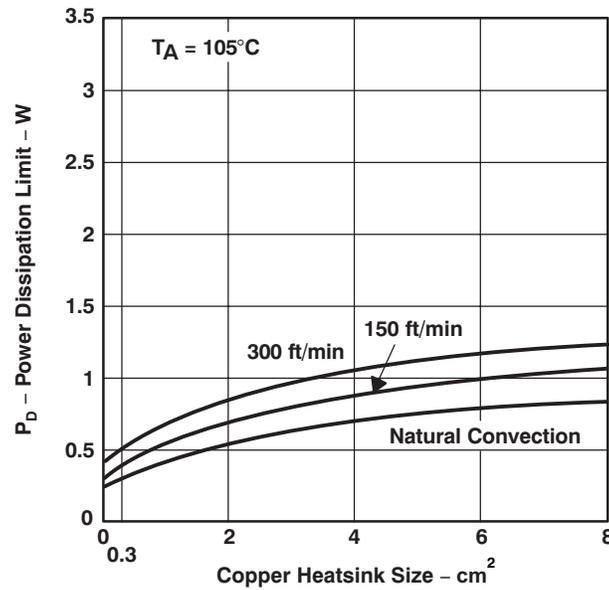
Figure 34.



(a)



(b)



(c)

Figure 35. Power Ratings of the PWP Package at Ambient Temperatures of +25°C, +55°C, and +105°C

Figure 36 is an example of a thermally-enhanced PWB layout for use with the new PWP package. This board configuration was used in the thermal experiments that generated the power ratings shown in Figure 34 and Figure 35. As discussed earlier, copper has been added on the PWB to conduct heat away from the device. $R_{\theta JA}$ for this assembly is illustrated in Figure 34 as a function of heat-sink area. A family of curves is included to illustrate the effect of airflow introduced into the system.

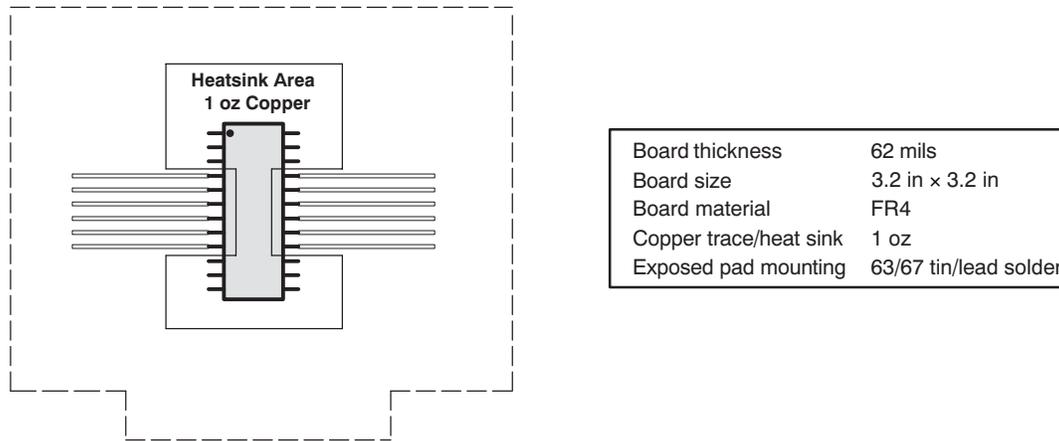


Figure 36. PWB Layout (Including Copper Heatsink Area) for Thermally-Enhanced PWP Package

From Figure 34, $R_{\theta JA}$ for a PWB assembly can be determined and used to calculate the maximum power-dissipation limit for the component/PWB assembly, with the equation:

$$P_{D(max)} = \frac{T_{Jmax} - T_A}{R_{\theta JA(system)}}$$

where:

- T_{Jmax} is the maximum specified junction temperature (+150°C absolute maximum limit, +125°C recommended operating limit) and T_A is the ambient temperature. (1)

$P_{D(max)}$ should then be applied to the internal power dissipated by the TPS704xx regulator. The equation for calculating total internal power dissipation of the TPS704xx is:

$$P_{D(total)} = (V_{IN1} - V_{OUT1}) \times I_{OUT1} + V_{IN1} \times \frac{I_Q}{2} + (V_{IN2} - V_{OUT2}) \times I_{OUT2} + V_{IN2} \times \frac{I_Q}{2} \quad (2)$$

Since the quiescent current of the TPS704xx is very low, the second term is negligible, further simplifying the equation to:

$$P_{D(total)} = (V_{IN1} - V_{OUT1}) \times I_{OUT1} + (V_{IN2} - V_{OUT2}) \times I_{OUT2} \quad (3)$$

For the case where $T_A = +55^\circ\text{C}$, airflow = 200 ft/min, copper heat-sink area = 4 cm², the maximum power-dissipation limit can be calculated. First, from Figure 34, we find the system $R_{\theta JA}$ is +50°C/W; therefore, the maximum power-dissipation limit is:

$$P_{D(max)} = \frac{T_{Jmax} - T_A}{R_{\theta JA(system)}} = \frac{+125^\circ\text{C} - 55^\circ\text{C}}{+50^\circ\text{C/W}} = 1.4 \text{ W} \quad (4)$$

If the system implements a TPS704xx regulator, where $V_{IN1} = 5.0\text{V}$, $V_{IN2} = 2.8 \text{ V}$, $I_{OUT1} = 500 \text{ mA}$, and $I_{OUT2} = 800 \text{ mA}$, the internal power dissipation is:

$$\begin{aligned} P_{D(total)} &= (V_{IN1} - V_{OUT1}) \times I_{OUT1} + (V_{IN2} - V_{OUT2}) \times I_{OUT2} \\ &= (5.0 - 3.3) \times 0.5 + (2.8 - 1.8) \times 0.8 = 1.25 \text{ W} \end{aligned} \quad (5)$$

Comparing $P_{D(\text{total})}$ with $P_{D(\text{max})}$ reveals that the power dissipation in this example does not exceed the calculated limit. When it does, one of two corrective actions should be made: raising the power-dissipation limit by increasing the airflow or the heat-sink area, or lowering the internal power dissipation of the regulator by reducing the input voltage or the load current. In either case, the above calculations should be repeated with the new system parameters. This parameter is measured with the recommended copper heat sink pattern on a 4-layer PWB, 2 oz. copper traces on 4-in \times 4-in ground layer. Simultaneous and continuous operation of both regulator outputs at full load may exceed the power dissipation rating of the PWP package.

Mounting Information

The primary requirement is to complete the thermal contact between the thermal pad and the PWB metal. The thermal pad is a solderable surface and is fully intended to be soldered at the time the component is mounted. Although voiding in the thermal-pad solder-connection is not desirable, up to 50% voiding is acceptable. The data included in [Figure 34](#) and [Figure 36](#) are for soldered connections with voiding between 20% and 50%. The thermal analysis shows no significant difference resulting from the variation in voiding percentage.

[Figure 37](#) shows the solder-mask land pattern for the PWP package. The minimum recommended heat-sink area is also illustrated. This is simply a copper plane under the body extent of the package, including metal routed under terminals 1, 12, 13, and 24.

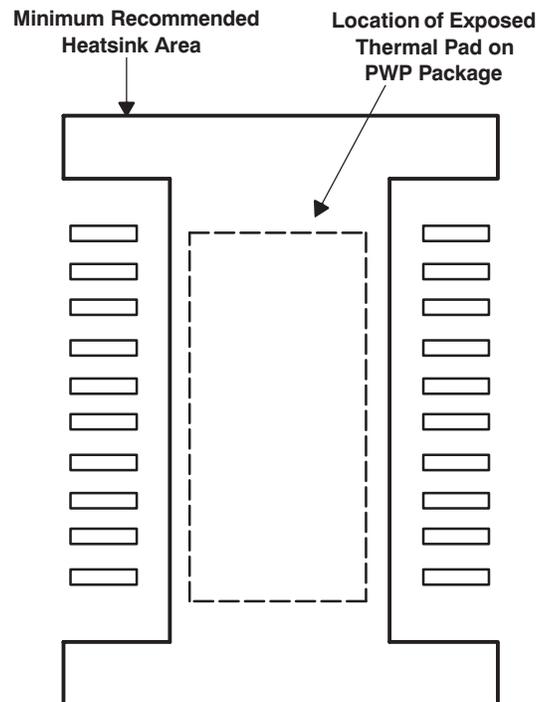


Figure 37. PWP Package Land Pattern

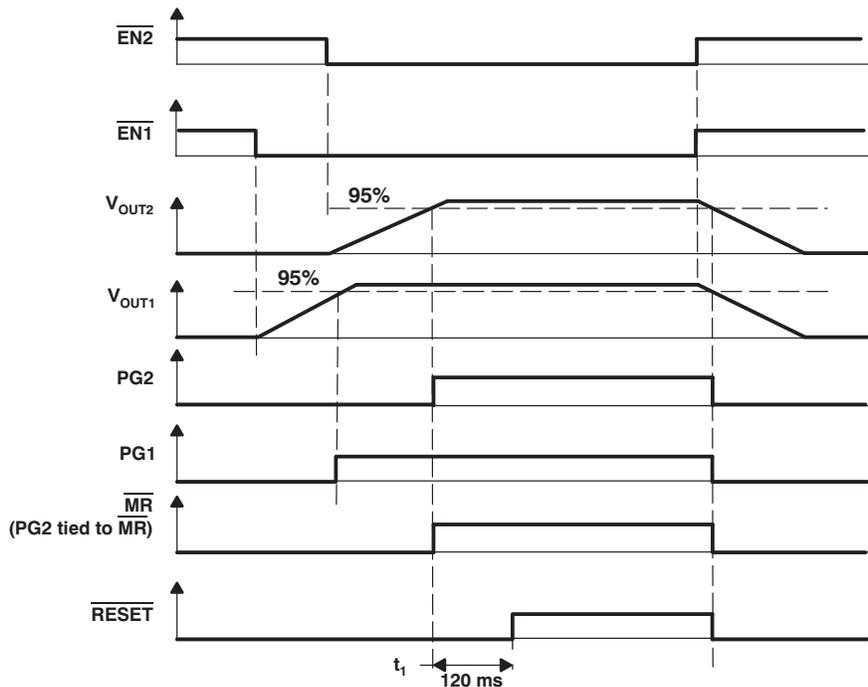
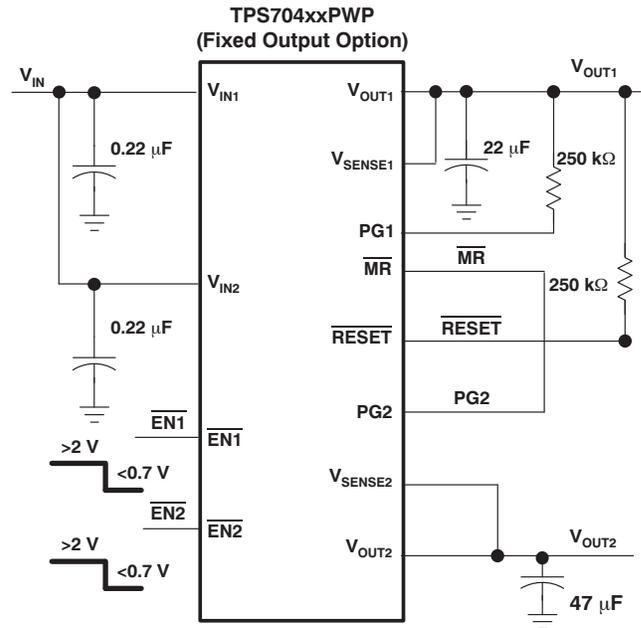
APPLICATION INFORMATION

Sequencing Timing Diagrams

This section provides a number of timing diagrams showing how this device functions in different configurations.

Application condition: V_{IN1} and V_{IN2} are tied to the same fixed input voltage greater than V_{UVLO} . PG2 is tied to \overline{MR} .

$\overline{EN1}$ and $\overline{EN2}$ are initially high; therefore, both regulators are off, and PG1 and PG2 (tied to \overline{MR}) are at logic low. Since \overline{MR} is at logic low, \overline{RESET} is also at logic low. When $\overline{EN1}$ is taken to logic low, V_{OUT1} turns on. Later, when $\overline{EN2}$ is taken to logic low, V_{OUT2} turns on. When V_{OUT1} reaches 95% of its regulated output voltage, PG1 goes to logic high. When V_{OUT2} reaches 95% of its regulated output voltage, PG2 (tied to \overline{MR}) goes to logic high. When V_{IN1} is greater than V_{UVLO} and \overline{MR} (tied to PG2) is at logic high, \overline{RESET} is pulled to logic high after a 120-ms delay. When $\overline{EN1}$ and $\overline{EN2}$ are returned to logic high, both devices power down and both PG1, PG2 (tied to \overline{MR}), and \overline{RESET} return to logic low.

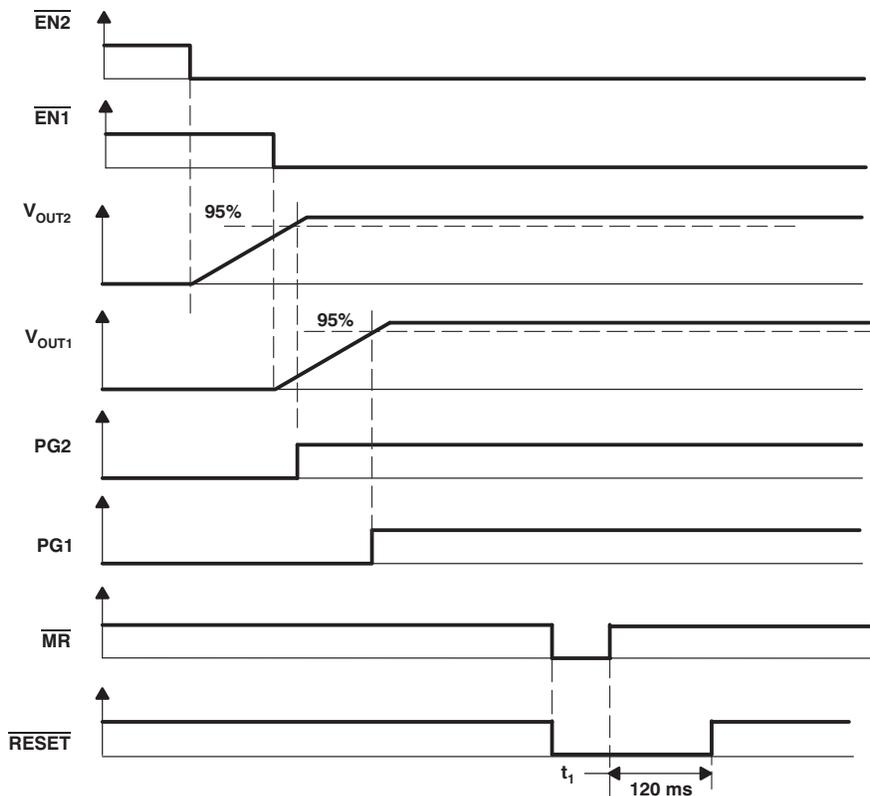
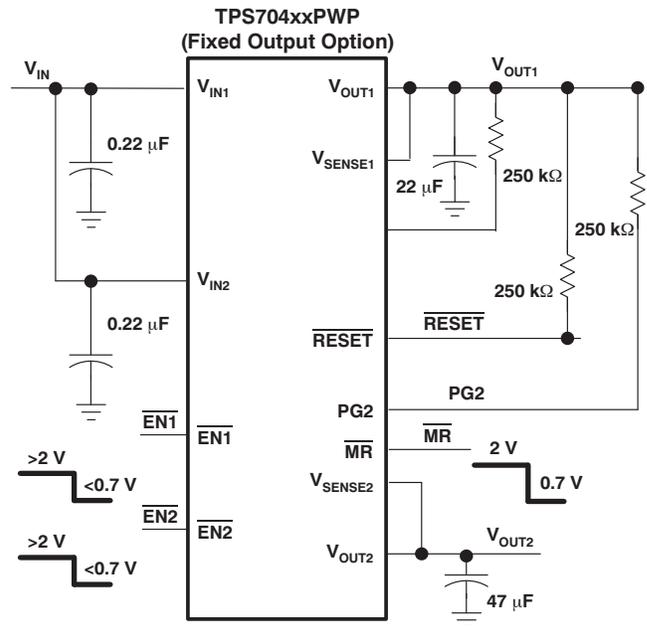


NOTES: A. t_1 : Time at which V_{IN} is greater than V_{UVLO} and \overline{MR} is logic high.
B. The timing diagram is not drawn to scale.

Figure 38. Timing When V_{OUT1} Is Enabled Before V_{OUT2}

Application condition: V_{IN1} and V_{IN2} are tied to the same fixed input voltage greater than V_{UVLO} . \overline{MR} is initially logic high but is eventually toggled.

$\overline{EN1}$ and $\overline{EN2}$ are initially high; therefore, both regulators are off, and PG1 and PG2 are at logic low. Since V_{IN1} is greater than V_{UVLO} and \overline{MR} is at logic high, \overline{RESET} is also at logic high. When $\overline{EN2}$ is taken to logic low, V_{OUT2} turns on. Later, when $\overline{EN1}$ is taken to logic low, V_{OUT1} turns on. When V_{OUT2} reaches 95% of its regulated output voltage, PG2 goes to logic high. When V_{OUT1} reaches 95% of its regulated output voltage, PG1 goes to logic high. When \overline{MR} is taken to logic low, \overline{RESET} is taken low. When \overline{MR} returns to logic high, \overline{RESET} returns to logic high after a 120-ms delay.

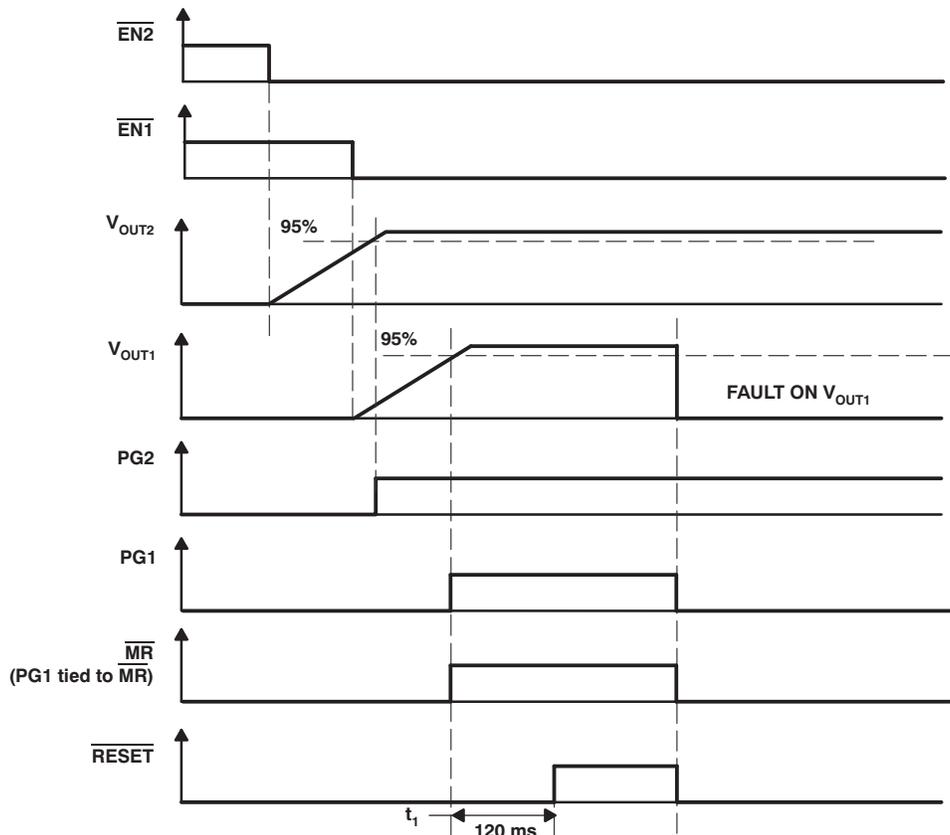
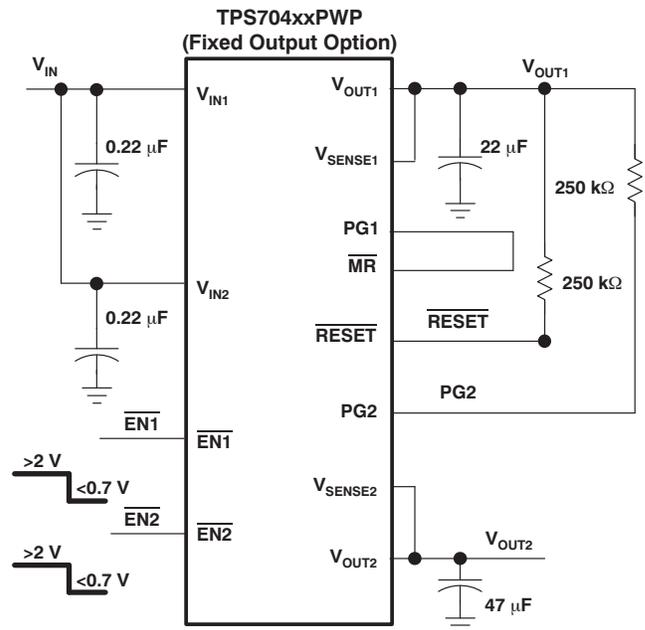


NOTES: A. t_1 : Time at which V_{IN} is greater than V_{UVLO} and \overline{MR} is logic high.
 B. The timing diagram is not drawn to scale.

Figure 39. Timing When \overline{MR} is Toggled

Application condition: V_{IN1} and V_{IN2} are tied to same fixed input voltage greater than V_{UVLO} . $\overline{PG1}$ is tied to \overline{MR} .

$\overline{EN1}$ and $\overline{EN2}$ are initially high; therefore, both regulators are off, and $\overline{PG1}$ (tied to \overline{MR}) and $\overline{PG2}$ are at logic low. Since \overline{MR} is at logic low, \overline{RESET} is also at logic low. When $\overline{EN2}$ is taken to logic low, V_{OUT2} turns on. Later, when $\overline{EN1}$ is taken to logic low, V_{OUT1} turns on. When V_{OUT2} reaches 95% of its regulated output voltage, $\overline{PG2}$ goes to logic high. When V_{OUT1} reaches 95% of its regulated output voltage, $\overline{PG1}$ goes to logic high. When V_{IN1} is greater than V_{UVLO} and \overline{MR} (tied to $\overline{PG2}$) is at logic high, \overline{RESET} is pulled to logic high after a 120-ms delay. When a fault on V_{OUT1} causes it to fall below 95% of its regulated output voltage, $\overline{PG1}$ (tied to \overline{MR}) goes to logic low. Since \overline{MR} is logic low, \overline{RESET} goes to logic low. V_{OUT2} is unaffected.



NOTES: A. t_1 : Time at which V_{IN} is greater than V_{UVLO} and \overline{MR} is logic high.
B. The timing diagram is not drawn to scale.

Figure 40. Timing When There is a Fault on V_{OUT1}

APPLICATION INFORMATION

Input Capacitor

For a typical application, a ceramic input bypass capacitor (0.22 μF to 1 μF) is recommended. This capacitor should be as close to the input pins as possible. Due to the impedance of the input supply, large transient currents cause the input voltage to droop. If this droop causes the input voltage to drop below the UVLO threshold, the device turns off. Therefore, it is recommended to place a larger capacitor in parallel with the ceramic bypass capacitor at the regulator input. The size of this capacitor depends on the output current, the response time of the main power supply, and the main power supply distance to the regulator. At a minimum, the capacitor should be sized to ensure that the input voltage does not drop below the minimum UVLO threshold voltage during normal operating conditions.

Output Capacitor

As with most LDO regulators, the TPS704xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance value for $V_{\text{OUT}1}$ is 22 μF and the ESR (equivalent series resistance) must be between 50 m Ω and 800 m Ω . The minimum recommended capacitance value for $V_{\text{OUT}2}$ is 47 μF and the ESR must be between 50 m Ω and 2 Ω . Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described above. Larger capacitors provide a wider range of stability and better load transient response. [Table 1](#) gives a partial listing of surface-mount capacitors suitable for use with the TPS704xx for fast transient response applications.

This information, along with the ESR graphs, is included to assist in selection of suitable capacitance for user applications. When necessary to achieve low height requirements along with high output current and/or high load capacitance, several higher ESR capacitors can be used in parallel to meet the guidelines above.

Table 1. Partial Listing of TPS704xx-Compatible Surface-Mount Capacitors

| VALUE | MANUFACTURER | MFR PART NO. |
|-------------------|--------------|----------------|
| 680 μF | Kemet | T510X6871004AS |
| 470 μF | Sanyo | 4TPB470M |
| 150 μF | Sanyo | 4TPC150M |
| 220 μF | Sanyo | 2R5TPC220M |
| 100 μF | Sanyo | 2R5TPC220M |
| 68 μF | Sanyo | 10TPC68M |
| 68 μF | Kemet | T495D6861006AS |
| 47 μF | Kemet | T495D4761010AS |
| 33 μF | Kemet | T495C3361016AS |
| 22 μF | Kemet | T495C2261010AS |

Programming the TPS70402 Adjustable LDO Regulator

The output voltage of the TPS70402 adjustable regulators is programmed using external resistor dividers as shown in Figure 41.

Resistors R1 and R2 should be chosen for approximately a 50- μ A divider current. Lower value resistors can be used, but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at the sense terminal increase the output voltage error. The recommended design procedure is to choose R2 = 30.1 k Ω to set the divider current at approximately 50 μ A, and then calculate R1 using Equation 6:

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \times R2 \quad (6)$$

where:

- $V_{REF} = 1.224$ V typ (the internal reference voltage)

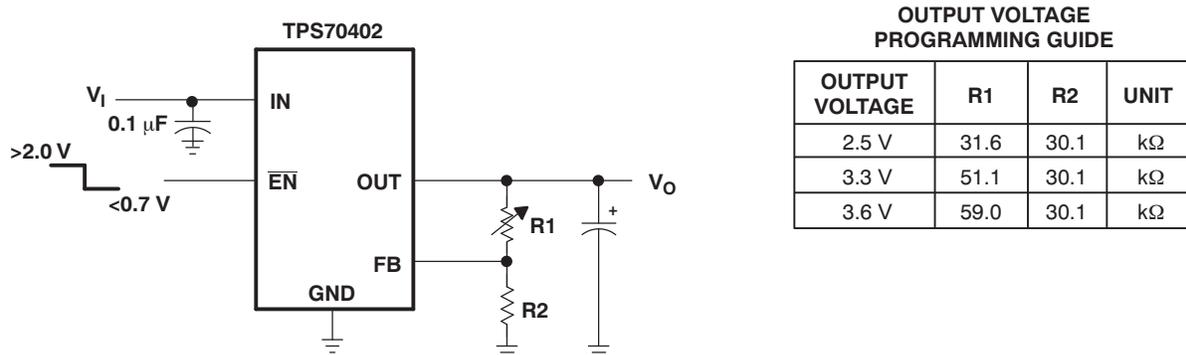


Figure 41. TPS70402 Adjustable LDO Regulator Programming

Regulator Protection

Both TPS704xx PMOS-pass transistors have built-in back diodes that conduct reverse currents when the input voltage drops below the output voltage (for example, during power-down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS704xx also features internal current limiting and thermal protection. During normal operation, the TPS704xx regulator 1 limits output current to approximately 1.75 A (typ) and regulator 2 limits output current to approximately 3.8 A (typ). When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds +150°C (typ), thermal-protection circuitry shuts it down. Once the device has cooled below +130°C (typ), regulator operation resumes.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (February 2010) to Revision F Page

- Changed *Tube* transport media, quatity values from 70 to 60 in Ordering Information table 3
-

Changes from Revision D (December, 2007) to Revision E Page

- Corrected pin description for pin 21 in pinout drawing 1
 - Updated *Dissipation Ratings* table values 4
 - Deleted *falling edge delay* specification 6
 - Updated *Fixed Voltage Version* block diagram 7
 - Updated *Adjustable Voltage Version* block diagram 8
-

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|------------------------------|---------------|----------------------|-------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| TPS70402PWP | Active | Production | HTSSOP (PWP) 24 | 60 TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PT70402 |
| TPS70402PWP.A | Active | Production | HTSSOP (PWP) 24 | 60 TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PT70402 |
| TPS70402PWPG4 | Active | Production | HTSSOP (PWP) 24 | 60 TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PT70402 |
| TPS70402PWPR | Active | Production | HTSSOP (PWP) 24 | 2000 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PT70402 |
| TPS70402PWPR.A | Active | Production | HTSSOP (PWP) 24 | 2000 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PT70402 |
| TPS70445PWP | NRND | Production | HTSSOP (PWP) 24 | 60 TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PT70445 |
| TPS70445PWP.A | NRND | Production | HTSSOP (PWP) 24 | 60 TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PT70445 |
| TPS70445PWPR | Active | Production | HTSSOP (PWP) 24 | 2000 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PT70445 |
| TPS70445PWPR.A | Active | Production | HTSSOP (PWP) 24 | 2000 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PT70445 |
| TPS70448PWP | Active | Production | HTSSOP (PWP) 24 | 60 TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PT70448 |
| TPS70448PWP.A | Active | Production | HTSSOP (PWP) 24 | 60 TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PT70448 |
| TPS70448PWPR | Active | Production | HTSSOP (PWP) 24 | 2000 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PT70448 |
| TPS70448PWPR.A | Active | Production | HTSSOP (PWP) 24 | 2000 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PT70448 |
| TPS70451PWP | Active | Production | HTSSOP (PWP) 24 | 60 TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PT70451 |
| TPS70451PWP.A | Active | Production | HTSSOP (PWP) 24 | 60 TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PT70451 |
| TPS70451PWPR | Active | Production | HTSSOP (PWP) 24 | 2000 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PT70451 |
| TPS70451PWPR.A | Active | Production | HTSSOP (PWP) 24 | 2000 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PT70451 |
| TPS70458PWP | Active | Production | HTSSOP (PWP) 24 | 60 TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PT70458 |
| TPS70458PWP.A | Active | Production | HTSSOP (PWP) 24 | 60 TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PT70458 |
| TPS70458PWPR | Active | Production | HTSSOP (PWP) 24 | 2000 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PT70458 |
| TPS70458PWPR.A | Active | Production | HTSSOP (PWP) 24 | 2000 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PT70458 |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

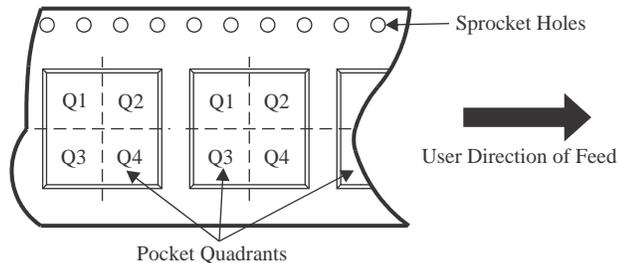
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


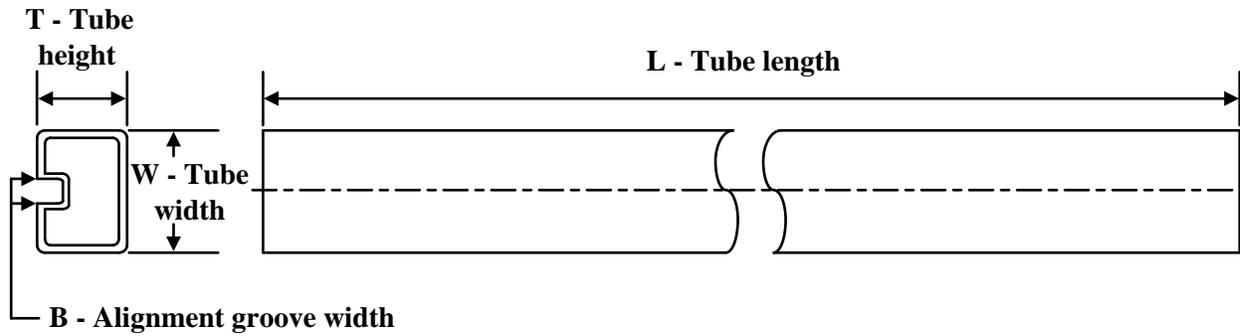
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS70402PWPR | HTSSOP | PWP | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |
| TPS70445PWPR | HTSSOP | PWP | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |
| TPS70448PWPR | HTSSOP | PWP | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |
| TPS70451PWPR | HTSSOP | PWP | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |
| TPS70458PWPR | HTSSOP | PWP | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS70402PWPR | HTSSOP | PWP | 24 | 2000 | 350.0 | 350.0 | 43.0 |
| TPS70445PWPR | HTSSOP | PWP | 24 | 2000 | 350.0 | 350.0 | 43.0 |
| TPS70448PWPR | HTSSOP | PWP | 24 | 2000 | 350.0 | 350.0 | 43.0 |
| TPS70451PWPR | HTSSOP | PWP | 24 | 2000 | 350.0 | 350.0 | 43.0 |
| TPS70458PWPR | HTSSOP | PWP | 24 | 2000 | 350.0 | 350.0 | 43.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|---------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| TPS70402PWP | PWP | HTSSOP | 24 | 60 | 530 | 10.2 | 3600 | 3.5 |
| TPS70402PWP.A | PWP | HTSSOP | 24 | 60 | 530 | 10.2 | 3600 | 3.5 |
| TPS70402PWPG4 | PWP | HTSSOP | 24 | 60 | 530 | 10.2 | 3600 | 3.5 |
| TPS70445PWP | PWP | HTSSOP | 24 | 60 | 530 | 10.2 | 3600 | 3.5 |
| TPS70445PWP.A | PWP | HTSSOP | 24 | 60 | 530 | 10.2 | 3600 | 3.5 |
| TPS70448PWP | PWP | HTSSOP | 24 | 60 | 530 | 10.2 | 3600 | 3.5 |
| TPS70448PWP.A | PWP | HTSSOP | 24 | 60 | 530 | 10.2 | 3600 | 3.5 |
| TPS70451PWP | PWP | HTSSOP | 24 | 60 | 530 | 10.2 | 3600 | 3.5 |
| TPS70451PWP.A | PWP | HTSSOP | 24 | 60 | 530 | 10.2 | 3600 | 3.5 |
| TPS70458PWP | PWP | HTSSOP | 24 | 60 | 530 | 10.2 | 3600 | 3.5 |
| TPS70458PWP.A | PWP | HTSSOP | 24 | 60 | 530 | 10.2 | 3600 | 3.5 |

GENERIC PACKAGE VIEW

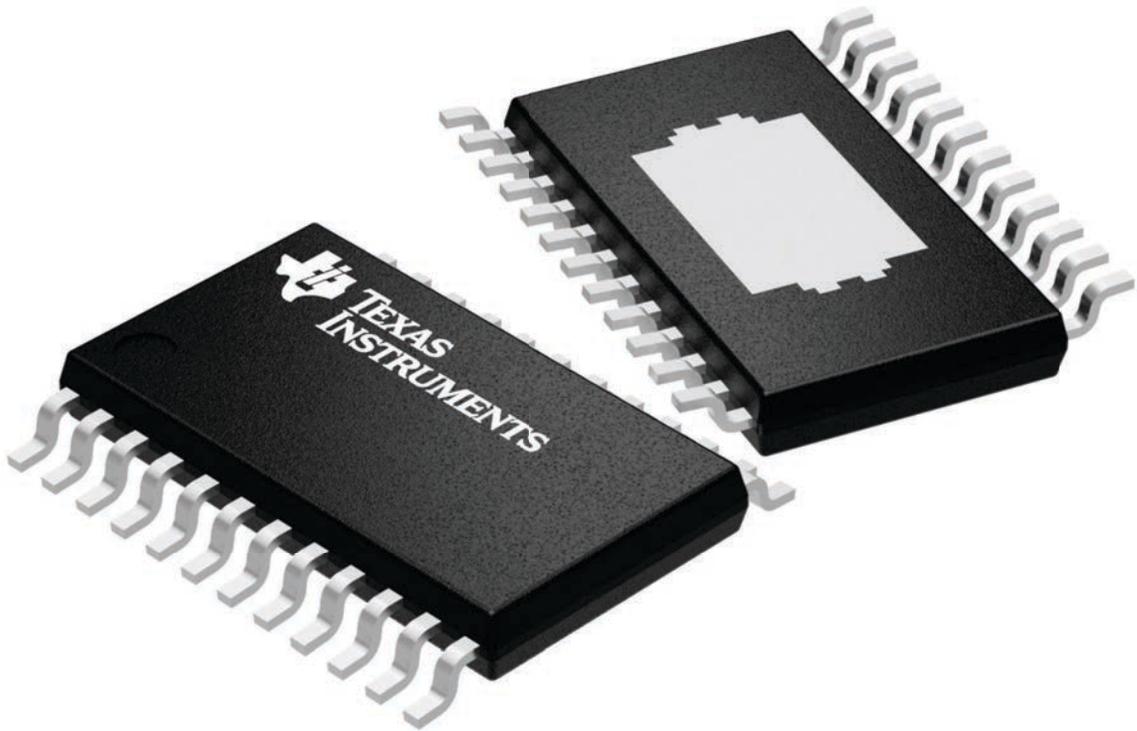
PWP 24

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 7.6, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

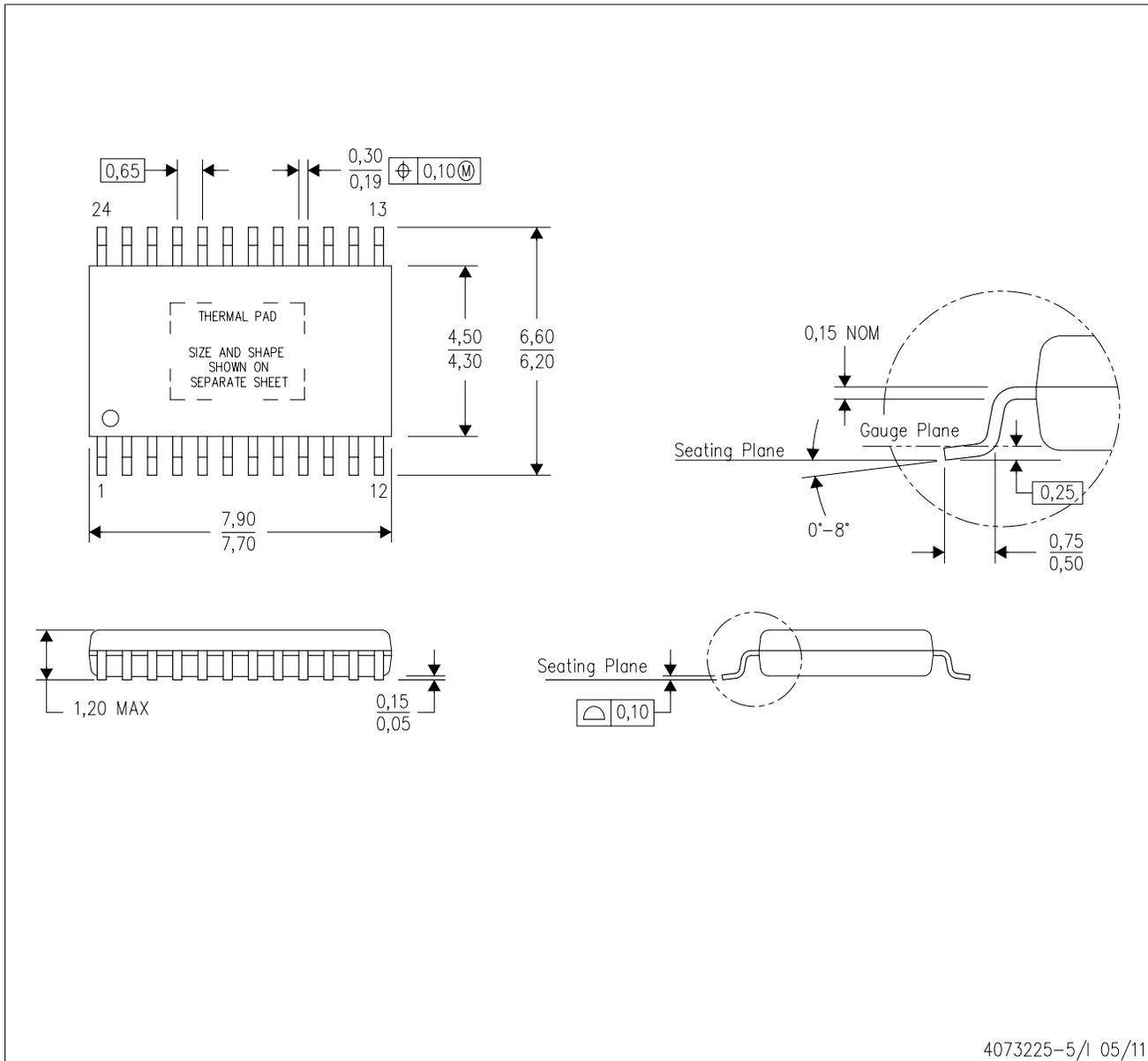


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MECHANICAL DATA

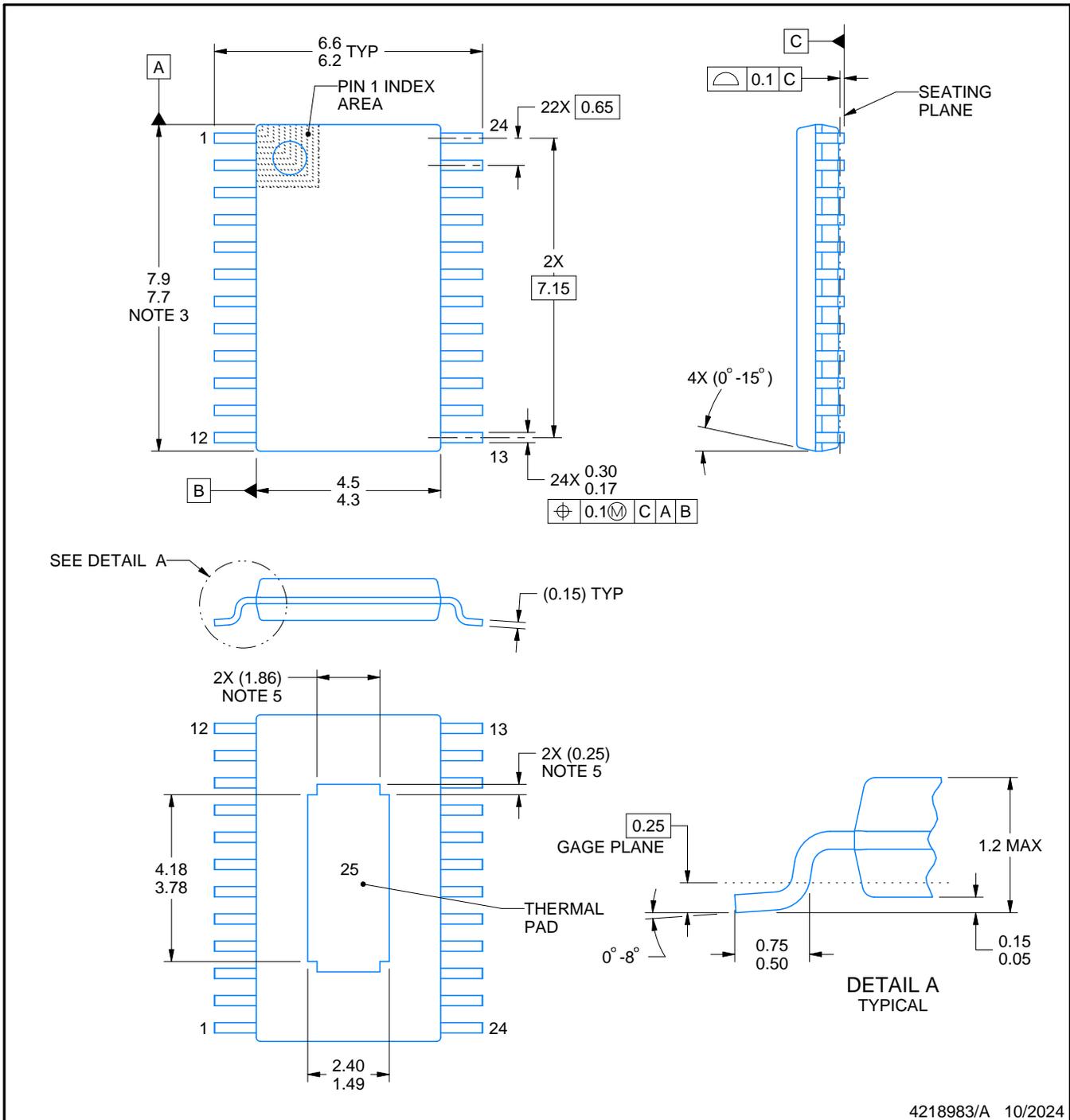
PWP (R-PDSO-G24)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.



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NOTES:

PowerPAD is a trademark of Texas Instruments.

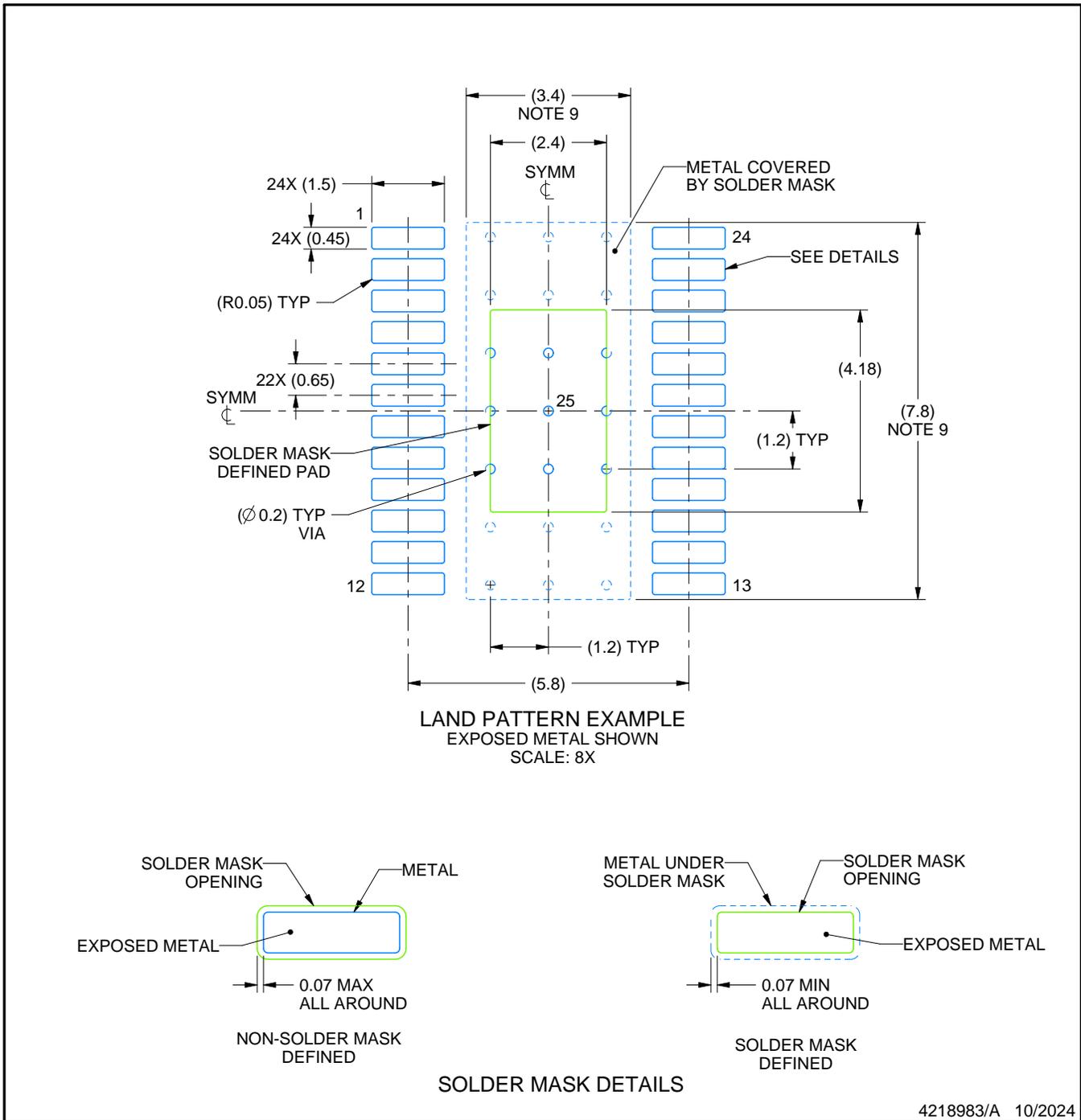
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

EXAMPLE BOARD LAYOUT

PWP0024A

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

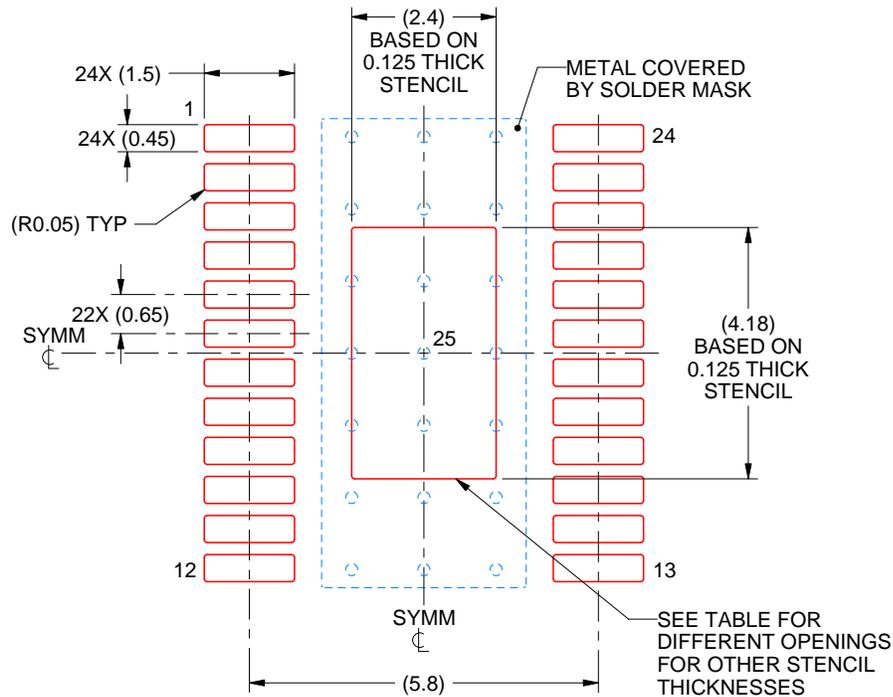
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

PWP0024A

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|-------------------|------------------------|
| 0.1 | 2.68 X 4.67 |
| 0.125 | 2.40 X 4.18 (SHOWN) |
| 0.15 | 2.19 X 3.82 |
| 0.175 | 2.03 X 3.53 |

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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