TPS923610/1/2 30V Synchronous Boost LED Driver with Ultra-low Shutdown Current and 0.1%-ratio PWM Controlled Analog Dimming

1 Features

- 2.5V to 5.5V input voltage
- Integrated 280mΩ/600mΩ LS/HS switch FETs
- Up to 95% efficiency
- 130nA ultra-low shutdown current
- High-accuracy PWM controlled analog dimming down to 0.1% dimming ratio
- Drives LED string up to
  - 24.5V for TPS923610
  - 30V for TPS923611 and TPS923612
- Switch current limit
  - 1.8A for TPS923610 and TPS923611
  - 2.25A for TPS923612
- FCCM with 1.1MHz/400KHz switching frequency options
- 200mV feedback voltage
- Internal compensation
- Protection Features
  - Over-voltage protection
  - Over-current protection
  - Under-voltage lockout protection
  - Thermal shutdown

2 Applications

- LCD back lighting
  - Smartphone
  - Thermostat
  - HMI panel
  - GPS personal navigation device
  - Dashboard camera
- General illumination
  - IP network camera
  - Video doorbell
  - Vacuum robot

3 Description

The TPS923610/1/2 is a synchronous boost LED driver that integrates both low-side and high-side switch FETs. It features an ultra-low 130nA shutdown current. The TPS923610/1/2 can drive single or parallel LED strings for LCD back lighting and general illumination.

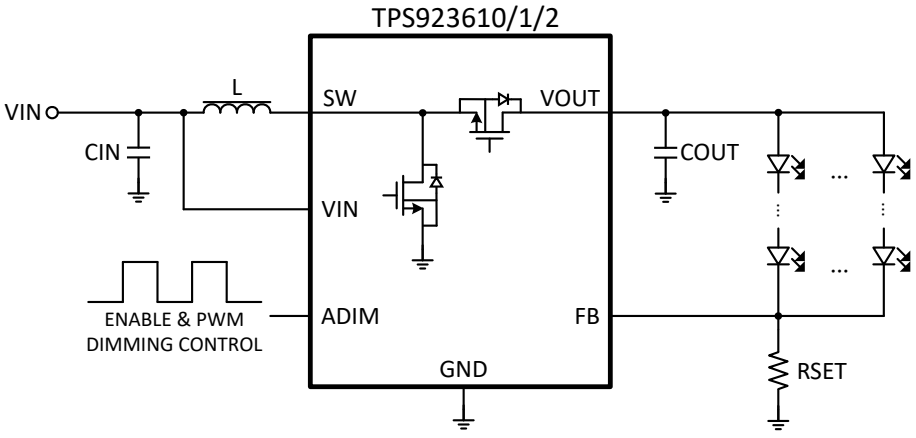
The feedback voltage is regulated to 200mV and the output current is set by an external sensor resistor, R_{SET}, as shown in the *Simplified Schematic*. During operation, a PWM signal applied to ADIM pin adjusts the feedback voltage proportionally to the PWM duty cycle, enabling precise analog dimming. The TPS923610/1/2 supports PWM controlled analog dimming with ratio as low as 0.1%, along with FCCM operation, avoiding audible noises at the output since current modulation remains purely analog.

The TPS923610/1/2 integrates over-voltage protection that disables the power stage to prevent the output voltage from exceeding the absolute maximum voltage rating during LED open conditions. The TPS923610/1/2 also provides over-current protection, under-voltage lockout protection and thermal shutdown protection.

Package Information

PART NUMBER(1)	PACKAGE	PACKAGE SIZE (NOM)
TPS923610	SOT563 (6)	1.60mm × 1.60mm
TPS923611	SOT563 (6)	1.60mm × 1.60mm
TPS923612	WSON (6)	2.00mm × 2.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

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4 Device Comparison Table

PART NUMBER	MATERIAL	MAX VOUT	CURRENT LIMIT	SWITCH FREQUENCY	PACKAGE
TPS923610	TPS923610DRLR	24.5V	1.8A	1.1MHz	SOT563-6
TPS923611	TPS923611DRLR	30V	1.8A	1.1MHz	
	TPS923611LSDRLR			400KHz	
TPS923612	TPS923612DRVR	30V	2.25A	1.1MHz	WSON-6
	TPS923612LSDRVR			400KHz	

5 Pin Configuration and Functions

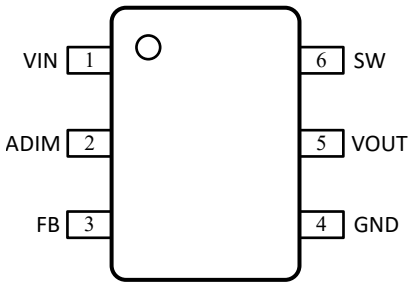


Figure 5-1. SOT563-6 DRL Package (Top View)

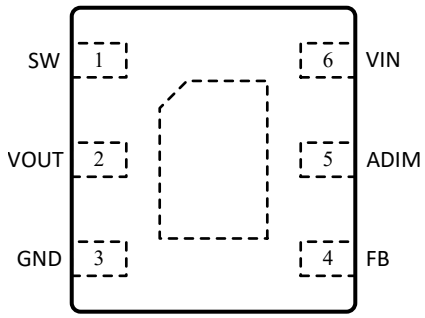


Figure 5-2. WSON-6 DRV Package (Top View)

Table 5-1. Pin Functions

PIN			TYPE[1]	DESCRIPTION
NAME	DRL	DRV		
VIN	1	6	I	Supply input pin.
ADIM	2	5	I	Enable, shutdown and PWM controlled analog dimming input pin. FB voltage is proportional to the input PWM dutycycle.
FB	3	4	I	Feedback pin for output current. Connect the sense resistor from FB to GND.
GND	4	3	G	Ground.
VOUT	5	2	P	Output pin.
SW	6	1	P	Switch pin of the converter. It is connected to the drain of the internal low-side switch FET and source of the internal high-side switch FET.

(1) I = Input, O = Output, P = Power, G = Ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage range at terminals (2)	VIN	–0.3	6	V
	SW	–1	32	V
	SW (transient <10ns)	–1	38	V
	VOUT	–0.3	32	V
	FB, PWM	–0.3	5.5	V
T_J (3)	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to network ground terminal.
(3) High junction temperatures degrade operating lifetime. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ (1)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(2)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(3)	±500	

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.
(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500V HBM is possible with the necessary precautions.
(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.5		5.5	V
V_{OUT}	Output voltage (TPS923610)	5		24.5	V
	Output voltage (TPS923611/2)	5		30	V
C_{IN}	Input capacitance, effective value	1			µF
C_{OUT}	Output capacitance, effective value	1			µF
T_J	Operating junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		SOT563 DRL 6 PINS		WSON DRV 6 PINS		UNIT
		Standard	EVM	Standard	EVM	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	142.7	87.85	93.71	81.69	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	72.6	NA	108.56	64.83	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	31.6	NA	54.15	55.55	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.3	14.53	11.58	24.91	°C/W
ψ_{JB}	Junction-to-board characterization parameter	30.5	57.6	54.27	56.13	°C/W

(1) For more information about traditional and new thermal metrics, see the TI application note *Semiconductor and IC Package Thermal Metrics*.

6.5 Electrical Characteristics

T_J = –40 to 125°C, V_{IN} = 3.6V. Typical values are at T_J = 25°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{IN}	Input voltage range		2.5		5.5	V
V_{IN_UVLO}	VIN under voltage lockout threshold	V_{IN} rising		2.3	2.49	V
		V_{IN} falling	2.05	2.17		V
I_Q	Quiescent current into V_{IN} pin	Chip enable. No switching.		260	300	µA
I_{SD}	Shutdown current into V_{IN} pin	ADIM = 0 (IC disabled), T_J = 25 °C		0.13	0.25	µA
		ADIM = 0 (IC disabled), T_J up to 85°C		0.13	0.5	µA
CONTROL LOGIC						
V_{ADIM_H}	ADIM Logic high threshold	T_J up to 85°C	1.2			V
V_{ADIM_L}	ADIM Logic low threshold	T_J up to 85°C			0.385	V
R_{ADIM_PD}	ADIM pin internal pull down resistor			600		kΩ
t_{ADIM_EN} (1)	ADIM first pulse high time to enable device		40			us
t_{ADIM_SD} (1)	ADIM logic low time to shutdown		2.5			ms
t_{ADIM_PWM} (1)	ADIM minimum PWM on time for dimming		20			ns
VOLTAGE REFERENCE						
V_{FB}	PWM duty cycle 100% (TPS923610, TPS923611)		195	200	206	mV
		T_J = 25°C	198	200	203	mV
	PWM duty cycle 10% (TPS923610, TPS923611)		14.5	20.2	25.5	mV
		T_J = 25°C	18	20.2	22	mV
	PWM duty cycle 1% (TPS923610, TPS923611)	T_J = 25°C	1.7	2.2	2.7	mV
	PWM duty cycle 0.1% (TPS923610, TPS923611)(1)	T_J = 25°C		0.3		mV
	PWM duty cycle 100% (TPS923612)		198	203	207	mV
		T_J = 25°C	201	203	206	mV
	PWM duty cycle 10% (TPS923612)		16	20.6	26	mV
		T_J = 25°C	18.6	20.6	22.6	mV
	PWM duty cycle 1% (TPS923612)	T_J = 25°C	1.75	2.25	2.75	mV
	PWM duty cycle 0.1% (TPS923612)(1)	T_J = 25°C		0.3		mV
I_{FB}	FB pin bias current	V_{FB}=200mV			0.1	uA
SWITCH CONVERTER						
R_{DSON_LS}	Low-side switch FET on resistance (TPS923610, TPS923611)			280	400	mΩ
		T_J = 25°C		280	300	mΩ
	Low-side switch FET on resistance (TPS923612)			300	420	mΩ
		T_J = 25°C		300	320	mΩ

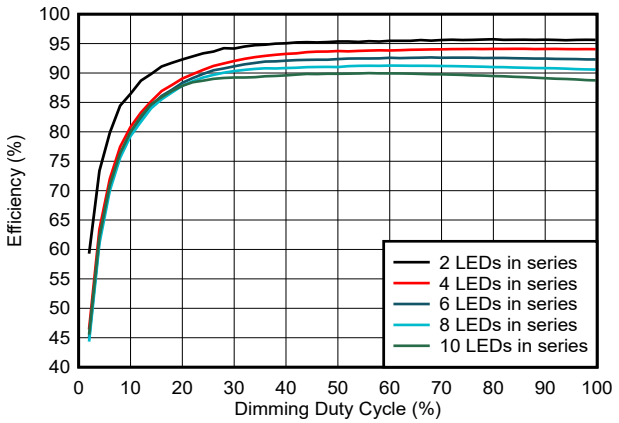
T_J = –40 to 125°C, V_{IN} = 3.6V. Typical values are at T_J = 25°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{DSON_HS}	High-side switch FET on resistance (TPS923610, TPS923611)			600	900	mΩ
		T_J = 25°C		600	680	mΩ
	High-side switch FET on resistance (TPS923612)			625	925	mΩ
		T_J = 25°C		625	705	mΩ
F_{SW} (1)	Switching frequency (TPS923610DRLR, TPS923611DRLR, TPS923612DRVR)			1.1		MHz
	Switching frequency (TPS923611LSDRLR, TPS923612LSDRVR)			0.4		MHz
V_{OVP_R}	VOUT over-voltage rising threshold (TPS923610)	T_J up to 85°C	24.25	25	25.5	V
	VOUT over-voltage rising threshold (TPS923611, TPS923612)	T_J up to 85°C	29.6	30.5	31.4	V
V_{OVP_HYS}	VOUT over-voltage falling threshold			1		V
CURRENT LIMIT						
I_{LIM}	FET switching peak current limit (TPS923610, TPS923611)		1.6	1.8	2.1	A
	FET switching peak current limit (TPS923612)		1.95	2.25	2.6	A
I_{LIM_START} (1)	FET switching start-up peak current			0.8		A
THERMAL SHUTDOWN						
T_{TSD_R} (1)	Thermal shutdown rising threshold	T_J rising		170		°C
T_{TSD_F} (1)	Thermal shutdown falling threshold	T_J falling		150		°C

(1) Not production tested. Guaranteed by simulation and bench test.

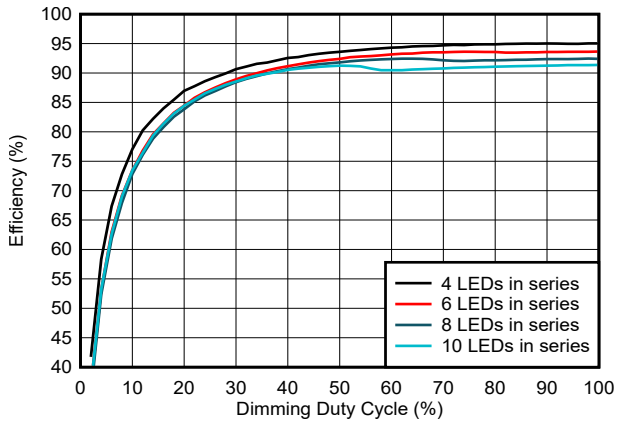
6.6 Typical Characteristics

At T_A = 25°C, unless otherwise noted.



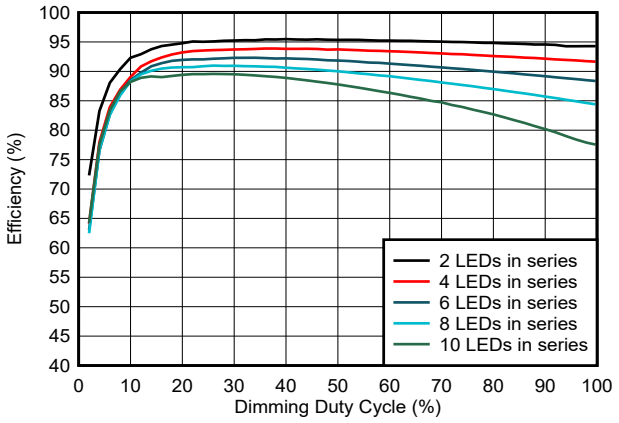
TPS923611DRLR 10uH Inductor
3.6V Input Voltage 60mA IOUT at 100% Dutycycle

Figure 6-1. Efficiency vs Dimming Dutycycle



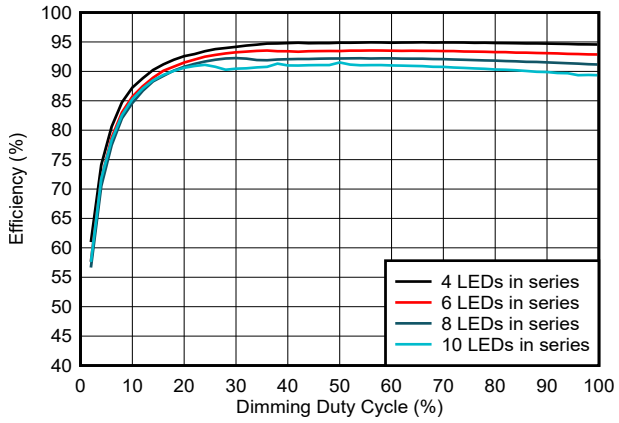
TPS923611DRLR 10uH Inductor
5V Input Voltage 60mA IOUT at 100% Dutycycle

Figure 6-2. Efficiency vs Dimming Dutycycle



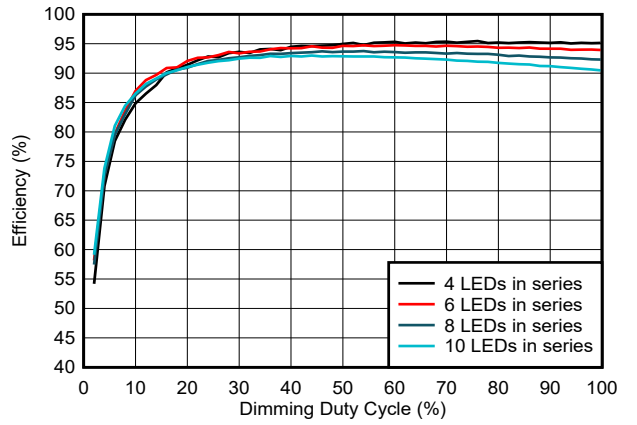
TPS923612DRVR 10uH Inductor
3.6V Input Voltage 120mA IOUT at 100% Dutycycle

Figure 6-3. Efficiency vs Dimming Dutycycle



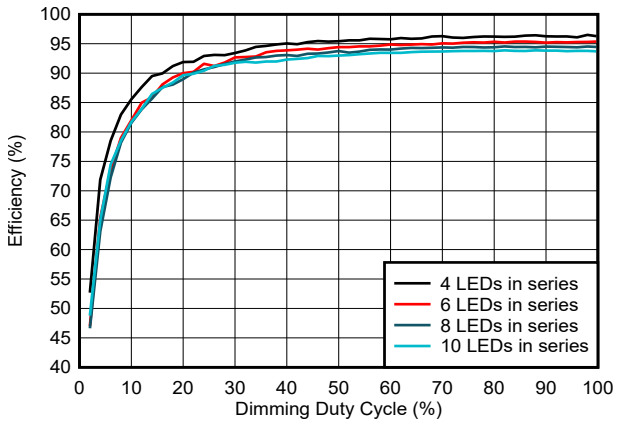
TPS923612DRVR 10uH Inductor
5V Input Voltage 120mA IOUT at 100% Dutycycle

Figure 6-4. Efficiency vs Dimming Dutycycle



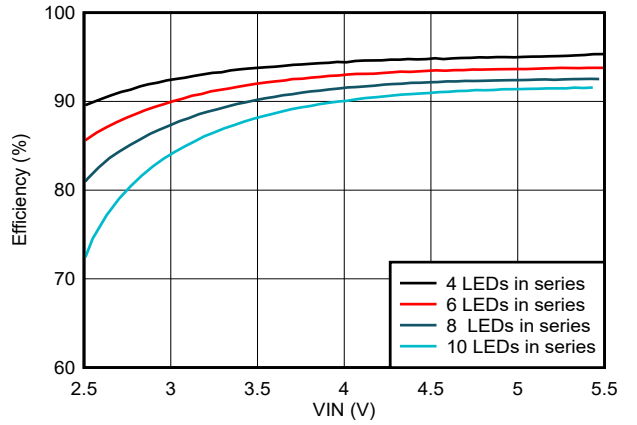
TPS923611LSDRLR 47uH Inductor
3.6V Input Voltage 60mA IOUT at 100% Dutycycle

Figure 6-5. Efficiency vs Dimming Dutycycle



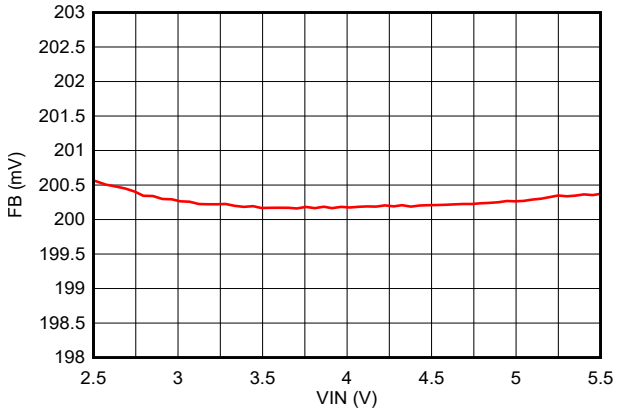
TPS923611LSDRLR 47uH Inductor
5V Input Voltage 60mA IOUT at 100% Dutycycle

Figure 6-6. Efficiency vs Dimming Dutycycle



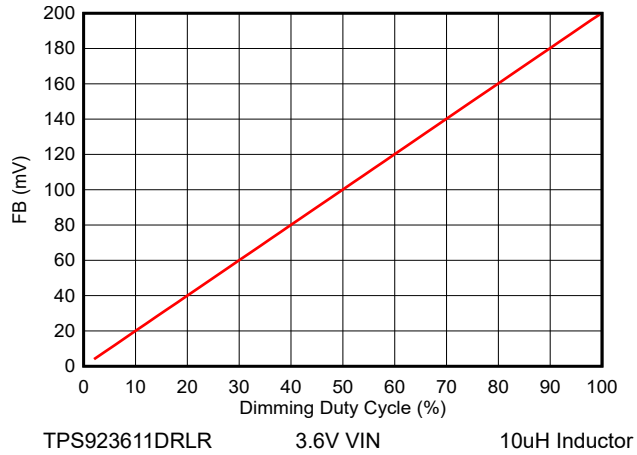
TPS923611DRLR 60mA IOUT 10uH Inductor

Figure 6-7. Efficiency vs VIN



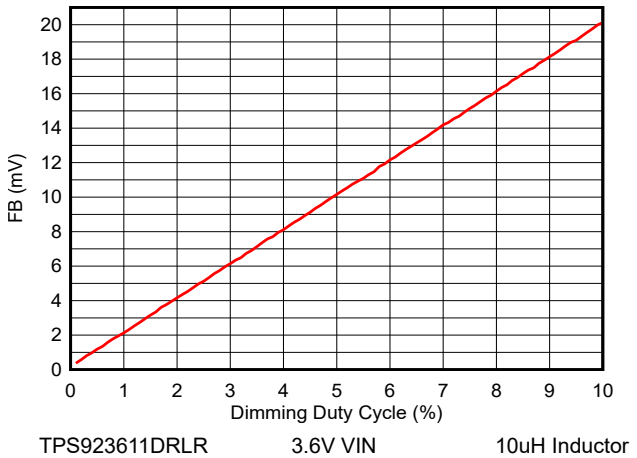
TPS923611DRLR 60mA IOUT 10uH Inductor

Figure 6-8. FB vs VIN



TPS923611DRLR 3.6V VIN 10uH Inductor

Figure 6-9. FB vs Dimming Dutycycle 1%~100%



TPS923611DRLR 3.6V VIN 10uH Inductor

Figure 6-10. FB vs Dimming Dutycycle 0.1%~10%

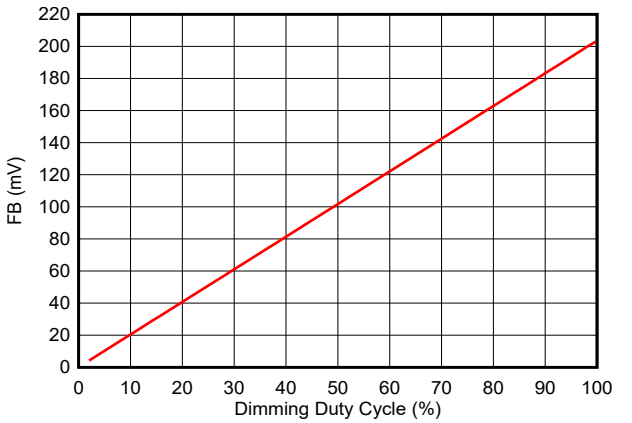


Figure 6-11. FB vs Dimming Dutycycle 1%~100%

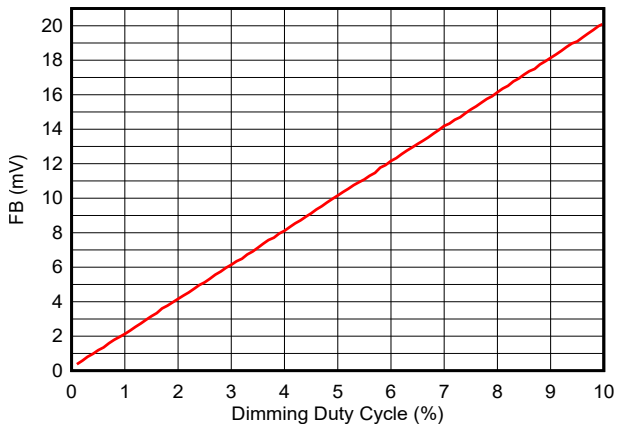


Figure 6-12. FB vs Dimming Dutycycle 0.1%~10%

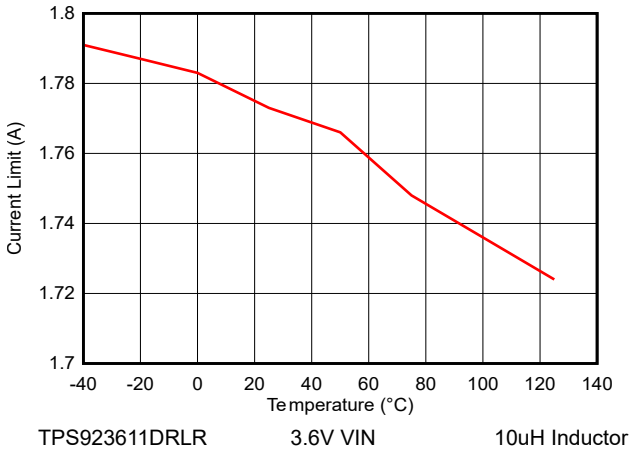


Figure 6-13. Current Limit vs Temperature

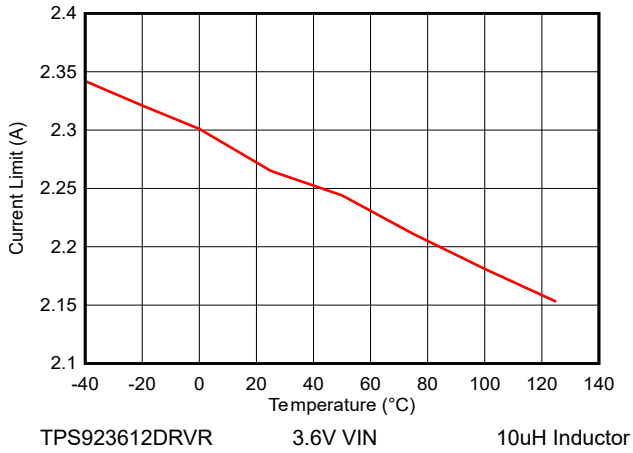


Figure 6-14. Current Limit vs Temperature

7 Detailed Description

7.1 Overview

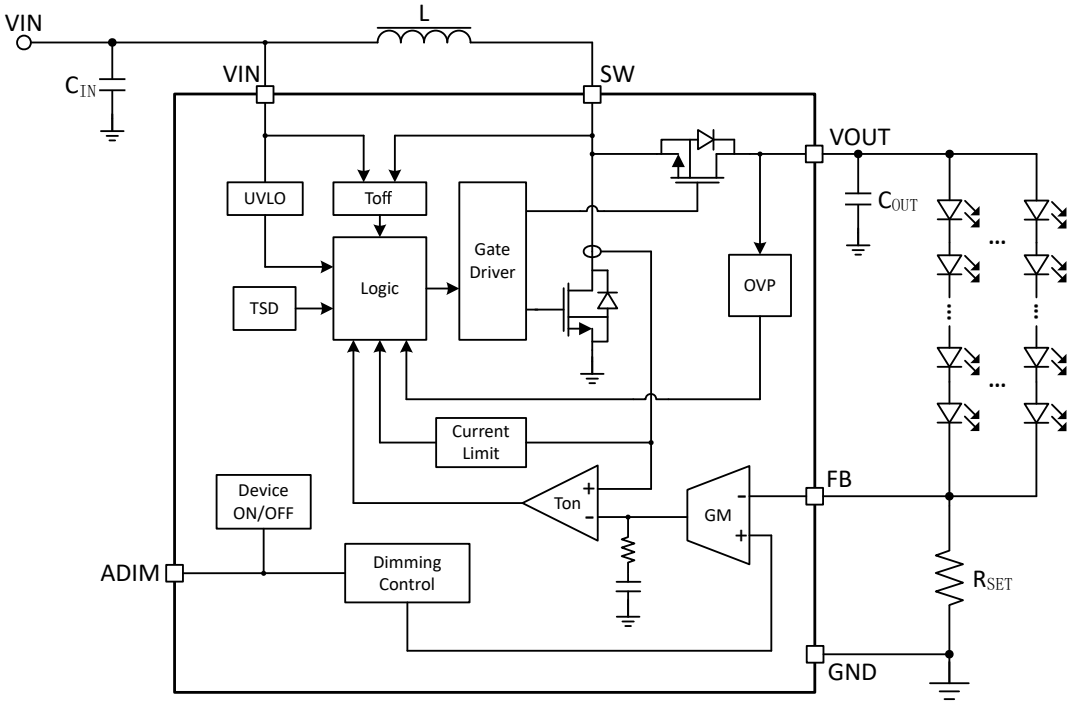
The TPS923610/1/2 is a high-current, high-efficiency, high-output-voltage fully-integrated synchronous boost converter in small package size. The device integrates 280mΩ low-side switch FET and 600mΩ high-side switch FET and is designed for output voltage up to 30V with a switch peak current limit of 2.25A. Its large driving capability can drive single or parallel LED strings for small to large size LCD panel back lighting or general illumination.

The TPS923610/1/2 operates in peak current mode (PCM) control with quasi-constant frequency. It is internally compensated for maximum flexibility and stability, which also enables a simple design. During the low-side switch FET on-time, the inductor current rises until reaching a threshold value set by the internal GM amplifier. Then, the low-side switch FET is turned off and the high-side switch FET is turned on which lets the current flow towards the output of the boost converter. The adaptive off-time varies as a function of V_{IN} and V_{OUT}, to maintain a nearly constant frequency, which provides better stability for the system over a wider range of input voltage and output voltage than conventional boost converters. The TPS923610/1/2 topology also has the benefits of providing very good load and line regulations, and excellent line and load transient responses.

The TPS923610/1/2 implements PWM controlled analog dimming by changing feedback (FB) voltage proportional to the duty cycle of PWM input signal in 0.1% to 100% range. The feedback loop regulates the FB pin to a reference voltage of 200mV for 100% PWM duty cycle, reducing the power dissipation in the current sense resistor.

The TPS923610/1/2 is optimized for single-cell lithium-ion battery applications, featuring an ultra-low 130nA shutdown current that extends battery life. It can support 2.5V low V_{IN} when battery near full discharge. The TPS923610/1/2 has both 1.1MHz version and 400KHz version switch frequency options. The 1.1MHz version supports ultra-compact surface-mount inductors and capacitors, while the 400KHz version is ideal for applications with EMI constraints near the 1.1MHz frequency band.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Enable and Start-up

The ADIM pin performs not only the dimming function, but also the enable/shutdown function. When the V_{IN} voltage is above the UVLO threshold, the TPS923610/1/2 can be enabled by driving the ADIM pin higher than the threshold voltage V_{ADIM_H} for a period longer than t_{ADIM_EN}.

Soft-start function is integrated into the device to avoid high inrush current spike during start-up. After the device is enabled, the GM amplifier output voltage ramps up very slowly. During this period, the switch current limit is set to I_{LIM_STRAT}. After this period, the switch current limit changes back to I_{LIM} and the FB pin voltage ramps up to reference voltage slowly. These features maintain the smooth start-up and minimize the inrush current.

7.3.2 Under-Voltage Lockout (UVLO)

The UVLO circuit prevents the device from malfunctioning at low input voltage and the battery from excessive discharge. When the input voltage, V_{IN}, falls below the UVLO falling threshold, the device is shut down, and the internal switch FETs is turned off. When the input voltage, V_{IN}, rises above the UVLO rising threshold, the device starts operating.

7.3.3 Shutdown

The TPS923610/1/2 enters shutdown mode when the ADIM pin voltage is logic low for more than 2.5ms. During shutdown, the input supply current for the device is only 130nA typically. Although there is still a path between the input and the LEDs through the inductor and body diode of internal high-side FET, the current of this path is neglectable since the forward voltage of the LED string added the forward voltage of internal high-side FET body diode exceeds the maximum input voltage, V_{IN}, which maintains that the LEDs remain off in shutdown and no contribution to shutdown current.

7.3.4 Boost Control Operation

The TPS923610/1/2 uses peak current mode (PCM) control and full internal compensation to provide high transient response performance over a wide range of operating conditions.

In the normal operation, at the beginning of each switching cycle, the low-side switch FET is turned on and the inductor current ramps up to a peak current determined by the output of the internal GM amplifier. After the peak current is reached, the current comparator trips and turns off the low-side switch FET. Then, the inductor current goes through the body diode of the high-side switch FET in a dead-time duration and the inductor current decreases. After the dead-time duration, the high-side switch FET is turned on and is not turned off until the calculated adaptive off-time is reached. The adaptive off-time varies as a function of V_{IN} and V_{OUT}, to maintain a nearly constant frequency. After the high-side switch FET is turned off, the inductor current goes through the body diode of the high-side switch FET again in another dead-time duration. After the dead-time duration, the low-side switch FET is turned on again and the switching cycle is repeated.

In light load condition, the TPS923610/1/2 works in forced continuous conduction mode (FCCM). During FCCM, the switching frequency is maintained at an almost constant level over the entire load range. This feature not only benefits the small output current accuracy, but also reduces output ripple and avoids audible noise caused by switching frequency drop.

7.3.5 Switching Peak Current Limit

To prevent an over-current stress, the output of the internal GM amplifier has a internal high clamp in order to set a cycle-by-cycle current limit to the inductor peak current. The low-side switch FET is turned off immediately as soon as the inductor current touches the current limit, I_{ILIM}.

7.3.6 Over-Voltage Protection

The TPS923610/1/2 integrates over-voltage protection preventing over-voltage on the output and securing the circuits connected to the output from excessive-voltage damage in fault conditions, such as LED string open circuit.

When the voltage of VOUT pin exceeds V_{OVP_R}, the TPS923610/1/2 stops switching immediately until the voltage at the VOUT pin drops the hysteresis value to lower than V_{OVP_R}-V_{OVP_HYS}. Then, the switching restarts again. After the detection above is triggered 3 times, the TPS923610/1/2 enters over-voltage protection mode, in which the switching stops and does not resume switching even if the voltage at the VOUT pin falls below V_{OVP_R}-V_{OVP_HYS}. The TPS923610/1/2 remains in over-voltage protection mode until it is reset by two ways, which are shutdown and re-enabling device by the ADIM pin or triggering UVLO by the VIN pin.

7.3.7 Output Current Setting

The FB voltage is regulated to a 200mV reference voltage. The LED current is set externally using a current-sense resistor in series with the LED strings. The value of the R_{SET} (R3 on EVM) is calculated using:

$$I_{OUT} = \frac{V_{FB}}{R_{SET}} \quad (1)$$

where

- I_{LED} = total output current of LED strings
- V_{FB} = regulated voltage of FB pin
- R_{SET} = current sense resistor

The output current tolerance depends on the FB accuracy and the current sensor resistor accuracy.

R2 is optional resistor paralleled with R3 to fine tune the R_{SET} to target value, or used to balance the total power loss on R_{SET}.

7.3.8 Output Current PWM Controlled Analog Dimming

The TPS923610/1/2 implements PWM controlled analog dimming to adjust the brightness of LED strings during operation. Pulse width modulation (PWM) signal can be applied at ADIM pin to control the total output current as an analog value. When the voltage of the ADIM pin is constantly high, the voltage of the FB pin is regulated to the full value, 200mV typically. When the signal applied to the ADIM pin is PWM, the regulation voltage at the FB pin is reduced to the full value multiplied by PWM duty cycle, and as a result, the total output current is reduced, too. The TPS923610/1/2 supports such dimming method with dimming ratio down to 0.1%.

The relationship between the PWM duty cycle and FB regulation voltage is given by:

$$V_{FB} = Duty \times 200mV \quad (2)$$

where

- Duty = Duty cycle of the input PWM signal
- 200mV = The full value of internal reference voltage

In this way, the user can easily control the LED strings brightness by controlling the duty cycle of the input PWM signal.

As shown in Figure 7-1, the TPS923610/1/2 chops up the internal 200mV reference voltage at the duty cycle of the PWM signal. The pulse signal is then filtered by an internal low-pass filter. The output of the filter is connected to the GM amplifier as the reference voltage for the FB pin regulation. Therefore, although a PWM signal is used for brightness dimming, only the LED DC current is modulated, which is often referred as analog dimming. This mechanism eliminates the audible noise which often occurs when the LED current is pulsed in replica of the frequency and duty cycle of PWM control. Unlike other methods which filter the PWM signal for analog dimming, TPS923610/1/2 regulation voltage is independent of the PWM logic voltage level which often has large variations.

For optimum performance, use the PWM dimming frequency in the range of 10kHz to 200kHz. If the PWM frequency is lower than 10kHz, it is out of the low pass filter's filter range, the FB regulation voltage ripple becomes large, causing large output ripple and may generate audible noise.

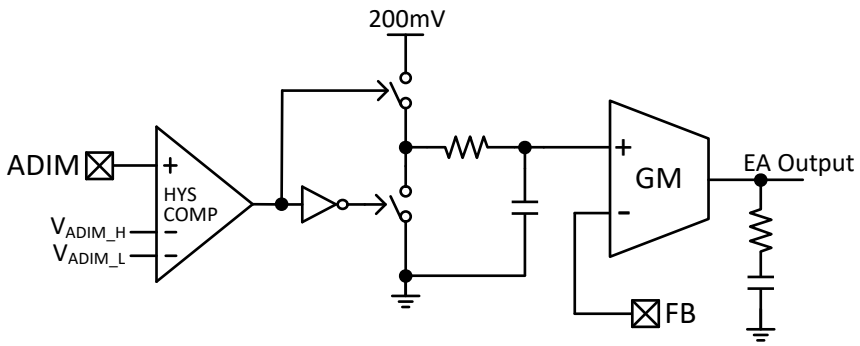


Figure 7-1. FB Voltage Adjusted by PWM Controlled Analog Dimming

7.3.9 Thermal Shutdown

The TPS923610/1/2 implements thermal shutdown protection to prevent damages due to excessive heat and power dissipation. The thermal shutdown happens when the device junction temperature reaches T_{TSD_R}. When the thermal shutdown is triggered, the TPS923610/1/2 stops switching until the junction temperature falls below T_{TSD_F}, then the device starts switching again.

7.4 Device Functional Modes

7.4.1 Normal Operation Mode

The TPS923610/1/2 enters normal operation mode from shutdown mode when the voltage of ADIM pin is higher than the threshold voltage V_{ADIM_H} for a period longer than t_{ADIM_EN}, along with the soft-start process. In normal operation mode, the TPS923610/1/2 uses peak current mode (PCM) control and operates in forced continuous conduction mode (FCCM) over the entire load range.

7.4.2 Over-Voltage Protection Mode

The TPS923610/1/2 enters over-voltage protection mode in a VOUT pin over-voltage condition and prevent device from keep turning on and off switching. If the voltage of VOUT pin is detected rising above V_{OVP_R} and then dropping below V_{OVP_R}-V_{OVP_HYS} for 3 times, the TPS923610/1/2 stays in over-voltage protection mode until the device is reset by one of two ways, which are shutdown and re-enabling device by the ADIM pin or triggering UVLO by the VIN pin. In over-voltage protection mode, the switching stops.

7.4.3 Shutdown Mode

The TPS923610/1/2 enters shutdown mode from normal operation mode or over-voltage protection mode when the voltage of ADIM pin is lower than the threshold voltage V_{ADIM_L} for a period longer than t_{ADIM_SD}. In shutdown mode, the input supply current for the device is I_{SD}.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS923610/1/2 is a boost LED driver which can drive single or parallel LED strings for LCD panel back lighting or general illumination. This section includes a design procedure (*Section 8.2.2*) to select component values for the TPS923610/1/2 typical application (Figure 8-1).

8.2 Typical Application

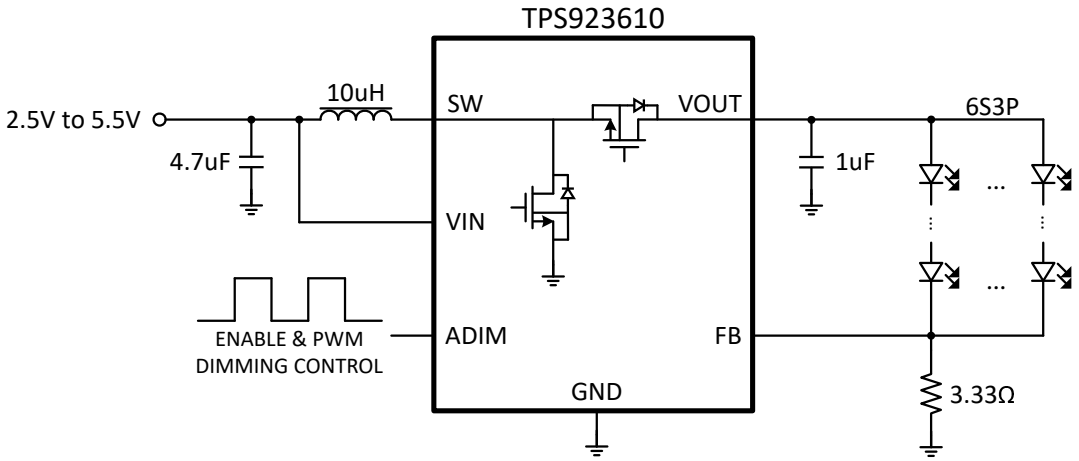


Figure 8-1. TPS923610/1/2 60mA Total Output Current Reference Design

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 8-1 as the input parameters.

Table 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	2.5V to 5.5V
Output, LED number in a string	6
Output, LED string number	3
Output, LED current per string	20mA

8.2.2 Detailed Design Procedure

8.2.2.1 LED Current Set Resistor

The resistor value to set the LED current (R_{SET}) can be calculated as

$$R_{SET} = \frac{V_{FB}}{I_{OUT}} \quad (3)$$

8.2.2.2 Inductor Selection

Inductor selection impacts power efficiency, steady-state operation, transient response and loop stability. These factors make inductor selction the most important component in power regulator design. There are three important inductor specifications, inductor value, DC resistance and saturation current. Considering inductor value alone is not enough. The inductor value determines the inductor ripple current. Choose an inductor that can handle the necessary peak current without saturating and optimize light load efficiency when using dimming. In a boost regulator, the input DC current can be calculated as

$$I_{L(DC)} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (4)$$

where

- V_{OUT} = boost output voltage
- I_{OUT} = boost output current
- V_{IN} = boost input voltage
- η = power conversion efficiency

The inductor current peak to peak ripple can be calculated as

$$\Delta I_{L(P-P)} = \frac{1}{L \times \left(\frac{1}{V_{OUT} - V_{IN}} + \frac{1}{V_{IN}}\right) \times F_S} \quad (5)$$

where

- $\Delta I_{L(PP)}$ = inductor peak-to-peak ripple
- L = inductor value
- F_S = boost switching frequency
- V_{OUT} = boost output voltage
- V_{IN} = boost input voltage

Therefore, the peak current $I_{L(P)}$ seen by the inductor is calculated with

$$I_{L(P)} = I_{L(DC)} + \frac{\Delta I_{L(P-P)}}{2} \quad (6)$$

Also, the valley current $I_{L(V)}$ seen by the inductor is calculated with

$$I_{L(V)} = I_{L(DC)} - \frac{\Delta I_{L(P-P)}}{2} \quad (7)$$

Inductor values can have ±20% tolerance with no current bias. When the inductor current approaches saturation level, inductance can decrease 20% to 35% from the 0A value depending on how the inductor vendor defines saturation current. When using an inductor with a smaller inductance value with relative light load, the inductor current ramps down to below zero before the end of each switching cycle due to forced continuous condition mode (FCCM), which reduces light load efficiency. Large inductance value provides much more output current and higher conversion efficiency. Thus, choose a sufficiently large inductor that that maintains a non-negative valley current under light-load conditions helps optimize efficiency.

For these reasons, a 10µH inductor is recommended based on input voltage, output voltage and output current condition of this application, to maintain non-negative current in most of load range by PWM controlled analog dimming.

8.2.2.3 Output Capacitor Selection

The output capacitor is mainly selected to meet the requirement for the output ripple and loop stability. This ripple voltage is related to capacitance and capacitor equivalent series resistance (ESR). Assuming a capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated with

$$C_{OUT} = \frac{(V_{OUT} - V_{IN}) \times I_{OUT}}{V_{OUT} \times F_S \times V_{ripple}} \quad (8)$$

where

- V_{ripple} = peak-to-peak output ripple

The additional part of the ripple caused by ESR is calculated using: $V_{ripple\_ESR} = I_{OUT} \times R_{ESR}$

Due to its low ESR, V_{ripple_ESR} could be neglected for ceramic capacitors, a 1µF to 4.7µF capacitor is recommended for typical application.

8.2.2.4 Thermal Considerations

The allowable IC junction temperature must be considered under normal operating conditions. This restriction limits the power dissipation of the TPS923610/1/2. The allowable power dissipation for the device can be determined by

$$P_D = \frac{T_J - T_A}{R_{\theta JA}} \quad (9)$$

where

- T_J is allowable junction temperature given in recommended operating conditions
- T_A is the ambient temperature for the application
- $R_{\theta JA}$ is the thermal resistance junction-to-ambient given in Power Dissipation Table

8.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.5V and 5.5V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS923610/1/2 devices, additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

8.4 Application Curves

Typical application condition is as in Section 8.2, V_{IN} = 3.6V, R_{SET} = 3.33Ω, L = 10µH, C_{OUT} = 1µF, 6 LEDs in serial in each string and total 3 strings in parallel (unless otherwise specified).

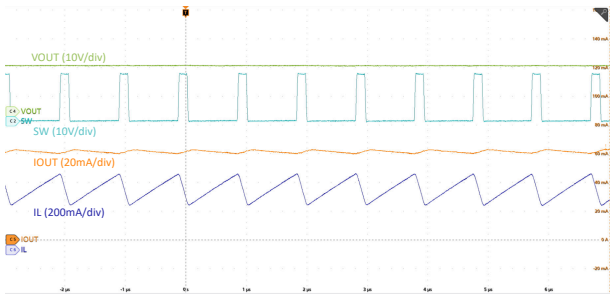


Figure 8-2. Switching Dimming Duty = 100%

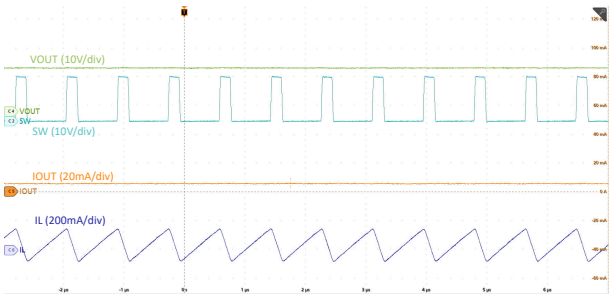


Figure 8-3. Switching Dimming Duty = 10%

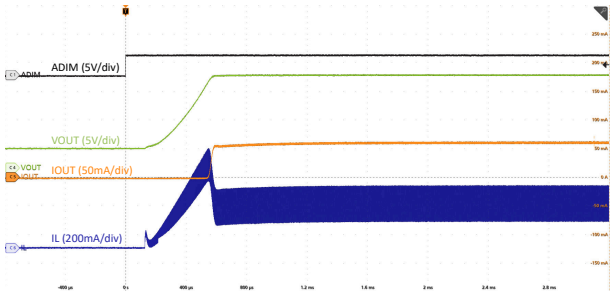


Figure 8-4. Start-up Dimming Duty 100%

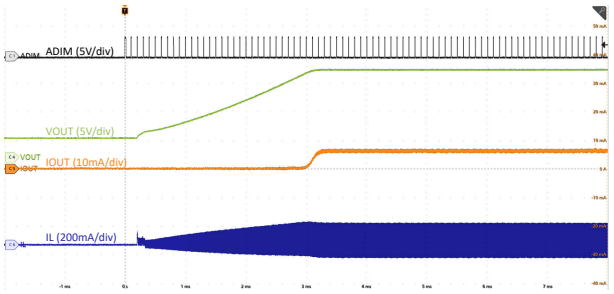


Figure 8-5. Start-up Dimming Duty 10%

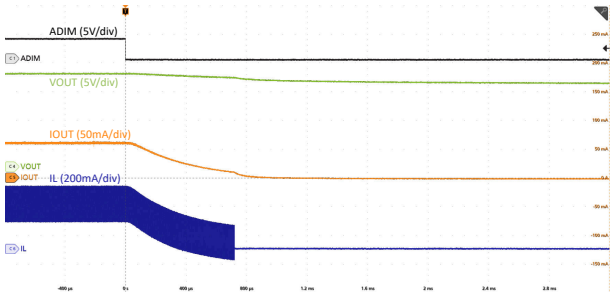


Figure 8-6. Shutdown Dimming Duty 100%

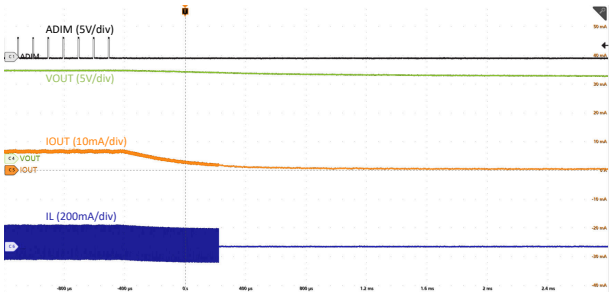
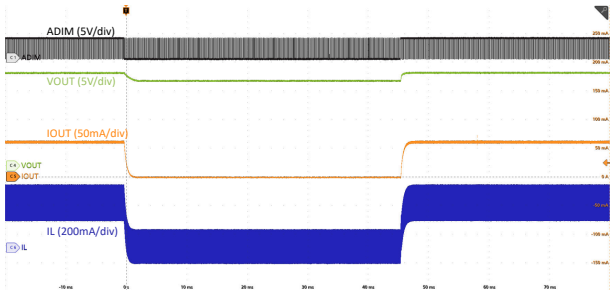
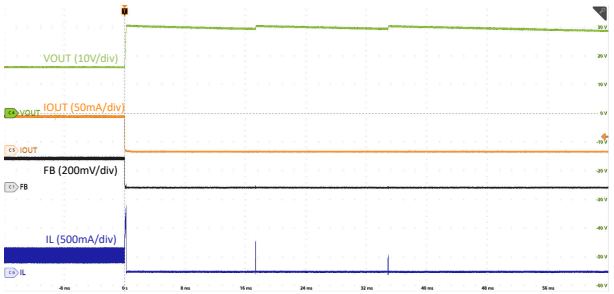


Figure 8-7. Shutdown Dimming Duty 10%



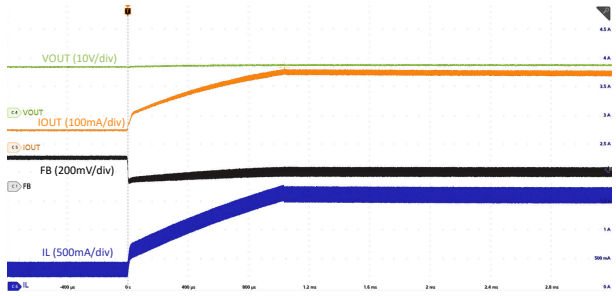
Dimming Duty 90% → 1% → 90%

Figure 8-8. Dimming Transient



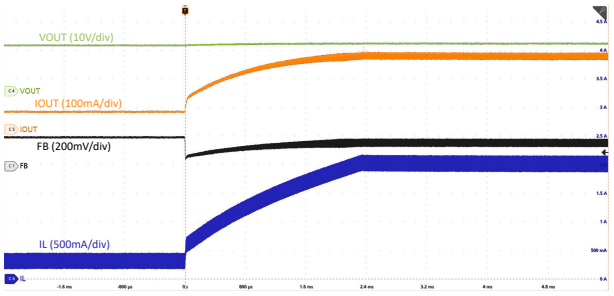
Trigger 3 times then latch

Figure 8-9. Open LED Over-voltage Protection



TPS923611DRLR

Figure 8-10. FB Short-to-ground Over-current Protection



TPS923612DRVR

Figure 8-11. FB Short-to-ground Over-current Protection

8.5 Layout

8.5.1 Layout Guidelines

As for all switching power supplies, especially those high frequency and high current ones, layout is an important design step. If layout is not carefully done, the regulator can suffer from instability as well as noise problems. Therefore, use wide and short traces for high current paths. Please follow the layout guidelines below.

1. The output capacitor C_{OUT} must be put close to VOUT pin. Having the ground of C_{OUT} close to the GND pin (GND copper pour) is also beneficial because there is large ground return current flowing between them. This minimizes the switching noise at output.
2. FB resistor must be put close to FB pin and GND pin (GND copper pour). This benefits the output current accuracy.
3. The SW pin carries high current with fast rising and falling edge; therefore, the connection between the SW pin to the inductor must be kept as short and wide as possible.
4. The input capacitor C_{IN} must be close to VIN pin and GND pin to reduce the input ripple seen by the device. If possible, choose a capacitance of higher value.
5. When laying out signal ground, TI recommends using short traces separated from power ground traces and connecting them together at a single point close to the GND pin.

8.5.2 Layout Example

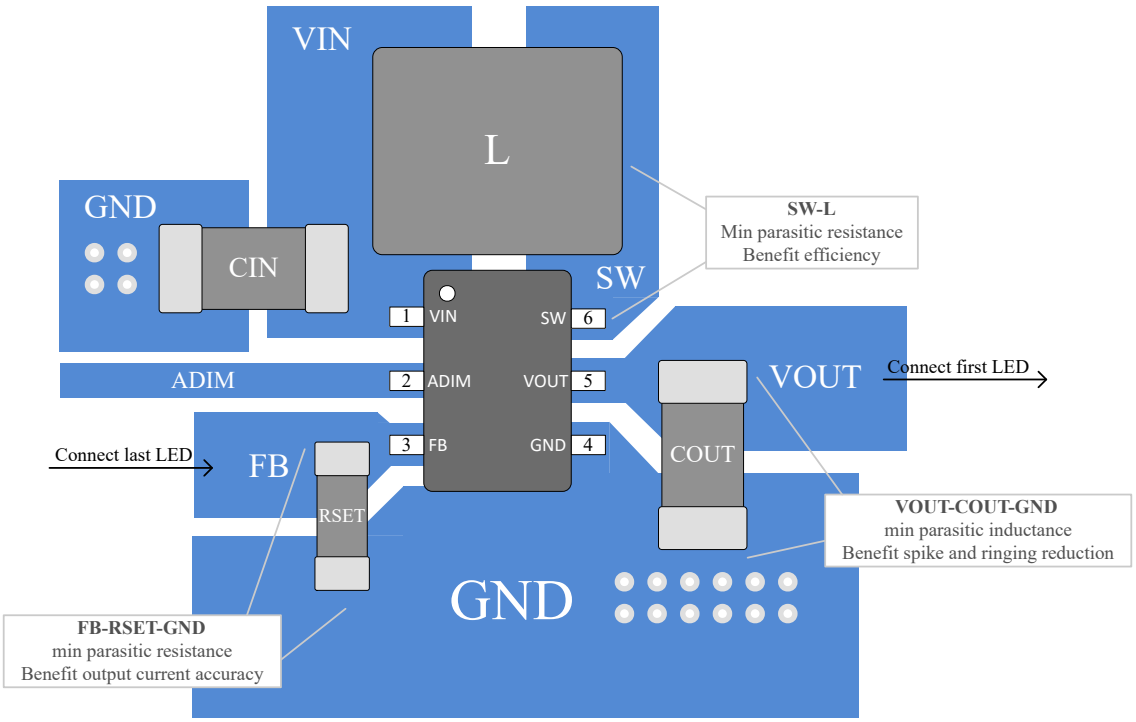


Figure 8-12. TPS923610/1 SOT563 Layout

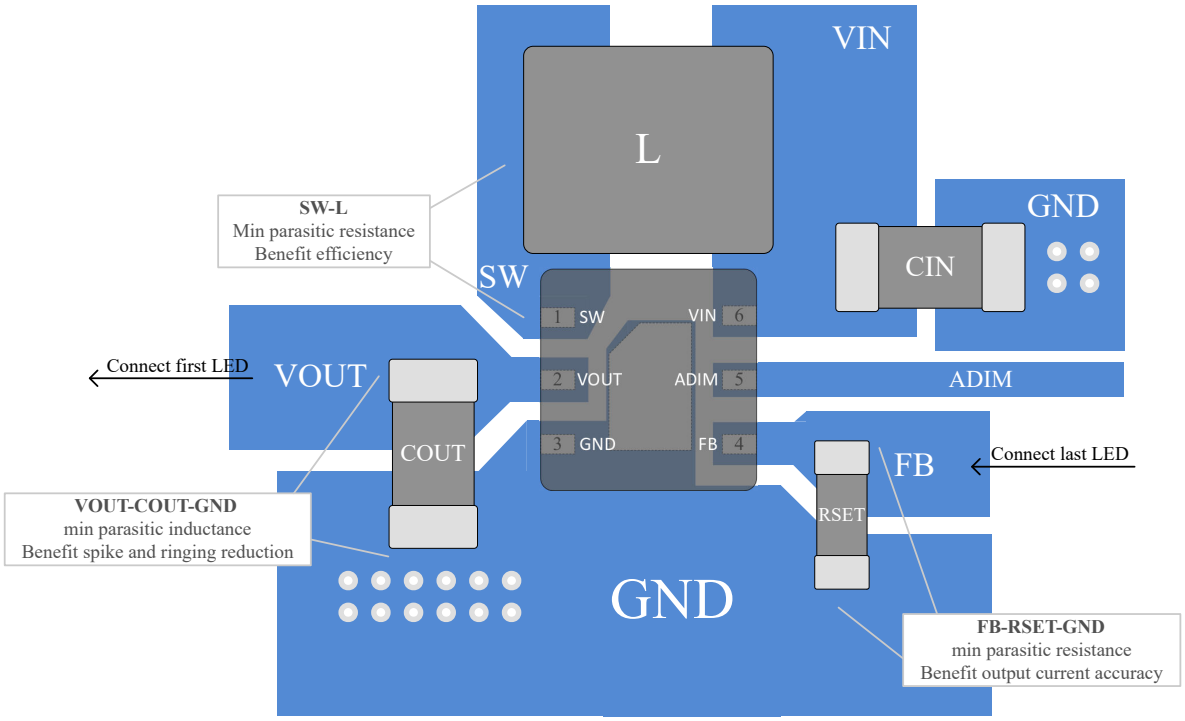


Figure 8-13. TPS923612 WSON Layout

9 Device and Documentation Support

9.1 Device Support

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (September 2023) to Revision A (November 2025)	Page
• Updated data sheet status from *Advanced Information* to *Production Data*	1

DATE	REVISION	NOTES
September 2025	*	Advance Information Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS923610DRLR	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	BARE COPPER	Level-1-260C-UNLIM	-40 to 125	T610
TPS923611DRLR	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	BARE COPPER	Level-1-260C-UNLIM	-40 to 125	T611
TPS923611LSDRLR	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	BARE COPPER	Level-1-260C-UNLIM	-40 to 125	611L
TPS923612DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T612
TPS923612LSDRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	612L

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

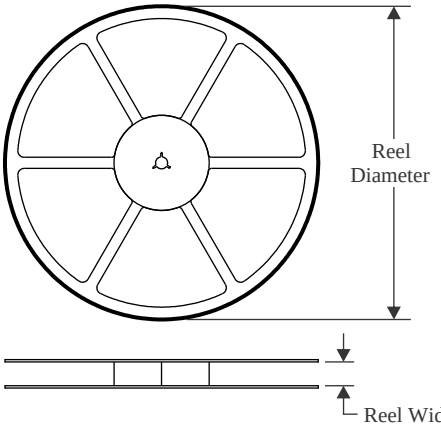
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

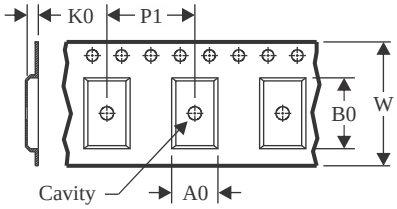
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

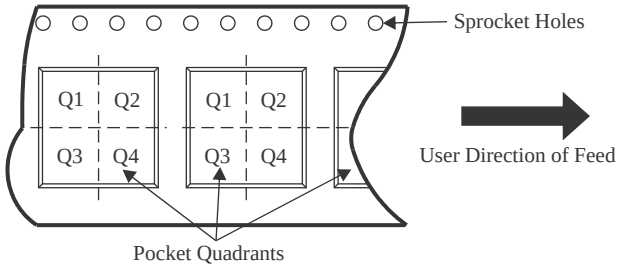


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

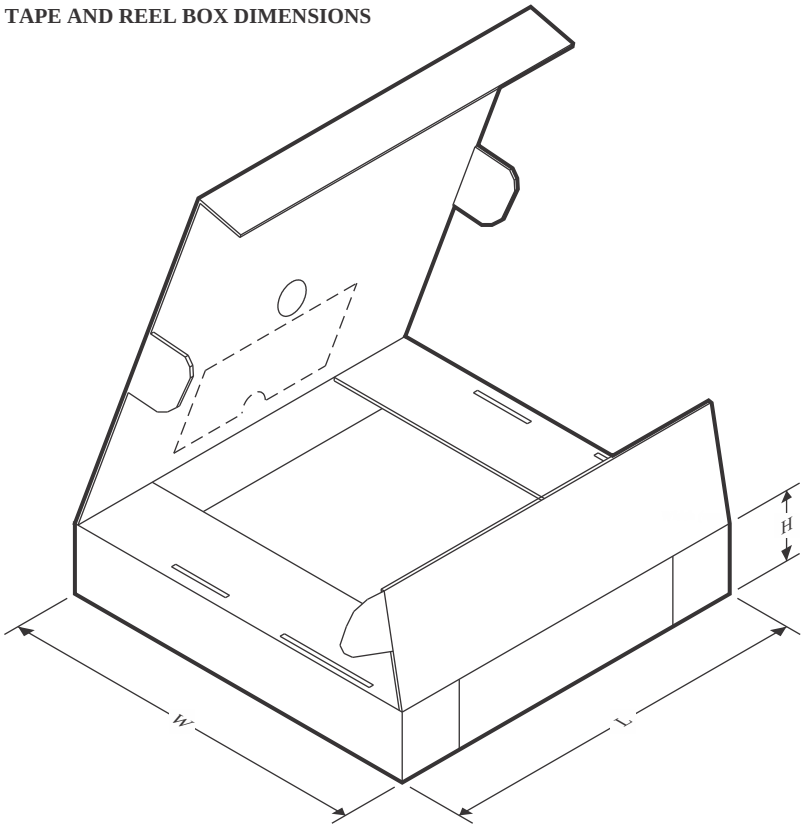
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS923610DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	1.8	1.8	0.75	4.0	8.0	Q3
TPS923611DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	1.8	1.8	0.75	4.0	8.0	Q3
TPS923611LSDRLR	SOT-5X3	DRL	6	4000	180.0	8.4	1.8	1.8	0.75	4.0	8.0	Q3
TPS923612DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS923612LSDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

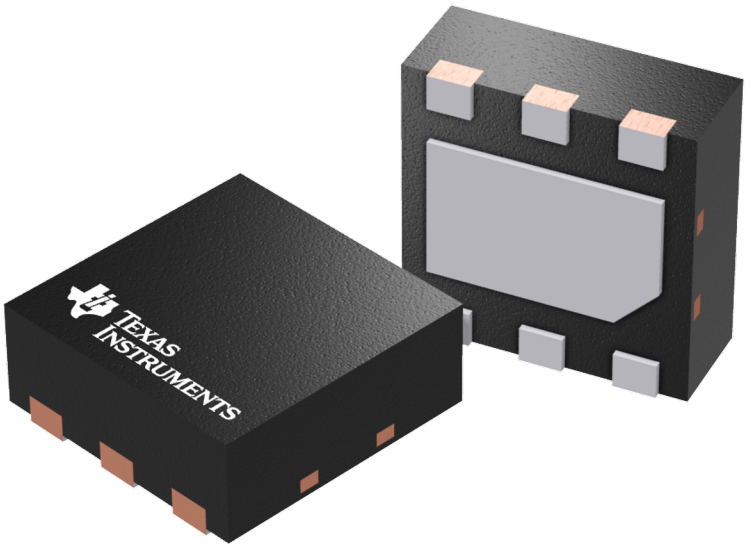


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS923610DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
TPS923611DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
TPS923611LSDRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
TPS923612DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TPS923612LSDRVR	WSON	DRV	6	3000	210.0	185.0	35.0

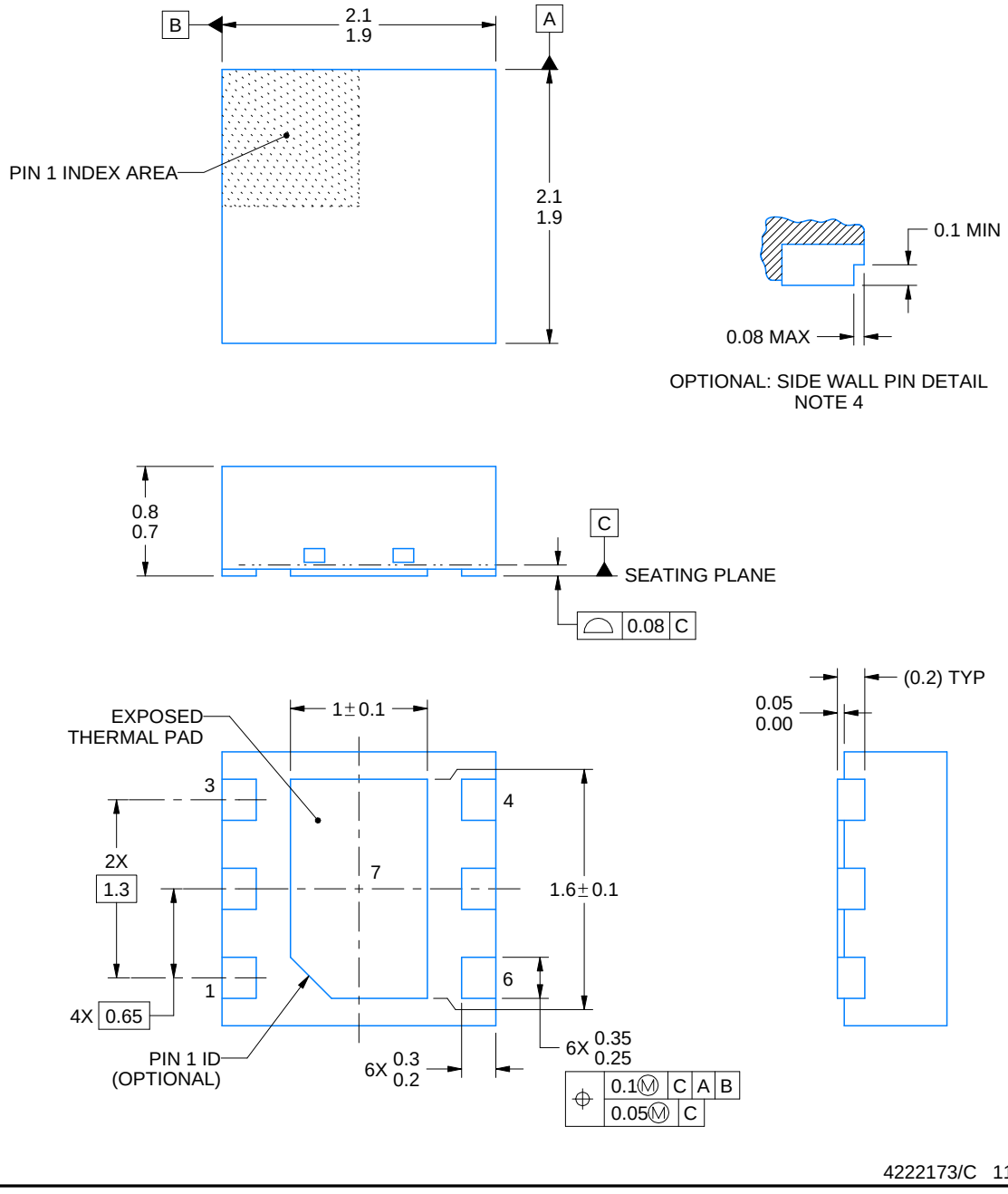
DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



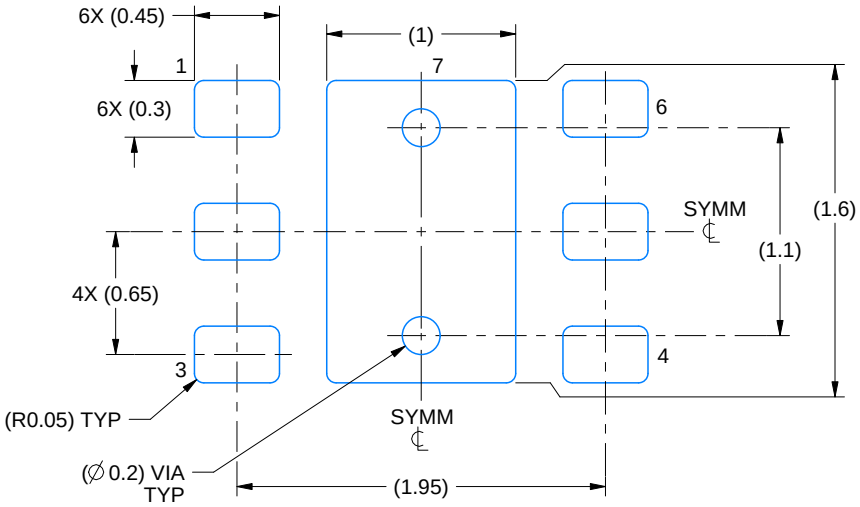
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PLASTIC SMALL OUTLINE - NO LEAD

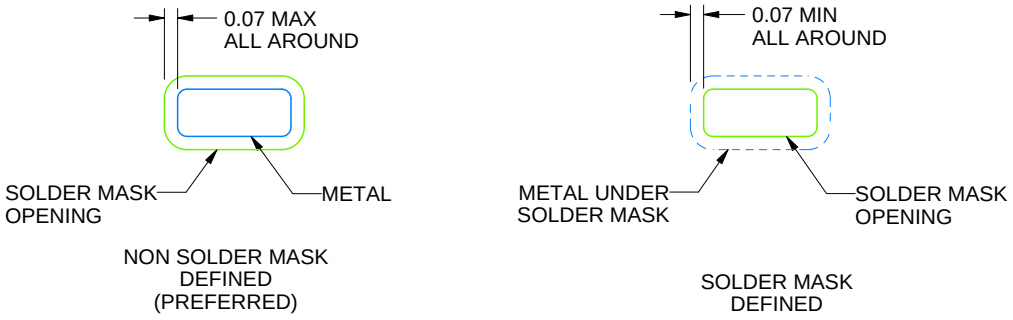


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Minimum 0.1 mm solder wetting on pin side wall. Available for wettable flank version only.



LAND PATTERN EXAMPLE
SCALE:25X

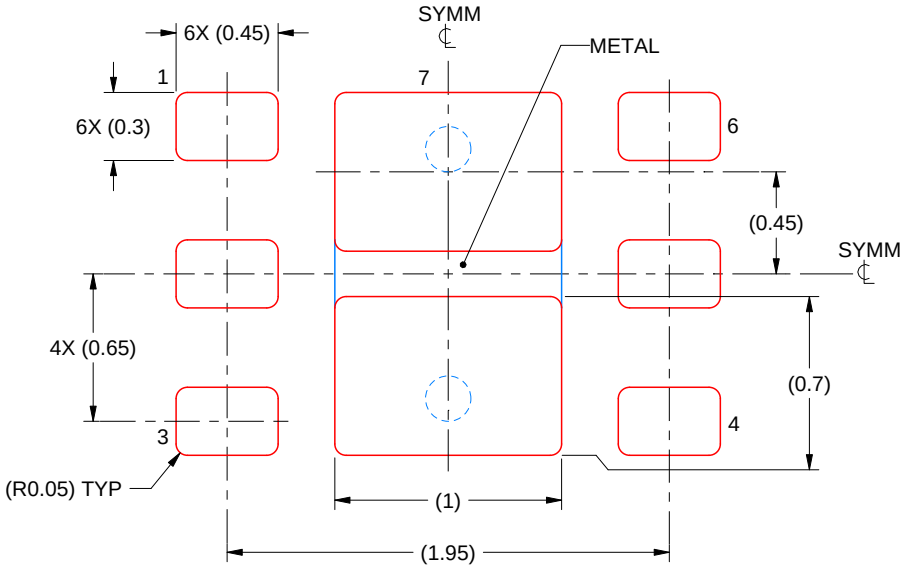


SOLDER MASK DETAILS

4222173/C 11/2025

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

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NOTES: (continued)

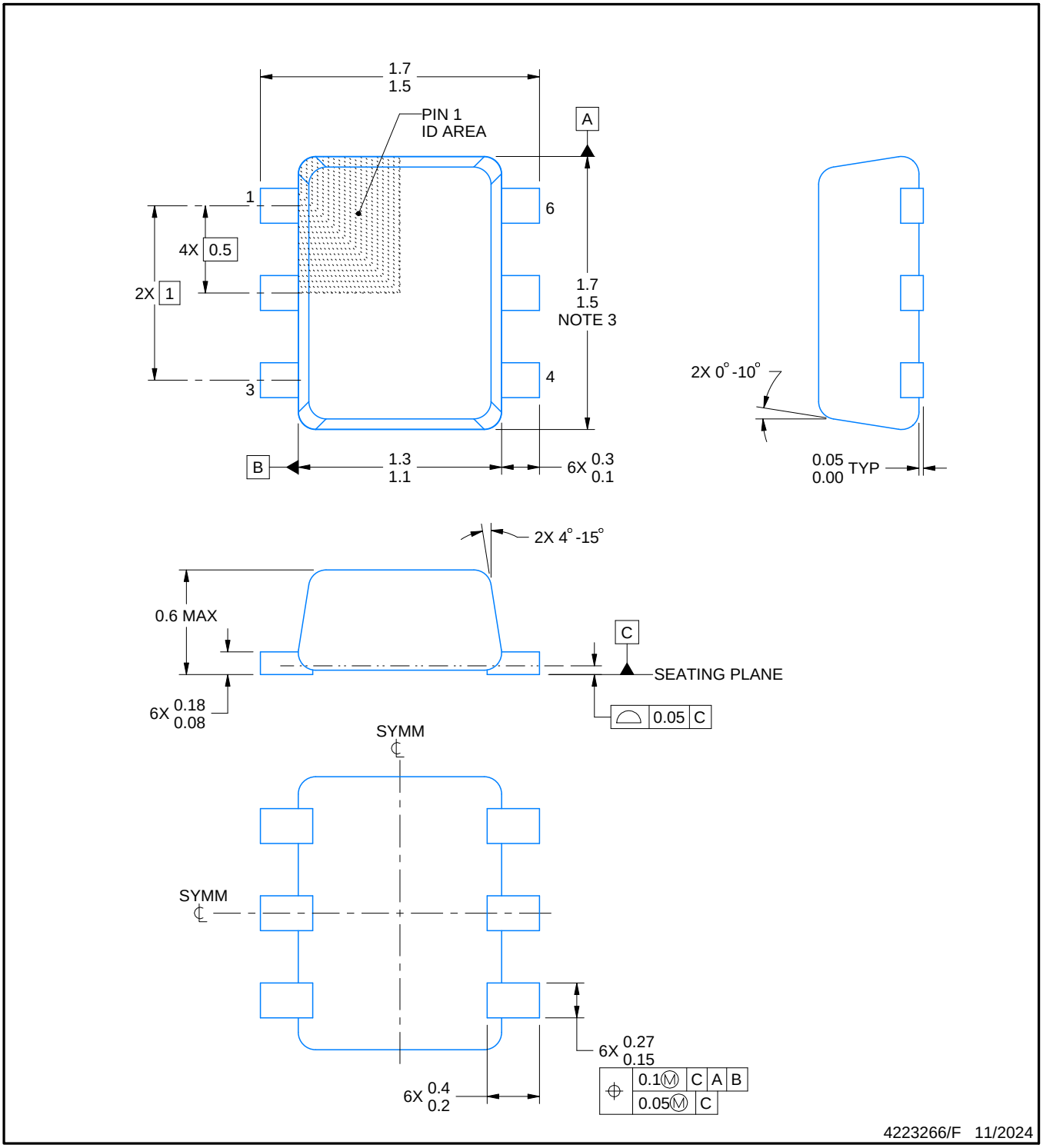
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



NOTES:

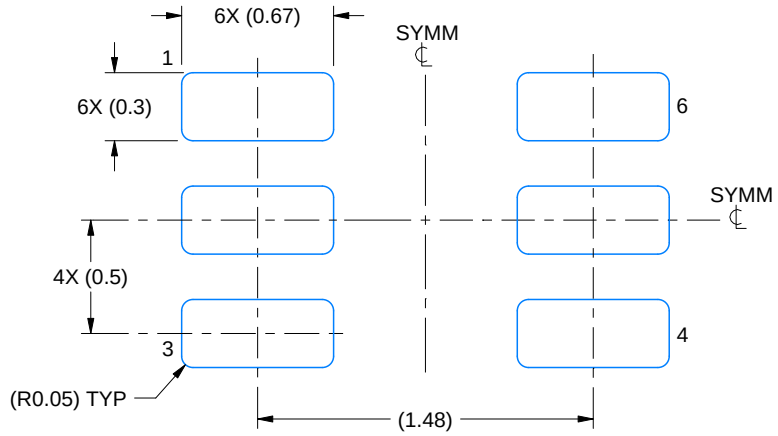
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD

EXAMPLE BOARD LAYOUT

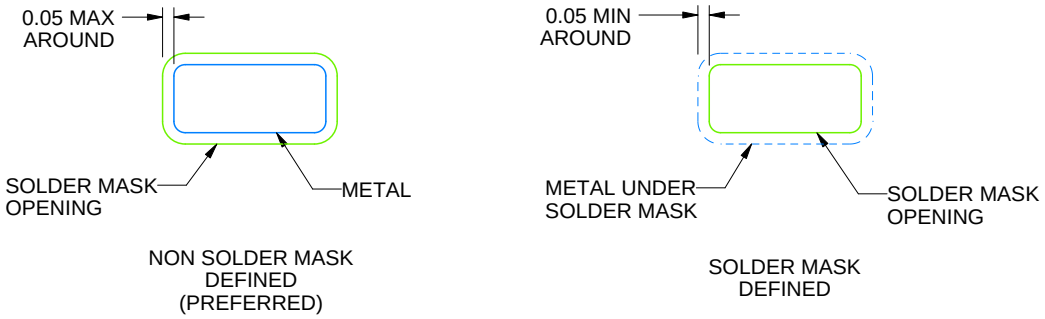
DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

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NOTES: (continued)

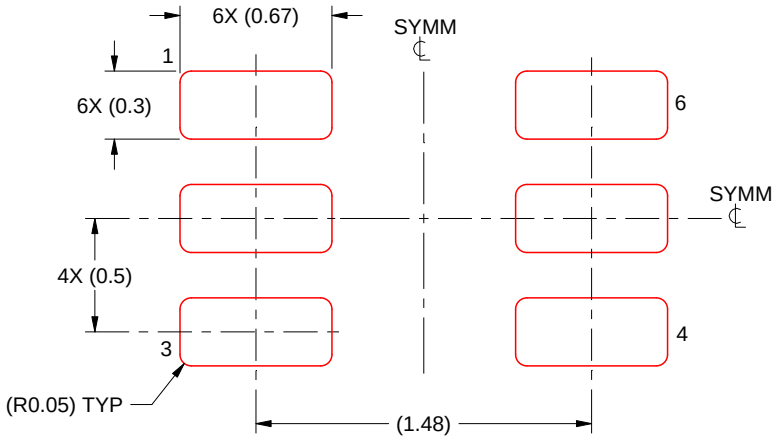
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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