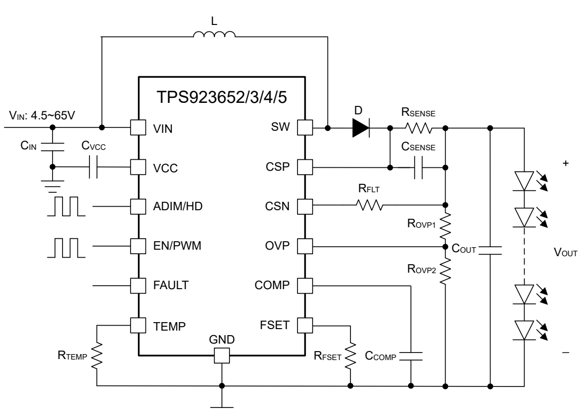
TPS92365x 65V 2A / 4A Boost / Buck-Boost LED Driver with Inductive Fast Dimming

1 Features

- 4.5V to 65V wide input range
- LED common cathode connection
- Integrated 150mΩ MOSFET with typical 3A / 6.5A / 8.5A current limit
- Optional switching frequency: 100kHz to 2.2MHz
- Spread spectrum for TPS923653 and TPS923655
- Advanced dimming options:
  – Analog dimming (256:1)
  – Fast PWM dimming (150ns pulse width)
  – Hybrid and flexible dimming (2,000:1 at 20kHz PWM, 10,000:1 at 4kHz PWM, 1,000,000:1 at 120Hz PWM)
- CC/CV charging mode
- Full protection features:
  – LED open and short protection
  – Switching FET open and short protection
  – External component failure protection
  – Cycle-by-cycle current limit
  – Thermal shutdown
  – Fault output (open drain)
- Configurable thermal foldback curve
- VSON, WSON and SOT23 package options

2 Applications

- Constant illumination:
  – Indoor, outdoor, professional lighting
  – Medical, surgical lighting
  – Projector, laser TV, printer, IP camera
- Instant illumination:
  – Machine vision, camera flash
  – Fire alarm, strobe
- CC and CV source:
  – LCD backlighting
  – Battery charging
  – TEC control



Simplified Schematic

3 Description

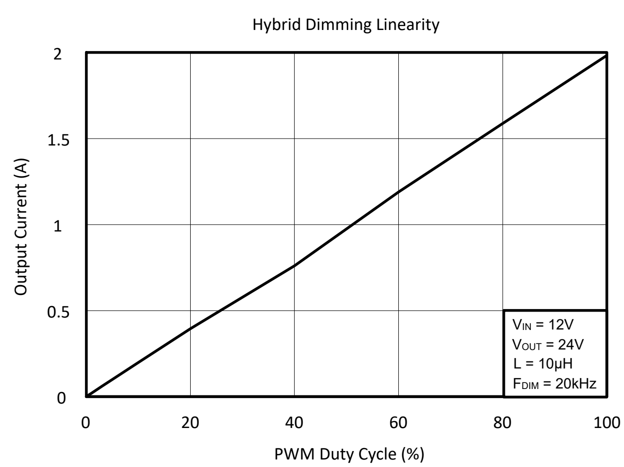
The TPS92365x family is a 2A / 4A non-synchronous Boost / Buck-Boost LED driver with 4.5V to 65V wide input range. By integrating the low-side NMOS switch, the device is capable of driving LEDs as well as charging batteries with high power density and high efficiency. The family also supports common cathode connection and single layer PCB design. The switching frequency is configurable from 100kHz to 2.2MHz with optional spread spectrum feature for better EMI performance.

The TPS92365x family supports four dimming options, including analog, PWM, hybrid and flexible dimming. Each dimming method can be configured through the PWM and ADIM input pins by means of simple high and low signals. The family adopts an adaptive off-time current mode control along with smart and accurate sampling to enable inductive fast dimming (IFD) and achieve high dimming accuracy.

The TPS92365x family also provides multiple systematic protections, including LED open and short, sense resistor open and short, configurable thermal foldback and thermal shutdown. A Fault output sends out acknowledge signals as soon as any fault condition is detected.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS92365x	VSON (14)	4.5mm x 3.0mm
	WSON (12)	3.0mm x 3.0mm
TPS923652, TPS923653	SOT-23-THN (14)	4.2mm x 3.3mm



LED Brightness Linearity

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4 Device Comparison Table

Part Number	Package	Typical Current Limit	Spread Spectrum	Operation Junction Temperature
TPS923652DMTR	VSON (14)	3A	Disabled	-40°C to 125°C
TPS923652DRRR	WSON (12)	3A	Disabled	-40°C to 125°C
TPS923652DYYR	SOT-23-THN (14)	3A	Disabled	-40°C to 125°C
TPS923653DMTR	VSON (14)	3A	Enabled	-40°C to 125°C
TPS923653DRRR	WSON (12)	3A	Enabled	-40°C to 125°C
TPS923653DYYR	SOT-23-THN (14)	3A	Enabled	-40°C to 125°C
TPS923654DMTR	VSON (14)	6.5A	Disabled	-40°C to 125°C
TPS923654DRRR	WSON (12)	6.5A	Disabled	-40°C to 125°C
TPS923654MDMTR	VSON (14)	6.5A	Disabled	-55°C to 125°C
TPS923654HMDMTR	VSON (14)	8.5A	Disabled	-55°C to 125°C
TPS923655DMTR	VSON (14)	6.5A	Enabled	-40°C to 125°C
TPS923655DRRR	WSON (12)	6.5A	Enabled	-40°C to 125°C
TPS923655MDMTR	VSON (14)	6.5A	Enabled	-55°C to 125°C
TPS923655HMDMTR	VSON (14)	8.5A	Enabled	-55°C to 125°C

5 Pin Configuration and Functions

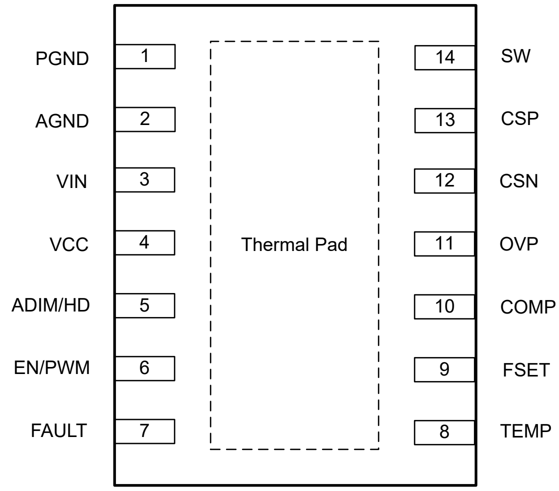


Figure 5-1. 14-Pin VSON Top View

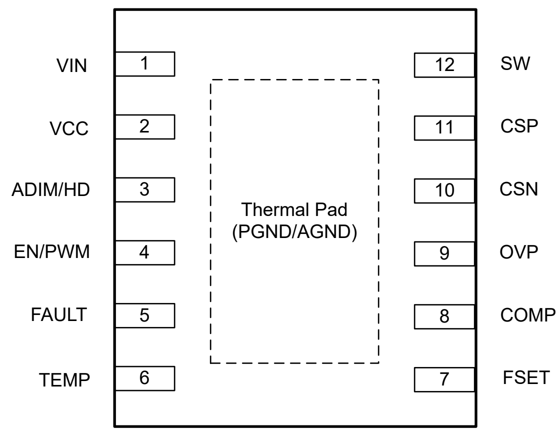


Figure 5-2. 12-Pin WSON Top View

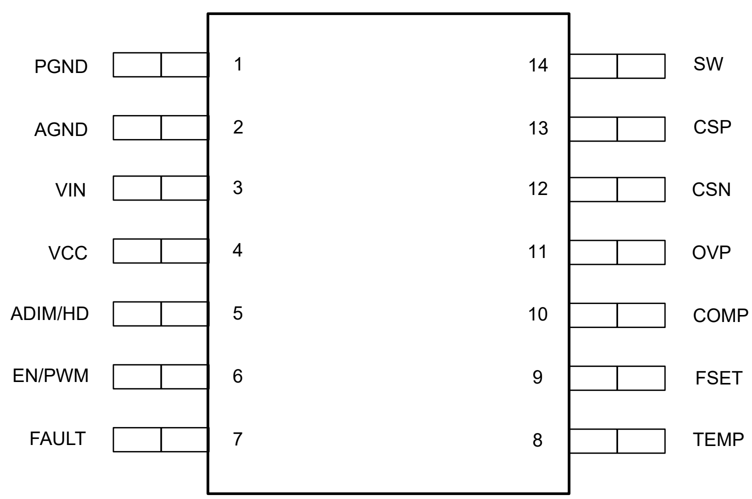


Figure 5-3. 14-Pin SOT-23-THIN Top View

Table 5-1. Pin Functions

PIN				TYPE[(1)]	DESCRIPTION
NAME	SOT23-14	VSON-14	WSON-12		
PGND	1	1	Thermal Pad	G	Power ground pin.
AGND	2	2	Thermal Pad	G	Analog ground pin.
VIN	3	3	1	P	Input power pin.
VCC	4	4	2	P	Internal LDO output pin. Connect with a 10V, 1μF capacitor to AGND. Different capacitor values determine different softstart times.
ADIM/HD	5	5	3	I	Analog dimming or hybrid dimming pin. Pull high for PWM dimming only, pull low for hybrid dimming, input PWM signal for analog dimming.
EN/PWM	6	6	4	I	Enable pin or PWM dimming pin. Pull high for always on, pull low for disabling the device, input PWM signal for PWM dimming.
FAULT	7	7	5	O	Open drain output pin. Internally pull low when fault is detected. Connect to AGND if fault pin is not used.
TEMP	8	8	6	I/O	Thermal foldback pin. Put different resistor values to AGND to set different thermal foldback behavior curves. Connect to AGND directly to disable thermal foldback.
FSET	9	9	7	I/O	Switching frequency set pin, with range of 100kHz to 2.2MHz. Add different resistor values to AGND for different switching frequencies. Do not leave the pin floating.
COMP	10	10	8	I/O	Error-amplifier output pin. Connect capacitors to AGND. Different capacitor values determine different bandwidths.
OVP	11	11	9	I	Overvoltage detection pin. Add different resistor dividers to set the LED open detection thresholds.
CSN	12	12	10	I	LED current sense positive pin.
CSP	13	13	11	I	LED current sense negative pin.
SW	14	14	12	P	Switching node pin. Internally connected to the low-side MOSFET. Connect with the power inductor and the Schottky diode.
Thermal Pad	N/A	Y	Y	G	Power/analog ground pin for WSON-12 package.

(1) I = Input, O = Output, P = Supply, G = Ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Voltage on pins	VIN, OVP, CSP, CSN, SW	–0.3	65	V
Voltage on pins	VCC, ADIM/HD, EN/PWM, FAULT, TEMP, FSET, COMP	–0.3	5.5	V
Operation junction temperature	T_J	–40	125	°C
Operation junction temperature (TPS923654MDMTR, TPS923654HMDMTR, TPS923655MDMTR, TPS923655HMDMTR)	T_J	–55	125	°C
Storage temperature	T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Theseare stress ratings only, which do not imply functional operation of the device at these or anyother conditions beyond those indicated under *Recommended OperatingConditions*. Exposure to absolute-maximum-rated conditions for extended periods mayaffect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage range	VIN	4.5	63	V
Input voltage range	OVP, CSP, CSN	0	63	V
Input voltage range	VCC, ADIM/HD, EN/PWM, TEMP, FSET	0	5	V
Output voltage range	SW	0	63	V
	FAULT, COMP	0	5	V
Operation junction temperature	T_J	–40	125	°C
Operation junction temperature (TPS923654MDMTR, TPS923654HMDMTR, TPS923655MDMTR, TPS923655HMDMTR)	T_J	–55	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		TPS92365x	TPS92365x	TPS92365x	UNIT
		SOT	WSON	VSON	
		14 PINS	12 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	96.0	47.4	39.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	33.5	44.2	39.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33.1	19.7	14.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.7	1.0	0.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	32.9	19.7	14.7	°C/W

(1) For more information about traditional and new thermalmetrics, see the *Semiconductor and IC Package Thermal Metrics*application report, SPRA953.

6.5 Electrical Characteristics

The electrical ratings specified in this section apply to all specifications in this document, unless otherwise noted. These specifications are interpreted as conditions that do not degrade the device parametric or functional specifications for the life of the product. T_J = –40°C to +125°C, V_{IN} = 4.5V to 60V, (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{VIN_UVLO}	V_{IN} undervoltage lockout	Rising V_{IN}	3.0	3.2	3.4	V
		Falling V_{IN}	2.8	3.0	3.2	V
	Hysteresis			0.2		V
I_{SD}	Shut down current from V_{IN}	V_{IN} = 12V, $V_{EN/PWM}$ = 0V, device disabled		0.8	2.3	µA
I_{OFF}	PWM off quiesent current from V_{IN}	V_{IN} = 12V, $V_{EN/PWM}$ = 0V, device enabled		2.5		mA
I_{OP}	Normal operating current	400kHz switching frequency		4.6		mA
I_{OP}	Normal operating current	2.2MHz switching frequency		10.0		mA
V_{VCC}	Internal LDO output voltage	I_{VCC} = 10mA	5.0	5.15	5.3	V
I_{VCC_LIM}	Internal LDO output current limit		38	47	56	mA
DIMMING						
V_{PWM_L}	Low-level input voltage				0.4	V
V_{PWM_H}	High-level input voltage		1.2			V
V_{ADIM_L}	Low-level input voltage				0.4	V
V_{ADIM_H}	High-level input voltage		1.2			V
$t_{PWM\_OUT\_ON}$	PWM output minimum on time				150	ns
$t_{PWM\_IN\_ON}$	PWM input minimum on time				150	ns
$t_{PWM\_IN\_OFF}$	PWM input minimum off time to disable device		57		77	ms
f_{ADIM}	Analog Dimming input frequency	6-bit ADIM resolution	0.1		156	kHz
f_{ADIM}	Analog Dimming input frequency	8-bit ADIM resolution	0.1		39	kHz
FAULT						
V_{OL}	Output level low	I = 3mA			0.1	V
$I_{LEAKAGE}$	Output leakage current	V = 5V			1	µA
FEEDBACK AND ERROR AMPLIFIER						
$g_{M(ea)}$	Transconductance gain	ADIM 100% duty cycle, $V_{CSP-CSN}$ = 200mV, V_{COMP} = 1.5V	205	265	325	µA/V
I_{COMP}	Source/sink current	ADIM 100% duty cycle, $V_{CSP-CSN}$ = 200mV ± 200mV, V_{COMP} = 1.5V	±24	±40	±56	µA
$V_{CSP-CSN}$	Current sense threshold	ADIM 100% duty cycle	194	200	206	mV
$V_{CSP-CSN}$	Current sense threshold	ADIM 12.5% duty cycle, compared with 100% duty cycle	11.875	12.5	13.125	%
$V_{CSP-CSN}$	Current sense threshold	ADIM 1.17% duty cycle, compared with 100% duty cycle	0.82	1.17	1.52	%
POWER STAGE						
R_{DSON}	Switching FET on resistance	V_{IN} ≥ 5V		150		mΩ
t_{min_ON}	Switching FET minimum on time			100		ns
t_{min_OFF}	Switching FET minimum off time			100		ns
f_{SW}	Switching FET frequency		0.1		2.2	MHz
CURRENT LIMIT						
I_{LIM}	Switching FET cycle-by-cycle current limit (TPS923652, TPS923653)		2.6	3	3.6	A
I_{LIM}	Switching FET cycle-by-cycle current limit (TPS923654, TPS923655)		5.8	6.5	7.6	A
I_{LIM}	Switching FET cycle-by-cycle current limit (TPS923654HMDMTR, TPS923655HMDMTR)		7.1	8.5	9.6	A
THERMAL PROTECTION						
T_{th}	Thermal foldback starting temperature threshold	R_{TEMP} = 20kΩ		130		°C

The electrical ratings specified in this section apply to all specifications in this document, unless otherwise noted. These specifications are interpreted as conditions that do not degrade the device parametric or functional specifications for the life of the product. T_J = –40°C to +125°C, V_{IN} = 4.5V to 60V, (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{TSD}	Thermal shutdown temperature			165		°C
	Hysteresis			15		°C

6.6 Typical Characteristics

V_{IN} = 12V, I_{OUT} = 1A, LED count = 12, L = 10μH, F_{SW} = 400kHz, unless otherwise specified

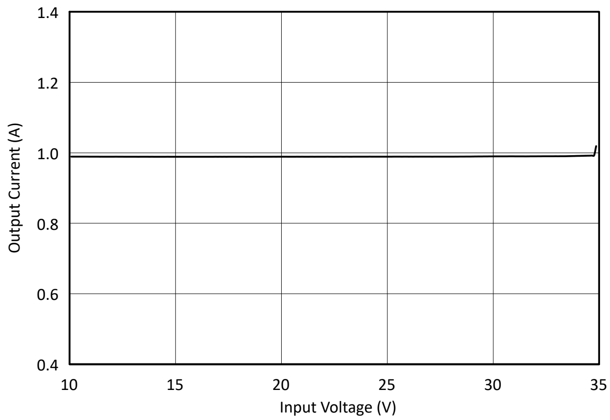


Figure 6-1. Output Current vs. Input Voltage

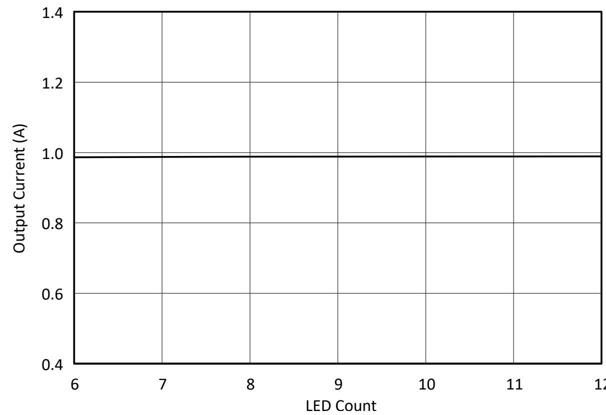


Figure 6-2. Output Current vs. LED Count

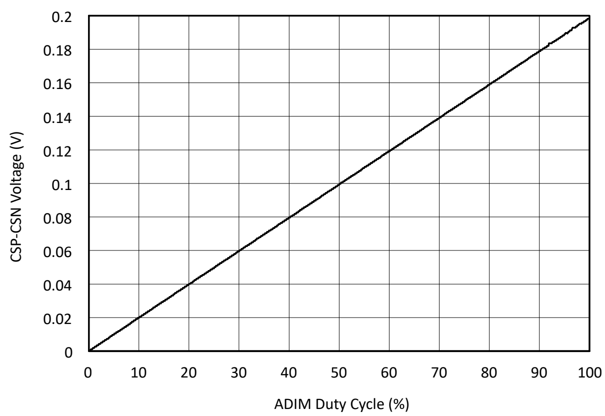


Figure 6-3. ADIM Duty Cycle vs. CSP-CSN Voltage in Analog Dimming

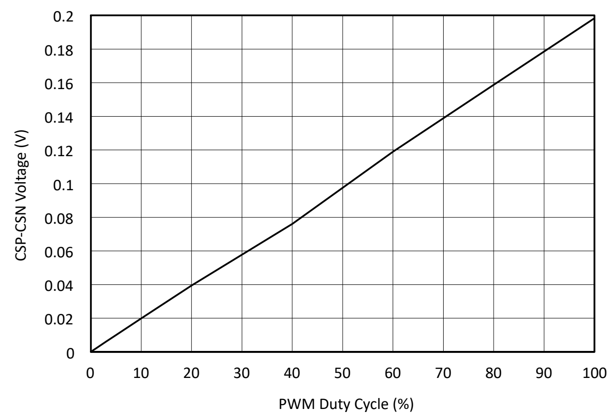


Figure 6-4. PWM Duty Cycle vs. CSP-CSN Voltage in 20kHz Hybrid Dimming

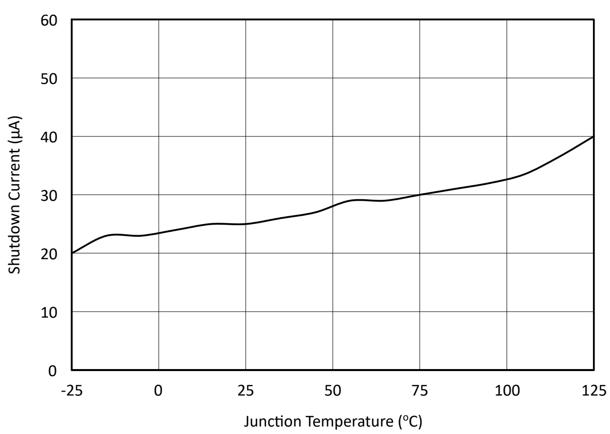


Figure 6-5. Shutdown Current vs. Junction Temperature

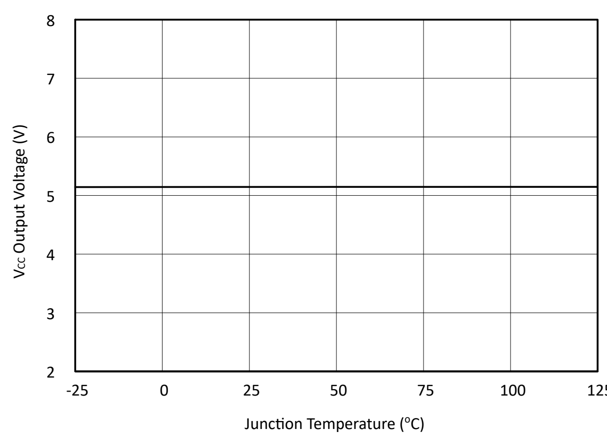


Figure 6-6. Internal LDO Output vs. Junction Temperature

6.6 Typical Characteristics (continued)

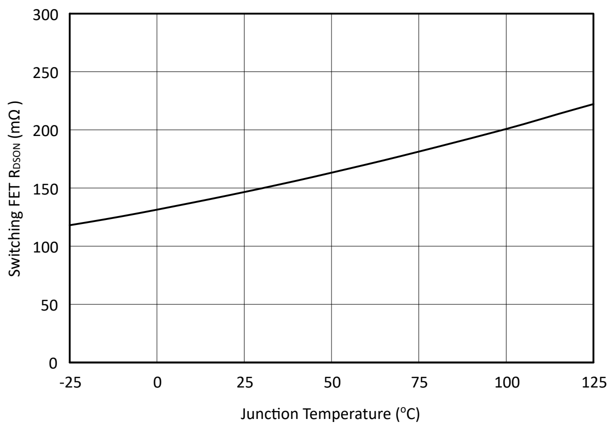


Figure 6-7. Switching FET R_{DSON} vs. Junction Temperature

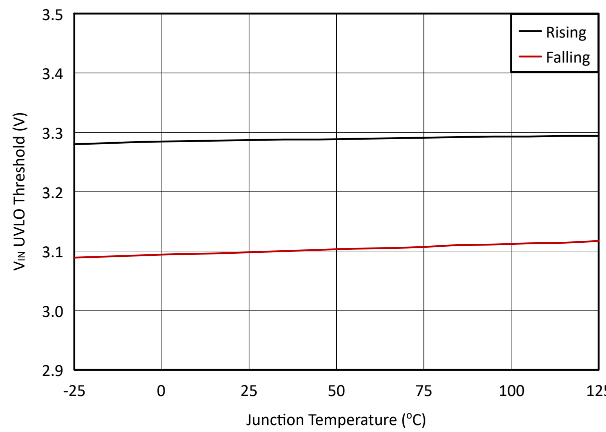


Figure 6-8. VIN UVLO Threshold vs. Junction Temperature

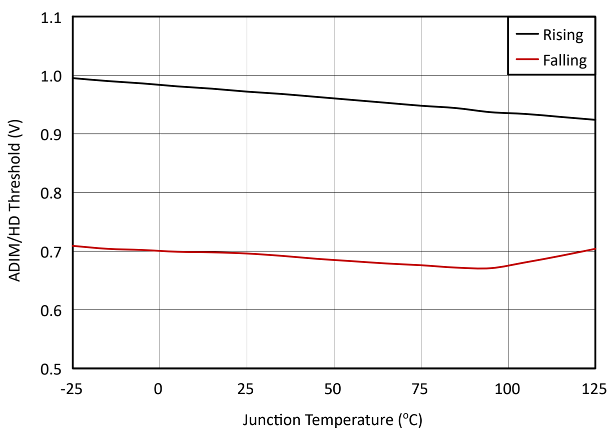


Figure 6-9. ADIM/HD Threshold vs. Junction Temperature

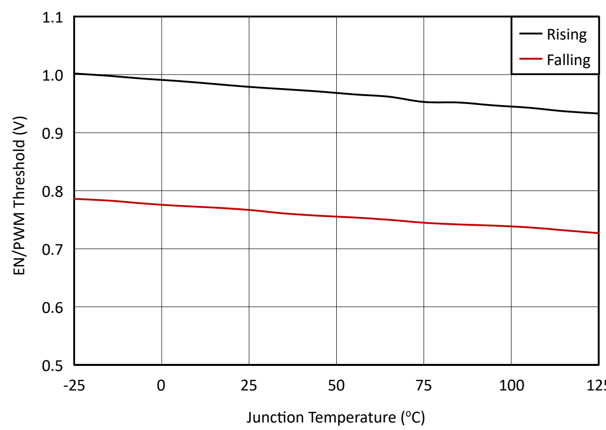


Figure 6-10. EN/PWM Threshold vs. Junction Temperature

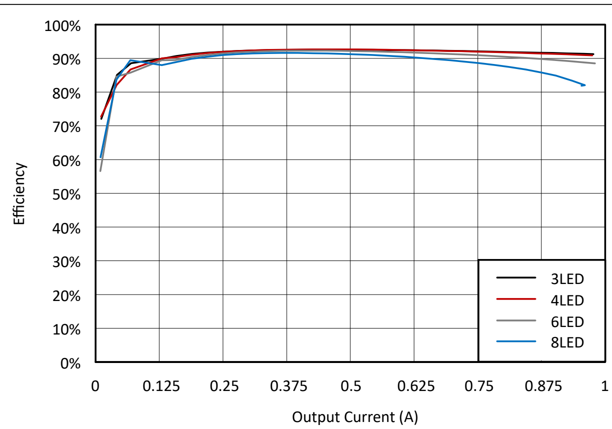


Figure 6-11. Efficiency at 7V Input Voltage, 1A Output Current

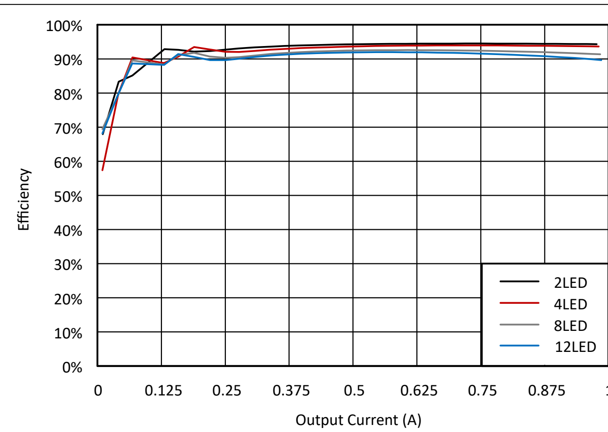


Figure 6-12. Efficiency at 13V Input Voltage, 1A Output Current

7 Detailed Description

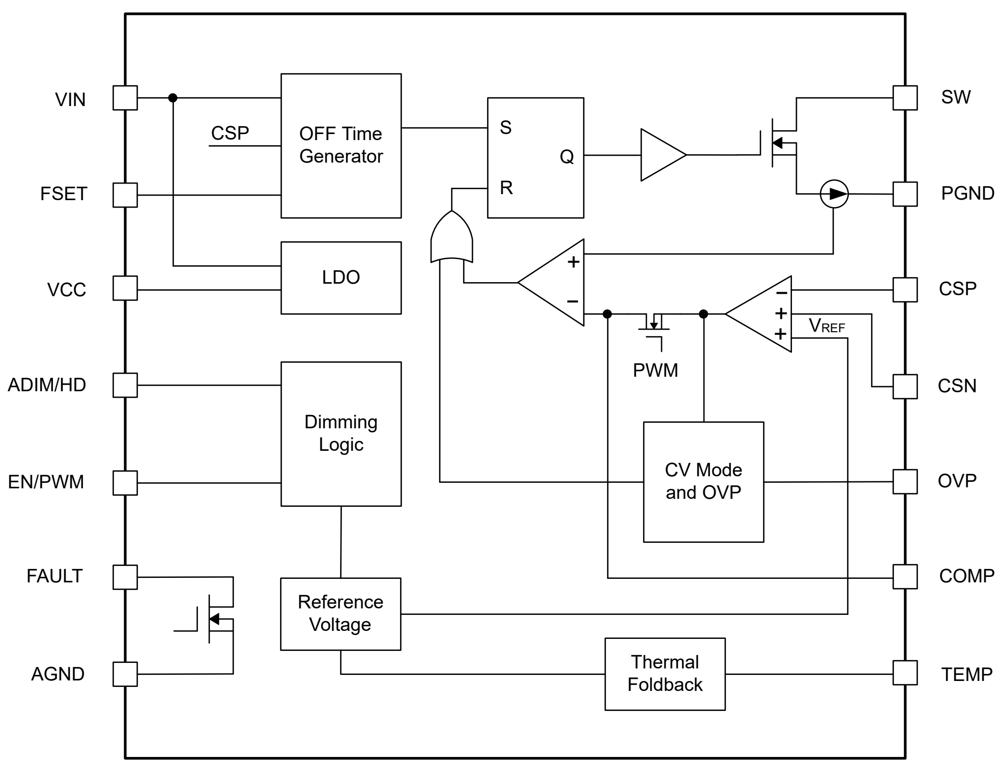
7.1 Overview

The TPS92365x family is a 2A / 4A non-synchronous Boost / Buck-Boost LED driver with 4.5V to 65V wide input range. By integrating the low-side NMOS switch with constant current and constant voltage controls, the device is capable of not only driving LEDs but also charging batteries with high power density and high efficiency. The device also supports common cathode connection and single layer PCB design, hence saving cost of connector, harness and PCB. The switching frequency is configurable through FSET pin, ranging from 100kHz to 2.2MHz, with optional spread spectrum feature to decrease the EMC emission and reduce the input filter size.

The device supports four dimming options, including analog dimming, PWM dimming, hybrid dimming and flexible dimming. Each dimming method can be configured through the PWM and ADIM input pins by means of simple high/low sequencing signals at startup. In PWM dimming mode, once the dimming mode is configured, LED is turned on and off corresponding to on and off of the PWM input signal at PWM input pin. The PWM dimming mode supports ultra-narrow pulse width down to 150ns. In analog dimming mode, LED current is regulated corresponding to the pulse width duty cycle of the PWM input signal at ADIM input pin. In hybrid dimming mode, the LED current is controlled by a predetermined combination of analog dimming and PWM dimming through the PWM input signal at PWM input pin. In flexible dimming mode, the LED current is controlled by analog dimming through the PWM input signal at ADIM input pins and PWM dimming through the PWM input signal at PWM input pins, respectively. The device adopts an adaptive off-time current mode control along with smart and accurate sampling to enable Inductive Fast Dimming (IFD) and achieve high dimming accuracy. The compensation bandwidth can be adjusted through an external capacitor based on system requirement.

For safety and protection, the devices support full systematic protections including LED open and short, sense resistor open and short, configurable thermal foldback and thermal shutdown protection. The fault output pin sends out acknowledge signals as soon as any fault condition is detected.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Adaptive Off-Time Current Mode Control

The TPS92365x device adopts an adaptive off-time current mode control to support fast transient response over a wide range of operation. The switching frequency is configurable through FSET pin, ranging from 100kHz to 2.2MHz.

For average output current regulation, the sensed voltage across the sensing resistor between the CSP and CSN pins is compared with the internal voltage reference, V_{REF} , through the error amplifier. The output of the error amplifier, V_{COMP}, passes through an external compensation network and is then compared with the peak current feedback at the PWM comparator. During each switching cycle, when the internal NMOS FET is turned on, the peak currernt is sensed through the internal FET. When the sensed value of peak current reaches V_{COMP} at the input of PWM comparator, the NMOS FET is turned off and the adaptive off-time counter starts counting. Once the adaptive off-time counter stops counting, the counter is reset until when the NMOS FET stays off. The counting off time is determined by the external resistor connected to the FSET pin and the input/output feedforward. Thus, the device is able to maintain a nearly constant switching frequency at steady state and regulate the output average current at a desired value.

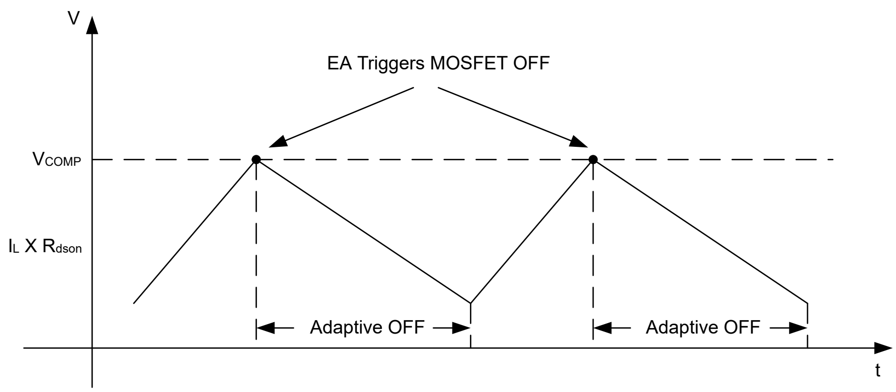


Figure 7-1. Adaptive off-time current mode control method

7.3.1.1 Switching Frequency Settings

The switching frequency of TPS92365x device is adjustable from 100kHz to 2.2MHz by means of changing R_{FSET} connected between FSET pin and AGND.

The resistor value and the corresponding switching frequency are listed in the below table:

Table 7-1. Switching Frequency vs. R_{FSET} Resistor Value

Switching Frequency	Resistor Value (kΩ)
100kHz	232
200kHz	138
300kHz	83
400kHz	59
600kHz	38
800kHz	28
1MHz	23
1.2MHz	18
1.5MHz	13
1.8MHz	11
2.2MHz	9

For example, if R_{FSET} is set to 59kΩ, the corresponding switching frequency is set to 400kHz.

In most cases, the lower switching frequency, the higher system efficiency and the better thermal behavior.

7.3.1.2 Spread Spectrum

The TPS923653 and TPS923655 devices enable the spread spectrum feature (±7% from central frequency, 2kHz modulation frequency) which reduces EMI noise at the switching frequency and its high-order harmonics.

On the other hand, the TPS923652 and TPS923654 devices disable the spread spectrum feature toward better brightness performance in low brightness scenario.

7.3.2 Setting LED Current

The LED current is set by the external sensing resistor between CSP and CSN pins. The internal voltage reference, V_{REF}, is fixed at 200 mV for full-scale LED current, I_{LED_FS}, and the sensing resistor can be calculated using Equation 1.

$$R_{SENSE} = \frac{V_{REF}}{I_{LED\_FS}} \tag{1}$$

where

- V_{REF} = 200 mV

7.3.3 Undervoltage Lockout

The TPS92365x family implements an internal undervoltage lockout (UVLO) circuitry connecting to the VCC pin. The UVLO is triggered and then the device is disabled when the VCC pin voltage falls below the internal UVLO threshold voltage, V_{VIN_UVLO} typically 3.0V, with a typical 0.2V hysteresis. The VCC pin is the output of an internal regulator of which the input is supplied by the VIN pin. Therefore, if VIN pin voltage falls close to above the V_{VIN_UVLO} (around 500mV above), the UVLO will be triggered.

7.3.4 Internal Soft Start

The TPS92365x family implements the internal soft-start function. Once V_{IN} rises above V_{VIN_MIN}, the internal LDO starts to charge V_{CC} capacitor. It takes approximately 800 µs for V_{CC} to rise above V_{VIN_UVLO} if a 1-µF capacitor is connected to V_{CC} pin. If EN/PWM pin is pulled high before V_{CC} rises above V_{VIN_UVLO}, the POR is enabled right after V_{CC} above V_{VIN_UVLO} and waits for 100 µs to start dimming mode. EN/PWM pin has to stay high for more than 5 µs after V_{CC} rises above V_{VIN_UVLO}. In this case, if using 1-µF V_{CC} capacitor, it is recommended to wait for 1 ms to start dimming mode after V_{IN} rises above V_{VIN_MIN}.

If EN/PWM pin has the first PWM pulse appearing after V_{CC} rises above V_{VIN_UVLO}, the device waits for 200 µs to enable POR and another 100 µs to start dimming mode. Hence, without triggering V_{IN} UVLO, the device can be renabled after disabled and waits for 300 µs to start dimming mode. Note that the initial enable PWM pulse lasting more than 5 µs is required at EN/PWM input pin to enable the device. After dimming mode is started, the device enters four different dimming modes based on the configuration of ADIM/HD pin and EN/PWM pin.

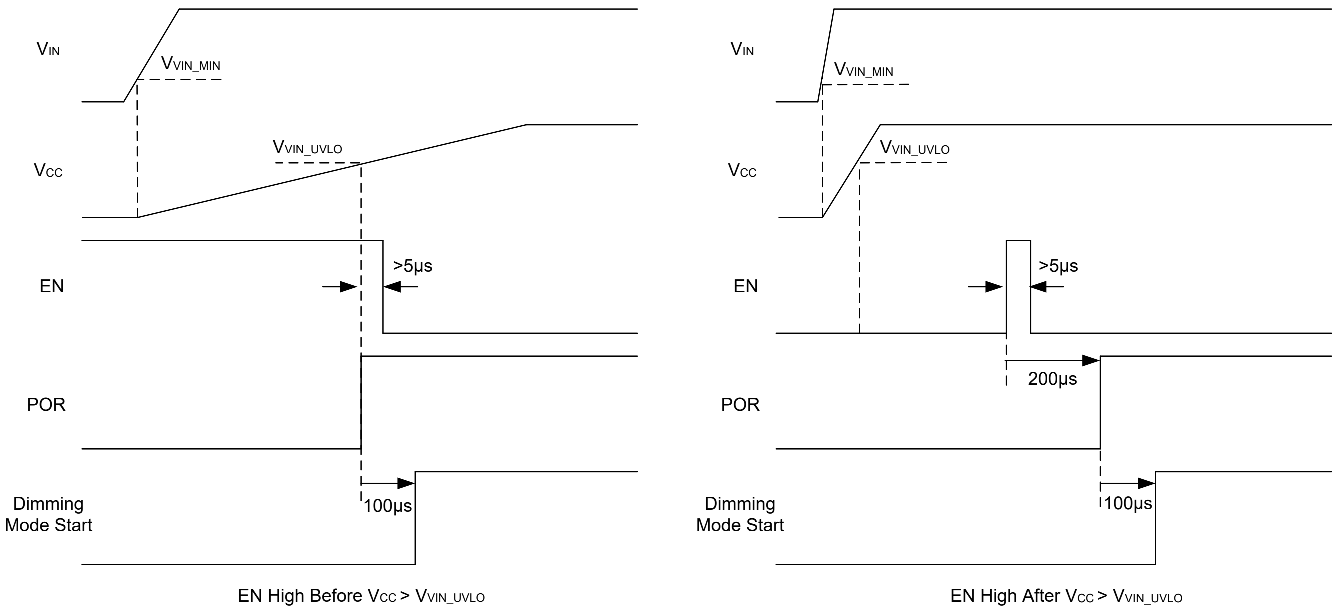


Figure 7-2. Startup Sequence

7.3.5 Dimming Mode

The TPS92365x family has four optional dimming modes:

- PWM dimming
- Analog dimming
- Hybrid dimming
- Flexible dimming

The dimming mode is started at 1ms after V_{IN} exits UVLO or 300µs after re-enable by EN/PWM pin. The configuration to one of the four dimming modes are shown as below:

Table 7-2. Dimming Mode Configuration

Dimming Mode	EN/PWM Pin	ADIM/HD Pin
PWM Dimming	PWM signal	High
Analog Dimming	High	PWM signal
Hybrid Dimming	PWM signal	Low
Flexible Dimming	PWM signal	PWM signal

7.3.5.1 PWM Dimming

The TPS92365x family supports PWM input signals with ultra-narrow pulse width down to 150 ns for direct PWM dimming. The PWM dimming mode is enabled when the ADIM/HD input pin is always high and the EN/PWM input pin is configured by a PWM input signal.

In PWM dimming mode, when the PWM input signal at the PWM pin turns from low to high, the internal NMOS FET starts switching and the inductor current rises to the determined value. The LED current is then regulated at the determined value as long as the PWM input signal stays high. When the PWM input signal turns from high to low, the internal FET is turned off causing the inductor current falling to zero. The internal FET maintains off and the LED current stays zero as long as the PWM input signal stays low.

7.3.5.2 Analog Dimming

The TPS92365x family supports analog dimming which regulates the LED current through the PWM input signal at the ADIM/HD pin. The analog dimming mode is enabled when the EN/PWM pin is always high and the ADIM/HD pin is configured by a PWM input signal.

The internal voltage reference, V_{REF}, starts to rise after the first PWM pulse appears at the ADIM/HD pin. A 1-µs minimum on-time of the first PWM pulse is required for the internal digital circuits to enter the analog dimming mode. The PWM duty cycle is detected until the end of the second PWM cycle and then V_{REF} changes to the desired value in proportion to the duty cycle of the PWM pulse. The minimum on-time of the PWM pulse other than the first is 100 ns for the digital circuits to detect the duty cycle.

V_{REF} is 180 mV when the PWM input signal at the ADIM/HD pin has a 90% duty cycle, for instance, and V_{REF} is 20 mV when the PWM input signal has a 10% duty cycle. It takes approximately 15 ms to detect 100% PWM duty cycle when ADIM/HD pin is always pulled low or detect 0% PWM duty cycle when ADIM/HD pin is always pulled high. The initial change takes approximately 5 ms if V_{REF} is 200 mV. The analog dimming enables 8-bit resolution which corresponds to 0.4% duty cycle step change at the ADIM/HD pin. Also, the circuit is able to respond to the duty cycle change of the PWM input signal with tens of micro-seconds delay.

7.3.5.3 Hybrid Dimming

The TPS92365x family supports a unique hybid dimming function to maximize the dimming performance, especially when both high dimming frequency and high dimming ratio are needed. The hybrid dimming mode is enabled when the ADIM/HD pin is always low and the EN/PWM pin is configured by a PWM input signal. A first falling edge at EN/PWM pin is necessary to enter hybrid dimming mode and then the EN/PWM pin can be always high for 100% duty cycle. The device exits hybrid dimming mode once a rising edge appears at ADIM/HD pin. Once the device exits hybrid dimming mode, the device can only work either in PWM, analog or flexible dimming mode until the device is disabled and renabled.

In the hybrid dimming mode, the LED current is regulated by the analog dimming at high brightness level (12.5% to 100%) and by the PWM dimming at low brightness level (0% to 12.5%), respectively. At high brightness level, the internal voltage reference, V_{REF}, changes in proportion to the duty cycle of the PWM input signal at the EN/PWM pin with 8-bit resolution. At low brightness level, V_{REF} stays unchanged and an internal PWM generator is enabled. Thus, the LED is turned on and off corresponding to the on and off of the internal PWM signal of which the frequency and the duty cycle are configured by the PWM input signal at the EN/PWM pin. In addition, the internal PWM signal has a 0.4% hystersis response when the PWM input duty cycle changes between increasing and decreasing. The detailed hybrid dimming behavior is illustrated in the below figure.

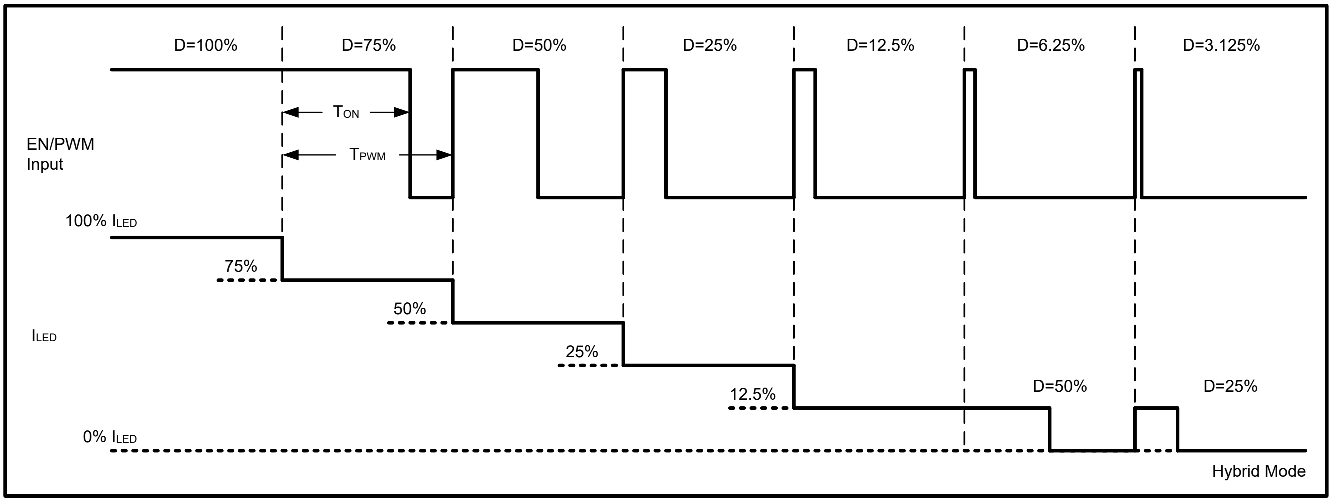


Figure 7-3. Hybrid Dimming

7.3.5.4 Flexible Dimming

The TPS92365x family also supports flexible dimming to maximize the dimming ratio and the flexibility of dimming control, in which the LED current value and the on/off behavior can be controlled independently. The flexible dimming mode is enabled when both the ADIM/HD pin and the EN/PWM pin are configured by PWM input signals at the same time. Therefore, in fleixble dimming mode, the LED is turned on and off corresponding to the on and off of the PWM input signal at the EN/PWM pin while the reference voltage changes in proportion to the duty cycle of the PWM input signal at the ADIM/HD pin. All the initial conditions and resolutions of PWM dimming and analog dimming apply to the flexible dimming.

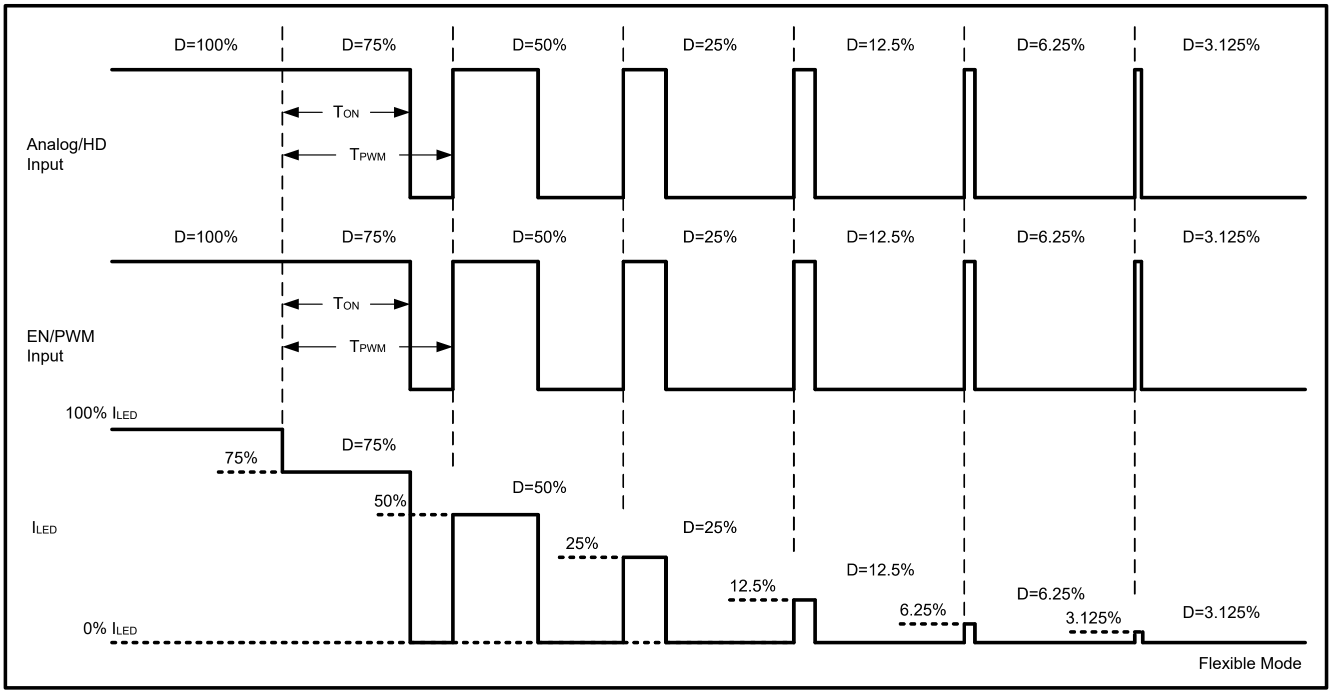


Figure 7-4. Flexible Dimming

7.3.6 CC/CV Charging Mode

The TPS92365x family enables constant current (CC) / constant voltage (CV) charging operation by configuring OVP pin. For CC charging operation, the device generates a controllable output current controlled by a PWM signal at ADIM/HD pin. If a low-current pre-charge is required, the device can generate a relatively low output current controlled by a low-duty-cycle PWM signal at ADIM/HD pin. CV charging operation is enabled and the output current continuously decreases after V_{OVP} rises above 1.15V. The device stop switching completely after V_{OVP} rises above 1.4V. The device can return to CC charging operation once V_{OVP} falls below 1.15V.

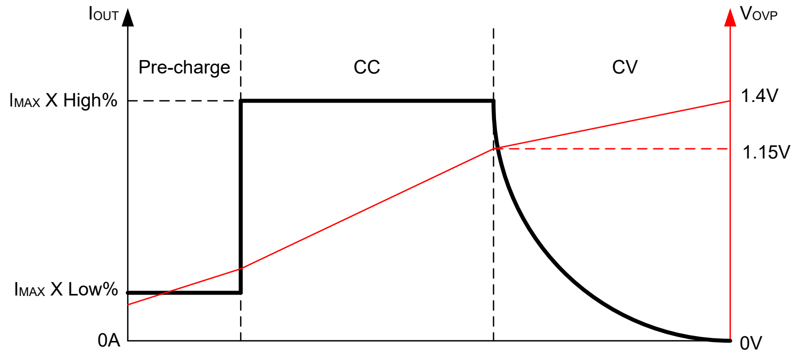


Figure 7-5. CC/CV Mode Transition

7.3.7 Fault Protection

The TPS92365x family is able to provide fault protections and send fault report signals in many fault conditions, including LED open, LED ± short, LED short to PGND, sense resistor open and short, internal switching FET open and short, and thermal shutdown.

Table 7-3. Protections

TYPE	CRITERION	BEHAVIOR
LED open load	V_{OVP} > 1.4V	FAULT pin pull low. The device stops switching and recovers when V_{OVP} < 1.35V.
LED+ and LED- short circuit (Buck-Boost)	V_{CSN} - V_{IN} < 750mV	FAULT pin pull low. The device keeps switching with minimum on time.
LED+ short to PGND	V_{CSP} - V_{CSN} > 300mV	FAULT pin pull low. The device stops switching and recovers when V_{CSP} - V_{CSN} < 300mV
Sense-resistor open circuit	V_{CSP} - V_{CSN} > 300mV	FAULT pin pull low. The device stops switching and recovers when V_{CSP} - V_{CSN} < 300mV.
Sense-resistor short circuit	COMP pin is clamped high	FAULT pin pull low. The device keeps switching under the cycle-by-cycle current limit.
Switching FET open circuit	COMP pin is clamped high	FAULT pin pull low. The device stops switching and recovers when open circuit is removed.
Switching FET short circuit	COMP pin is clamped high	FAULT pin pull low. The device stops switching and recovers when short circuit is removed.
Thermal shutdown	T_J > T_{TSD}	FAULT pin pull low. The device stops switching and recovers when T_J falls below the hysteresis level.

7.3.8 Thermal Foldback

The TPS92365x family integrates thermal shutdown protection to prevent the device from overheating. In order to provide design margin of system thermal performance, the device enables a programmable thermal foldback function which automatically reduces the full-scale max output current, I_{MAX}, at high junction temperature. When the device along with the LEDs are mounted on the same thermal substrate, the thermal performance is effectively improved due to the reduction of dissipation need for both device and LED.

As the device junction temperature rises above the thermal foldback threshold temperature, T_{TH}, the full-scale max current starts to reduce following the current-temperature curve shown in the below figure. The current starts to reduce from the 100% level at typically rate of 2% of I_{MAX} per °C until it drops to 50% of the full scale. Once the junction temperature rises 25°C above the T_{TH}, the current continues to decrease at a lower rate until the temperature reaches above the over-temperature shutdown threshold temperature, T_{TSD}.

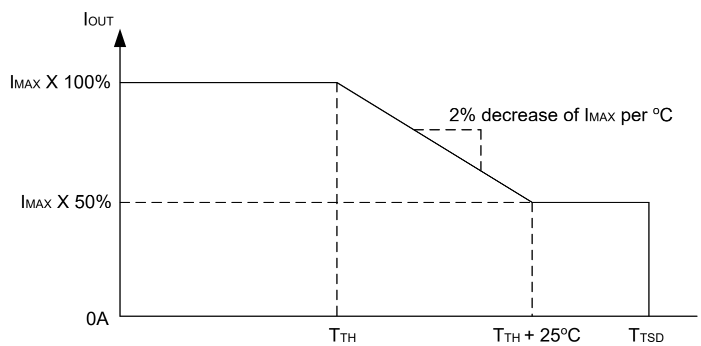


Figure 7-6. Thermal Foldback

The T_{TH} can be adjusted by changing the resistor R_{TEMP} connected between the TEMP and AGND pin. The T_{TH} and the corresponding R_{TEMP} value are listed in below table.

Table 7-4. T_{TH} vs. R_{TEMP} resistor value

T_{TH} (°C)	Resistor Value (kΩ)
80	200
90	100
100	60
110	40
120	28
130	20
140	15
150	10

8 Application and Implementation

8.1 Application Information

The TPS92365x family is typically used as a Boost / Buck-Boost converter to drive one or more LEDs from an input from 4.5V to 63V range.

8.2 Typical Application

8.2.1 TPS923654 Boost, 12V Input, 1A Output, 12-piece WLED Driver With Analog Dimming

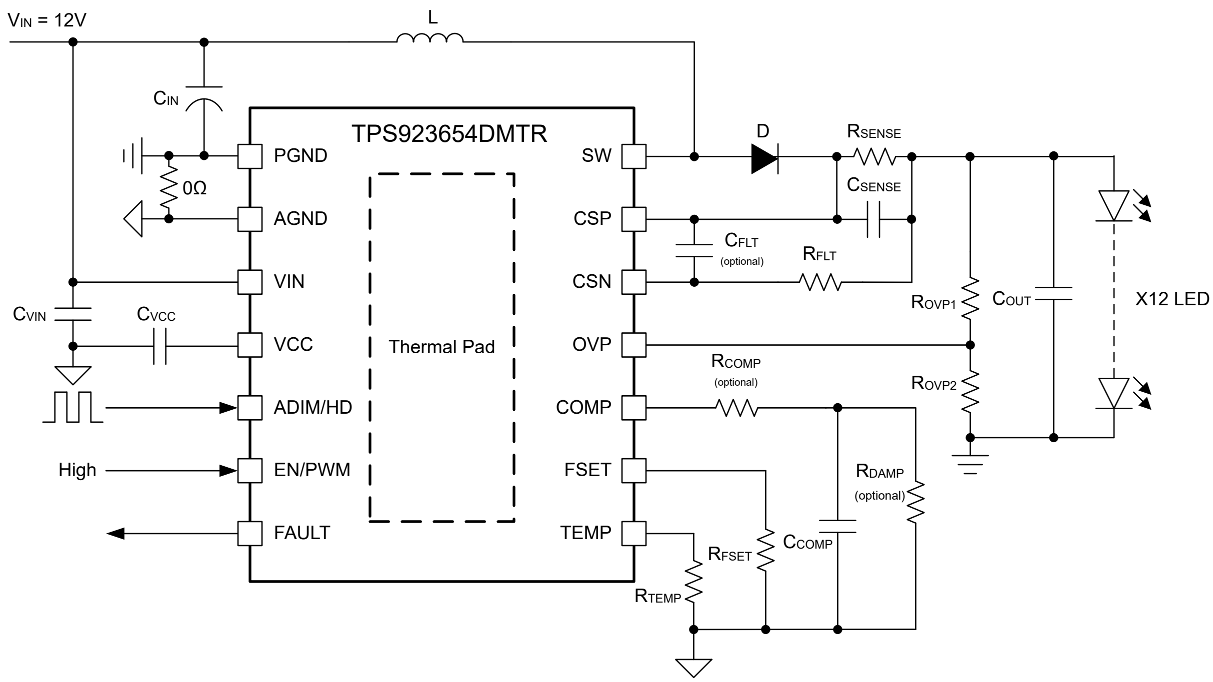


Figure 8-1. Boost, 12V Input, 1A Output, 12-piece WLED, Analog Dimming Reference Design

8.2.1.1 Design Requirements

For this design example, use the parameters in the following table.

Table 8-1. Design Parameters

PARAMETER	VALUE
Input voltage range	12V ±10%
LED forward voltage	3.0V
Output voltage	36V (3.0 × 12)
Maximum LED current	1A
Inductor current ripple	60% of maximum inductor current
LED current ripple	200mA or less
Input voltage ripple	500mV or less
Dimming type	Analog dimming with TPS923654: 1kHz, 1% to 100% PWM input at the ADIM pin

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Inductor Selection

For this design, the input voltage is a 12V, rail with 10% variation. The output is 12 white LEDs in series and the inductor current ripple by requirement is less than 60% of maximum inductor current. To choose a proper peak-to-peak inductor current ripple, the low-side FET current limit should not be violated when the converter works in full-load condition. This requires half of the peak-to-peak inductor current ripple to be lower than that limit. Another consideration is to ensure reasonable inductor core loss and copper loss caused by the peak-to-peak current ripple. Once this peak-to-peak inductor current ripple is chosen, use Equation 2 to calculate the recommended value of the output inductor L.

$$L = \frac{V_{IN(max)} \times \left(V_{OUT} - V_{IN(max)}\right)}{V_{OUT} \times K_{IND} \times I_{L(max)} \times f_{SW}} \quad (2)$$

where

- K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum LED current.
- $I_{L(max)}$ is the maximum inductor current.
- f_{SW} is the switching frequency.
- $V_{IN(max)}$ is the maximum input voltage.
- V_{OUT} is the sum of the voltage across LED load and the voltage across sense resistor.

With the chosen inductor value, the user can calculate the actual inductor current ripple using Equation 3.

$$I_{L(ripple)} = \frac{V_{IN(max)} \times \left(V_{OUT} - V_{IN(max)}\right)}{V_{OUT} \times L \times f_{SW}} \quad (3)$$

The ratings of inductor RMS current and saturation current must be greater than those seen in the system requirement. This is to ensure no inductor overheat or saturation occurring. During power up, transient conditions or fault conditions, the inductor current may exceed its normal operating current and reach the current limit. Therefore, it is preferred to select a saturation current rating equal to or greater than the converter current limit. The peak-inductor-current and RMS current equations are shown in Equation 4 and Equation 5.

$$I_{L(peak)} = I_{L(max)} + \frac{I_{L(ripple)}}{2} \quad (4)$$

$$I_{L(rms)} = \sqrt{I_{L(max)}^{\ 2} + \frac{I_{L(ripple)}^{\ 2}}{12}} \quad (5)$$

In this design, $V_{IN(max)}$ = 12V, V_{OUT} = 36V, I_{LED} = 1A, f_{SW} = 500kHz, choose K_{IND} = 0.6, the calculated inductance is 8.9µH. A 10µH inductor is chosen. With this inductor, the ripple, peak, and rms currents of the inductor are 1.6A, 3.8A, and 3.04A, respectively.

8.2.1.2.2 Input Capacitor Selection

An input capacitor is required to reduce the surge current drawn from the input supply and the switching noise coming from the device. Electrolytic capacitors are recommended for energy storage. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, it is recommended to place a 1µF ceramic capacitor along with a 0.1µF capacitor from VIN to PGND/AGND to provide high-frequency filtering. The input capacitor voltage rating must be greater than the maximum input voltage. Use Equation 6 to calculate the input ripple voltage, where ESR_{CIN} is the ESR of input capacitor, and K_{DR} is the derating coefficient of ceramic capacitance at the applied DC voltage.

$$V_{IN(ripple)} = \frac{I_{L(ripple)}}{8 \times C_{IN} \times f_{SW}} \quad (6)$$

In this design, a 33µF, 25V electrolytic capacitor, a 1µF, 25V X7R ceramic capacitor and a 0.1µF, 100V X7R ceramic capacitor are chosen, yielding around 400mV input ripple voltage.

8.2.1.2.3 Output Capacitor Selection

The output capacitor reduces the high-frequency current ripple through the LED string. Excessive current ripple increases the RMS current in the LED string, therefore increasing the LED temperature.

1. Calculate the total dynamic resistance of the LED string (R_{LED}) using the LED manufacturer's data sheet.

2. Calculate the required impedance of the output capacitor (Z_{OUT}) given the acceptable peak-to-peak ripple current through the LED string, $I_{LED(ripple)}$. $I_{L(ripple)}$ is the peak-to-peak inductor ripple current as calculated with the selected inductor.

3. Calculate the minimum effective output capacitance required.

4. Increase the output capacitance appropriately due to the derating effect of applied DC voltage.

See Equation 7, Equation 8, and Equation 9.

$$R_{LED} = \frac{\Delta V_F}{\Delta I_F} \times \#\ of\ LEDs \tag{7}$$

$$Z_{COUT} = \frac{R_{LED} \times I_{LED(ripple)}}{I_{L(max)} - I_{LED(ripple)}} \tag{8}$$

$$C_{COUT} = \frac{1}{2\pi \times f_{SW} \times Z_{COUT}} \tag{9}$$

Once the output capacitor is chosen, Equation 10 can be used to estimate the peak-to-peak ripple current through the LED string.

$$I_{LED(ripple)} = \frac{Z_{COUT} \times I_{L(max)}}{Z_{COUT} + R_{LED}} \tag{10}$$

CREE WLED is used here. The dynamic resistance of the LED is 0.67Ω at 3A forward current. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. In this design, a 22µF, 100V X7R ceramic capacitor and a 0.1µF, 100V X7R ceramic capacitor are chosen. The calculated ripple current of the LED is about 65mA.

8.2.1.2.4 Sense Resistor Selection

The maximum LED current is 1A at 100% PWM duty and the corresponding V_{REF} is 200mV. By using Equation 1, the sense resistance is calculated as 200mΩ.

Note that the power consumption of the sense resistor is 200mW, requiring enough margin of the resistor's power rating in selection.

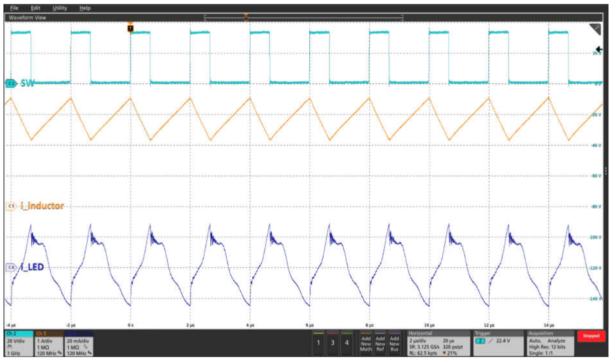
8.2.1.2.5 Other External Components Selection

In this design, a 100Ω, 0603 resistor is recommended for R_{FLT} at CSN pin to avoid noise injection and increase robustness. An optional 1nF, 50V X7R ceramic capacitor is chosen for C_{FLT} across CSP-CSN pins to filter high-frequency noise of sense feedback. Using Equation 11, a 10µF, 50V X7R ceramic capacitor is chosen for C_{SENSE} to suppress the ac magnitude of sense feedback less than 200mV.

$$C_{SENSE} = \frac{0.25 \times I_{L(max)}}{200mV \times f_{SW}} \tag{11}$$

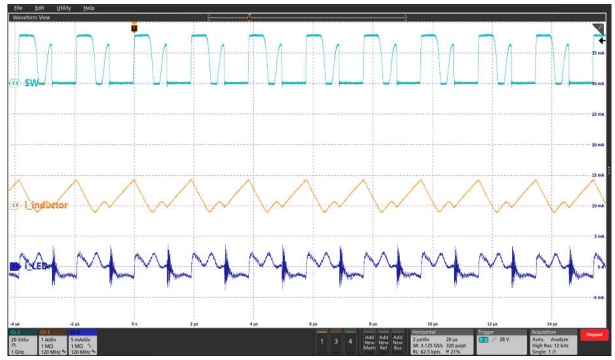
For loop stability, it is recommended to select a 1nF, 10V X7R ceramic capacitor for C_{COMP} and an optional 100Ω resistor for R_{COMP}. An optional 1MΩ resistor is chosen for R_{DAMP} to suppress the overshoot current at startup.

8.2.1.3 Application Curves



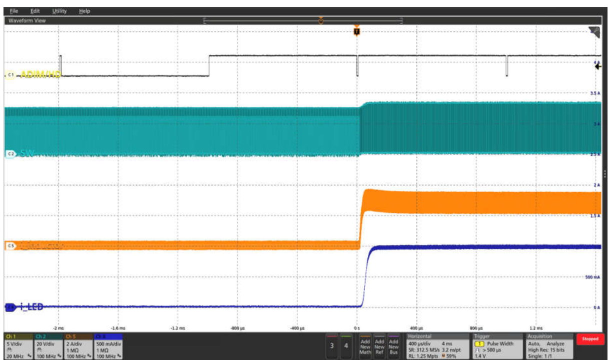
Light Blue: SW, Orange: Inductor Current, Deep Blue: LED Current Ripple (AC)

Figure 8-2. LED Current Ripple at PWM_{ADIM} = 100%, 1kHz and F_{SW} = 500kHz



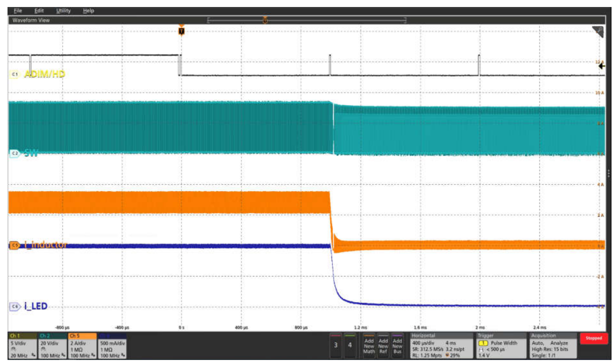
Light Blue: SW, Orange: Inductor Current, Deep Blue: LED Current Ripple (AC)

Figure 8-3. LED Current Ripple at PWM_{ADIM} = 10%, 1kHz and F_{SW} = 500kHz



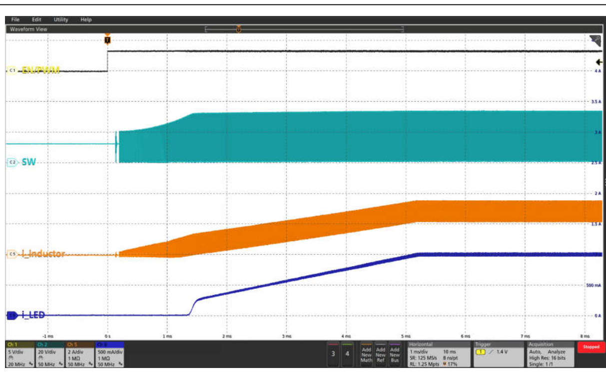
Black: PWM_{ADIM}, Light Blue: SW, Orange: Inductor Current, Deep Blue: LED Current

Figure 8-4. LED Current Transient for a PWM_{ADIM} Transition from 1% to 99%, 1kHz



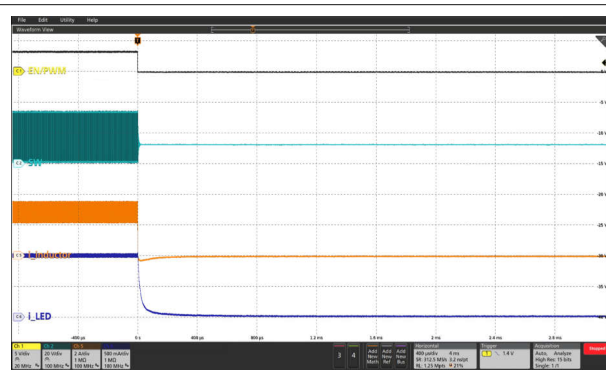
Black: PWM_{ADIM}, Light Blue: SW, Orange: Inductor Current, Deep Blue: LED Current

Figure 8-5. LED Current Transient for a PWM_{ADIM} Transition from 99% to 1%, 1kHz



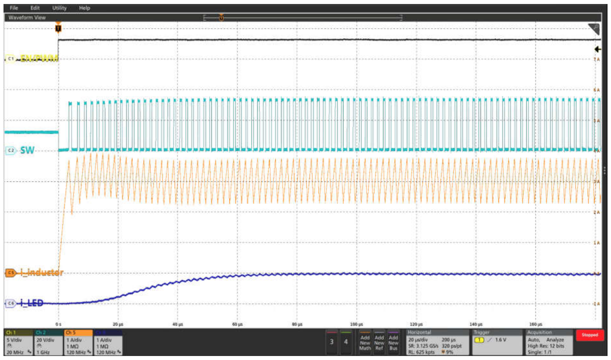
Black: PWM_{PWM}, Light Blue: SW, Orange: Inductor Current, Deep Blue: LED Current

Figure 8-6. Start-Up at PWM_{ADIM} = 100%, 1kHz



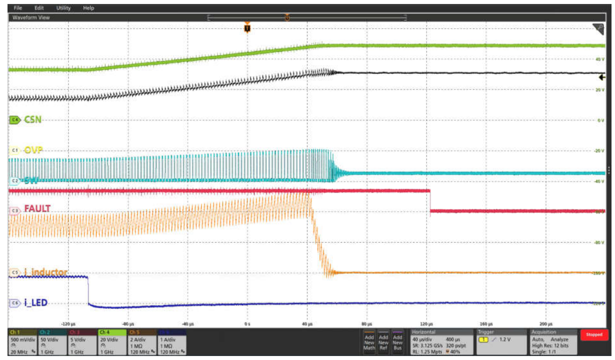
Black: PWM_{PWM}, Light Blue: SW, Orange: Inductor Current, Deep Blue: LED Current

Figure 8-7. Shutdown at PWM_{ADIM} = 100%, 1kHz



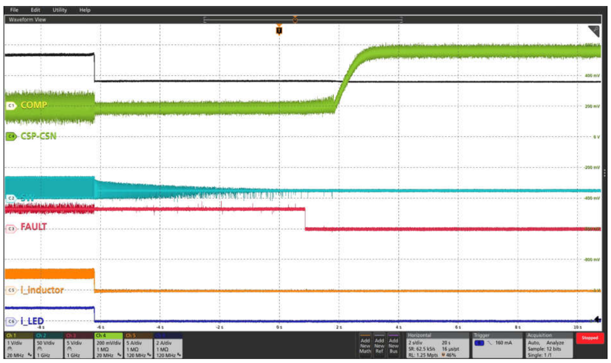
Black: PWM_{PWM}, Light Blue: SW, Orange: Inductor Current, Deep Blue: LED Current

Figure 8-8. LED PWM Dimming Rising Edge at PWM_{PWM} = 50%, 20kHz



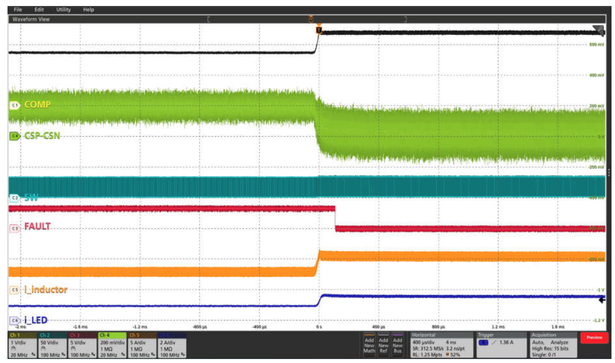
Black: OVP, Light Blue: SW, Red: FAULT, Orange: Inductor Current, Deep Blue: LED Current, Green: CSN

Figure 8-9. LED Open-Load Protection



Black: COMP, Light Blue: SW, Red: FAULT, Orange: Inductor Current, Deep Blue: LED Current, Green: CSP-CSN

Figure 8-10. Sense-Resistor Open Protection



Black: COMP, Light Blue: SW, Red: FAULT, Orange: Inductor Current, Deep Blue: LED Current, Green: CSP-CSN

Figure 8-11. Sense-Resistor Short-Circuit Protection

8.2.2 TPS923654 Buck-Boost, 24V Input, 2A Output, 4-piece WLED Driver with PWM Dimming

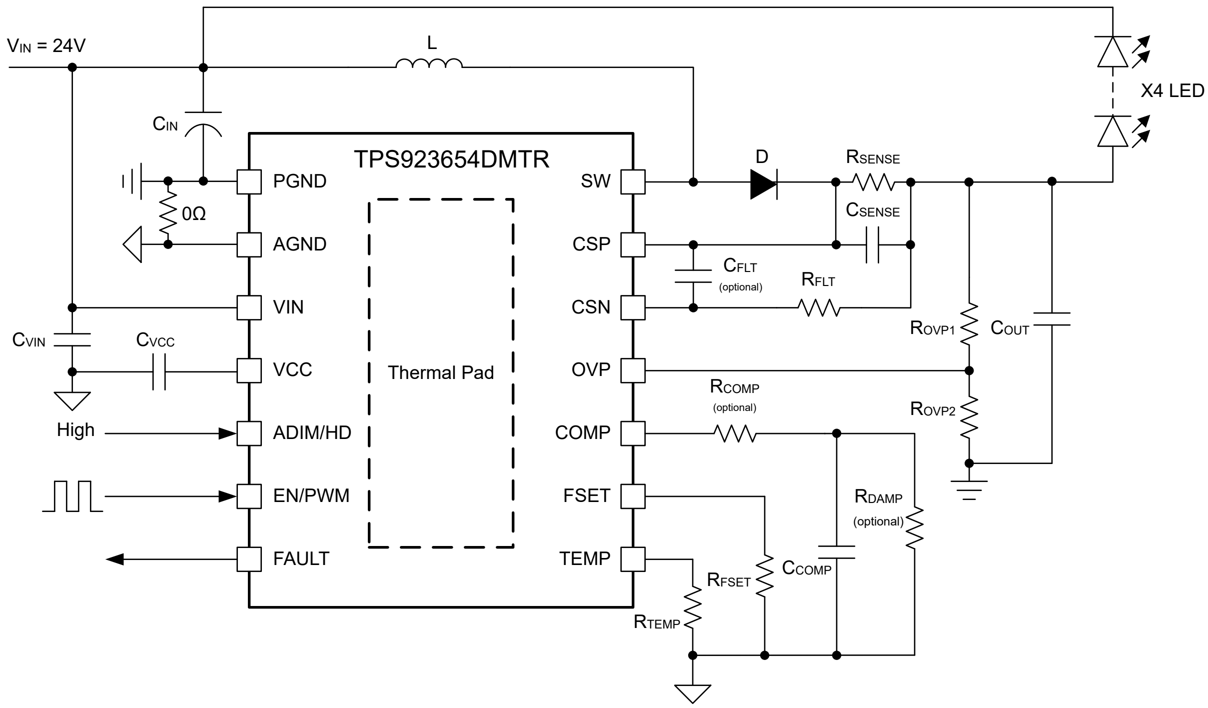


Figure 8-12. Buck-Boost, 24V Input, 2A Output, 4-piece WLED, PWM Dimming Reference Design

8.2.2.1 Design Requirements

For this design example, use the parameters in the following table.

Table 8-2. Design Parameters

PARAMETER	VALUE
Input voltage range	24V ±10%
LED forward voltage	3.0V
Output voltage	12V (3.0 × 4)
Maximum LED current	2A
Inductor current ripple	50% of maximum inductor current
LED current ripple	200mA or less
Input voltage ripple	200mV or less
Dimming type	PWM dimming with TPS923654: 1kHz, 1% to 100% PWM input at the PWM pin

8.2.2.2 Detailed Design Procedure

8.2.2.2.1 Inductor Selection

For this design, the input voltage is a 24V, rail with 10% variation. The output is 4 white LEDs in series and the inductor current ripple by requirement is less than 50% of maximum inductor current. To choose a proper peak-to-peak inductor current ripple, the low-side FET current limit should not be violated when the converter works in no-load condition. This requires half of the peak-to-peak inductor current ripple to be lower than that limit. Another consideration is to ensure reasonable inductor core loss and copper loss caused by the peak-to-peak current ripple. Once this peak-to-peak inductor current ripple is chosen, use Equation 12 to calculate the recommended value of the output inductor L.

$$L = \frac{V_{IN(max)} \times V_{OUT}}{\left(V_{OUT} + V_{IN(max)}\right) \times K_{IND} \times I_{L(max)} \times f_{SW}} \tag{12}$$

where

- K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum LED current.
- $I_{L(max)}$ is the maximum inductor current.
- f_{SW} is the switching frequency.
- $V_{IN(max)}$ is the maximum input voltage.
- V_{OUT} is the sum of the voltage across LED load and the voltage across sense resistor.

With the chosen inductor value, the user can calculate the actual inductor current ripple using Equation 13.

$$I_{L(ripple)} = \frac{V_{IN(max)} \times V_{OUT}}{\left(V_{OUT} + V_{IN(max)}\right) \times L \times f_{SW}} \tag{13}$$

The ratings of inductor RMS current and saturation current must be greater than those seen in the system requirement. This is to ensure no inductor overheat or saturation occurring. During power up, transient conditions or fault conditions, the inductor current may exceed its normal operating current and reach the current limit. Therefore, it is preferred to select a saturation current rating equal to or greater than the converter current limit. The peak-inductor-current and RMS current equations are shown in Equation 14 and Equation 15.

$$I_{L(peak)} = I_{L(max)} + \frac{I_{L(ripple)}}{2} \tag{14}$$

$$I_{L(rms)} = \sqrt{{I_{L(max)}}^2 + \frac{{I_{L(ripple)}}^2}{12}} \tag{15}$$

In this design, $V_{IN(max)}$ = 24V, V_{OUT} = 12V, I_{LED} = 2A, f_{SW} = 1.2MHz, choose K_{IND} = 0.5, the calculated inductance is 4.4μH. A 4.7μH inductor is chosen. With this inductor, the ripple, peak, and rms currents of the inductor are 1.4A, 3.7A, and 3.03A, respectively.

8.2.2.2.2 Input Capacitor Selection

An input capacitor is required to reduce the surge current drawn from the input supply and the switching noise coming from the device. Electrolytic capacitors are recommended for energy storage. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, it is recommended to place a 10-μF capacitor along with a 0.1-μF capacitor from VIN to PGND/AGND to provide high-frequency filtering. The input capacitor voltage rating must be greater than the maximum input voltage. Use Equation 16 to calculate the input ripple voltage, where ESR_{CIN} is the ESR of input capacitor, and K_{DR} is the derating coefficient of ceramic capacitance at the applied DC voltage.

$$V_{IN(ripple)} = I_{L(max)} \times \left(\frac{V_{OUT}}{K_{DR} \times C_{IN} \times f_{SW} \times \left(V_{IN(max)} + V_{OUT}\right)} + ESR_{CIN}\right) \tag{16}$$

In this design, a 100-μF, 50V electrolytic capacitor, a 4.7-μF, 100V X7R ceramic capacitor and a 0.1-μF, 100V X7R ceramic capacitor are chosen, yielding around 190-mV input ripple voltage.

8.2.2.2.3 Output Capacitor Selection

The output capacitor reduces the high-frequency current ripple through the LED string. Excessive current ripple increases the RMS current in the LED string, therefore increasing the LED temperature.

1. Calculate the total dynamic resistance of the LED string (R_{LED}) using the LED manufacturer's datasheet.

2. Calculate the required impedance of the output capacitor (Z_{OUT}) given the acceptable peak-to-peak ripple current through the LED string, $I_{LED(ripple)}$. $I_{L(ripple)}$ is the peak-to-peak inductor ripple current as calculated with the selected inductor.

3. Calculate the minimum effective output capacitance required.

4. Increase the output capacitance appropriately due to the derating effect of applied DC voltage.

See Equation 17, Equation 18, and Equation 19.

$$R_{LED} = \frac{\Delta V_F}{\Delta I_F} \times \#\ of\ LEDs \tag{17}$$

$$Z_{COUT} = \frac{R_{LED} \times I_{LED(ripple)}}{I_{L(max)} - I_{LED(ripple)}} \tag{18}$$

$$C_{COUT} = \frac{1}{2\pi \times f_{SW} \times Z_{COUT}} \tag{19}$$

Once the output capacitor is chosen, Equation 20 can be used to estimate the peak-to-peak ripple current through the LED string.

$$I_{LED(ripple)} = \frac{Z_{COUT} \times I_{L(max)}}{Z_{COUT} + R_{LED}} \tag{20}$$

Cree WLED is used here. The dynamic resistance of the LED is 0.67 ohm at 1-A forward current. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. In this design, a 10-μF, 100-V X7R ceramic capacitor and a 0.1-μF, 100-V X7R ceramic capacitor are chosen. The calculated ripple current of the LED is about 70 mA.

8.2.2.2.4 Sense Resistor Selection

The maximum LED current is 2 A at 100% PWM duty and the corresponding V_{REF} is 200 mV. By using Equation 1, the sense resistance is calculated as 100 mΩ.

Note that the power consumption of the sense resistor is 400 mW, requiring enough margin of the resistor's power rating in selection.

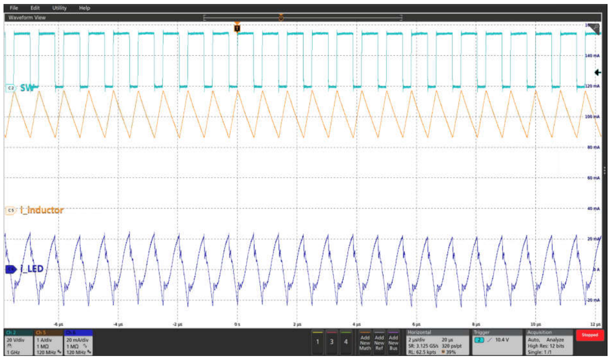
8.2.2.2.5 Other External Components Selection

In this design, a 100Ω, 0603 resistor is recommended for R_{FLT} at CSN pin to avoid noise injection and increase robustness. An optional 1nF, 50V X7R ceramic capacitor is chosen for C_{FLT} across CSP-CSN pins to filter high-frequency noise of sense feedback. Using Equation 21, a 10μF, 50V X7R ceramic capacitor is chosen for C_{SENSE} to suppress the ac magnitude of sense feedback less than 200mV.

$$C_{SENSE} = \frac{0.25 \times I_{L(max)}}{200mV \times f_{SW}} \tag{21}$$

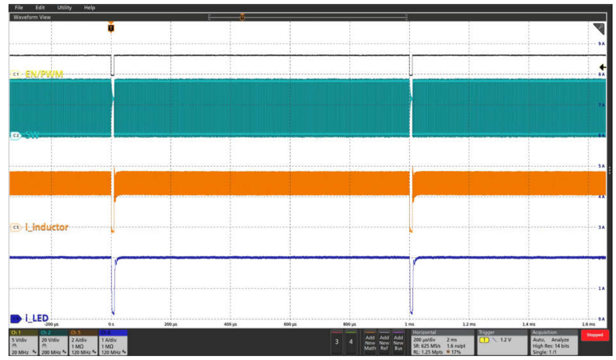
For loop stability, it is recommended to select a 1nF, 10V X7R ceramic capacitor for C_{COMP} and an optional 100Ω resistor for R_{COMP}. An optional 1MΩ resistor is chosen for R_{DAMP} to suppress the overshoot current at rising edge of PWM on.

8.2.2.3 Application Curves



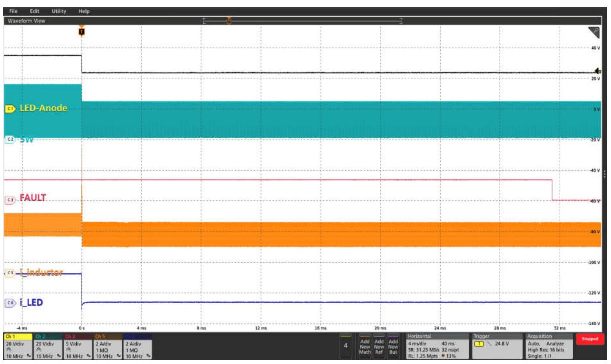
Light Blue: SW, Orange: Inductor Current, Deep Blue: LED Current Ripple (AC)

Figure 8-13. LED Current Ripple at PWM_{ADIM} = 100%, 1kHz and F_{SW} = 1.2MHz



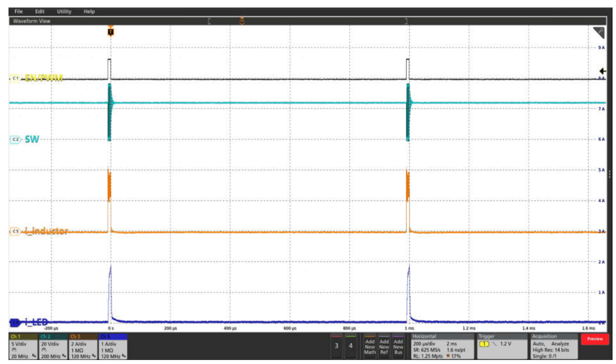
Black: PWM_{PWM}, Light Blue: SW, Orange: Inductor Current, Deep Blue: LED Current

Figure 8-14. LED PWM Dimming at PWM_{PWM} = 99%, 1kHz



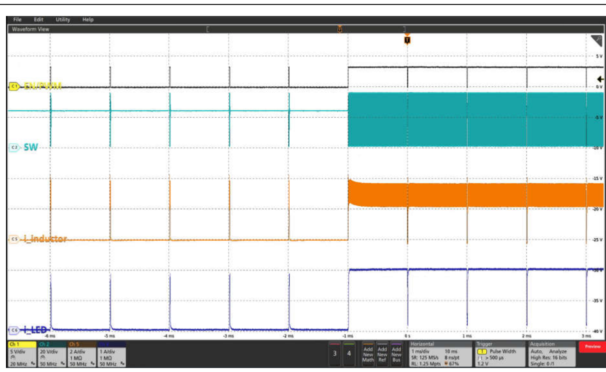
Black: PWM_{PWM}, Light Blue: SW, Red: FAULT, Orange: Inductor Current, Deep Blue: LED Current

Figure 8-15. LED+ Short-to-VIN Protection



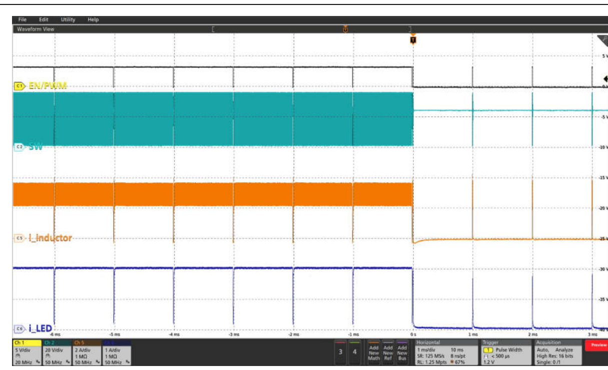
Black: PWM_{PWM}, Light Blue: SW, Orange: Inductor Current, Deep Blue: LED Current

Figure 8-16. LED PWM Dimming at PWM_{PWM} = 1%, 1kHz



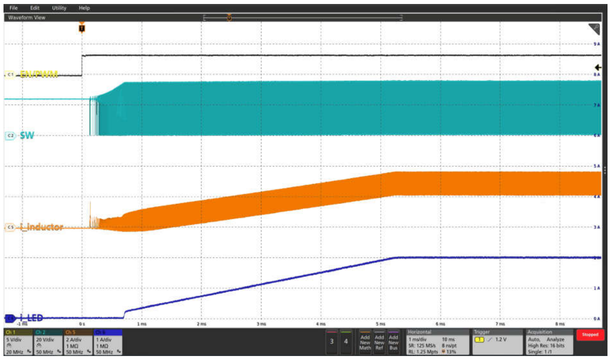
Black: PWM_{PWM}, Light Blue: SW, Orange: Inductor Current, Deep Blue: LED Current

Figure 8-17. LED Current Transient for a PWM_{PWM} Transition from 1% to 99%, 1kHz



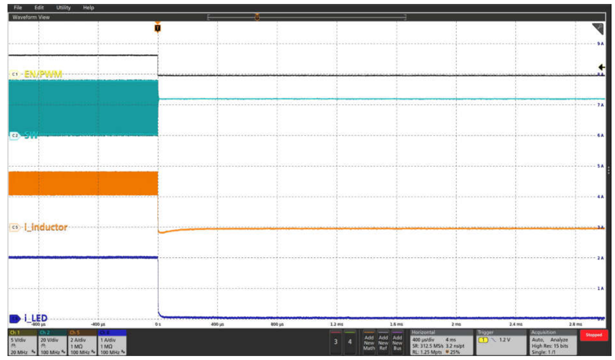
Black: PWM_{PWM}, Light Blue: SW, Orange: Inductor Current, Deep Blue: LED Current

Figure 8-18. LED Current Transient for a PWM_{PWM} Transition from 99% to 1%, 1kHz



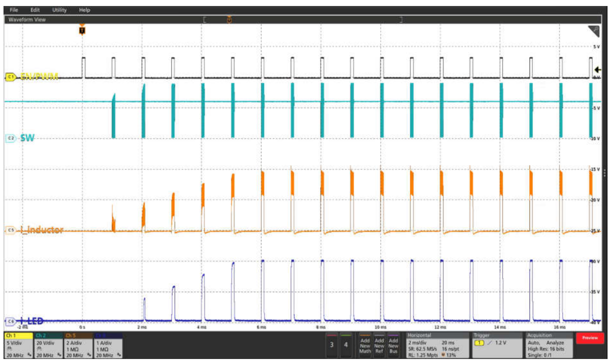
Black: PWM_{PWM}, Light Blue: SW, Orange: Inductor Current, Deep Blue: LED Current

Figure 8-19. Start-Up at PWM_{PWM} = 100%, 1kHz



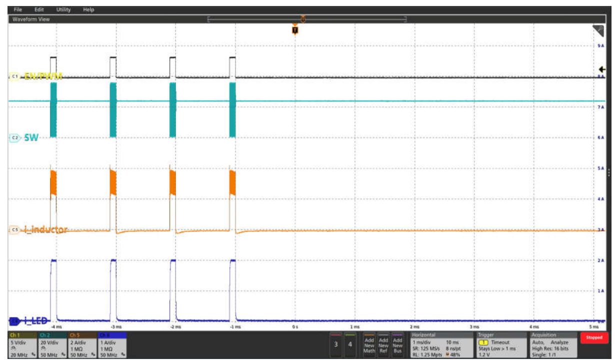
Black: PWM_{PWM}, Light Blue: SW, Orange: Inductor Current, Deep Blue: LED Current

Figure 8-20. Shutdown at PWM_{PWM} = 100%, 1kHz



Black: PWM_{PWM}, Light Blue: SW, Orange: Inductor Current, Deep Blue: LED Current

Figure 8-21. Start-Up at PWM_{PWM} = 10%, 1kHz



Black: PWM_{PWM}, Light Blue: SW, Orange: Inductor Current, Deep Blue: LED Current

Figure 8-22. Shutdown at PWM_{PWM} = 10%, 1kHz

8.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply ranging between 4.5V and 65V. This input supply must be well regulated. The device requires an input capacitor to reduce the surge current drawn from the input supply and the switching noise from the device. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 10μF capacitor is enough.

8.4 Layout

The TPS92365x family requires a proper layout for optimal performance. The following section gives some guidelines to ensure a proper layout.

8.4.1 Layout Guidelines

An example of a proper layout for the TPS92365x family is shown in .Section 8.4.2

- Creating a large PGND plane for good electrical and thermal performance is important.
- The IN and PGND traces should be as wide as possible to reduce trace impedance. Wide traces have the additional advantage of providing excellent heat dissipation.
- Thermal vias can be used to connect the top-side PGND plane to additional printed-circuit board (PCB) layers for heat dissipation and grounding.
- The input capacitors must be located as close as possible to the IN pin and the PGND/AGND pin.
- The VCC capacitor should be placed as close as possible to VCC pin to ensure stable LDO output voltage.
- The SW trace must be kept as short as possible to reduce parasitic inductance and thereby reduce transient voltage spikes. Short SW trace also reduces radiated noise and EMI.
- Do not allow switching current to flow under the device.
- The routing of CSN and CSP traces are recommended to be in parallel and kept as short as possible and placed away from the high-voltage switching trace and the ground shield.
- The compensation capacitor must be placed as close as possible to COMP pin so as to prevent oscillation and system instability.

8.4.2 Layout Example

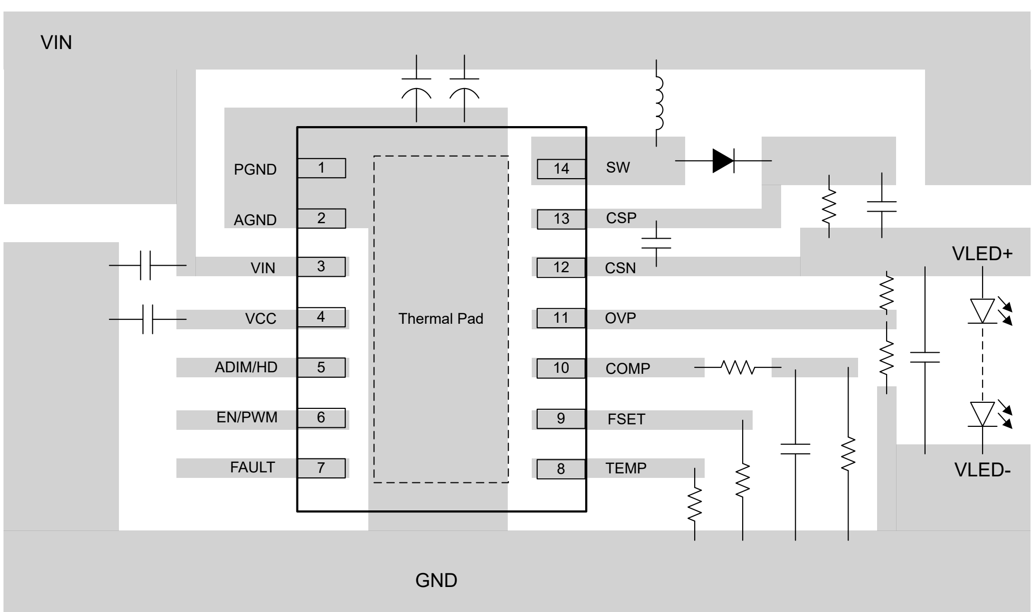


Figure 8-23. 14-Pin VSON Top View Layout Example

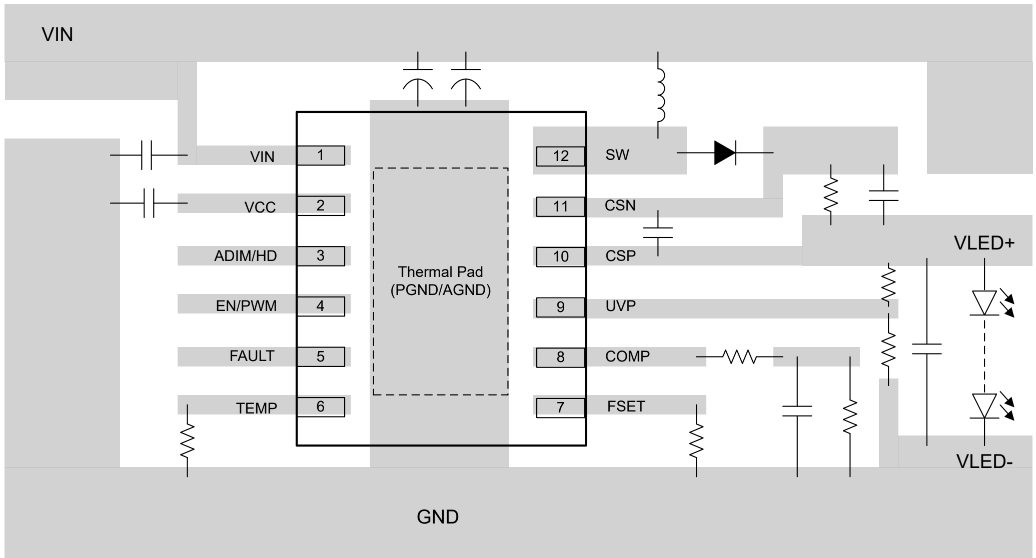


Figure 8-24. 12-Pin WSON Top View Layout Example

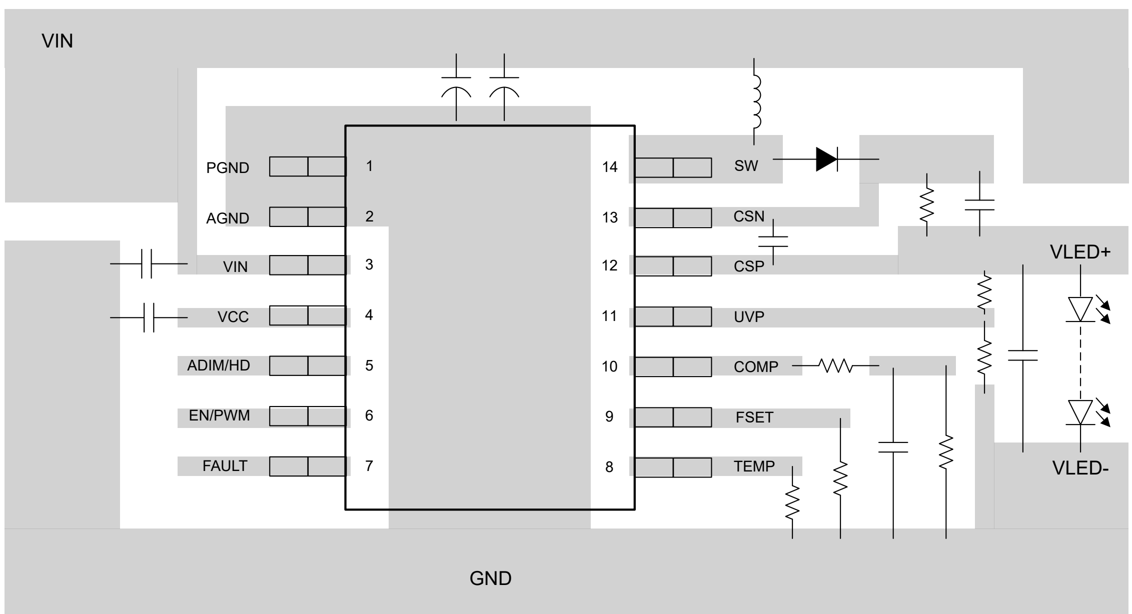


Figure 8-25. 14-Pin SOT-23-TH Top View Layout Example

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.3 Trademarks

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9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

Changes from Revision A (September 2023) to Revision B (February 2025)	Page
• Added 8.5A current limit for TPS923654HMDMTR and TPS923655HMDMTR	1
• Added RFLT in simplified schematic	1
• Changed pin function description wording for VCC, FAULT, TEMP, FSET and COMP	4
• Added comments on 0% and 100% analog dimming	15
• Added comments on entering and exiting hybrid dimming mode	15
• Changed CC/CV modes wording and added CV hysteresis window in transition diagram	17
• Changed protection behavior wording	19
• Added RFLT in reference design schematic	21
• Changed other external components selection wording	23
• Added RFLT in reference design schematic	26
• Changed other external components selection wording	28
• Changed PWM frequency from 20kHz to 1kHz in waveform figure titles	29

Changes from Revision * (June 2023) to Revision A (September 2023)	Page
• Updated document from Advance Information to Production Data	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS923652DMTR	Active	Production	VSON (DMT) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T3652
TPS923652DMTR.A	Active	Production	VSON (DMT) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T3652
TPS923652DRRR	Active	Production	WSON (DRR) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T23652
TPS923652DRRR.A	Active	Production	WSON (DRR) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T23652
TPS923652DYYR	Active	Production	SOT-23-THIN (DYY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T3652
TPS923652DYYR.A	Active	Production	SOT-23-THIN (DYY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T3652
TPS923653DMTR	Active	Production	VSON (DMT) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T3653
TPS923653DMTR.A	Active	Production	VSON (DMT) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T3653
TPS923653DRRR	Active	Production	WSON (DRR) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T23653
TPS923653DRRR.A	Active	Production	WSON (DRR) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T23653
TPS923653DYYR	Active	Production	SOT-23-THIN (DYY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T3653
TPS923653DYYR.A	Active	Production	SOT-23-THIN (DYY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T3653
TPS923654DMTR	Active	Production	VSON (DMT) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T3654
TPS923654DMTR.A	Active	Production	VSON (DMT) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T3654
TPS923654DRRR	Active	Production	WSON (DRR) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T23654
TPS923654DRRR.A	Active	Production	WSON (DRR) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T23654
TPS923654HMDMTR	Active	Production	VSON (DMT) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T364H
TPS923654HMDMTR.A	Active	Production	VSON (DMT) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T364H
TPS923654MDMTR	Active	Production	VSON (DMT) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T364M
TPS923654MDMTR.A	Active	Production	VSON (DMT) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T364M
TPS923655DMTR	Active	Production	VSON (DMT) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T3655
TPS923655DMTR.A	Active	Production	VSON (DMT) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T3655
TPS923655DRRR	Active	Production	WSON (DRR) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T23655
TPS923655DRRR.A	Active	Production	WSON (DRR) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T23655
TPS923655HMDMTR	Active	Production	VSON (DMT) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T365H
TPS923655HMDMTR.A	Active	Production	VSON (DMT) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T365H

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS923655MDMTR	Active	Production	VSON (DMT) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T365M
TPS923655MDMTR.A	Active	Production	VSON (DMT) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T365M

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

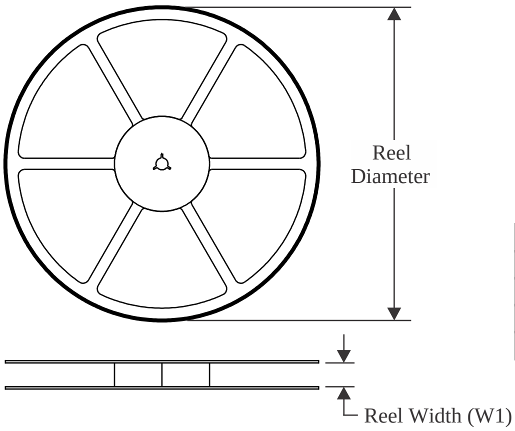
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

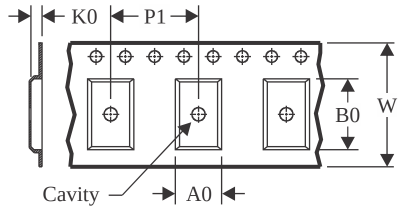
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

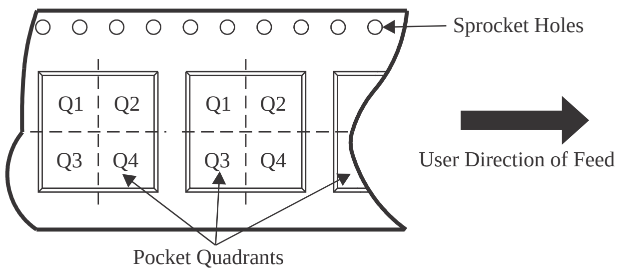


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

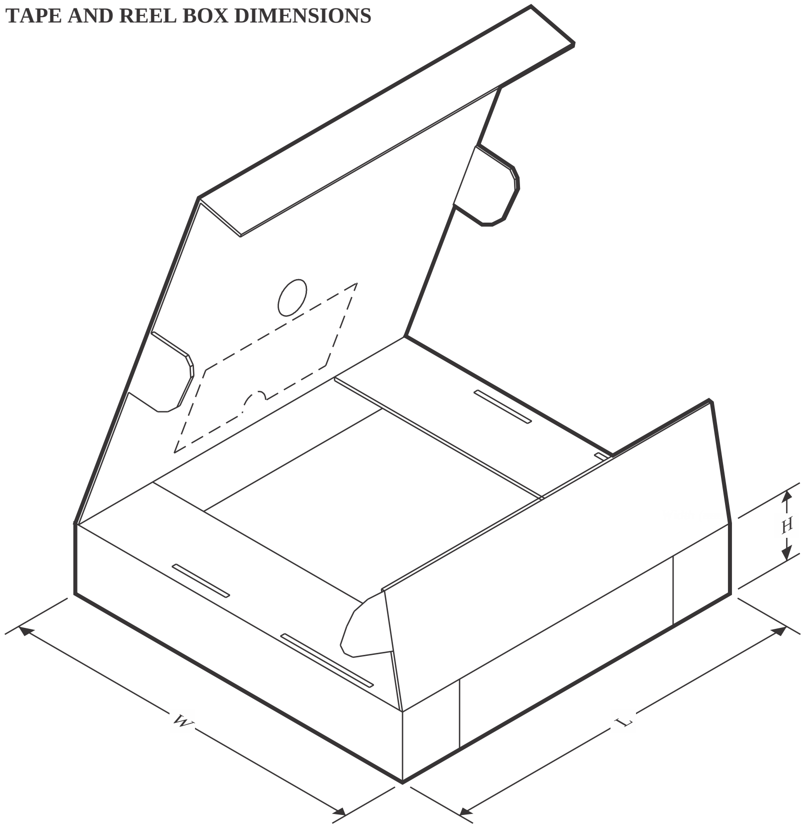
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS923652DMTR	VSON	DMT	14	3000	330.0	12.4	3.3	4.8	1.2	8.0	12.0	Q1
TPS923652DRRR	WSON	DRR	12	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS923652DYYR	SOT-23-THIN	DYY	14	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
TPS923653DMTR	VSON	DMT	14	3000	330.0	12.4	3.3	4.8	1.2	8.0	12.0	Q1
TPS923653DRRR	WSON	DRR	12	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS923653DYYR	SOT-23-THIN	DYY	14	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
TPS923654DMTR	VSON	DMT	14	3000	330.0	12.4	3.3	4.8	1.2	8.0	12.0	Q1
TPS923654DRRR	WSON	DRR	12	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS923654HMDMTR	VSON	DMT	14	3000	330.0	12.4	3.3	4.8	1.2	8.0	12.0	Q1
TPS923654MDMTR	VSON	DMT	14	3000	330.0	12.4	3.3	4.8	1.2	8.0	12.0	Q1
TPS923655DMTR	VSON	DMT	14	3000	330.0	12.4	3.3	4.8	1.2	8.0	12.0	Q1
TPS923655DRRR	WSON	DRR	12	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS923655HMDMTR	VSON	DMT	14	3000	330.0	12.4	3.3	4.8	1.2	8.0	12.0	Q1
TPS923655MDMTR	VSON	DMT	14	3000	330.0	12.4	3.3	4.8	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS923652DMTR	VSON	DMT	14	3000	367.0	367.0	35.0
TPS923652DRRR	WSON	DRR	12	3000	367.0	367.0	35.0
TPS923652DYYR	SOT-23-THIN	DYY	14	3000	336.6	336.6	31.8
TPS923653DMTR	VSON	DMT	14	3000	367.0	367.0	35.0
TPS923653DRRR	WSON	DRR	12	3000	367.0	367.0	35.0
TPS923653DYYR	SOT-23-THIN	DYY	14	3000	336.6	336.6	31.8
TPS923654DMTR	VSON	DMT	14	3000	367.0	367.0	35.0
TPS923654DRRR	WSON	DRR	12	3000	367.0	367.0	35.0
TPS923654HMDMTR	VSON	DMT	14	3000	367.0	367.0	35.0
TPS923654MDMTR	VSON	DMT	14	3000	367.0	367.0	35.0
TPS923655DMTR	VSON	DMT	14	3000	367.0	367.0	35.0
TPS923655DRRR	WSON	DRR	12	3000	367.0	367.0	35.0
TPS923655HMDMTR	VSON	DMT	14	3000	367.0	367.0	35.0
TPS923655MDMTR	VSON	DMT	14	3000	367.0	367.0	35.0

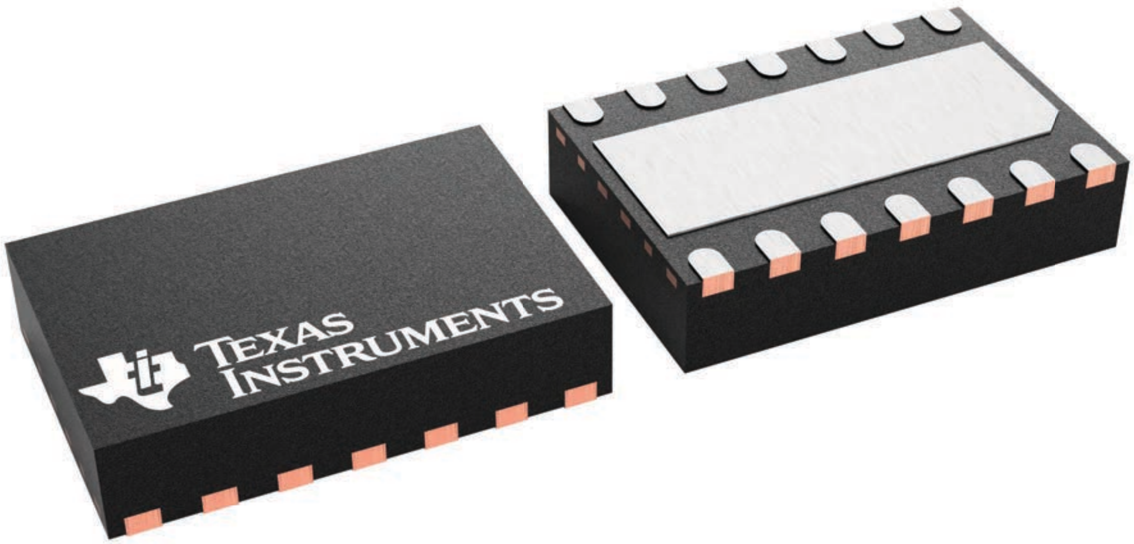
DMT 14

VSON - 0.9 mm max height

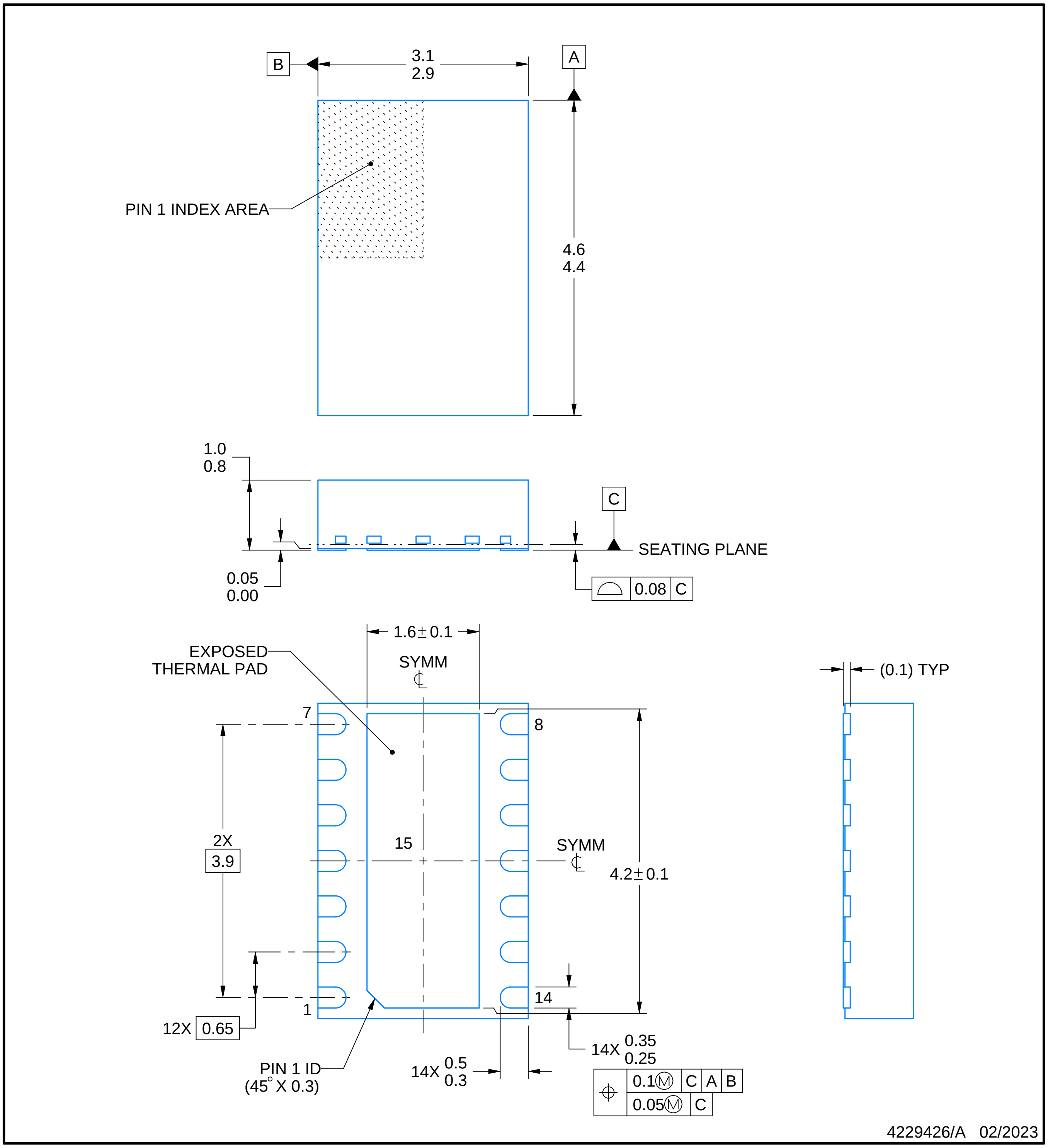
3 x 4.5, 0.65 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

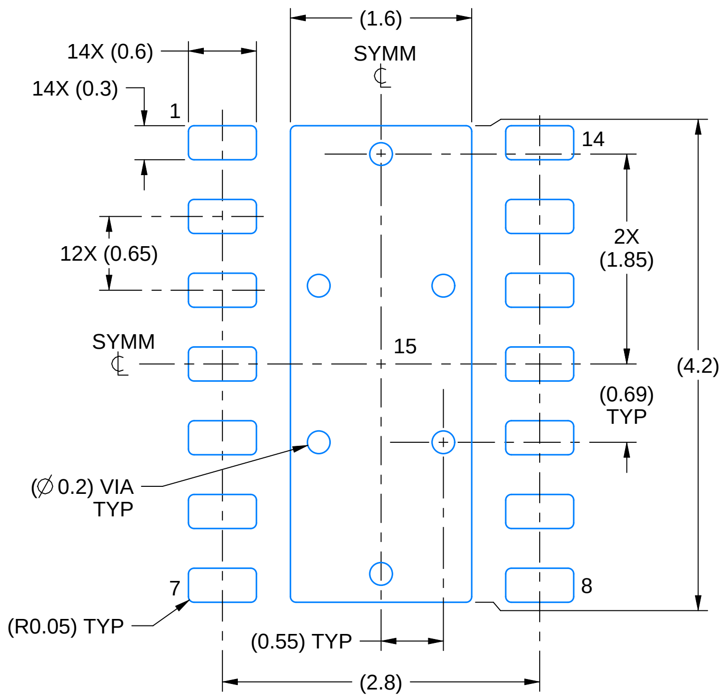


4225088/A

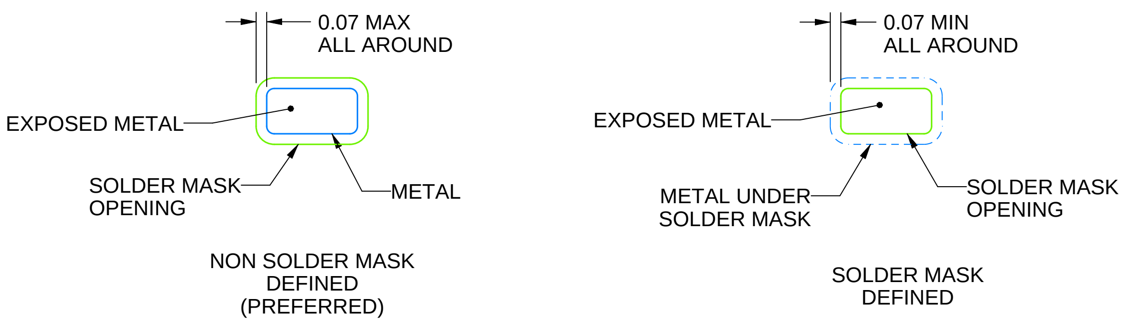


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

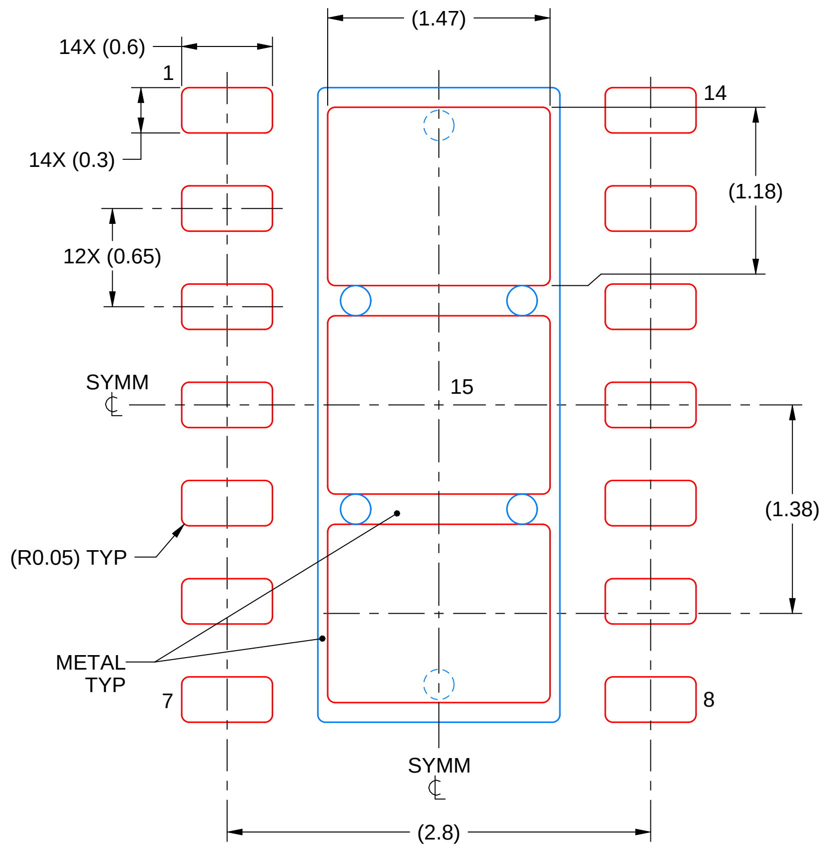


SOLDER MASK DETAILS

4229426/A 02/2023

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 15
77.4% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4229426/A 02/2023

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

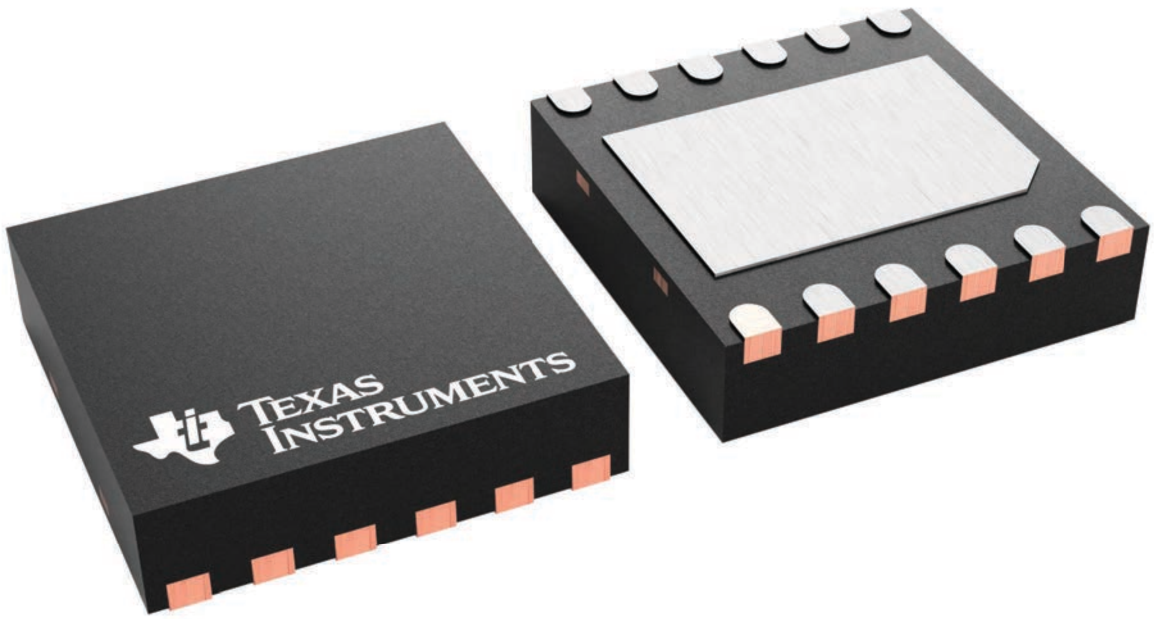
DRR 12

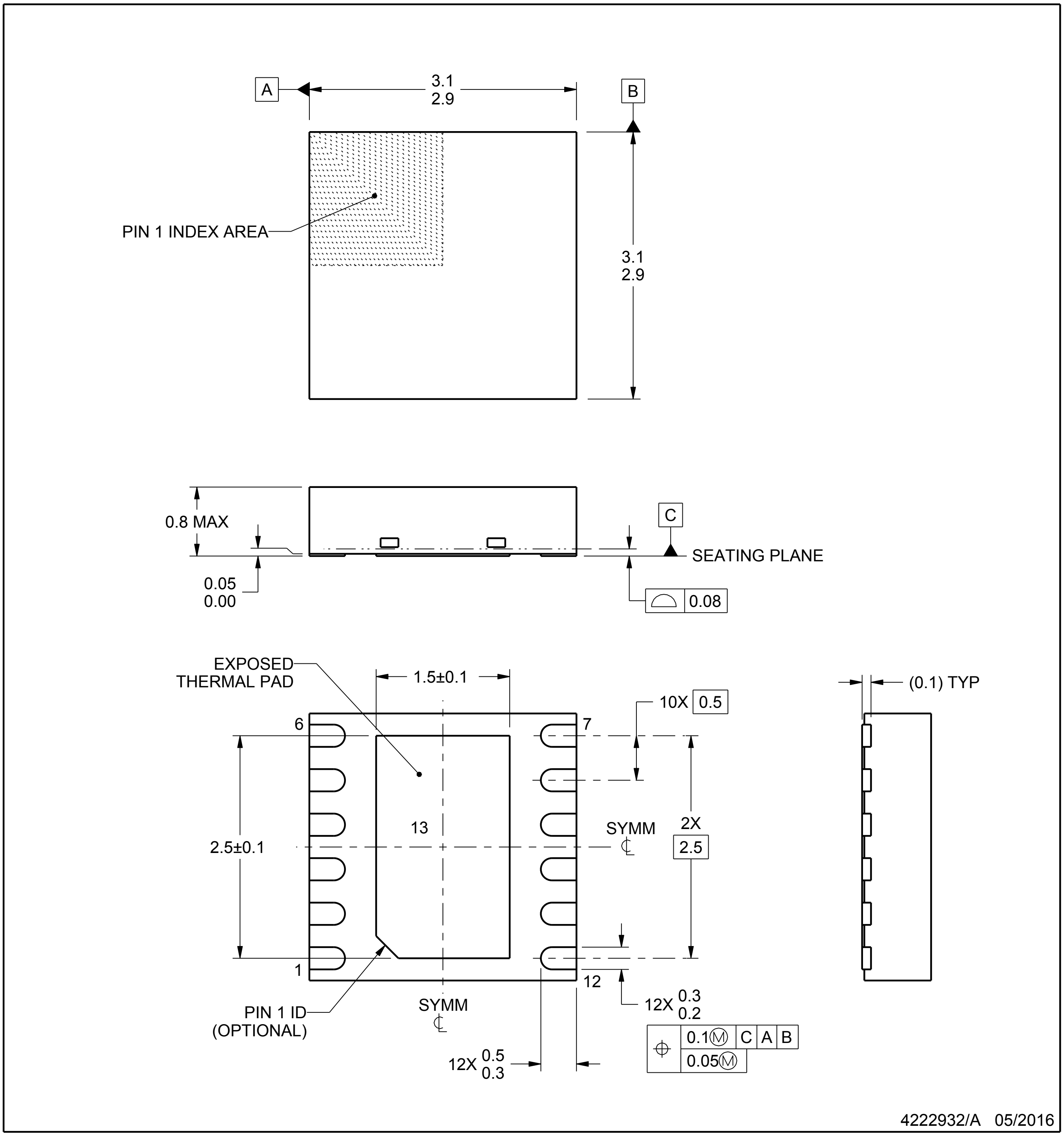
WSON - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

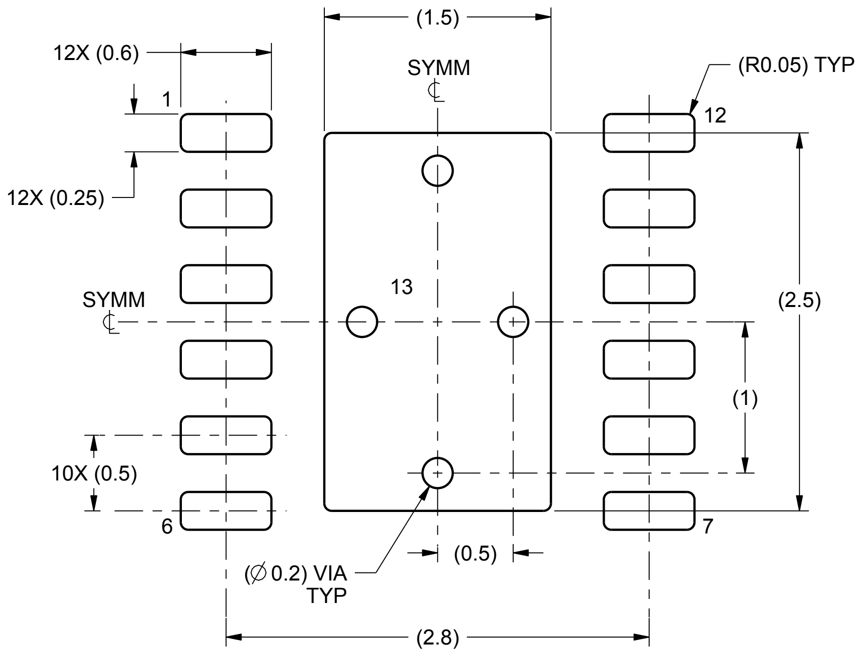
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



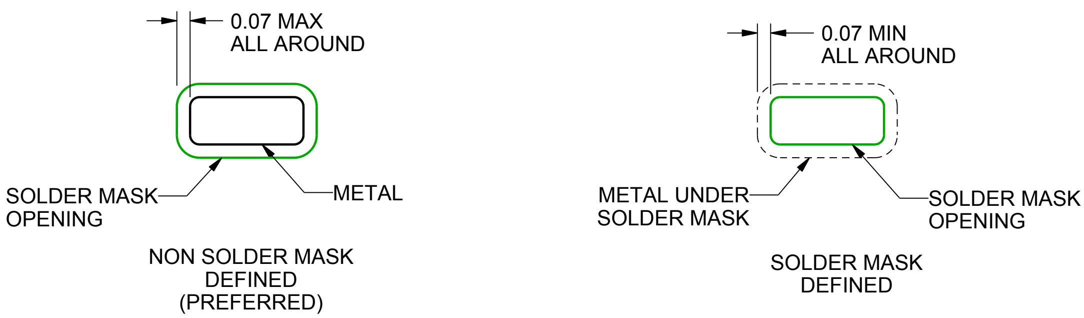


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

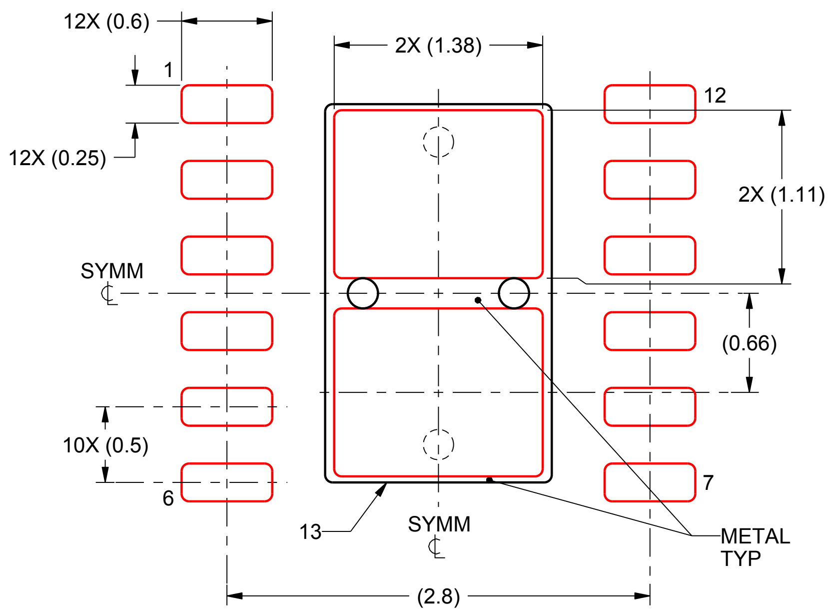


SOLDER MASK DETAILS

4222932/A 05/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



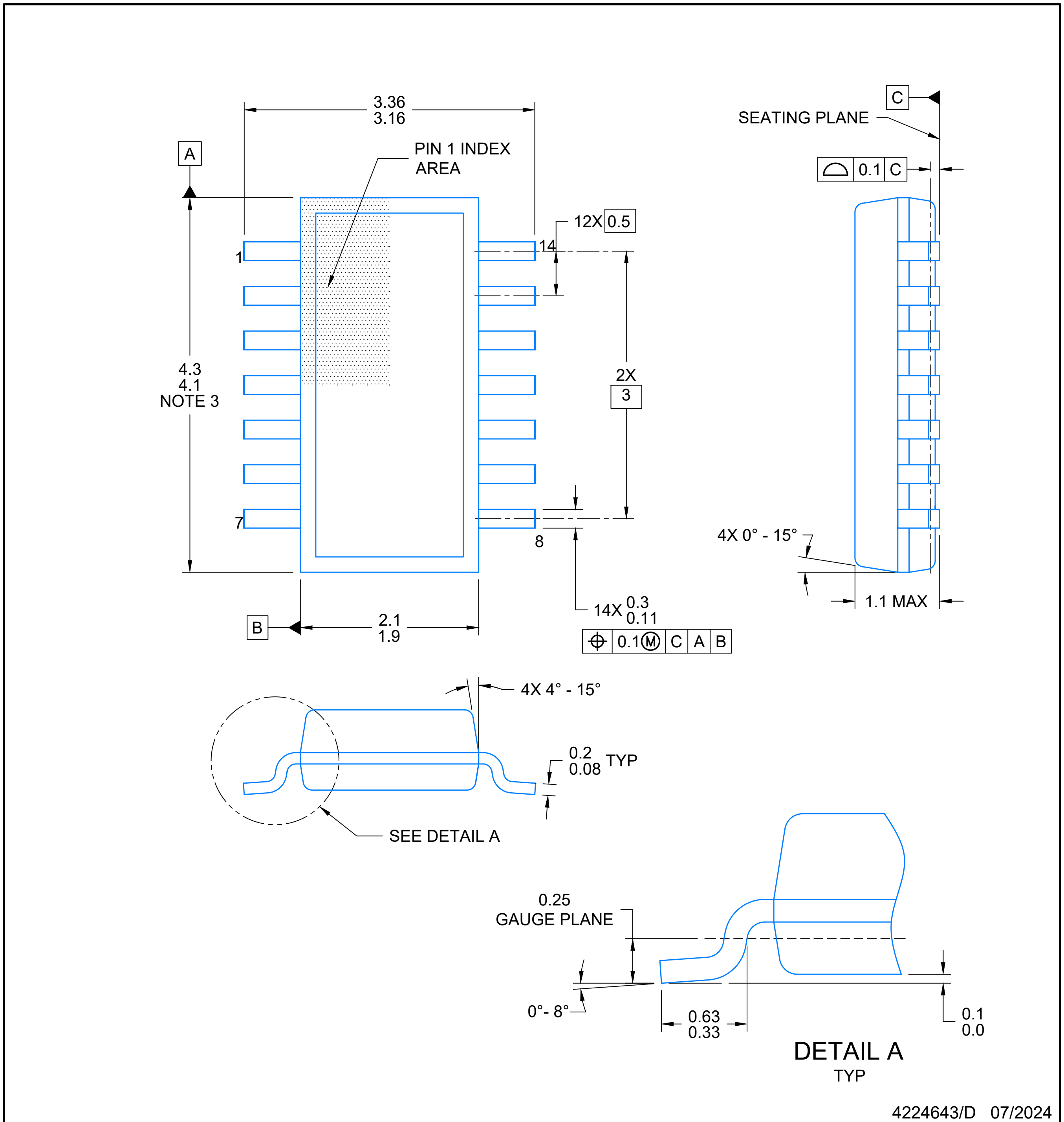
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 13
81.7% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4222932/A 05/2016

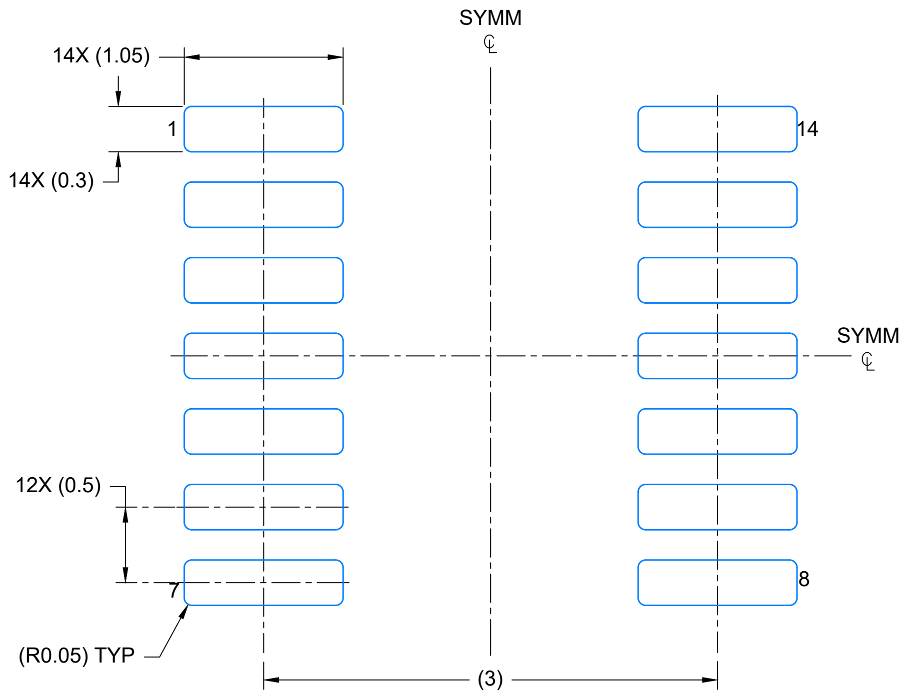
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

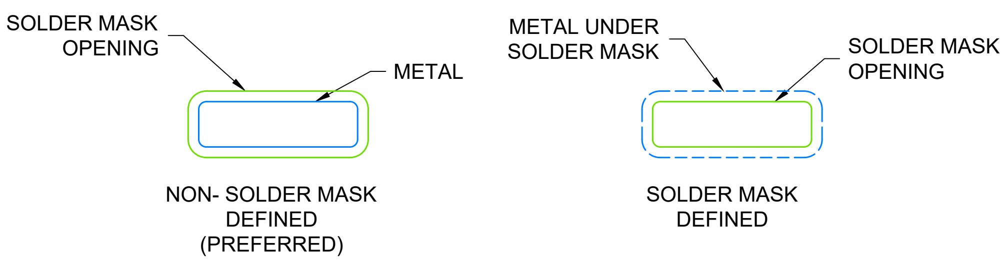


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

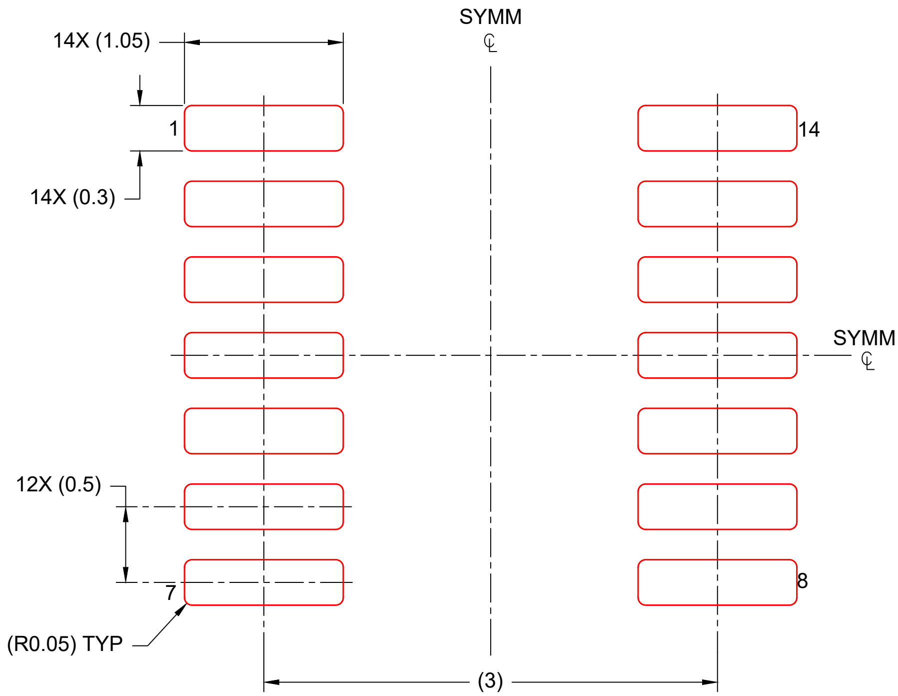


SOLDER MASK DETAILS

4224643/D 07/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224643/D 07/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.