TRF3302-Q1 1165MHz to 1630MHz, Multiband, GPS and GNSS, Low-Noise Amplifier

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
- GNSS L1 (GPS), E1, and B1 bands:
  - Noise figure (NF): 0.85dB
  - Input return loss (S11): –11.7dB
  - Output return loss (S22): –15.3dB
  - 2-element input match
- Multiband GPS/GNSS L1, L2, and L5 support:
  - Noise figure (NF): 1.2dB
  - Input return loss (S11): –12dB
  - Output return loss (S22): –12.3dB
  - 4-element input match
- Power gain (G_P): 16.9dB
- Input IP3 (V_{CC} = 2.5V):
  - In-band = –5.4dBm
  - Out-of-band = –4.8dBm
- Input P1dB: –10.2dBm (V_{CC} = 2.5V)
- Integrated 50Ω output match
- Supply current: 4.6mA (10nA shutdown)
- Flexible supply voltage: 1.8V to 3.3V
- Automatic optical inspection (AOI) compatible package: WSON-FCRLF-6 with wettable flanks

2 Applications

- GNSS receiver LNA
- Global positioning receivers
- Asset trackers
- Smart trackers
- Telematics control unit (TCU)
- Intelligent antenna module
- Automotive emergency call (eCall)
- Electronic toll collection (ETC)
- Navigation and global positioning systems

3 Description

The TRF3302-Q1 is a high-gain, low-noise amplifier (LNA) designed for GNSS receiver applications. The device has 16.9dB power gain with an ultra-low noise figure of 0.85dB for high sensitivity GNSS receivers. An input-referred P1dB of –10.2dBm and IP3 of –5.4dBm helps maintain the receiver sensitivity in the presence of jamming signals from cellular bands.

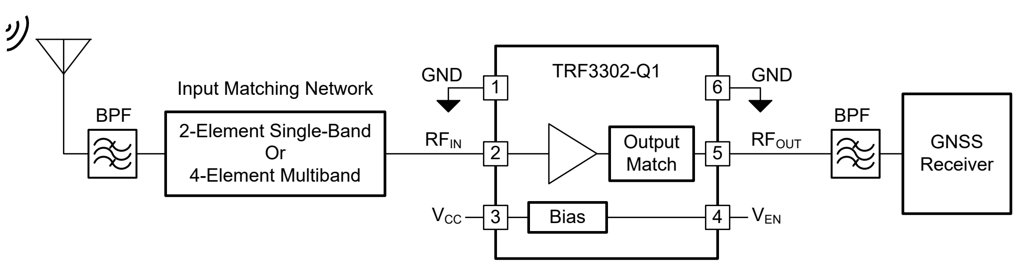
The broadband design of TRF3302-Q1 supports a wide array of bands in GNSS satellite constellations such as GPS, Galileo, BeiDou, QZSS, NavIC/IRNSS, and GLONASS. The device also supports L-band of Iridium satellite system. A 2-element (capacitor and inductor) input match provides low noise and good return loss performance for L1 (GPS), E1 (Galileo), and B1 (BeiDou) bands. The inductor value is adjustable to achieve nearly 150MHz of bandwidth with minimal performance degradation for applications that need coverage for lower GPS bands L2 through L5, Galileo E6 through E5a, BeiDou B3 through B2a, QZSS L6, NavIC L5, and GLONASS bands G2 through G3. A 4-element external input matching network combined with the wideband output of TRF3302-Q1 delivers performance coverage for all major GNSS bands with a ≅ 1.2dB NF, and S11 and S22 better than –10dB.

The TRF3302-Q1 operates on a 1.8V to 3.3V single supply and consumes only 4.6mA of current for power and thermal sensitive designs. The device features a digital logic compatible enable pin for additional power savings. The TRF3302-Q1 is rated for an operating ambient temperature of –40°C to +125°C.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TRF3302-Q1	VBL (WSON-FCRLF, 6) with wettable flanks	1.3mm × 1mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical GNSS Receiver System

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

4 Pin Configuration and Functions

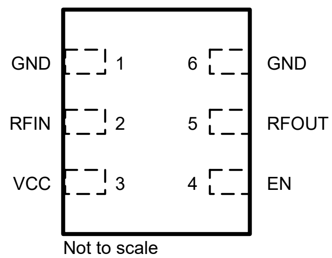


Figure 4-1. VBL Package, 6-Pin WSON-FCRLF (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	GND	Ground	RF and dc ground. Connect to PCB ground plane.
2	RFIN	Input	RF input. Optional external dc-blocking capacitor. Internally matched to 50Ω.
3	VCC	Power	Power supply.
4	EN	Input	Device enable signal, referenced to ground. Voltage must be forced. Logic 1 = enable. Logic 0 = power down.
5	RFOUT	Output	RF output. Integrated dc-blocking capacitor and internally matched to 50Ω.
6	GND	Ground	RF and dc ground. Connect to PCB ground plane.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)			3.45	V
RF_{IN}, RF_{OUT}	Voltage on RF pins(2)	V_{CC} ≤ 2.05V, no RF	–1.4V	V_{CC} + 1.4V	V
		V_{CC} > 2.05V, no RF	–1.4V	3.45V	
P_{IN}	Input RF power			10	dBm
V_{EN}	Enable pin voltage(2)	V_{CC} ≤ 2.75V	–0.7V	V_{CC} + 0.7V	V
		V_{CC} > 2.75V	–0.7V	3.45V	
T_J	Junction temperature		–40	150	°C
T_{stg}	Storage temperature		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Referenced to GND.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002, all pins(1)	±1750	V
		Charged device model (CDM), per AEC Q100-011, all pins	±1500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	1.75		3.3	V
T_A	Ambient temperature	–40		125	°C

5.4 Thermal Information

THERMAL METRIC(1)		TRF3302-Q1	UNIT
		VBL (WSON-FCRLF)	
		6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	152.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	44.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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5.5 Electrical Characteristics - GPS L1 Band

at T_A = 27°C, V_{CC} = 2.5V, f = 1575MHz (L1 band), source impedance (Z_S) = load impedance (Z_L) = 50Ω, and input matched to 50Ω with L1 = 8.2nH (0402DC-8N2XGRW) and C1 = 10pF (GJM1555C1H100JB01) with input and output configuration as shown in Figure 6-2, de-embedded up to capacitor, C1, on input and RFOUT pin on the output (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
RF PERFORMANCE							
	Operating frequency			1300	1575	1630	MHz
G_P	Small-signal power gain	P_{IN} = –27dBm	V_{CC} = 1.8V	12.3	16.9	19.5	dB
			V_{CC} = 2.5V	12.8	16.8	19.7	
			V_{CC} = 3.3V	12.8	16.8	20.7	
NF	Noise figure	V_{CC} = 1.8V to 3.3V			0.85		dB
S_{11}	Input return loss	P_{IN} = –27dBm, V_{CC} = 1.8V to 3.3V			–11.7		dB
S_{22}	Output return loss	P_{IN} = –27dBm, V_{CC} = 1.8V to 3.3V			–15.3		dB
S_{12}	Reverse isolation	P_{IN} = –27dBm, V_{CC} = 1.8V to 3.3V			–42.5		dB
IP1dB	Input 1dB compression point	No jammer	V_{CC} = 1.8V		–13.2		dBm
			V_{CC} = 2V		–11.7		
			V_{CC} = 2.5V	–14.7	–10.2		
			V_{CC} > 2.5V		–10.2		
	Input 1dB compression point	f_{JAM} = 850MHz, P_{JAM} = –20dBm	V_{CC} = 1.8V		–14.4		dBm
			V_{CC} ≥ 2.5V		–10.7		
	Input 1dB compression point	f_{JAM} = 1850MHz, P_{JAM} = –20dBm	V_{CC} = 1.8V		–13.8		dBm
			V_{CC} ≥ 2.5V		–10.8		
IIP3	In-band input third-order intercept point	P_{IN} = –25dBm/tone, 5MHz tone spacing	V_{CC} = 1.8V		–5.5		dBm
			V_{CC} ≥ 2V		–5.4		
$IIP3_{OOB}$	Out-of-band input third-order intercept point	P_{IN} = –25dBm/tone, at f = 1575MHz with out-of-band f_1 = 1713MHz and f_2 = 1851MHz	V_{CC} = 1.8V		–5.7		dBm
			V_{CC} = 2V		–5.2		
			V_{CC} ≥ 2.2V		–4.8		
K	Rollett stability factor			1			
DC PARAMETERS							
V_{CC}	Supply voltage			1.8		3.3	V
I_{CC}	Active supply current	V_{CC} = 1.8V, no RF		3	4.6	5.9	mA
		V_{CC} = 2.5V, no RF		3.2	4.6	5.9	mA
		V_{CC} = 3.3V, no RF		3.2	4.6	7	mA
	Active power dissipation	V_{CC} = 1.8V, no RF			8.3	10.6	mW
		V_{CC} = 2.5V, no RF			11.5	14.8	
		V_{CC} = 3.3V, no RF			15.2	23.1	
I_{SHDN}	Shutdown supply current	V_{CC} = 1.8V, no RF			0.01	1	μA
		V_{CC} = 2.5V, no RF			0.01	1	
		V_{CC} = 3.3V, no RF			0.05		
t_{ON}	Turn-on time	50% EN control to 90% P_O			1.4		μs
t_{OFF}	Turn-off time	50% EN control to 10% P_O			0.4		μs
POWER DOWN CONTROL LEVELS							
V_{IH}	High-level input voltage	Logic 1, V_{CC} = 1.8V to 3.3V		1.5			V
V_{IL}	Low-level input voltage	Logic 0, V_{CC} = 1.8V to 3.3V				0.4	V

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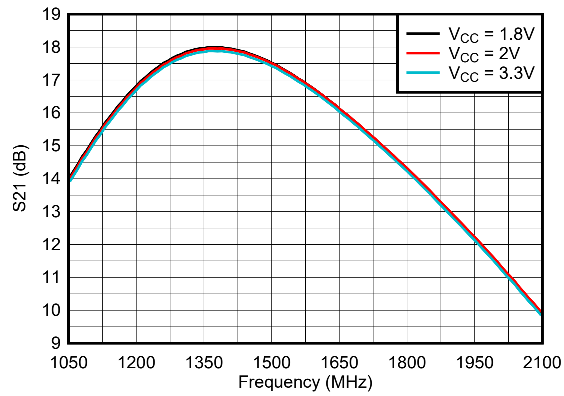
5.6 Electrical Characteristics - GPS L5 and L2 Bands

at T_A = 27°C, V_{CC} = 2.5V, f = 1176MHz (L5 band), source impedance (Z_S) = load impedance (Z_L) = 50Ω, and input matched to 50Ω with L1 = 11nH (0402DC-11NXGRW) and C1 = 10pF (GJM1555C1H100JB01) with input and output configuration as shown in Figure 6-2, de-embedded up to capacitor, C1, on input and RFOUT pin on the output (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
RF PERFORMANCE							
	Operating frequency			1165	1176	1320	MHz
G_P	Small-signal power gain	V_{CC} = 1.8V to 3.3V, P_{IN} = –27dBm			16.5		dB
NF	Noise figure	V_{CC} = 1.8V to 3.3V			0.8		dB
S_{11}	Input return loss	P_{IN} = –27dBm, V_{CC} = 1.8V to 3.3V			–12.9		dB
S_{22}	Output return loss	P_{IN} = –27dBm, V_{CC} = 1.8V to 3.3V			–9		dB
S_{12}	Reverse isolation	P_{IN} = –27dBm, V_{CC} = 1.8V to 3.3V			–43.6		dB
IP1dB	Input 1dB compression point	No jammer	V_{CC} = 1.8V		–13.4		dBm
			V_{CC} = 2V		–12		
			V_{CC} ≥ 2.5V		–10.6		
IIP3	In-band input third-order intercept point	P_{IN} = –25dBm/tone, 5MHz tone spacing	V_{CC} = 1.8V		–6.1		dBm
			V_{CC} ≥ 2V		–6		
K	Rollett stability factor			1			

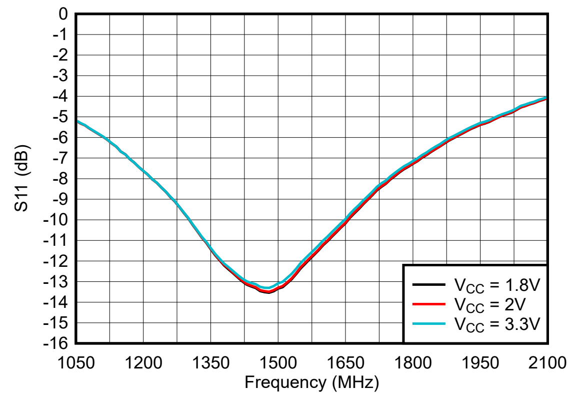
5.7 Typical Characteristics – GPS L1 Band

at T_A = 27°C, V_{CC} = 2.5V, f = 1575MHz (L1 band), source impedance (Z_S) = load impedance (Z_L) = 50Ω, input matched to 50Ω with L1 = 8.2nH (0402DC-8N2XGRW) and C1 = 10pF (GJM1555C1H100JB01) with input and output configuration as shown in Figure 6-2, de-embedded up to capacitor, C1, on input and RFOUT pin on the output, ambient temperatures shown (unless otherwise noted)



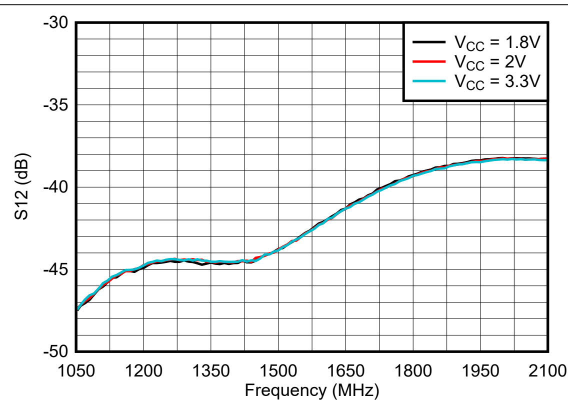
P_{IN} = –27dBm

Figure 5-1. Power Gain (S21) Across V_{CC}



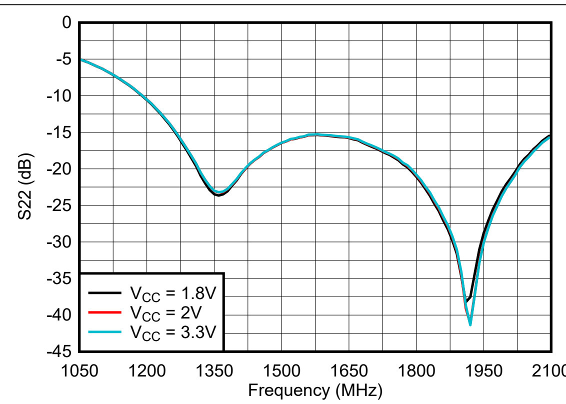
P_{IN} = –27dBm

Figure 5-2. Input Return Loss (S11) Across V_{CC}



P_{IN} = –27dBm

Figure 5-3. Reverse Isolation (S12) Across V_{CC}



P_{IN} = –27dBm

Figure 5-4. Output Return Loss (S22) Across V_{CC}

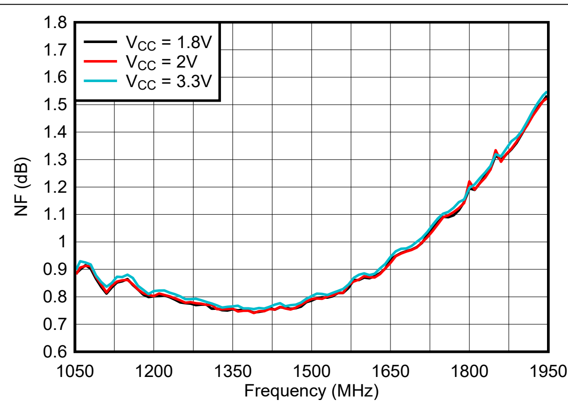


Figure 5-5. NF Across V_{CC}

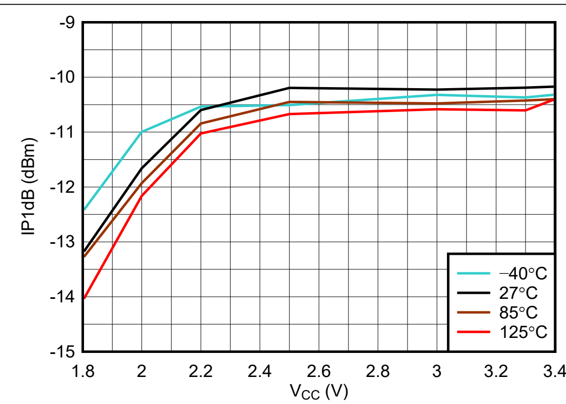


Figure 5-6. IP1dB vs V_{CC} Across Temperature

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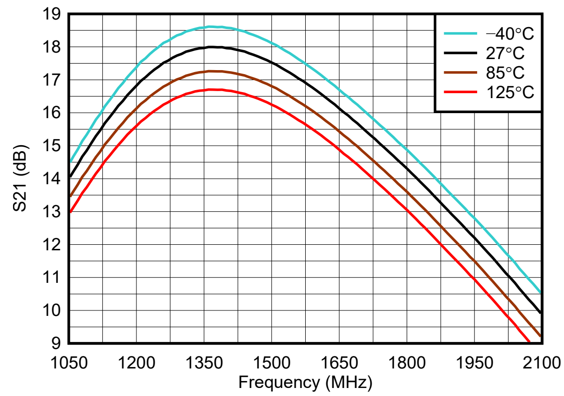
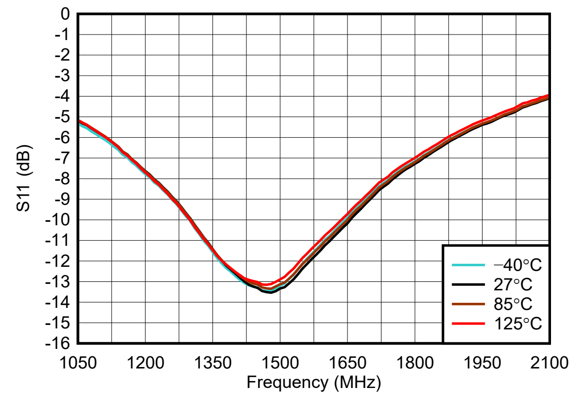
5.7 Typical Characteristics – GPS L1 Band (continued)

at T_A = 27°C, V_{CC} = 2.5V, f = 1575MHz (L1 band), source impedance (Z_S) = load impedance (Z_L) = 50Ω, input matched to 50Ω with L1 = 8.2nH (0402DC-8N2XGRW) and C1 = 10pF (GJM1555C1H100JB01) with input and output configuration as shown in Figure 6-2, de-embedded up to capacitor, C1, on input and RFOUT pin on the output, ambient temperatures shown (unless otherwise noted)



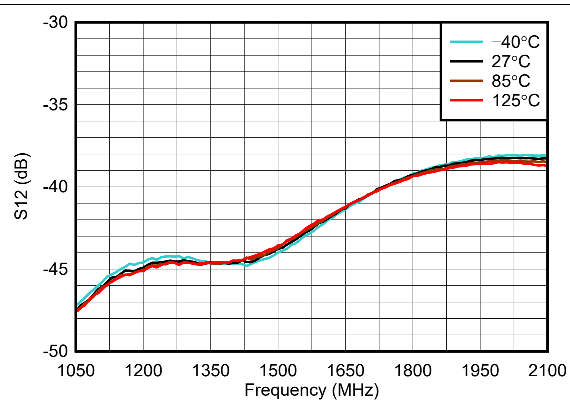
V_{CC} = 1.8V, P_{IN} = –27dBm

Figure 5-7. Power Gain (S21) Across Temperature



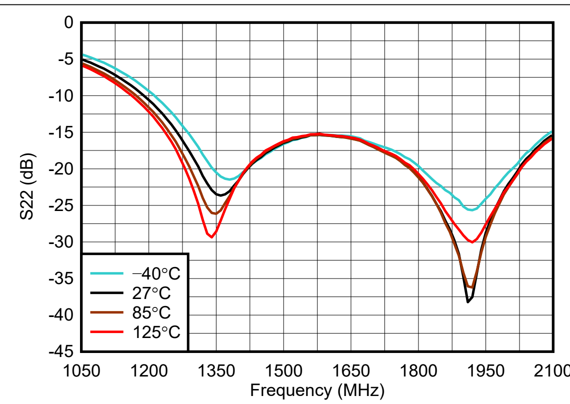
V_{CC} = 1.8V, P_{IN} = –27dBm

Figure 5-8. Input Return Loss (S11) Across Temperature



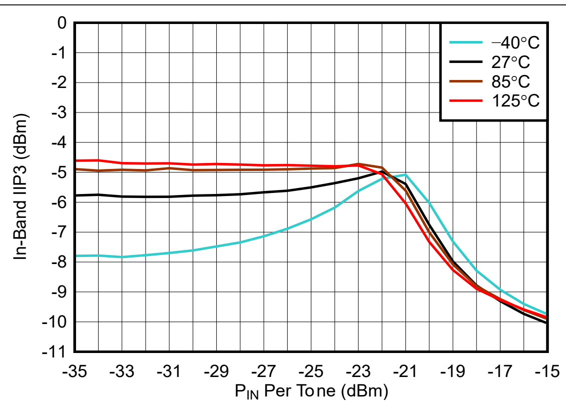
V_{CC} = 1.8V, P_{IN} = –27dBm

Figure 5-9. Reverse Isolation (S12) Across Temperature



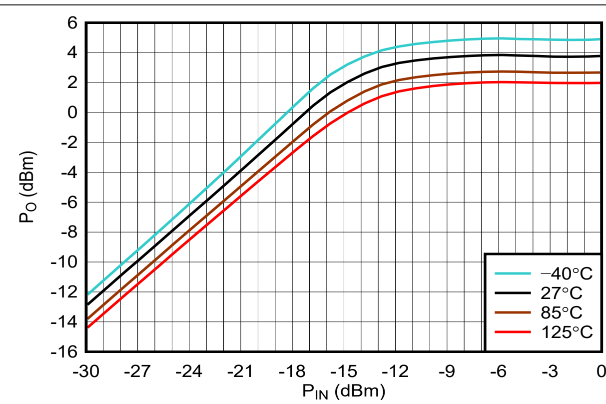
V_{CC} = 1.8V, P_{IN} = –27dBm

Figure 5-10. Output Return Loss (S22) Across Temperature



V_{CC} = 1.8V, 5MHz tone spacing

Figure 5-11. In-Band IIP3 vs Input Power (Pin) Across Temperature

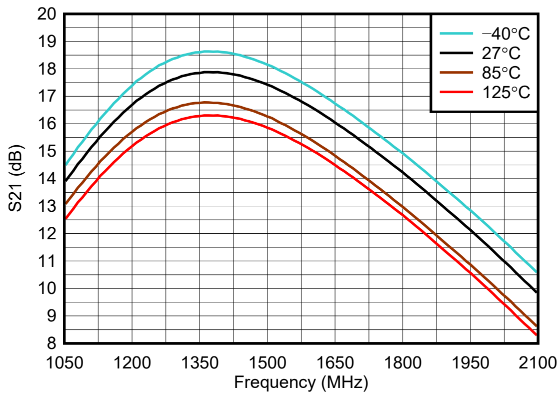


V_{CC} = 1.8V

Figure 5-12. Output Power (P_O) vs Input Power (P_{IN}) Across Temperature

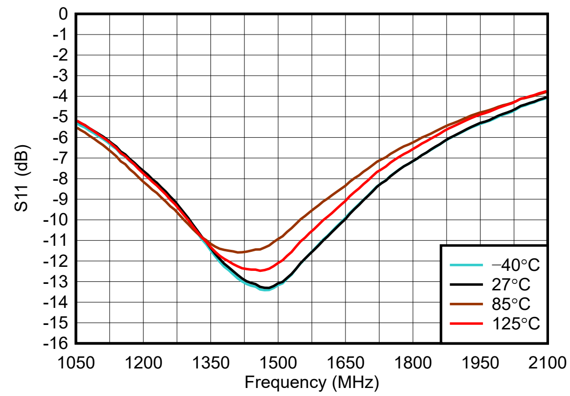
5.7 Typical Characteristics – GPS L1 Band (continued)

at T_A = 27°C, V_{CC} = 2.5V, f = 1575MHz (L1 band), source impedance (Z_S) = load impedance (Z_L) = 50Ω, input matched to 50Ω with L1 = 8.2nH (0402DC-8N2XGRW) and C1 = 10pF (GJM1555C1H100JB01) with input and output configuration as shown in Figure 6-2, de-embedded up to capacitor, C1, on input and RFOUT pin on the output, ambient temperatures shown (unless otherwise noted)



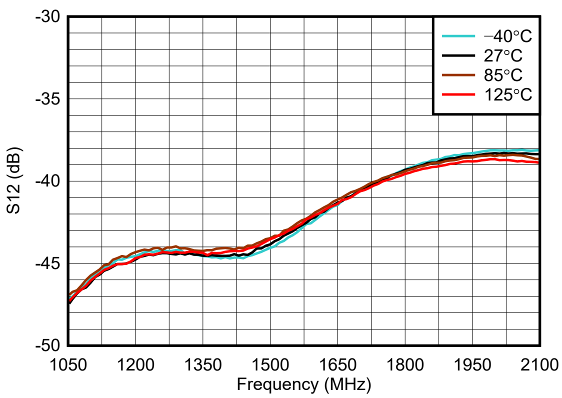
V_{CC} = 3.3V, P_{IN} = –27dBm

Figure 5-13. Power Gain (S21) Across Temperature



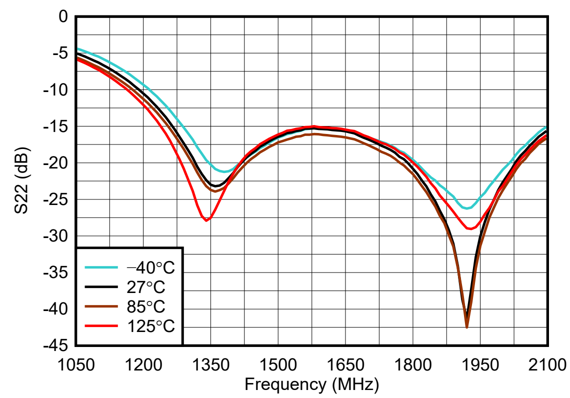
V_{CC} = 3.3V, P_{IN} = –27dBm

Figure 5-14. Input Return Loss (S11) Across Temperature



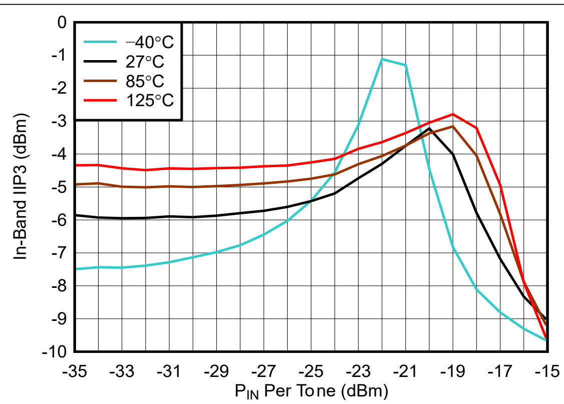
V_{CC} = 3.3V, P_{IN} = –27dBm

Figure 5-15. Reverse Isolation (S12) Across Temperature



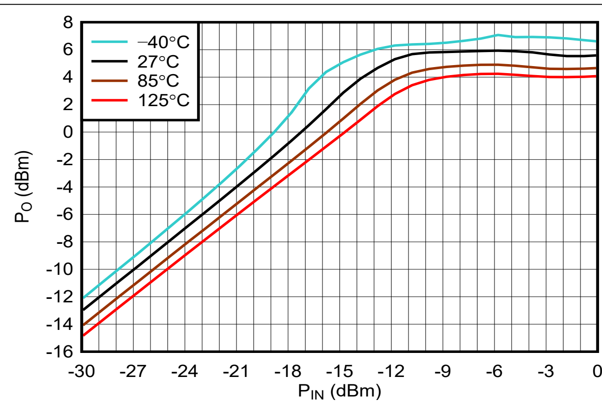
V_{CC} = 3.3V, P_{IN} = –27dBm

Figure 5-16. Output Return Loss (S22) Across Temperature



V_{CC} = 3.3V, 5MHz tone spacing

Figure 5-17. In-Band IIP3 vs Input Power (P_{IN}) Across Temperature



V_{CC} = 3.3V

Figure 5-18. Output Power (P_O) vs Input Power (P_{IN}) Across Temperature

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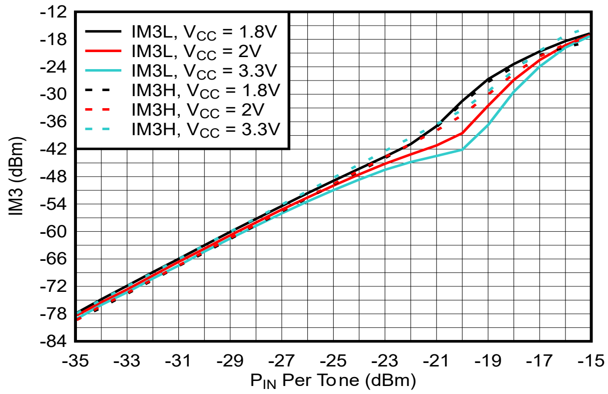
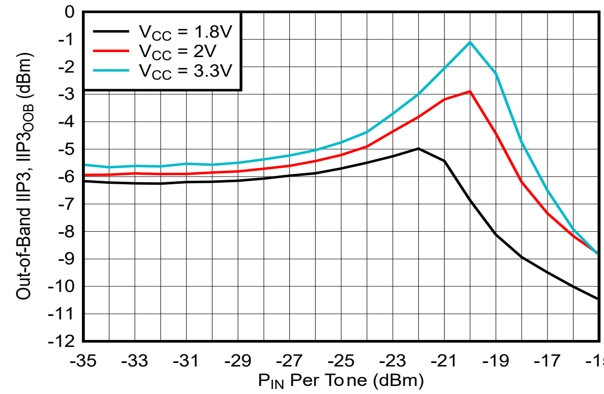
5.7 Typical Characteristics – GPS L1 Band (continued)

at T_A = 27°C, V_{CC} = 2.5V, f = 1575MHz (L1 band), source impedance (Z_S) = load impedance (Z_L) = 50Ω, input matched to 50Ω with L1 = 8.2nH (0402DC-8N2XGRW) and C1 = 10pF (GJM1555C1H100JB01) with input and output configuration as shown in Figure 6-2, de-embedded up to capacitor, C1, on input and RFOUT pin on the output, ambient temperatures shown (unless otherwise noted)



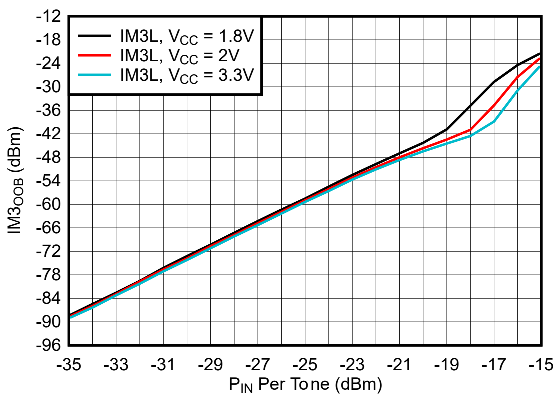
5MHz tone spacing

Figure 5-19. In-Band IM3 vs Input Power (P_{IN}) Across V_{CC}



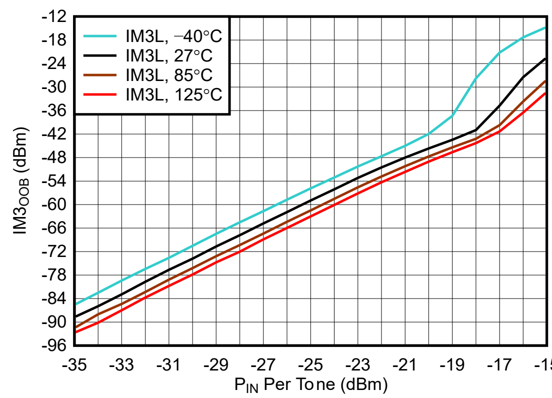
f1 = 1713MHz, f2 = 1851MHz

Figure 5-20. Out-of-Band IIP3 vs Input Power (P_{IN}) Across V_{CC}



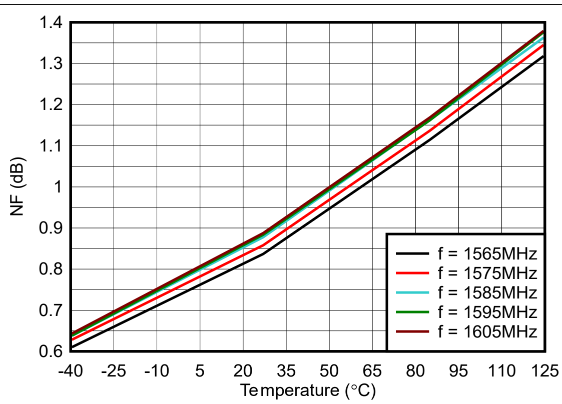
f1 = 1713MHz, f2 = 1851MHz

Figure 5-21. Out-of-Band IM3 vs Input Power (P_{IN}) Across V_{CC}



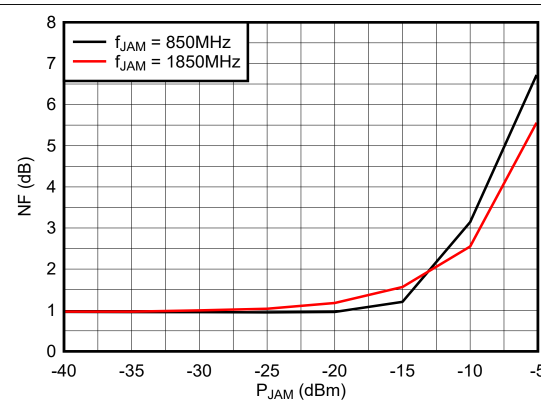
V_{CC} = 2V, f1 = 1713MHz, f2 = 1851MHz

Figure 5-22. Out-of-Band IM3 vs Input Power (P_{IN}) Across Temperature



V_{CC} = 2V

Figure 5-23. NF vs Temperature Across Frequency

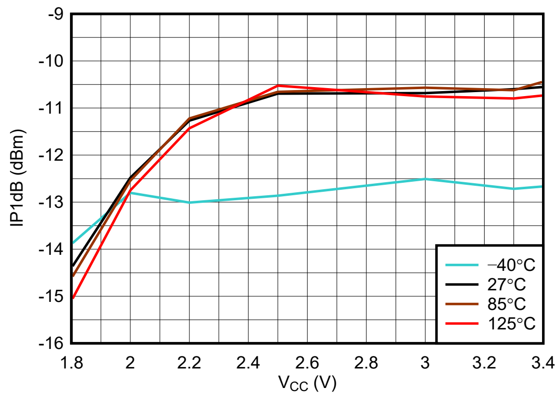


V_{CC} = 3.3V

Figure 5-24. NF vs Jammer Power (P_{JAM}) Across Jammer Frequency (f_{JAM})

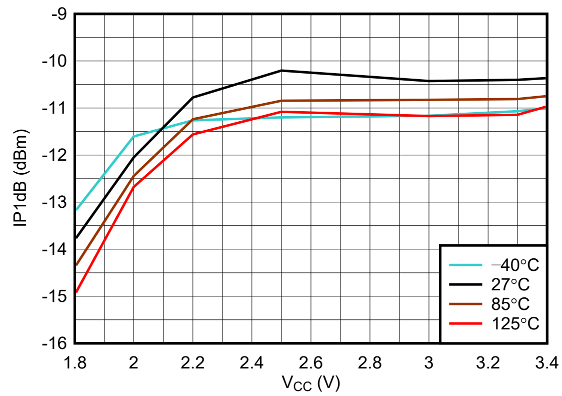
5.7 Typical Characteristics – GPS L1 Band (continued)

at T_A = 27°C, V_{CC} = 2.5V, f = 1575MHz (L1 band), source impedance (Z_S) = load impedance (Z_L) = 50Ω, input matched to 50Ω with L1 = 8.2nH (0402DC-8N2XGRW) and C1 = 10pF (GJM1555C1H100JB01) with input and output configuration as shown in Figure 6-2, de-embedded up to capacitor, C1, on input and RFOUT pin on the output, ambient temperatures shown (unless otherwise noted)



f_{JAM} = 850MHz, P_{JAM} = –20dBm

Figure 5-25. IP1dB vs V_{CC} Across Temperature With Jammer



f_{JAM} = 1850MHz, P_{JAM} = –20dBm

Figure 5-26. IP1dB vs V_{CC} Across Temperature With Jammer

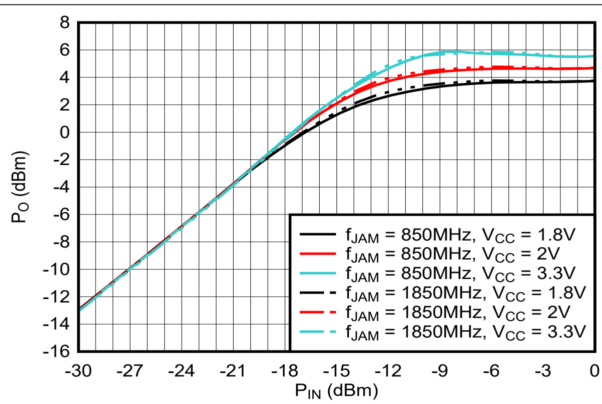
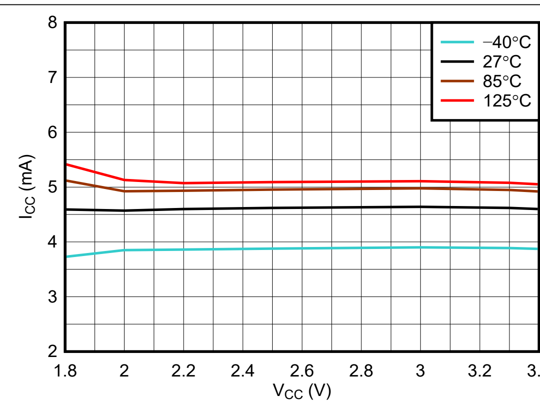


Figure 5-27. Output Power (P_O) vs Input Power (P_{IN}) Across Jammer and V_{CC}



P_{IN} = –35dBm

Figure 5-28. I_{CC} vs V_{CC} Across Temperature

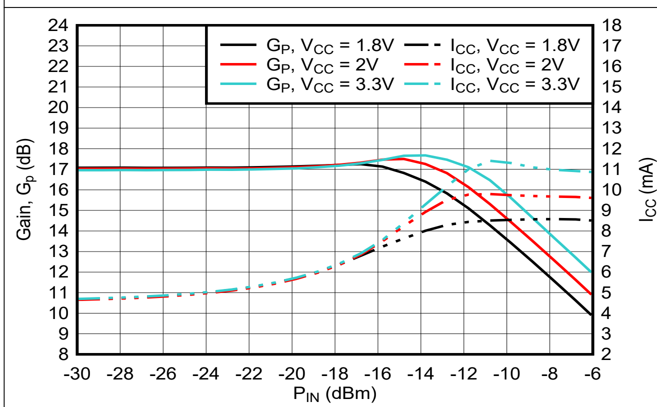
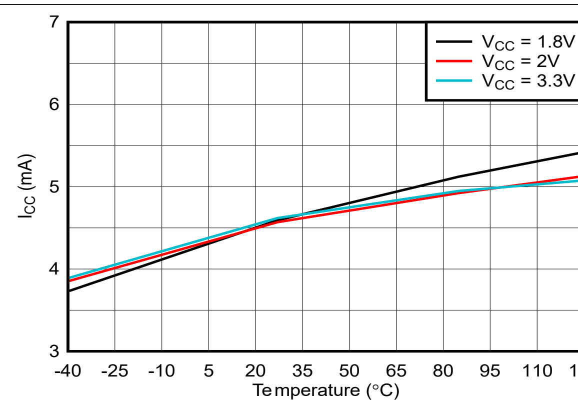


Figure 5-29. Gain and I_{CC} vs P_{IN} Across V_{CC}



P_{IN} = –35dBm

Figure 5-30. I_{CC} vs Temperature Across V_{CC}

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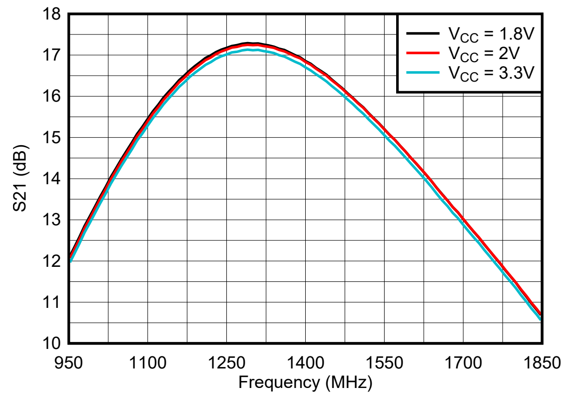
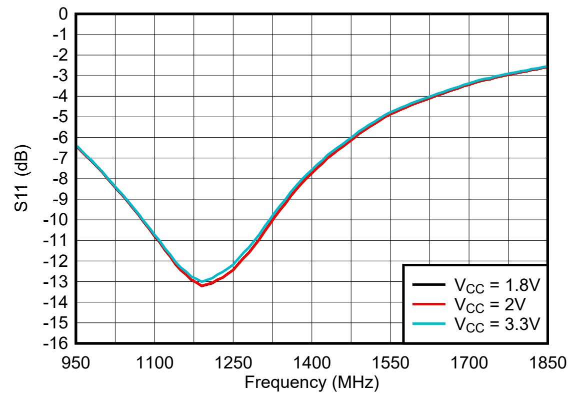
5.8 Typical Characteristics – GPS L5 and L2 Bands

at T_A = 27°C, V_{CC} = 2.5V, f = 1176MHz (L5 band), source impedance (Z_S) = load impedance (Z_L) = 50Ω, input matched to 50Ω with L1 = 11nH (0402DC-11NXGRW) and C1 = 10pF (GJM1555C1H100JB01) with input and output configuration as shown in Figure 6-2, de-embedded up to capacitor, C1, on input and RFOUT pin on the output, ambient temperatures shown (unless otherwise noted)



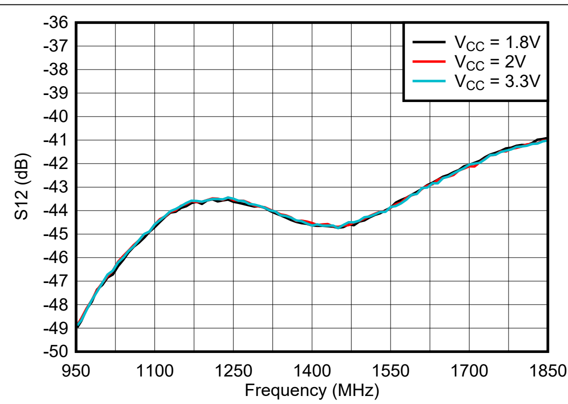
P_{IN} = –27dBm

Figure 5-31. Power Gain (S21) Across V_{CC}



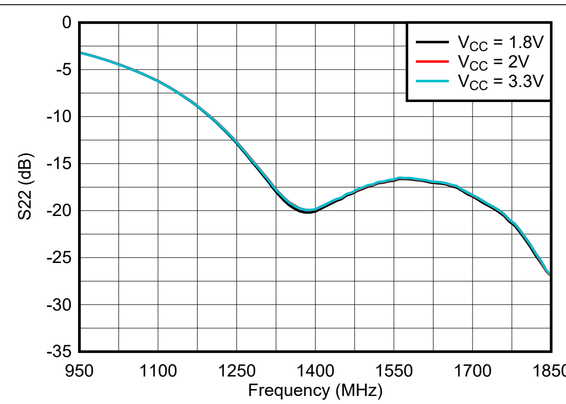
P_{IN} = –27dBm

Figure 5-32. Input Return Loss (S11) Across V_{CC}



P_{IN} = –27dBm

Figure 5-33. Reverse Isolation (S12) Across V_{CC}



P_{IN} = –27dBm

Figure 5-34. Output Return Loss (S22) Across V_{CC}

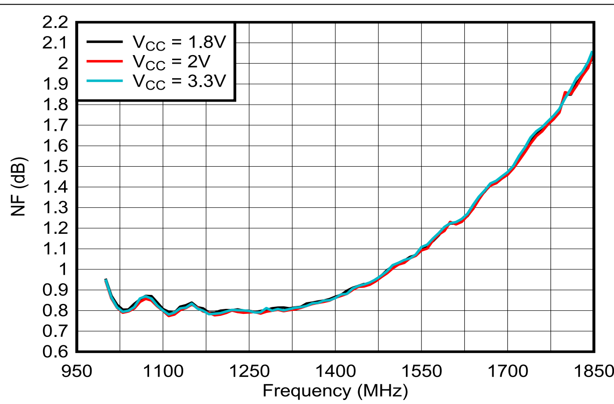


Figure 5-35. NF Across V_{CC}

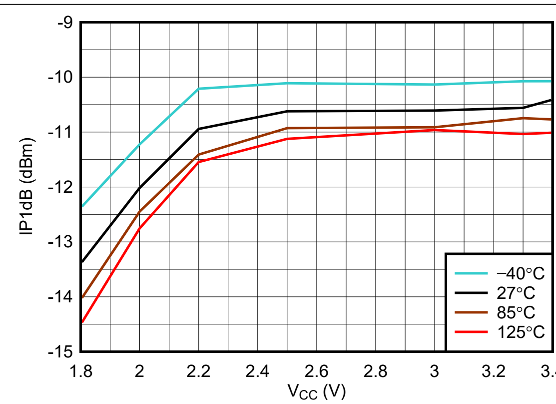


Figure 5-36. IP1dB vs V_{CC} Across Temperature

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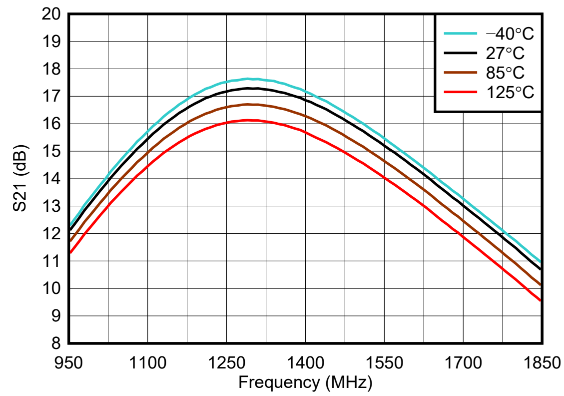
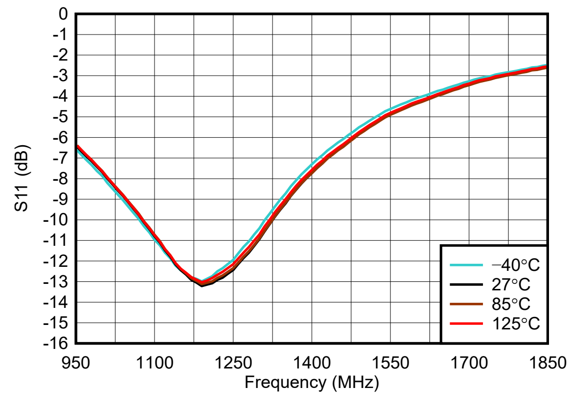
5.8 Typical Characteristics – GPS L5 and L2 Bands (continued)

at T_A = 27°C, V_{CC} = 2.5V, f = 1176MHz (L5 band), source impedance (Z_S) = load impedance (Z_L) = 50Ω, input matched to 50Ω with L1 = 11nH (0402DC-11NXGRW) and C1 = 10pF (GJM1555C1H100JB01) with input and output configuration as shown in Figure 6-2, de-embedded up to capacitor, C1, on input and RFOUT pin on the output, ambient temperatures shown (unless otherwise noted)



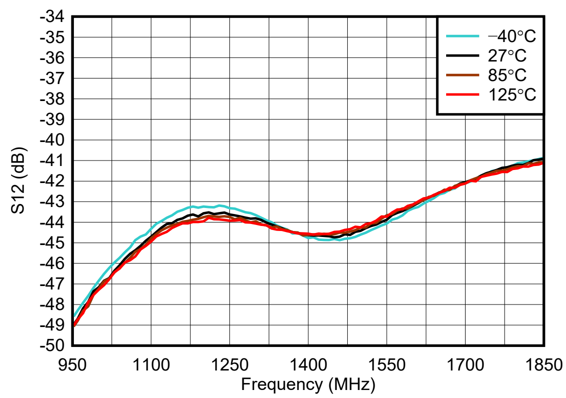
V_{CC} = 1.8V, P_{IN} = –27dBm

Figure 5-37. Power Gain (S21) Across Temperature



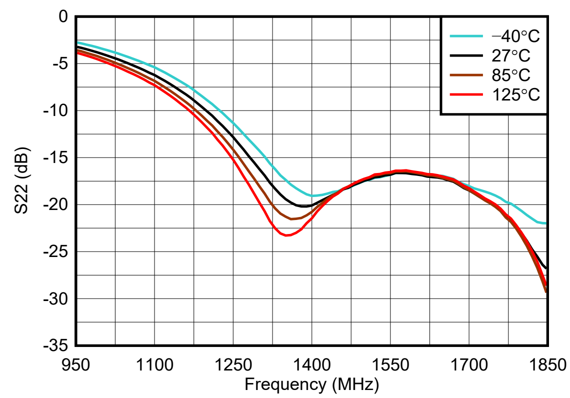
V_{CC} = 1.8V, P_{IN} = –27dBm

Figure 5-38. Input Return Loss (S11) Across Temperature



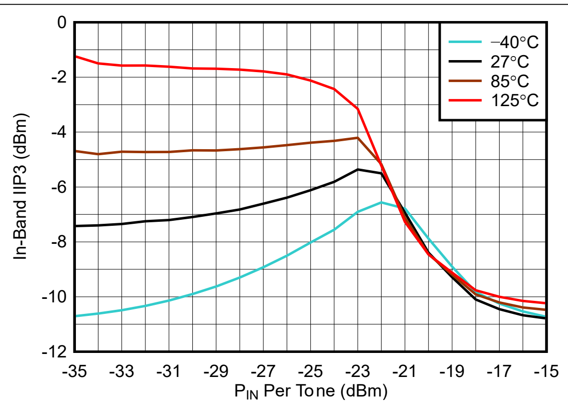
V_{CC} = 1.8V, P_{IN} = –27dBm

Figure 5-39. Reverse Isolation (S12) Across Temperature



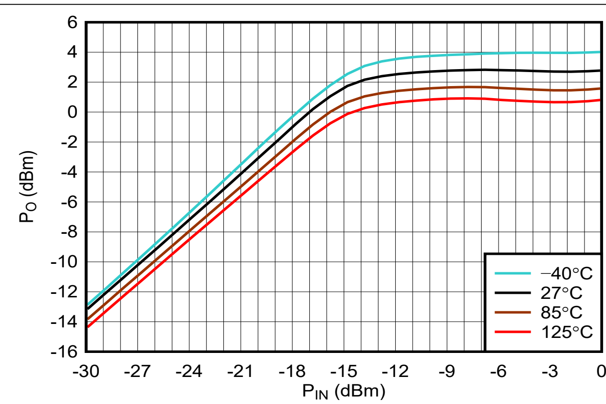
V_{CC} = 1.8V, P_{IN} = –27dBm

Figure 5-40. Output Return Loss (S22) Across Temperature



V_{CC} = 1.8V, 5MHz tone spacing

Figure 5-41. In-Band IIP3 vs Input Power (P_{IN}) Across Temperature



V_{CC} = 1.8V

Figure 5-42. Output Power (P_O) vs Input Power (P_{IN}) Across Temperature

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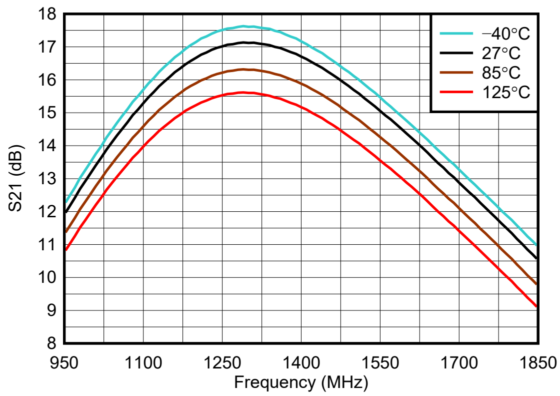
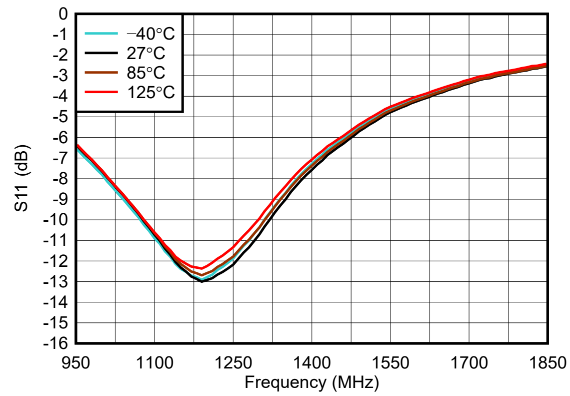
5.8 Typical Characteristics – GPS L5 and L2 Bands (continued)

at T_A = 27°C, V_{CC} = 2.5V, f = 1176MHz (L5 band), source impedance (Z_S) = load impedance (Z_L) = 50Ω, input matched to 50Ω with L1 = 11nH (0402DC-11NXGRW) and C1 = 10pF (GJM1555C1H100JB01) with input and output configuration as shown in Figure 6-2, de-embedded up to capacitor, C1, on input and RFOUT pin on the output, ambient temperatures shown (unless otherwise noted)



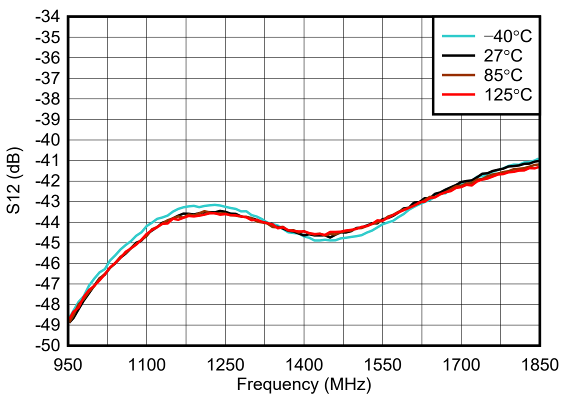
V_{CC} = 3.3V, P_{IN} = –27dBm

Figure 5-43. Power Gain (S21) Across Temperature



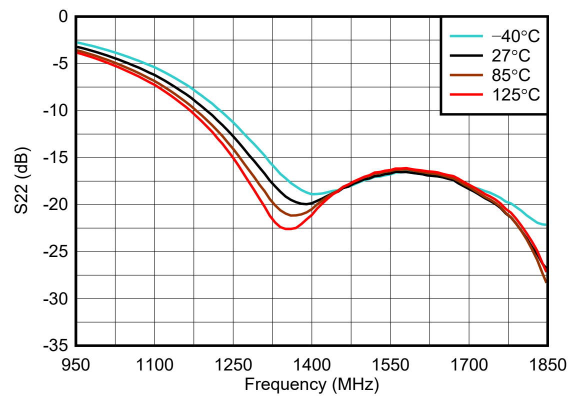
V_{CC} = 3.3V, P_{IN} = –27dBm

Figure 5-44. Input Return Loss (S11) Across Temperature



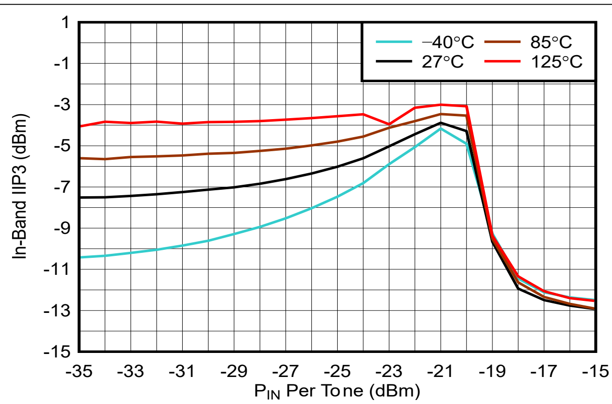
V_{CC} = 3.3V, P_{IN} = –27dBm

Figure 5-45. Reverse Isolation (S12) Across Temperature



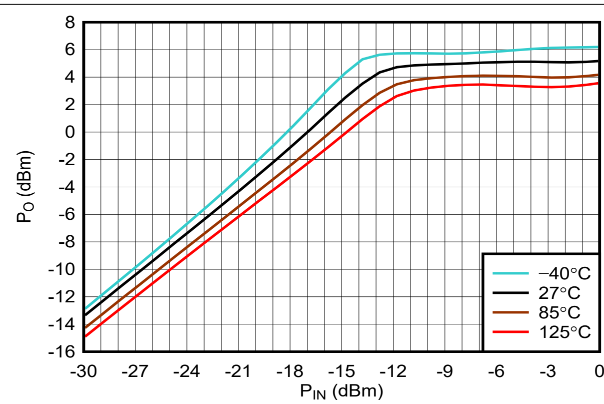
V_{CC} = 3.3V, P_{IN} = –27dBm

Figure 5-46. Output Return Loss (S22) Across Temperature



V_{CC} = 3.3V, 5MHz tone spacing

Figure 5-47. In-Band IIP3 vs Input Power (P_{IN}) Across Temperature



V_{CC} = 3.3V

Figure 5-48. Output Power (P_O) vs Input Power (P_{IN}) Across Temperature

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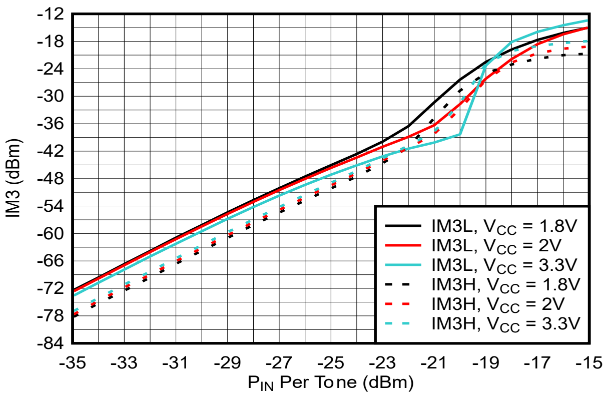
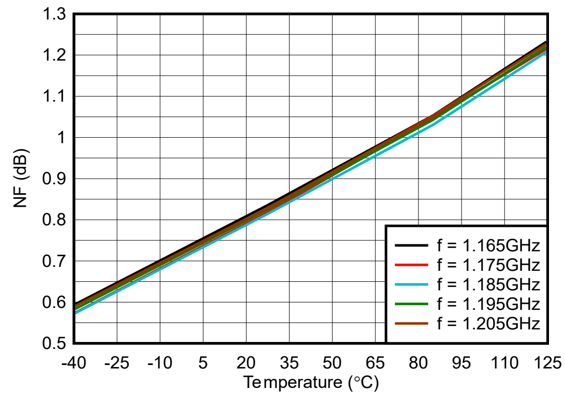
5.8 Typical Characteristics – GPS L5 and L2 Bands (continued)

at T_A = 27°C, V_{CC} = 2.5V, f = 1176MHz (L5 band), source impedance (Z_S) = load impedance (Z_L) = 50Ω, input matched to 50Ω with L1 = 11nH (0402DC-11NXGRW) and C1 = 10pF (GJM1555C1H100JB01) with input and output configuration as shown in Figure 6-2, de-embedded up to capacitor, C1, on input and RFOUT pin on the output, ambient temperatures shown (unless otherwise noted)



5MHz tone spacing

Figure 5-49. In-Band IM3 vs Input Power (P_{IN}) Across V_{CC}



V_{CC} = 2V

Figure 5-50. NF vs Temperature Across Frequency

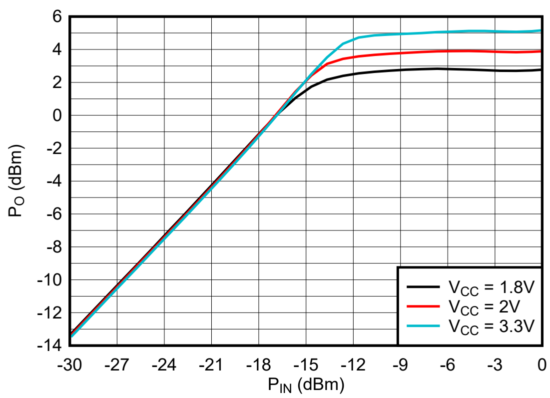


Figure 5-51. Output Power (P_O) vs Input Power (P_{IN}) Across V_{CC}

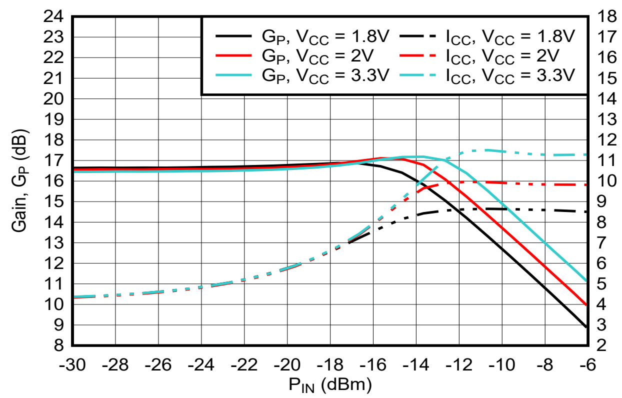


Figure 5-52. Gain and I_{CC} vs P_{IN} Across V_{CC}

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6 Detailed Description

6.1 Overview

The TRF3302-Q1 is a GNSS/GPS LNA designed to improve GNSS signal sensitivity for GNSS/GPS receivers and supports a wide array of satellite constellations that provide global positioning, navigation, and timing services. The device features an enable pin (EN) that is used to put the device in a power-saving shutdown mode. This feature eliminates the need for an external supply disconnect switch or bringing down the entire V_{CC} supply.

Operating on a single 1.8V to 3.3V supply and consuming a typical supply current of 4.6mA, the device achieves –10.2dBm IP1dB. The device is available in a space-saving 1.3mm × 1mm, 6-pin, WSON-FCRLF package with wettable flanks.

6.2 Functional Block Diagram

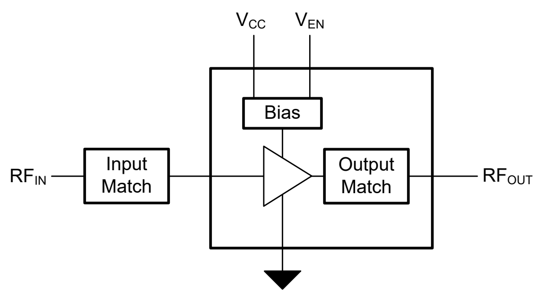

Figure 6-1. TRF3302-Q1 Functional Block Diagram

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6.3 Feature Description

The TRF3302-Q1 is a versatile LNA that is configurable to optimize performance for a single GNSS band matching for either the upper or lower L-band frequencies, or configurable for a wide frequency coverage across multiple GNSS bands from 1165MHz to 1630MHz.

The TRF3302-Q1 features an integrated wideband output match, eliminating external matching components to interface with GNSS receivers, thus reducing BOM count and design size. The required off-chip input match allows flexibility to optimize device performance to the system-specific requirements. A two-element match (see Figure 6-2) suffices for single GNSS band operation. A four-element match (see Figure 6-3) allows wide multiband matching to optimize performance across NF, gain, and S11.

The 6-pin WSON-FCRLF package has wettable flanks that allows visual inspection of solder joints by automatic optical inspection (AOI), thus improving product reliability without the added manufacturing cost of expensive X-ray inspection systems. The TRF3302-Q1 pinout (see Figure 4-1) is optimized for PCB layout and RF performance by having RF ground pins (VCC and GND) around the RFIN pin, and EN and GND around the RFOUT pin.

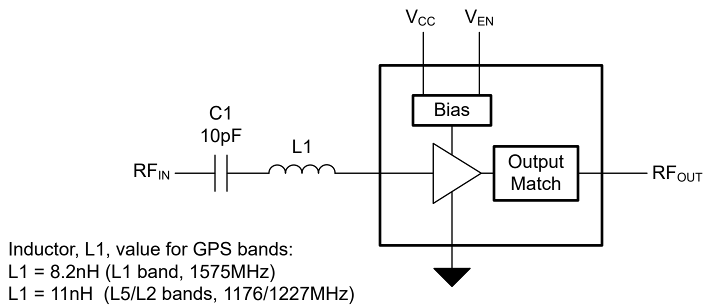

Figure 6-2. TRF3302-Q1 Typical Single-GNSS-Band Configuration

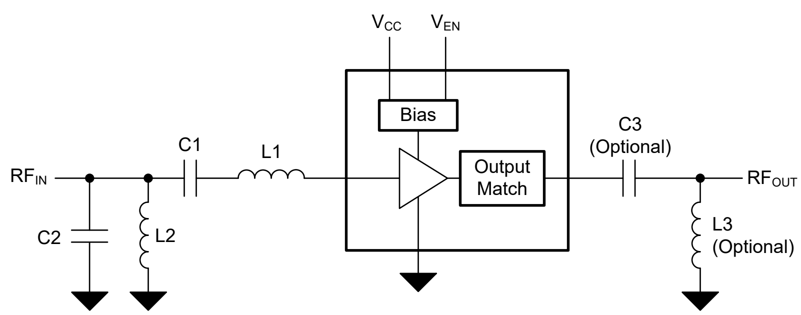

Figure 6-3. TRF3302-Q1 Typical Multi-GNSS-Band Configuration

6.4 Device Functional Modes

The TRF3302-Q1 features an EN pin which must be forced high (logic 1) to enable the device. To power down the device, connect the EN pin to ground potential (logic 0). EN pin cannot be floated and a voltage must be forced for proper device operation.

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TRF3302-Q1 is a single-ended input and output LNA. The device is typically used in GNSS global positioning systems to improve the sensitivity of the GNSS receivers. This improvement comes by virtue of the 0.8dB NF of the device combined with ≈17dB of gain for upper or lower L-band GNSS systems. In systems where the receive antenna is far from the GNSS receiver and connected by a cable or a long trace, the TRF3302-Q1 helps improve the signal immunity to noise pickup by amplifying the signal before the signal reaches the GNSS receiver while adding minimal amplifier noise. For systems that need to simultaneously support upper and lower L-bands, a broadband input matching network is used with the TRF3302-Q1 (see Section 7.2.1).

7.2 Typical Application

7.2.1 The TRF3302-Q1 in a Multiband Configuration

Figure 7-1 shows a typical application of the TRF3302-Q1 in a multiband configuration, simultaneously covering upper and lower GNSS L-bands driving an AFE.

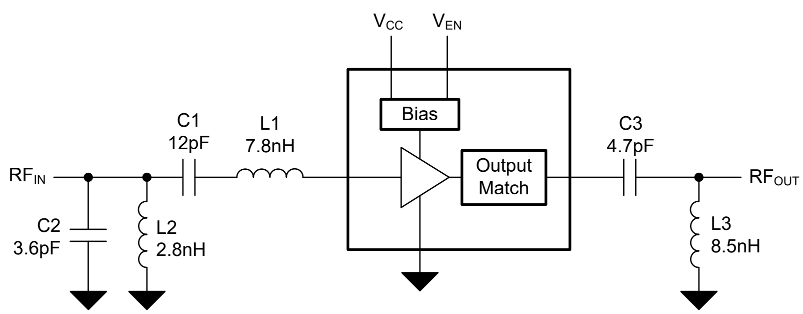


Figure 7-1. TRF3302-Q1 in Configuration Covering L1, L2, and L5 GPS Bands

7.2.1.1 Design Requirements

Key design requirements for a multiband receive applications is to optimize NF, gain, and S11 to the frequency range of interest. Choose the input matching network for the Figure 6-3 to support a frequency range of 1165MHz to ≈1630MHz that covers all the major upper and lower GNSS L-bands. The S22 of TRF3302-Q1 is inherently wideband and less than –10dB from 1200MHz to beyond 1630MHz. Choose an optional output match to achieve an output return loss (S22) of less than –10dB in the entire frequency range of interest from 1165MHz to 1630MHz.

7.2.1.2 Detailed Design Procedure

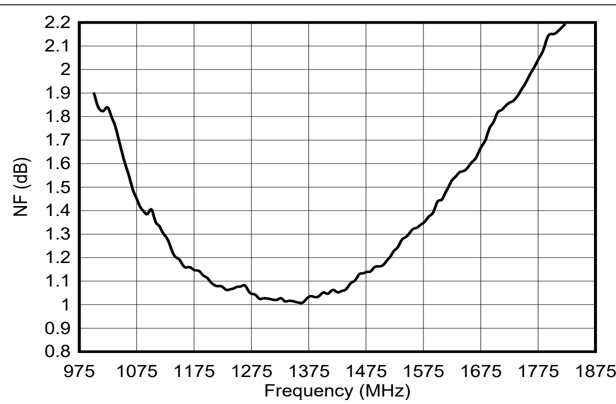
Table 7-1 shows the matching network components chosen for the design requirements. The S-parameters of the TRF3302-Q1 are used to obtain component values optimized for gain, S11, and S22 responses, and verified on the bench using the TRF3302-Q1 EVM.

Table 7-1. Matching Network Component Values

COMPONENT	COMPONENT VALUE	PART NUMBER
Inductor, L1	7.8nH	0402DC-7N8
Capacitor, C1	12pF	GJM1555C1H120JB01
Inductor, L2	2.8nH	0402DC-2N8
Capacitor, C2	3.6pF	GJM1555C1H3R6BB01
Inductor, L3	8.5nH	0402DC-8N5
Capacitor, C3	4.7pF	GJM1555C1H4R7BB01

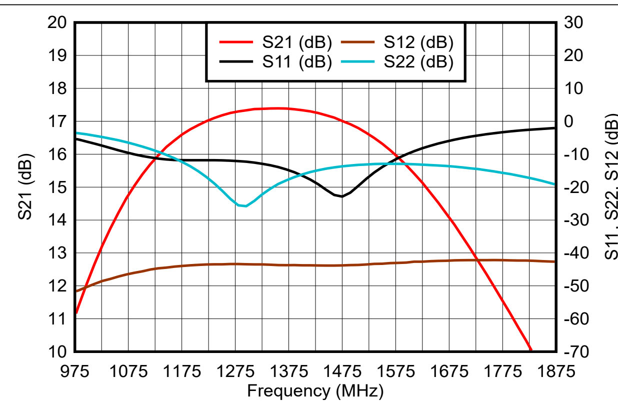
7.2.1.3 Application Curves

Figure 7-2 and Figure 7-3 show the NF and s-parameter response, respectively, of the multiband design.



V_{CC} = 3.3V

Figure 7-2. Noise Figure (NF) of the Multiband Design



V_{CC} = 3.3V, P_{IN} = –20dBm

Figure 7-3. S-Parameters of the Multiband Design

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7.3 Power Supply Recommendations

The TRF3302-Q1 operates on a 1.8V to 3.3V single-supply voltage. Isolate the supply voltage through decoupling capacitors placed close to the device. Select capacitors with self-resonant frequency greater than the application frequency. When multiple capacitors are used in parallel to create a broadband decoupling network, place the capacitor with the higher self-resonant frequency closer to the device.

7.4 Layout

7.4.1 Layout Guidelines

Figure 7-4 shows a good layout example for TRF3302-Q1. Only the top signal layer is shown. When designing with relatively wideband RF LNAs that have high gain, take certain board layout precautions to maintain stability and optimized performance. Use a multilayer board to maintain signal integrity and power integrity.

- Place all the input and output matching components as close to the RF pins as possible, and especially the high Q input matching inductor.
- Route the RF input and output signals as grounded coplanar waveguide (GCPW) traces.
- Maintain that the ground planes on the top and any internal layers are well stitched with vias, and the second layer of the PCB has a continuous ground layer without any cutouts in the vicinity of the LNA.
- Avoid routing clocks and digital control lines near RF signal lines.
- Do not route RF or DC signal lines over noisy power planes.
- Place supply decoupling caps close to the device.

See the *TRF3302-Q1 Evaluation Module user's guide* for more details on board layout and design.

7.4.2 Layout Example

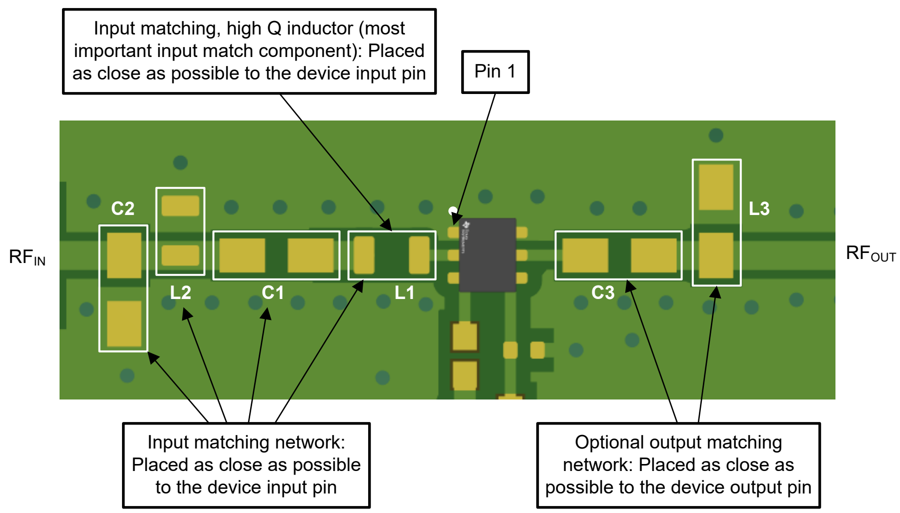

Figure 7-4. Layout Example

8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
October 2025	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TRF3302VBLRQ1	Active	Production	WSON-FCRLF (VBL) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	Q30

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TRF3302-Q1 :

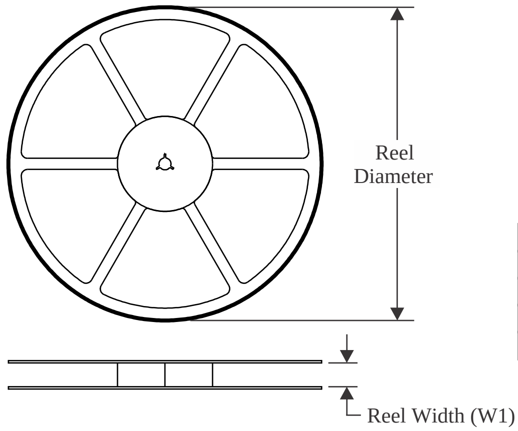
- Catalog : TRF3302

NOTE: Qualified Version Definitions:

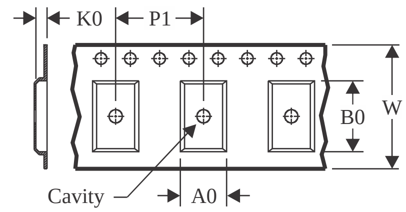
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

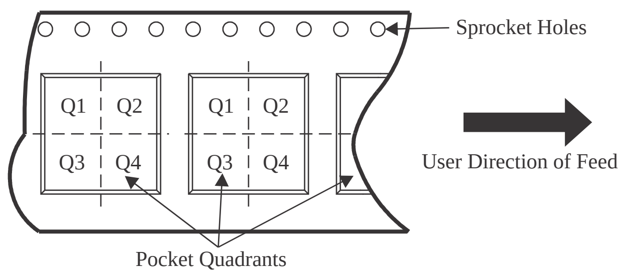


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

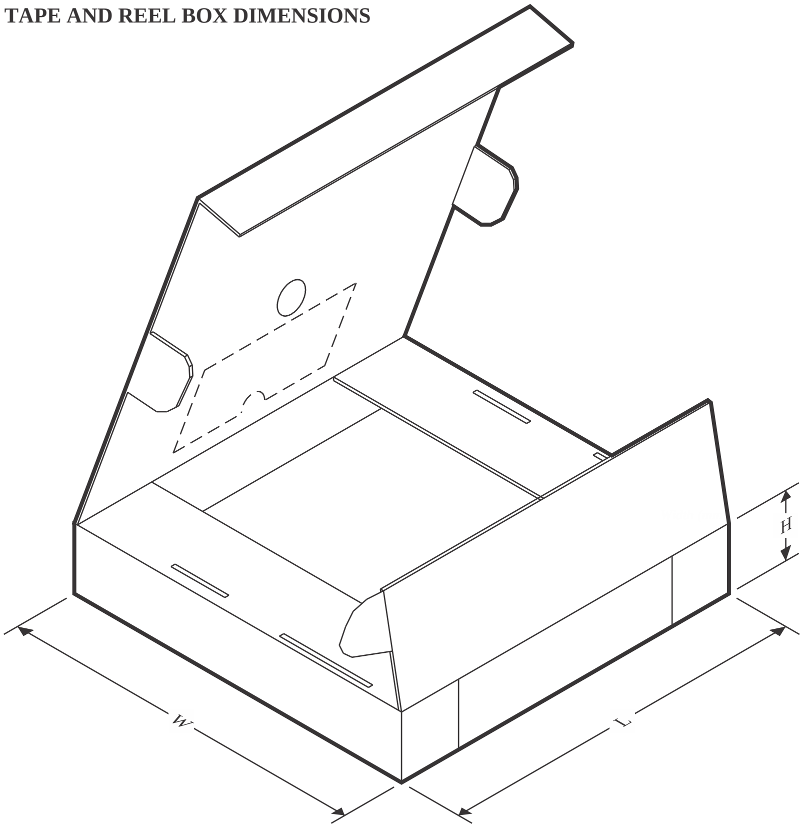
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

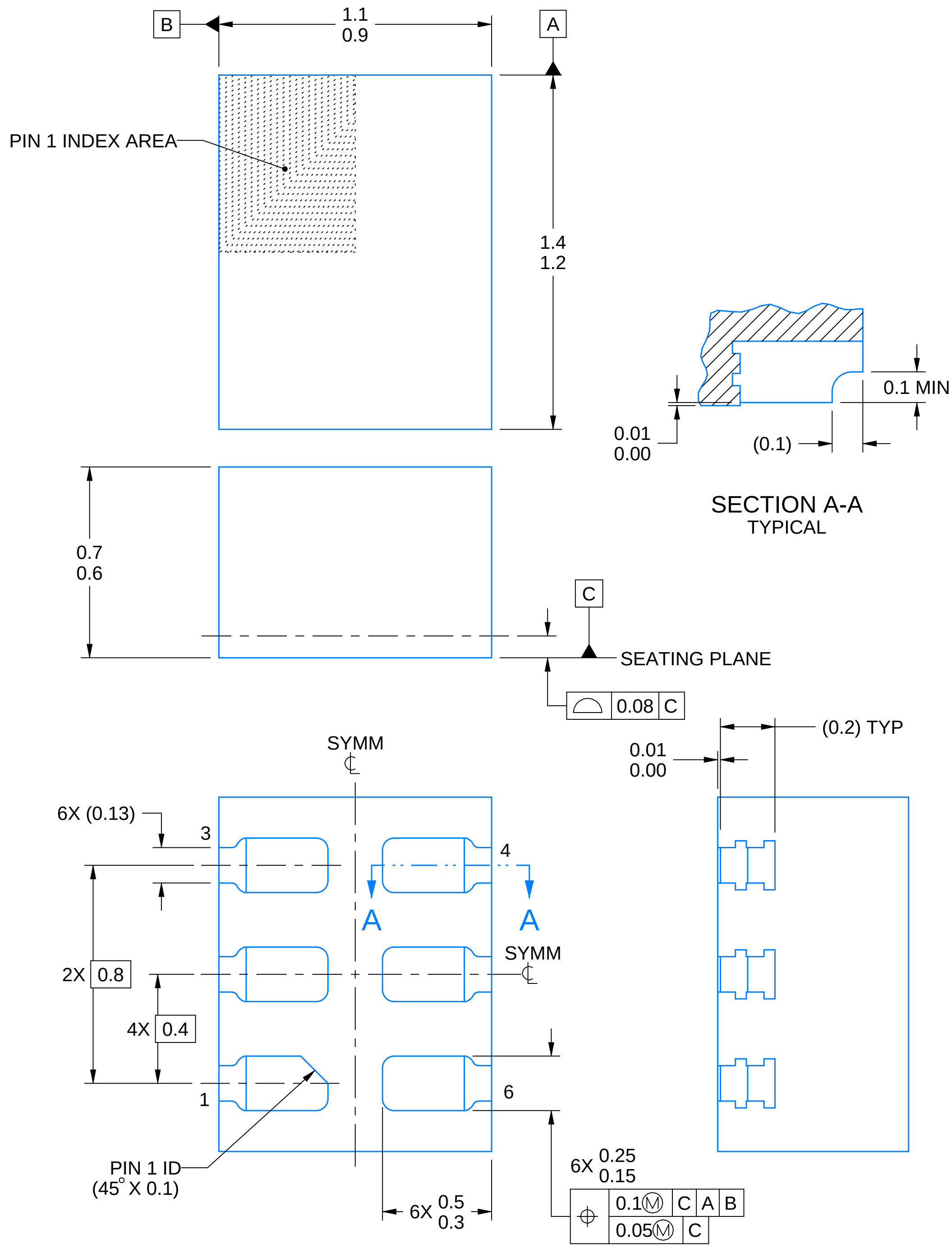
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRF3302VBLRQ1	WSON-FCRLF	VBL	6	3000	180.0	8.4	1.2	1.55	0.78	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



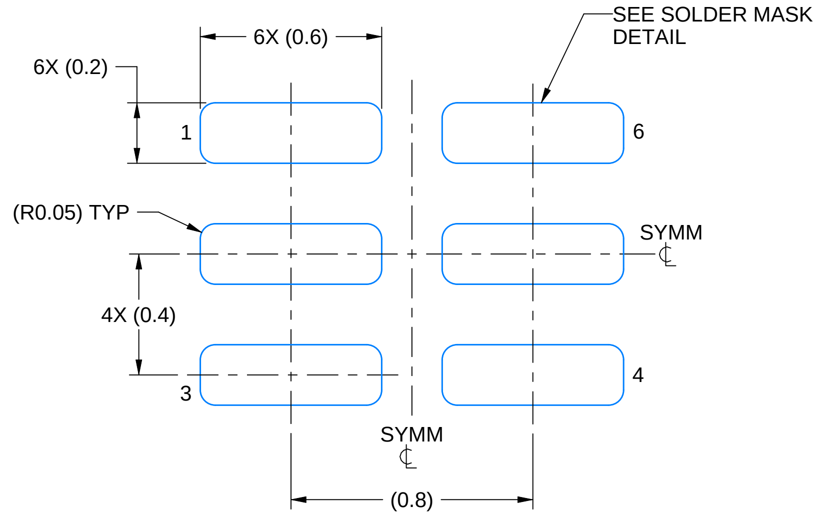
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRF3302VBLRQ1	WSON-FCRLF	VBL	6	3000	210.0	185.0	35.0

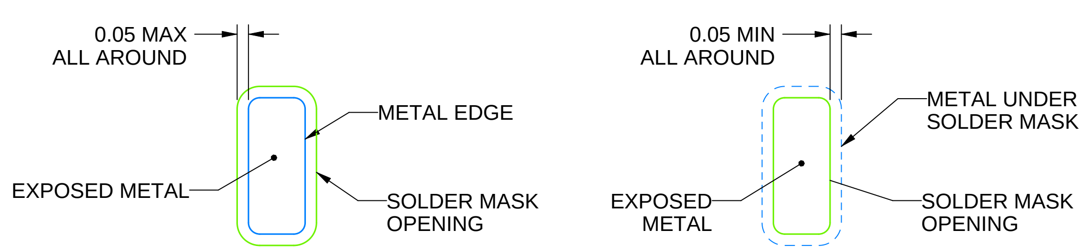


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 40X



NON SOLDER MASK DEFINED (PREFERRED)

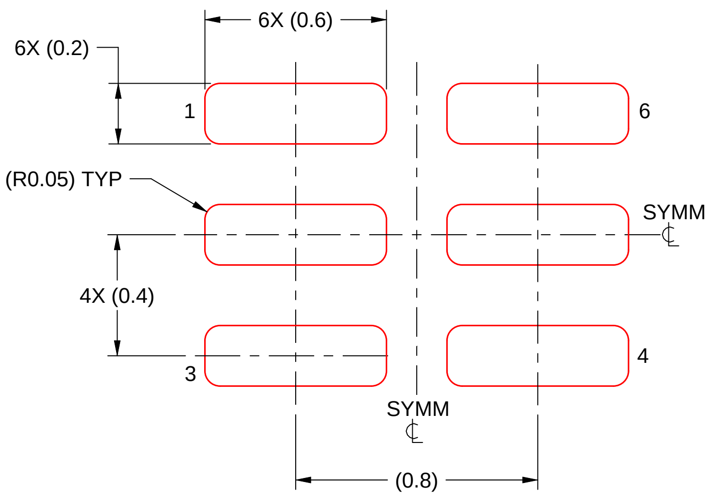
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4230092/B 01/2025

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 MM THICK STENCIL
SCALE: 40X

4230092/B 01/2025

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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