

## TRS202 5-V Dual RS-232 Line Driver and Receiver With $\pm 15$ -kV ESD Protection

### 1 Features

- ESD Protection for RS-232 Bus Pins:
  - $\pm 15$ -kV Human-Body Model (HBM)
- Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU v.28 Standards
- Operates at 5-V  $V_{CC}$  Supply
- Operates up to 120 kbit/s
- External Capacitors:  $4 \times 0.1 \mu\text{F}$
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

### 2 Applications

- Battery-Powered Systems
- Notebooks
- Set Top Boxes
- Palmtop PCs
- Hand-Held Equipment

### 3 Description

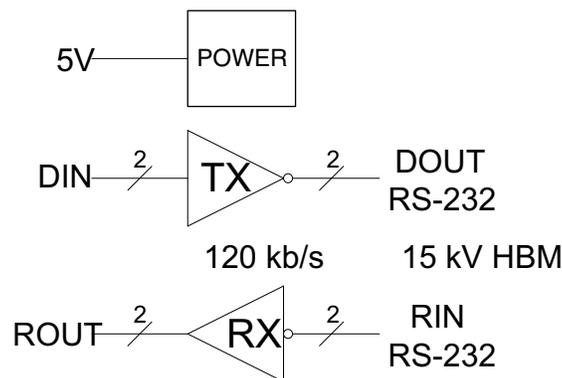
The TRS202 device consists of two line drivers, two line receivers, and a dual charge-pump circuit with  $\pm 15$ -kV ESD protection pin-to-pin (serial-port connection pins, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 5-V supply. The device operates at data signaling rates up to 120 kbit/s and a maximum of  $30\text{-V}/\mu\text{s}$  driver output slew rate.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TRS202ID	SOIC (16)	9.90 mm x 3.91 mm
TRS202IPW	TSSOP (16)	5.00 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Block Diagram



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## 4 Revision History

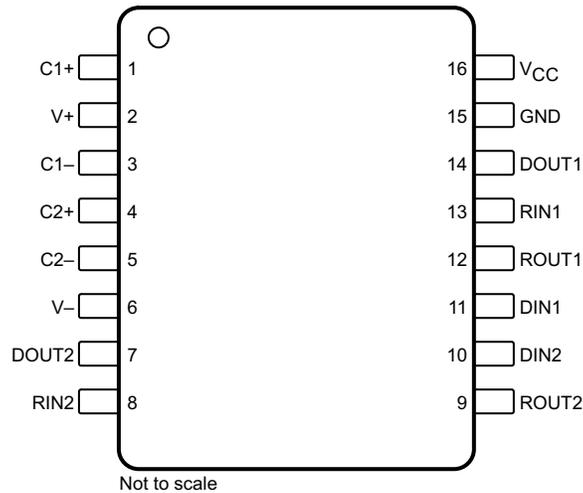
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from Original (July 2007) to Revision A

Page

• Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	<b>1</b>
• Deleted <i>Ordering Information</i> table; see <i>Package Option Addendum</i> at the end of the data sheet .....	<b>1</b>
• Changed Junction-to-ambient, $R_{\theta JA}$ , values in <i>Thermal Information</i> table From: 73°C/W To: 76.2°C/W (D) and From: 108°C/W To: 101°C/W (PW) .....	<b>5</b>
• Deleted $R_{\theta JA}$ values for DW and N packages .....	<b>5</b>

## 5 Pin Configuration and Functions



**Pin Functions**

PIN		I/O	DESCRIPTION
NO.	NAME		
1	C1+	—	Positive lead of C1 capacitor
2	V+	O	Positive charge pump output for storage capacitor only
3	C1-	—	Negative lead of C1 capacitor
4	C2+	—	Positive lead of C2 capacitor
5	C2-	—	Negative lead of C2 capacitor
6	V-	O	Negative charge pump output for storage capacitor only
7	DOUT2	O	RS-232 line data output (to remote RS-232 system)
8	RIN2	I	RS-232 line data input (from remote RS-232 system)
9	ROUT2	O	Logic data output (to UART)
10	DIN2	I	Logic data input (from UART)
11	DIN1	I	Logic data input (from UART)
12	ROUT1	O	Logic data output (to UART)
13	RIN1	I	RS-232 line data input (from remote RS-232 system)
14	DOUT1	O	RS-232 line data output (to remote RS-232 system)
15	GND	—	Ground
16	V <sub>CC</sub>	—	Supply voltage, connect to external 5-V power supply

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Supply voltage, $V_{CC}$ <sup>(2)</sup>		-0.3	6	V
Positive charge pump voltage, $V_+$ <sup>(2)</sup>		$V_{CC} - 0.3$	14	V
Negative charge pump voltage, $V_-$ <sup>(2)</sup>		-14	0.3	V
Input voltage, $V_I$	Drivers	-0.3	$V_+ + 0.3$	V
	Receivers		$\pm 30$	
Output voltage, $V_O$	Drivers	$V_- - 0.3$	$V_+ + 0.3$	V
	Receivers	-0.3	$V_{CC} + 0.3$	
Short-circuit duration, $DO_{UT}$		Continuous		
Operating virtual junction temperature, $T_J$			150	°C
Storage temperature, $T_{stg}$		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network GND.

### 6.2 ESD Ratings

			VALUE	UNIT	
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	Pins 7, 8, 13, 14, and 15	$\pm 15000$	V
			All other pins	$\pm 2000$	
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>			

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

see [Figure 12](#)<sup>(1)</sup>

		MIN	NOM	MAX	UNIT
Supply voltage		4.5	5	5.5	V
$V_{IH}$	Driver high-level input voltage (DIN)	2			V
$V_{IL}$	Driver low-level input voltage (DIN)			0.8	V
$V_I$	Driver input voltage (DIN)	0		5.5	V
	Receiver input voltage (RIN)	-30		30	
$T_A$	Operating free-air temperature	TRS202C		70	°C
		TRS202I	-40	85	

- (1) Test conditions are  $C_1$  to  $C_4 = 0.1 \mu\text{F}$  at  $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ .

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TRS202		UNIT
		D (SOIC)	PW (TSSOP)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	76.2	101	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	36.8	36.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33.9	45.9	°C/W
$\psi_{JT}$	Junction-to-top characterization parameter	6.7	2.7	°C/W
$\psi_{JB}$	Junction-to-board characterization parameter	33.6	45.3	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted; see [Figure 12](#))<sup>(1)</sup>

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX	UNIT	
$I_{CC}$	Supply current	No load and $V_{CC} = 5\text{ V}$		8	15	mA

(1) Test conditions are C1 to C4 = 0.1  $\mu\text{F}$  at  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ .

(2) All typical values are at  $V_{CC} = 5\text{ V}$  and  $T_A = 25^\circ\text{C}$ .

## 6.6 Electrical Characteristics: Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted; see [Figure 12](#))<sup>(1)</sup>

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX	UNIT	
$V_{OH}$	High-level output voltage	DOUT at $R_L = 3\text{ k}\Omega$ to GND and DIN = GND		5	9	V
$V_{OL}$	Low-level output voltage	DOUT at $R_L = 3\text{ k}\Omega$ to GND and DIN = $V_{CC}$		-5	-9	V
$I_{IH}$	High-level input current	$V_I = V_{CC}$		15	200	$\mu\text{A}$
$I_{IL}$	Low-level input current	$V_I$ at 0 V		-15	-200	$\mu\text{A}$
$I_{OS}$ <sup>(3)</sup>	Short-circuit output current	$V_{CC} = 5.5\text{ V}$ and $V_O = 0\text{ V}$		$\pm 10$	$\pm 60$	mA
$r_o$	Output resistance	$V_{CC}$ , $V_+$ , $V_- = 0\text{ V}$ , and $V_O = \pm 2\text{ V}$		300		$\Omega$

(1) Test conditions are C1 to C4 = 0.1  $\mu\text{F}$  at  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ .

(2) All typical values are at  $V_{CC} = 5\text{ V}$  and  $T_A = 25^\circ\text{C}$ .

(3) Short-circuit durations must be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output must be shorted at a time.

## 6.7 Electrical Characteristics: Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted; see [Figure 12](#))<sup>(1)</sup>

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX	UNIT
$V_{OH}$	High-level output voltage	3.5	$V_{CC} - 0.4$		V
$V_{OL}$	Low-level output voltage			0.4	V
$V_{IT+}$	Positive-going input threshold voltage		1.7	2.4	V
$V_{IT-}$	Negative-going input threshold voltage	0.8	1.2		V
$V_{hys}$	Input hysteresis ( $V_{IT+} - V_{IT-}$ )	0.2	0.5	1	V
$r_i$	Input resistance	3	5	7	k $\Omega$

(1) Test conditions are C1 to C4 = 0.1  $\mu\text{F}$  at  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ .

(2) All typical values are at  $V_{CC} = 5\text{ V}$  and  $T_A = 25^\circ\text{C}$ .

### 6.8 Switching Characteristics: Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted; see Figure 12)<sup>(1)</sup>

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX	UNIT
Maximum data rate	$C_L = 50$ to $1000$ pF, one DOUT switching, and $R_L = 3$ k $\Omega$ to $7$ k $\Omega$ (see Figure 6)	120			kbit/s
$t_{PLH(D)}$ Propagation delay time, low- to high-level output	$C_L = 2500$ pF, all drivers loaded, and $R_L = 3$ k $\Omega$ (see Figure 6)		2		$\mu$ s
$t_{PHL(D)}$ Propagation delay time, high- to low-level output	$C_L = 2500$ pF, all drivers loaded, and $R_L = 3$ k $\Omega$ (see Figure 6)		2		$\mu$ s
$t_{sk(p)}$ Pulse skew <sup>(3)</sup>	$C_L = 150$ pF to $2500$ pF and $R_L = 3$ k $\Omega$ to $7$ k $\Omega$ (see Figure 7)		300		ns
SR(tr) Slew rate, transition region	$C_L = 50$ pF to $1000$ pF, $V_{CC} = 5$ V, and $R_L = 3$ k $\Omega$ to $7$ k $\Omega$ (see Figure 6)	3	6	30	V/ $\mu$ s

- (1) Test conditions are  $C1$  to  $C4 = 0.1$   $\mu$ F at  $V_{CC} = 5$  V  $\pm 0.5$  V.
- (2) All typical values are at  $V_{CC} = 5$  V and  $T_A = 25^\circ$ C.
- (3) Pulse skew is defined as  $|t_{PLH} - t_{PHL}|$  of each channel of the same device.

### 6.9 Switching Characteristics: Receiver

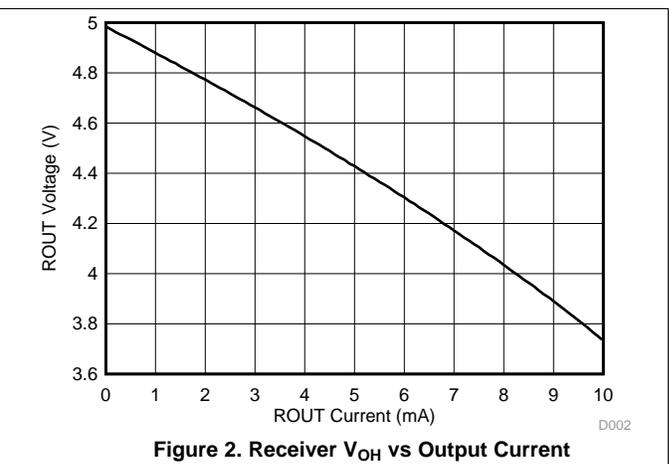
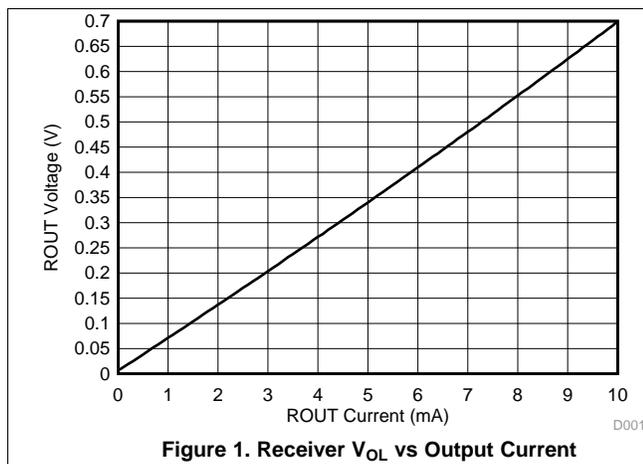
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted; see Figure 8)<sup>(1)</sup>

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX	UNIT
$t_{PLH(R)}$ Propagation delay time, low- to high-level output	$C_L = 150$ pF		0.5	10	$\mu$ s
$t_{PHL(R)}$ Propagation delay time, high- to low-level output	$C_L = 150$ pF		0.5	10	$\mu$ s
$t_{sk(p)}$ Pulse skew <sup>(3)</sup>			300		ns

- (1) Test conditions are  $C1$  to  $C4 = 0.1$   $\mu$ F at  $V_{CC} = 5$  V  $\pm 0.5$  V.
- (2) All typical values are at  $V_{CC} = 5$  V and  $T_A = 25^\circ$ C.
- (3) Pulse skew is defined as  $|t_{PLH} - t_{PHL}|$  of each channel of the same device.

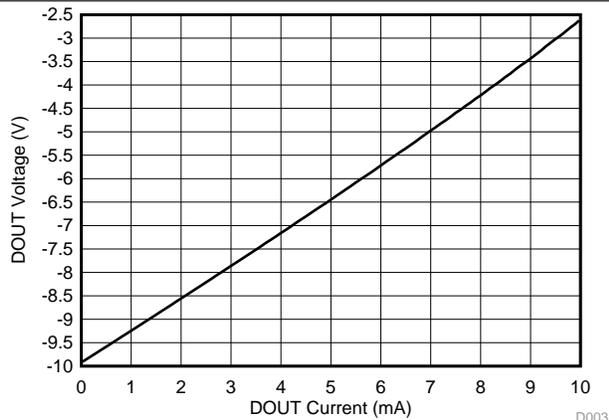
### 6.10 Typical Characteristics

$T_A = 25^\circ$ C (unless otherwise noted)

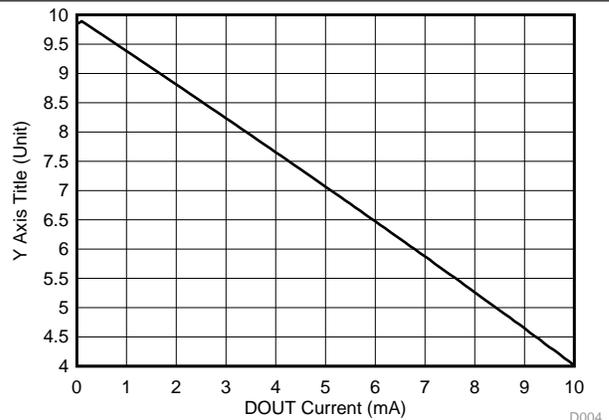


**Typical Characteristics (continued)**

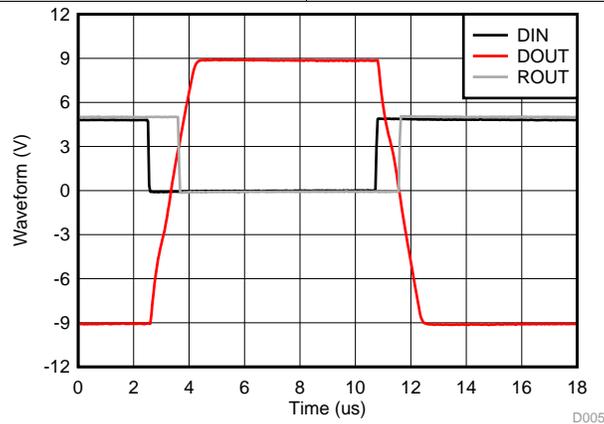
T<sub>A</sub> = 25°C (unless otherwise noted)



**Figure 3. Driver V<sub>OL</sub> vs Output Current**

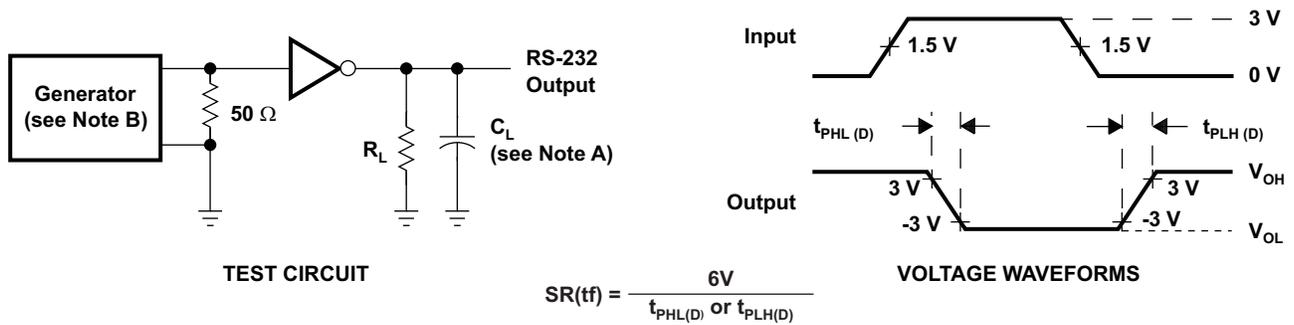


**Figure 4. Driver V<sub>OH</sub> vs Output Current**



**Figure 5. Driver and Receiver Loopback Waveforms**

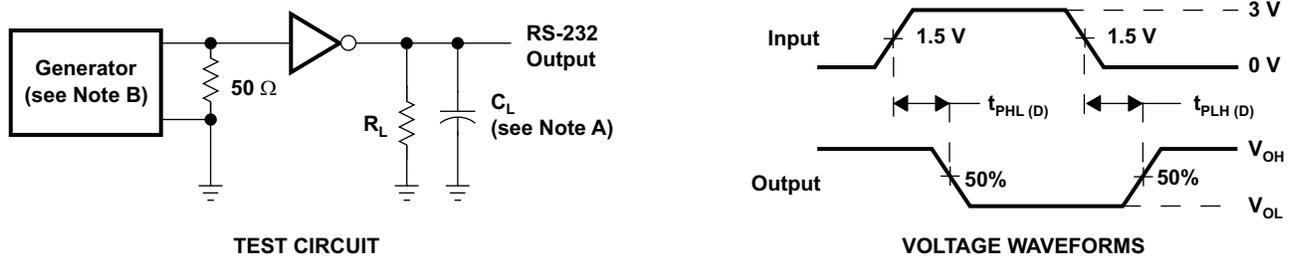
## 7 Parameter Measurement Information



NOTES: A.  $C_L$  includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 120 kbit/s,  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10 \text{ ns}$ ,  $t_f \leq 10 \text{ ns}$ .

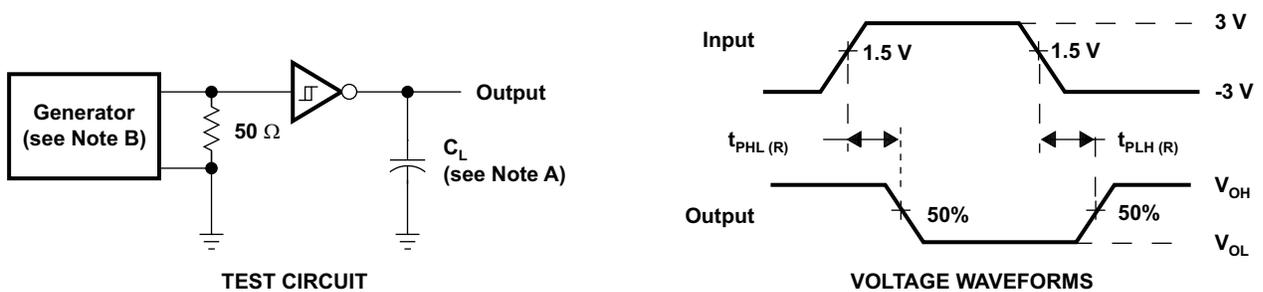
**Figure 6. Driver Slew Rate**



NOTES: A.  $C_L$  includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 120 kbit/s,  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10 \text{ ns}$ ,  $t_f \leq 10 \text{ ns}$ .

**Figure 7. Driver Pulse Skew**



NOTES: A.  $C_L$  includes probe and jig capacitance.

B. The pulse generator has the following characteristics:  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10 \text{ ns}$ ,  $t_f \leq 10 \text{ ns}$ .

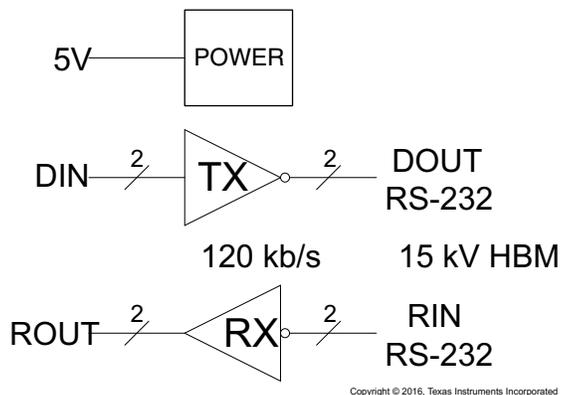
**Figure 8. Receiver Propagation Delay Times**

## 8 Detailed Description

### 8.1 Overview

The TRS202 device is a dual driver and receiver that includes a capacitive voltage generator using four capacitors to supply TIA/EIA-232-F voltage levels from a single 5-V supply. Each receiver converts TIA/EIA-232-F inputs to 5-V TTL/CMOS levels. These receivers have shorted and open fail safe. The receiver can accept up to  $\pm 30$ -V inputs and decode inputs as low as  $\pm 3$  V. Each driver converts TTL/CMOS input levels into TIA/EIA-232-F levels. Outputs are protected against shorts to ground.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 Power

The power block increases and inverts the 5-V supply for the RS-232 driver using a charge pump that requires four 0.1- $\mu$ F external capacitors.

#### 8.3.2 RS-232 Driver

Two drivers interface standard logic levels to RS-232 levels. The driver inputs do not have internal pullup resistors. Do not float the driver inputs.

#### 8.3.3 RS-232 Receiver

Two Schmitt trigger receivers interface RS-232 levels to standard logic levels. Each receiver has an internal 5-k $\Omega$  load to ground. An open input results in a high output on ROUT.

### 8.4 Device Functional Modes

#### 8.4.1 $V_{CC}$ Powered by 5 V

The device is in normal operation when powered by 5 V.

#### 8.4.2 $V_{CC}$ Unpowered

When TRS202 is unpowered, it can be safely connected to an active remote RS-232 device.

**Device Functional Modes (continued)**
**8.4.3 Truth Tables**

Table 1 and Table 2 list the function for each driver and receiver (respectively). Figure 9 shows the logic diagram.

**Table 1. Function Table for Each Driver<sup>(1)</sup>**

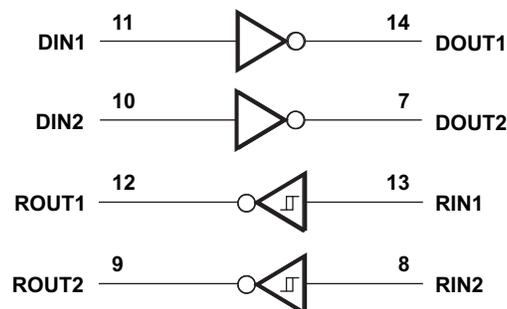
INPUT DIN	OUTPUT DOUT
L	H
H	L

(1) H = High level, L = Low level

**Table 2. Function Table for Each Receiver<sup>(1)</sup>**

INPUT RIN	OUTPUT ROUT
L	H
H	L
Open	H

(1) H = High level, L = Low level,  
Open = Input disconnected or connected driver off


**Figure 9. Logic Diagram (Positive Logic)**

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

For proper operation, add capacitors as shown in [Figure 12](#). Pins 9 through 12 connect to UART or general purpose logic lines. RS-232 lines on pins 7, 8, 13, and 14 connect to a connector or cable.

#### 9.1.1 Capacitor Selection

The capacitor type used for C1–C4 is not critical for proper operation. The TRS202 requires 0.1- $\mu\text{F}$  capacitors, although capacitors up to 10  $\mu\text{F}$  can be used without harm. Ceramic dielectrics are suggested for the 0.1- $\mu\text{F}$  capacitors. When using the minimum recommended capacitor values, make sure the capacitance value does not degrade excessively as the operating temperature varies. If in doubt, use capacitors with a larger (for example, 2 $\times$ ) nominal value. The capacitors' effective series resistance (ESR), which usually rises at low temperatures, influences the amount of ripple on V+ and V–.

Use larger capacitors (up to 10  $\mu\text{F}$ ) to reduce the output impedance at V+ and V–.

Bypass  $V_{\text{CC}}$  to ground with at least 0.1  $\mu\text{F}$ . In applications sensitive to power-supply noise generated by the charge pumps, decouple  $V_{\text{CC}}$  to ground with a capacitor the same size as (or larger than) the charge-pump capacitors (C1 to C4).

#### 9.1.2 Electrostatic Discharge (ESD) Protection

TI TRS202 devices have standard ESD protection structures incorporated on the pins to protect against electrostatic discharges encountered during assembly and handling. In addition, the RS232 bus pins (driver outputs and receiver inputs) of these devices have an extra level of ESD protection. Advanced ESD structures were designed to successfully protect these bus pins against ESD discharge of  $\pm 15$  kV when powered down.

#### 9.1.3 ESD Test Conditions

Stringent ESD testing is performed by TI, based on various conditions and procedures. Contact TI for a reliability report that documents test setup, methodology, and results.

#### 9.1.4 Human-Body Model (HBM)

The HBM of ESD testing is shown in [Figure 10](#). [Figure 11](#) shows the current waveform that is generated during a discharge into a low impedance. The model consists of a 100-pF capacitor, charged to the ESD voltage of concern, and subsequently discharged into the device under test (DUT) through a 1.5-k $\Omega$  resistor.

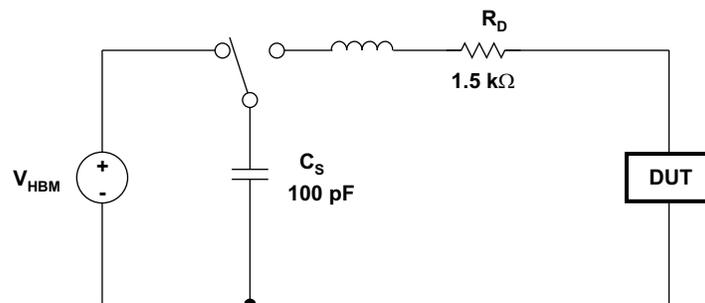


Figure 10. HBM ESD Test Circuit

## Application Information (continued)

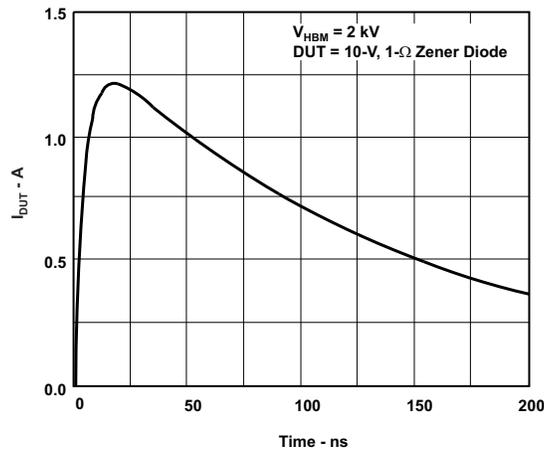
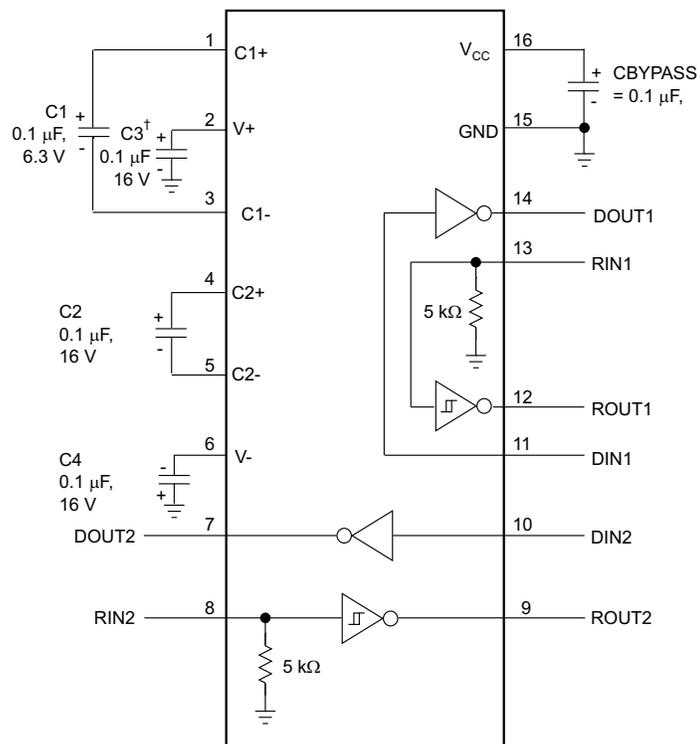


Figure 11. Typical HBM Current Waveform

## 9.2 Typical Application

Two driver and two receiver channels are supported for full duplex transmission with hardware flow control. The two 5-k $\Omega$  resistors are internal to the TRS202.



<sup>†</sup> C3 can be connected to V<sub>CC</sub> or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

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Figure 12. Typical Operating Circuit and Capacitor Values

**Typical Application (continued)**

**9.2.1 Design Requirements**

- $V_{CC}$  minimum is 4.5 V and maximum is 5.5 V.
- Maximum recommended bit rate is 120 kbps.

**9.2.2 Detailed Design Procedure**

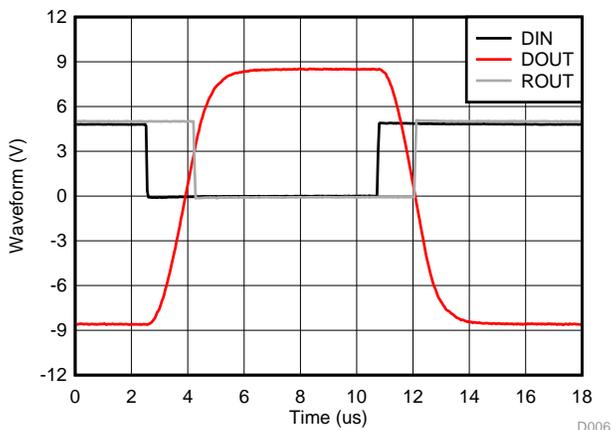
**9.2.2.1 Capacitor Selection**

The capacitor type used for C1 through C4 is not critical for proper operation. The TRS202 requires 0.1- $\mu$ F capacitors. Capacitors up to 10  $\mu$ F can be used without harm. Ceramic dielectrics are suggested for the 0.1- $\mu$ F capacitors. When using the minimum recommended capacitor values, make sure the capacitance value does not degrade excessively as the operating temperature varies. If in doubt, use capacitors with a larger (for example, 2x) nominal value. The capacitors' effective series resistance (ESR), which usually rises at low temperatures, influences the amount of ripple on V+ and V-.

Use larger capacitors (up to 10  $\mu$ F) to reduce the output impedance at V+ and V-.

Bypass  $V_{CC}$  to ground with at least 0.1  $\mu$ F. In applications sensitive to power-supply noise generated by the charge pumps, decouple  $V_{CC}$  to ground with a capacitor the same size as (or larger than) the charge-pump capacitors (C1 to C4).

**9.2.3 Application Curve**



120 kbit/s, 1-nF load

**Figure 13. Driver and Receiver Loopback Signal**

## 10 Power Supply Recommendations

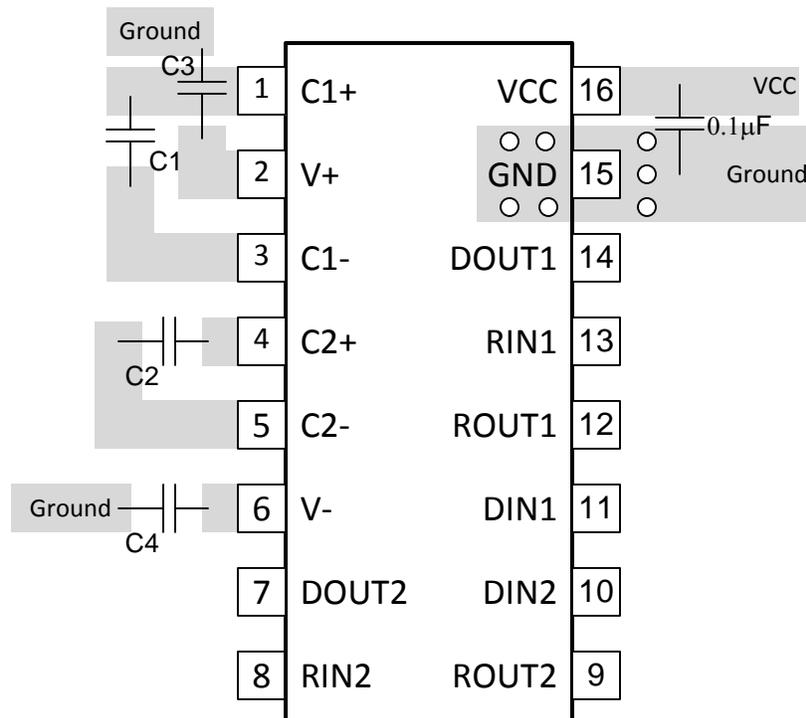
The  $V_{CC}$  voltage must be connected to the same power source used for logic device connected to DIN and ROUT pins.  $V_{CC}$  must be between 4.5 V and 5.5 V.

## 11 Layout

### 11.1 Layout Guidelines

Keep the external capacitor traces short. This is more important on C1 and C2 nodes that have the fastest rise and fall times. For best ESD performance, make the impedance from TRS202 ground pin to the ground plane of the circuit board as low as possible. Use wide metal and multiple vias on both sides of ground pin.

### 11.2 Layout Example



**Figure 14. TRS202 Circuit Board Layout**

## 12 Device and Documentation Support

### 12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.3 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TRS202ID</a>	Obsolete	Production	SOIC (D)   16	-	-	Call TI	Call TI	-40 to 85	TRS202I
<a href="#">TRS202IDR</a>	Obsolete	Production	SOIC (D)   16	-	-	Call TI	Call TI	-40 to 85	TRS202I
<a href="#">TRS202IPWR</a>	Obsolete	Production	TSSOP (PW)   16	-	-	Call TI	Call TI	-40 to 85	RU02I

**(1) Status:** For more details on status, see our [product life cycle](#).

**(2) Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

**(3) RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

**(4) Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**(5) MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

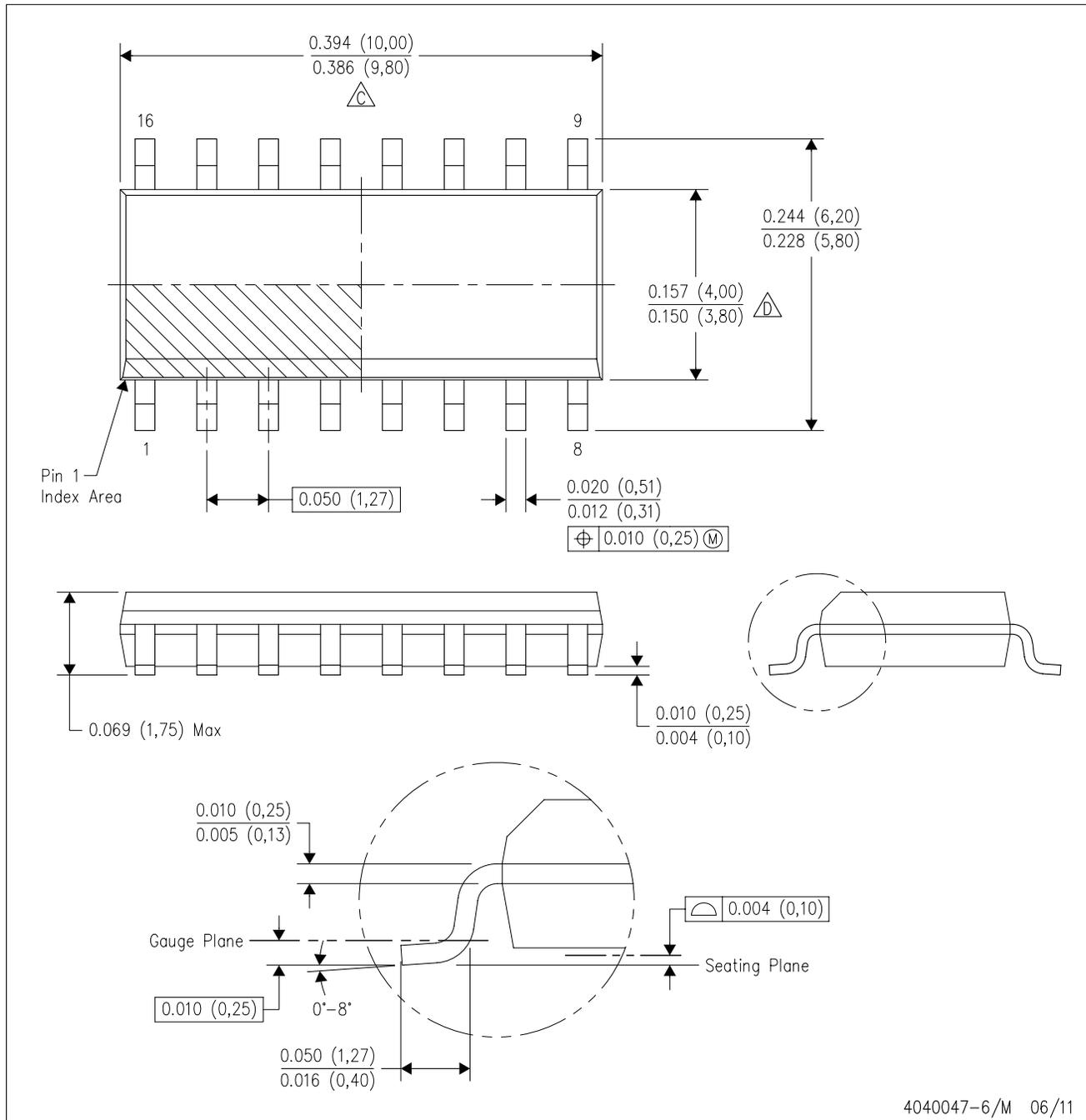
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

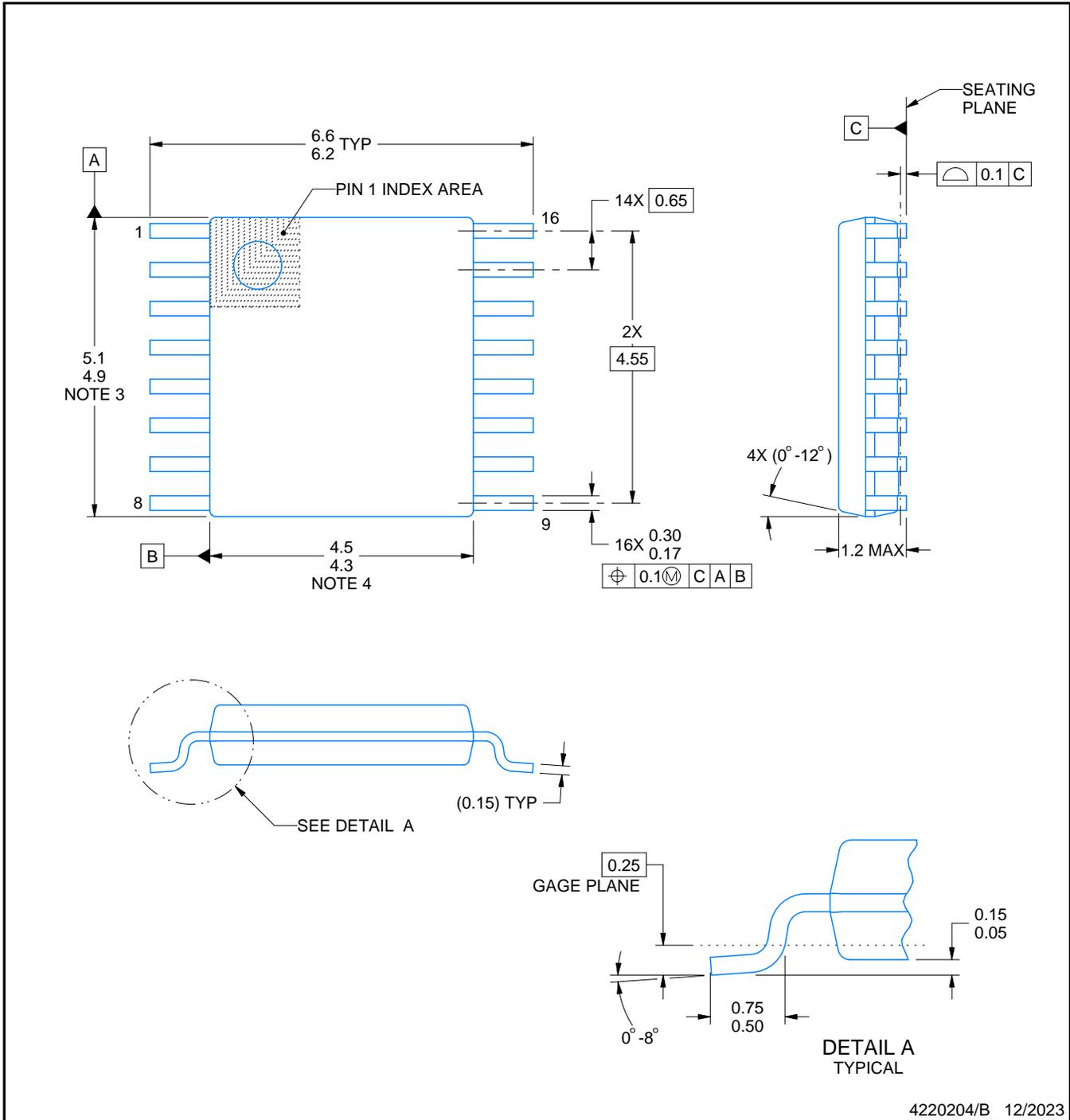
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.



4220204/B 12/2023

NOTES:

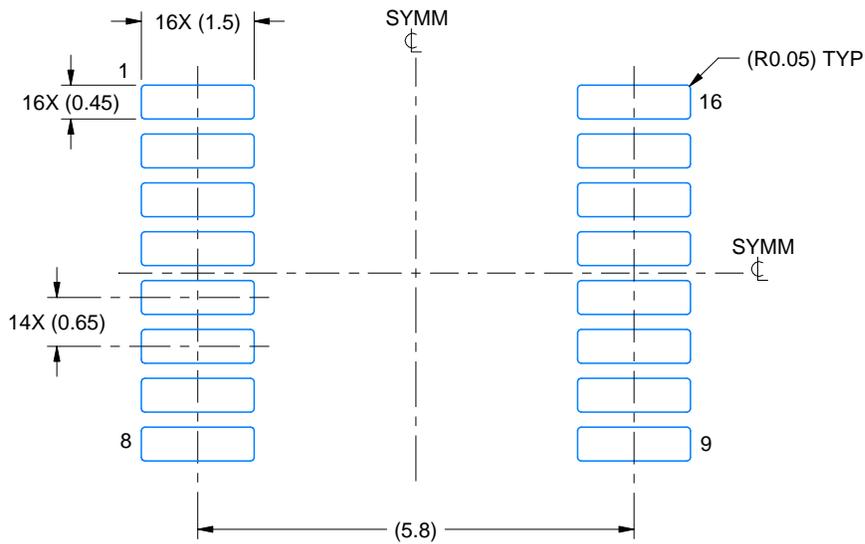
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

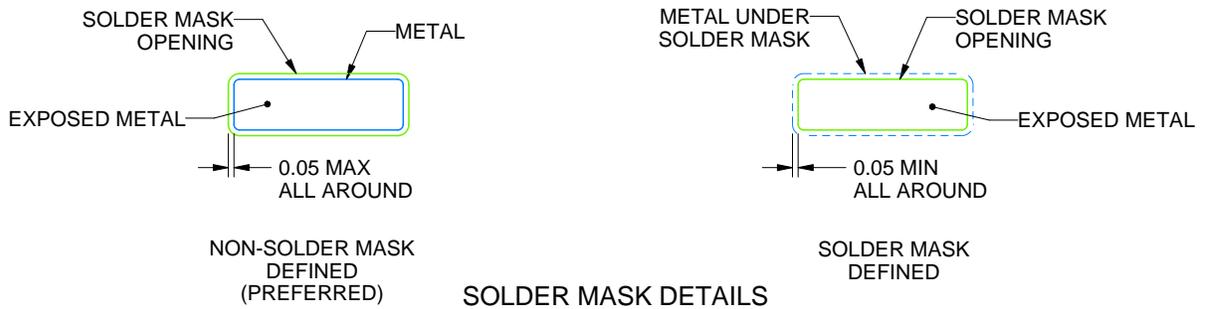
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

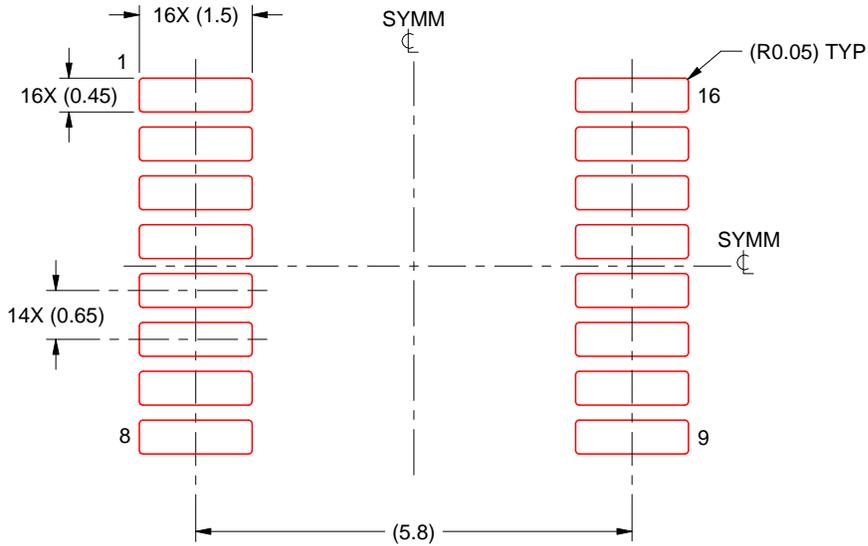
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025