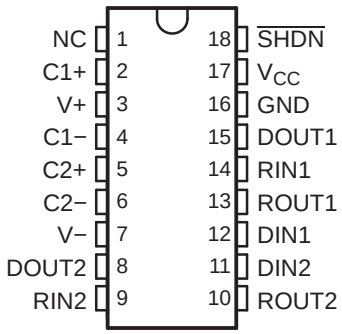
TRS222
5-V DUAL RS-232 LINE DRIVER/RECEIVER WITH ±15-kV ESD PROTECTION

SLLS813 – JULY 2007

FEATURES

- **ESD Protection for RS-232 Bus Pins**
  - **±15-kV Human-Body Model (HBM)**
- **Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU v.28 Standards**
- **Operates at 5-V V_{CC} Supply**
- **Operates up to 200 kbit/s**
- **Low Supply Current in Shutdown Mode . . . 2 µA Typical**
- **External Capacitors . . . 4 × 0.1 µF**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**

DW OR N PACKAGE
(TOP VIEW)



APPLICATIONS

- **Battery-Powered Systems**
- **PDAs**
- **Notebooks**
- **Laptops**
- **Palmtop PCs**
- **Hand-Held Equipment**

DESCRIPTION/ORDERING INFORMATION

The TRS222 consists of two line drivers, two line receivers, and a dual charge-pump circuit with ±15-kV ESD protection pin to pin (serial-port connection pins, including GND). This device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 5-V supply. This device operates at data signaling rates up to 200 kbit/s and a maximum of 30-V/µs driver output slew rate. By using shutdown ($\overline{SHDN}$), all receivers can be disabled.

ORDERING INFORMATION

T_A	PACKAGE(1)(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube of 20	TRS222CN	TRS222CN
	SOIC – DW	Tube of 20	TRS222CDW	TRS222C
		Reel of 1000	TRS222CDWR	
–40°C to 85°C	PDIP – N	Tube of 20	TRS222IN	TRS222IN
	SOIC – DW	Tube of 20	TRS222IDW	TRS222I
		Reel of 1000	TRS222IDWR	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

FUNCTION TABLES

Each Driver(1)

INPUT DIN	OUTPUT DOUT
L	H
H	L

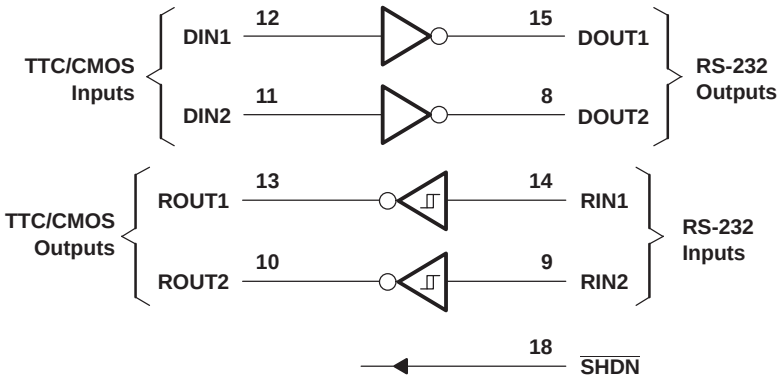
(1) H = high level, L = low level

Each Receiver(1)

INPUT RIN	OUTPUT ROUT
L	H
H	L
Open	H

(1) H = high level, L = low level,
Open = input disconnected or
connected driver off

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range(2)		–0.3	6	V
V_I	Input voltage range	Drivers	–0.3	V_{CC} – 0.3	V
		Receivers		±30	
V_O	Output voltage range	Drivers		±15	V
		Receivers	–0.3	V_{CC} + 0.3	
D_{OUT}	Short-circuit duration			Continuous	
θ_{JA}	Package thermal impedance(3)(4)	DW package		58	°C/W
		N package		TBD	
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network GND.
(3) Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions(1)

See Figure 4

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	Driver high-level input voltage	DIN	2			V
	Shutdown high-level input voltage	$\overline{SHDN}$	2			
V_{IL}	Driver and control low-level input voltage	DIN			0.8	V
	Shutdown low-level input voltage	$\overline{SHDN}$			0.8	
V_I	Driver input voltage	DIN	0		5.5	V
	Receiver input voltage		–30		30	
T_A	Operating free-air temperature	TRS222C	0		70	°C
		TRS222I	–40		85	

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 5 V ± 0.5 V.

Electrical Characteristics(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 4)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
I_{CC}	Supply current	V_{CC} = 5 V,	$\overline{SHDN}$ = V_{CC}	No load		4	10	mA
				3 kΩ on both inputs		15		
	Shutdown supply current					2	50	µA
$\overline{SHDN}$	Shutdown input leakage current						±1	µA

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 5 V ± 0.5 V.

DRIVER SECTION

Electrical Characteristics(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 4)

PARAMETER		TEST CONDITIONS		MIN	TYP(2)	MAX	UNIT
V_{OH}	High-level output voltage	DOUT at R_L = 3 kΩ to GND,	DIN = GND	5	8		V
V_{OL}	Low-level output voltage	DOUT at R_L = 3 kΩ to GND,	DIN = V_{CC}	–5	–8		V
I_{IH}	Driver high-level input current	DIN = V_{CC}			5	40	µA
	Control high-level input current	$\overline{SHDN}$ = V_{CC}			0.01	1	
I_{IL}	Driver low-level input current	DIN = 0 V			–5	–40	µA
	Control low-level input current	$\overline{SHDN}$ = 0 V			–0.01	–1	
I_{OS}	Short-circuit output current(3)	V_{CC} = 5.5 V,	V_O = 0 V	±7	±22		mA
I_{off}	Output leakage current	V_{CC} = 5.5 V, $\overline{SHDN}$ = GND,	V_O = ±10 V		±0.01	±10	µA
r_o	Output resistance	V_{CC}, V+, and V– = 0 V,	V_O = ±2 V	300	10 M		Ω

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 5 V, and T_A = 25°C.
(3) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

Switching Characteristics(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 4)

PARAMETER		TEST CONDITIONS		MIN	TYP(2)	MAX	UNIT
	Data rate	C_L = 1000 pF, One DOUT switching,	R_L = 3 kΩ, See Figure 1	200			kbit/s
$t_{PLH(D)}$	Propagation delay time, low- to high-level output	See Figure 1			1.5	3.5	µs
$t_{PHL(D)}$	Propagation delay time, high- to low-level output	See Figure 1			1.3	3.5	µs
$t_{PHL(D)} – t_{PLH(D)}$	Driver (+ to –) propagation delay difference				300		ns
$t_{sk(p)}$	Pulse skew(3)	C_L = 150 pF to 2500 pF, See Figure 2	R_L = 3 kΩ to 7 kΩ,		300		ns
SR(tr)	Slew rate, transition region (see Figure 1)	C_L = 50 pF to 2500 pF, V_{CC} = 5 V	R_L = 3 kΩ to 7 kΩ,	6	12	30	V/µs
t_{ET}	Driver output enable time (after $\overline{SHDN}$ goes high)				250		µs
t_{DT}	Driver output disable time (after $\overline{SHDN}$ goes low)				300		ns

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 5 V, and T_A = 25°C.
(3) Pulse skew is defined as $|t_{PLH} – t_{PHL}|$ of each channel of the same device.

RECEIVER SECTION

Electrical Characteristics(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 4)

PARAMETER		TEST CONDITIONS	MIN	TYP(2)	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA	3.5	V_{CC} – 0.2		V
V_{OL}	Low-level output voltage	I_{OH} = 3.2 mA			0.4	V
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 5 V		1.7	2.4	V
$V_{IT–}$	Negative-going input threshold voltage	V_{CC} = 5 V	0.8	1.3		V
V_{hys}	Input hysteresis ($V_{IT+} – V_{IT–}$)		0.2	0.5	1	V
r_i	Input resistance	V_I = ±3 V to ±25 V	3	5	7	kΩ

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 5 V, and T_A = 25°C.

Switching Characteristics(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 3)

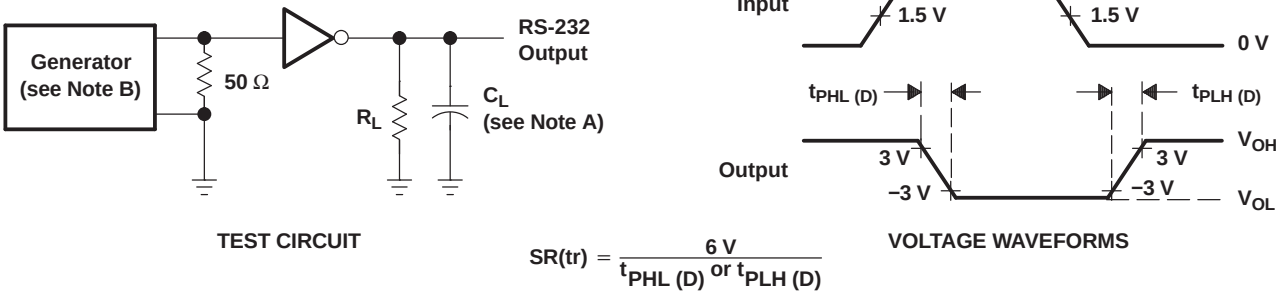
PARAMETER		TEST CONDITIONS	MIN	TYP(2)	MAX	UNIT
$t_{PLH(R)}$	Propagation delay time, low- to high-level output	C_L = 150 pF		0.6	1	µs
$t_{PHL(R)}$	Propagation delay time, high- to low-level output	C_L = 150 pF		0.5	1	µs
$t_{PHL(R)} – t_{PLH(R)}$	Receiver (+ to –) propagation delay difference			100		ns
$t_{sk(p)}$	Pulse skew(3)			100		ns

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 5 V, and T_A = 25°C.
(3) Pulse skew is defined as $|t_{PLH} – t_{PHL}|$ of each channel of the same device.

ESD Protection

PIN	TEST CONDITIONS	TYP	UNIT
DOUT, RIN	Human-Body Model	±15	kV

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

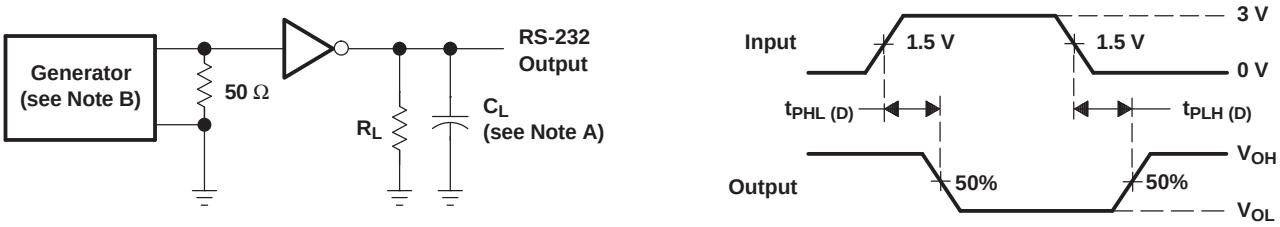
VOLTAGE WAVEFORMS

$$SR(tr) = \frac{6\ V}{t_{PHL\ (D)} \text{ or } t_{PLH\ (D)}}$$

A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, t_r ≤10 ns, t_f ≤ 10 ns.

Figure 1. Driver Slew Rate



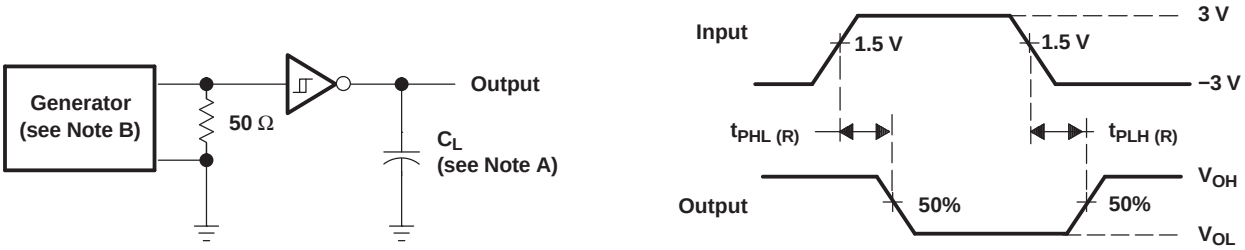
TEST CIRCUIT

VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, t_r ≤10 ns, t_f ≤ 10 ns.

Figure 2. Driver Pulse Skew



TEST CIRCUIT

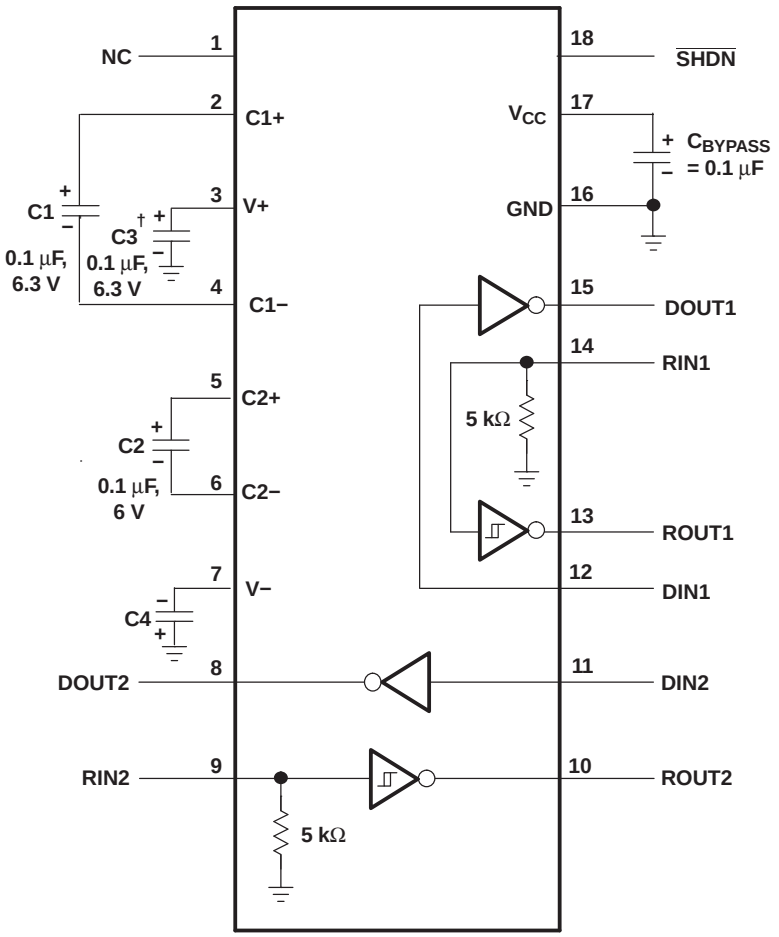
VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, t_r ≤10 ns, t_f ≤ 10 ns.

Figure 3. Receiver Propagation Delay Times

APPLICATION INFORMATION



† C3 can be connected to V_{CC} or GND.

A. Resistor values shown are nominal

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

Figure 4. Typical Operating Circuit and Capacitor Values

APPLICATION INFORMATION (continued)

Capacitor Selection

The capacitor type used for C1–C4 is not critical for proper operation. The TRS222 requires 0.1-µF capacitors, although capacitors up to 10 µF can be used without harm. Ceramic dielectrics are suggested for the 0.1-µF capacitors. When using the minimum recommended capacitor values, ensure that the capacitance value does not degrade excessively as the operating temperature varies. If in doubt, use capacitors with a larger (e.g., 2×) nominal value. The capacitors' effective series resistance (ESR), which usually rises at low temperatures, influences the amount of ripple on V+ and V–.

Use larger capacitors (up to 10 µF) to reduce the output impedance at V+ and V–.

Bypass V_{CC} to ground with at least 0.1 µF. In applications sensitive to power-supply noise generated by the charge pumps, decouple V_{CC} to ground with a capacitor the same size as (or larger than) the charge-pump capacitors (C1–C4).

Electrostatic Discharge (ESD) Protection

TI TRS222 devices have standard ESD protection structures incorporated on the pins to protect against electrostatic discharges encountered during assembly and handling. In addition, the RS-232 bus pins (driver outputs and receiver inputs) of these devices have an extra level of ESD protection. Advanced ESD structures were designed to successfully protect these bus pins against ESD discharge of ±15 kV when powered down.

ESD Test Conditions

ESD testing stringently is performed by TI, based on various conditions and procedures. Contact TI for a reliability report that documents test setup, methodology, and results.

Human-Body Model (HBM)

The HBM of ESD testing is shown in Figure 5, while Figure 6 shows the current waveform that is generated during a discharge into a low impedance. The model consists of a 100-pF capacitor, charged to the ESD voltage of concern, and subsequently discharged into the DUT through a 1.5-kΩ resistor.

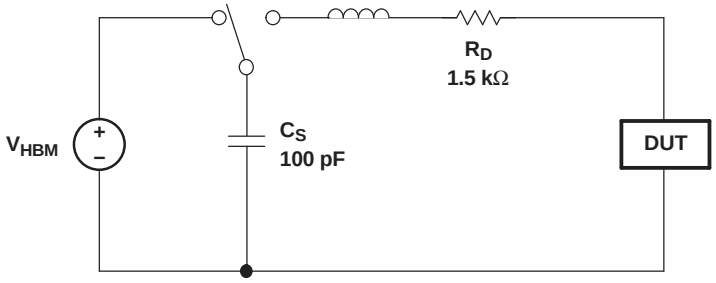


Figure 5. HBM ESD Test Circuit

APPLICATION INFORMATION (continued)

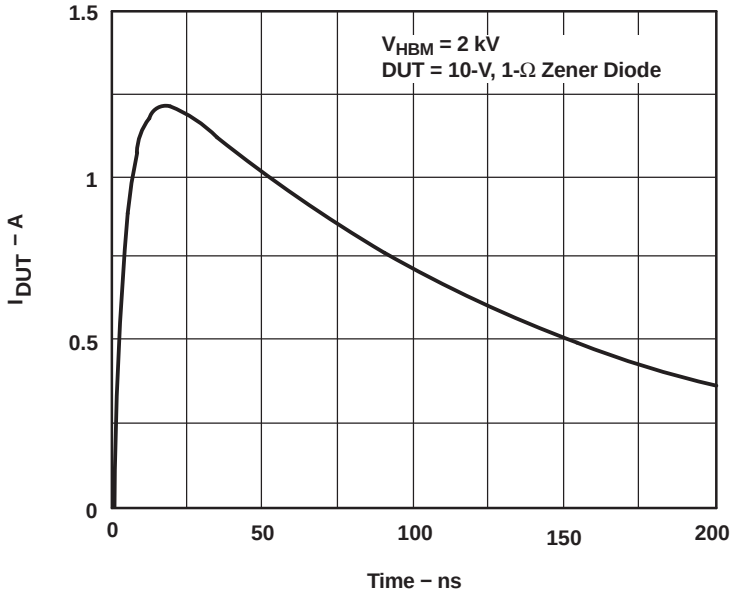


Figure 6. Typical HBM Current Waveform

Machine Model (MM)

The MM ESD test applies to all pins using a 200-pF capacitor with no discharge resistance. The purpose of the MM test is to simulate possible ESD conditions that can occur during the handling and assembly processes of manufacturing. In this case, ESD protection is required for all pins, not just RS-232 pins. However, after PC board assembly, the MM test no longer is as pertinent to the RS-232 pins.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TRS222IDWR	Obsolete	Production	SOIC (DW) | 18	-	-	Call TI	Call TI	-40 to 85	TRS222I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

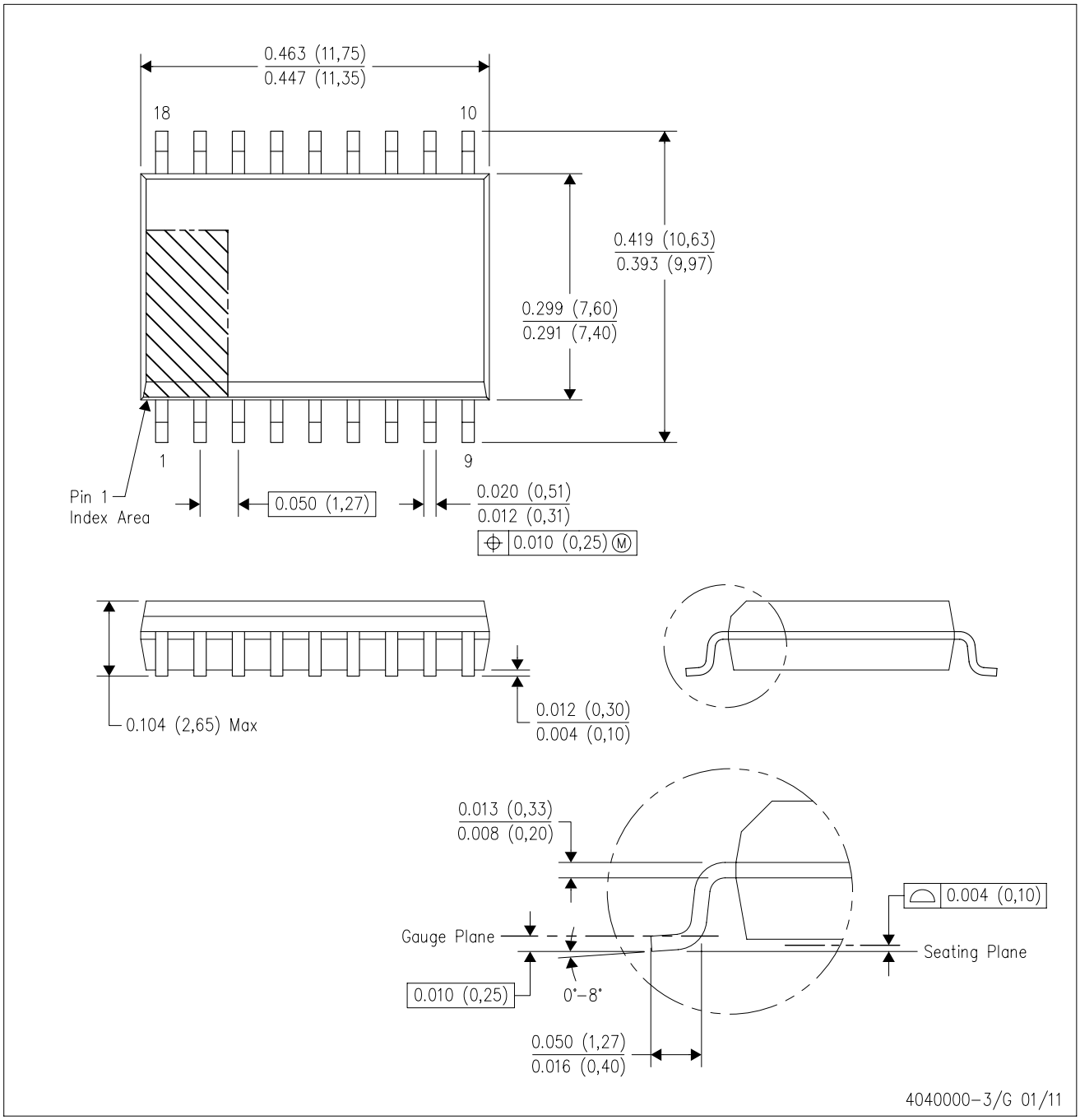
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

DW (R–PDSO–G18) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AB.

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