TVS5800 58V Flat-Clamp Surge Protection Device

1 Features

- IEC 61000-4-5 Surge Protection:
  - 25A (8/20µs)
  - Clamping voltage: 70.9V at 20A (8/20µs)
- Low leakage current:
  - 6nA typical at 27°C
  - 50nA typical at 85°C
- Low capacitance: 150pF
- Integrated IEC 61000-4-2 ESD protection

2 Applications

- Power over Ethernet (PoE)
- PLC I/O Modules
- Appliances
- Industrial Sensors
- Power lines

3 Description

The TVS5800 robustly shunts up to 25A of IEC 61000-4-5 fault current to protect systems from high power transients or lightning strikes. The TVS5800 uses a unique feedback mechanism to maintain precise flat clamping during a fault, supporting system exposure below 76V. The tight voltage regulation allows designers to confidently select system components with a lower voltage tolerance, lowering system costs and complexity without sacrificing robustness.

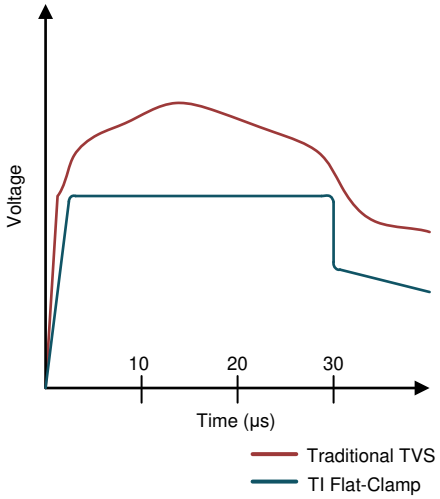
In addition, the TVS5800 is available in a 1.6mm x 1.6mm footprint which is designed for space constrained applications. The extremely low device leakage and capacitance allows a minimal effect on the protected line.

The TVS5800 is part of TI's Flat-Clamp family of surge devices. For more information on the other devices in the family, see the *Device Comparison Table*

Package Information

PART NUMBER	PACKAGE (1)	PACKAGE SIZE (2)
TVS5800	VEB (DFN1616, 6)	1.6mm × 1.6mm

(1) For more information, see the orderable addendum at the end of the data sheet.
(2) The package size (length x width) is a nominal value and includes pins, where applicable.



Voltage Clamp Response to 8/20µs Surge Event

Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Device Comparison Table....3
5 Pin Configuration and Functions....3
6 Specifications....4
6.1 Absolute Maximum Ratings....4
6.2 ESD Ratings - JEDEC....4
6.3 ESD Ratings - IEC....4
6.4 Recommended Operating Conditions....4
6.5 Thermal Information....4
6.6 Electrical Characteristics....5
6.7 Typical Characteristics....6
7 Detailed Description....7
7.1 Overview....7
7.2 Functional Block Diagram....7
7.3 Feature Description....7
7.4 Device Functional Modes....7
8 Application and Implementation....8
8.1 Application Information....8
8.2 Typical Application....8
9 Power Supply Recommendations....9
10 Layout....9
10.1 Layout Guidelines....9
10.2 Layout Example....9
11 Device and Documentation Support....10
11.1 Documentation Support....10
11.2 Receiving Notification of Documentation Updates....10
11.3 Support Resources....10
11.4 Trademarks....10
11.5 Electrostatic Discharge Caution....10
11.6 Glossary....10
12 Revision History....10
13 Mechanical, Packaging, and Orderable Information....10

4 Device Comparison Table

Device	V_{rwm} (V)	V_{clamp} at I_{pp} (V)	I_{pp} (8/20µs) (A)	V_{rwm} leakage (nA)	Package Options	Polarity
TVS0500	5	9.2	43	0.07	SON	Unidirectional
TVS1400	14	18.4	43	2	SON	Unidirectional
TVS1800	18	22.8	40	0.5	SON	Unidirectional
TVS2200	22	27.7	40	3.2	SON	Unidirectional
TVS2700	27	32.5	40	1.7	SON	Unidirectional
TVS3300	33	38	35	19	WCSP, SON	Unidirectional
TVS4000 (1)	40	50.4	24	4.45	DFN1616	Unidirectional
TVS5200 (1)	52	58.8	20	18.3	DFN1616	Unidirectional
TVS5800	58	70.9	25	6	DFN1616	Unidirectional

(1) Preview information (not Production Data)

5 Pin Configuration and Functions

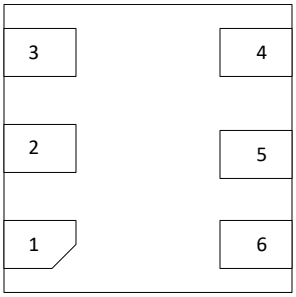


Figure 5-1. VEB Package, 6-Pin DFN1616 (Bottom View)

Table 5-1. Pin Functions

PIN		TYPE (1)	DESCRIPTION
NAME	NO.		
IN	4, 5, 6	I	ESD and surge protected channel
GND	1, 2, 3	GND	Ground

(1) I = input, GND = ground

6 Specifications

6.1 Absolute Maximum Ratings

T_A = 27°C (unless otherwise noted)(1)

		MIN	MAX	UNIT
Maximum Surge	IEC 61000-4-5 Current (8/20 µs)		25	A
	IEC 61000-4-5 Power (8/20 µs)		1880	W
EFT	IEC 61000-4-4 EFT Protection		80	A
T_A	Ambient Operating Temperature	-40	125	°C
T_{stg}	Storage Temperature	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings - JEDEC

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings - IEC

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	±15	kV
		IEC 61000-4-2 air-gap discharge	±15	

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
V_{RWM}	Reverse Stand-off Voltage			58	V

6.5 Thermal Information

THERMAL METRIC(1)		TVS5800 VEB (DFN1616) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	132.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	61.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	34.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.04	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	34.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

6.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse Stand-off Voltage		-0.5		58	V
I_{LEAK}	Leakage Current	Measured at $V_{IN} = V_{RWM}$ T_A = 27°C		6	300	nA
		Measured at $V_{IN} = V_{RWM}$ T_A = 85°C		50	1200	nA
		Measured at $V_{IN} = V_{RWM}$ T_A = 105°C		140	2400	nA
V_F	Forward Voltage	I_{IN} = 1mA from GND to IO	0.25	0.5	0.65	V
V_{BR}	Break-down Voltage	I_{IN} = 1mA from IO to GND	65.8	69.8		V
V_{CLAMP}	Clamp Voltage	10A IEC 61000-4-5 Surge (8/20µs) from IO to GND, V_{IN} = 0V before surge, 27°C	66.5	70.7	74.7	V
		20A IEC 61000-4-5 Surge (8/20µs) from IO to GND, V_{IN} = 0V before surge, 27°C	66.7	70.9	75	V
R_{DYN}	8/20 µs surge dynamic resistance	Calculated from V_{CLAMP} at .5*I_{pp} and I_{pp} surge current levels, 27°C		40		mΩ
C_{IN}	Input pin capacitance	$V_{IN} = V_{RWM}$, f = 1MHz, 30mV_{pp}, IO to GND		150		pF

6.7 Typical Characteristics

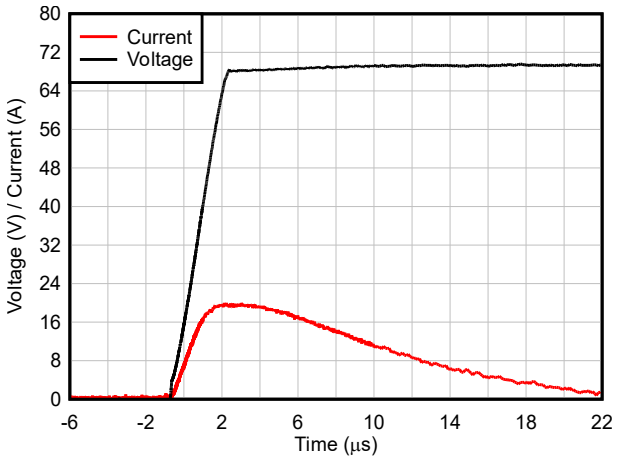


Figure 6-1. 8/20µs Surge Response at 20A

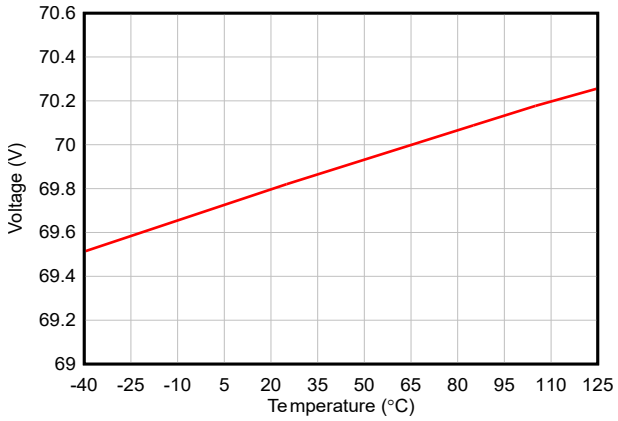


Figure 6-2. Breakdown Voltage (1mA) vs Temperature

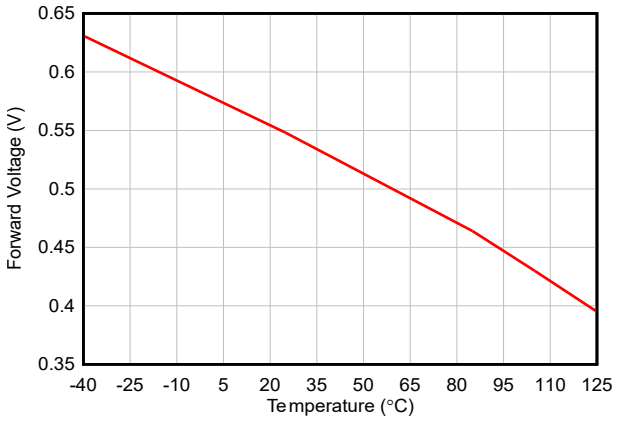


Figure 6-3. Forward Voltage vs Temperature

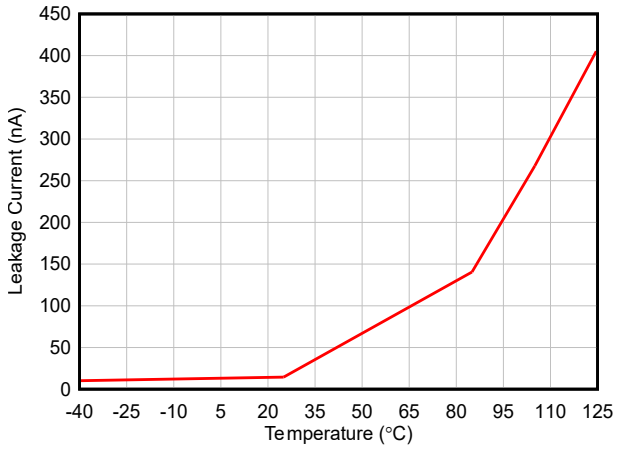


Figure 6-4. Leakage Current vs Temperature at 58V

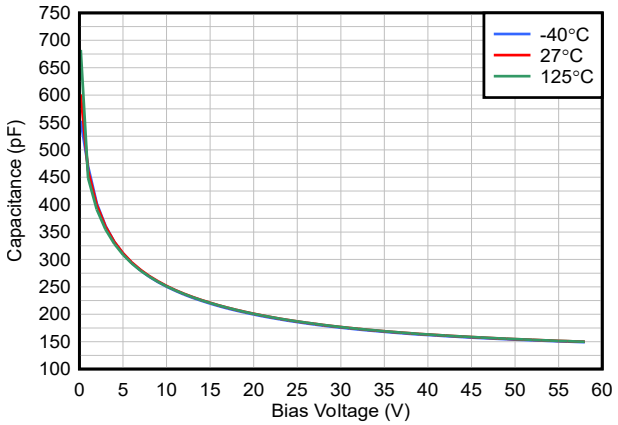


Figure 6-5. Capacitance vs Bias Voltage Across Temperature

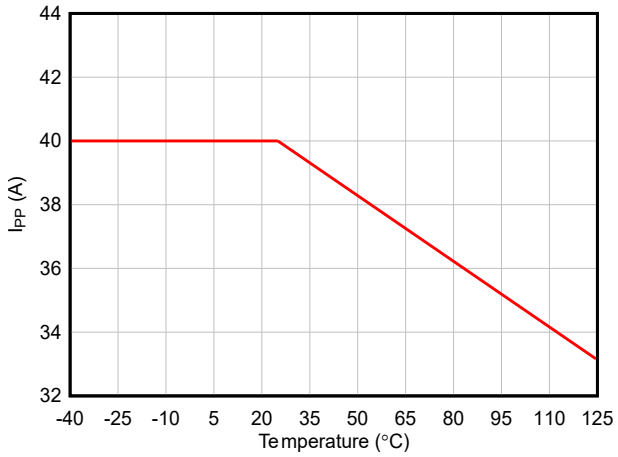


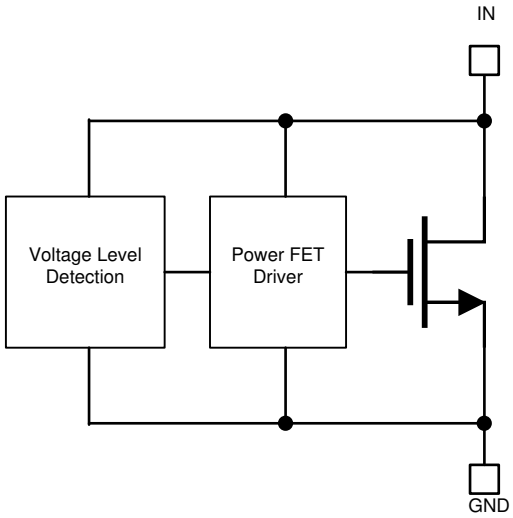
Figure 6-6. Max Surge Current (8/20µs) vs Temperature

7 Detailed Description

7.1 Overview

The TVS5800 is a precision clamp with a low, flat clamping voltage during transient overvoltage events like surge and protecting the system with zero voltage overshoot. For a detailed overview of the Flat-Clamp family of devices, please reference TI's Flat-Clamp surge protection technology for efficient system protection white paper. This document explains in detail the functional operation of the devices and how the TVS5800 impacts and improves system design.

7.2 Functional Block Diagram



7.3 Feature Description

The TVS5800 is a precision clamp that handles 25A of IEC 61000-4-5 8/20µs surge pulse. The flat clamping feature helps keep the clamping voltage very low to keep the downstream circuits from being stressed. The flat clamping feature can also help end-equipment designers save cost by opening up the possibility to use lower-cost, lower voltage tolerant downstream ICs. The TVS5800 has minimal leakage under the standoff voltage of 58V, making TVS5800 an desirable candidate for applications where low leakage and power dissipation is a necessity. IEC 61000-4-2 rating make TVS5800 a robust protection design for ESD events. Wide ambient temperature range of -40°C to +125°C, a good candidate for most applications. Compact package enables the TVS5800 to be used in small devices and save board area.

7.4 Device Functional Modes

7.4.1 Protection Specifications

The TVS5800 is specified according to the IEC 61000-4-5 standard. The IEC 61000-4-5 standards requires protection against a pulse with a rise time of 8µs and a half length of 20µs.

The TVS5800 has been tested according to IEC 61000-4-5 to pass a ±1kV surge test through a 42Ω coupling resistor and a 0.5µF capacitor. This test is a common test requirement for industrial signal I/O lines and the TVS5800 serves as an desired protection design for applications with that requirement.

The TVS5800 also integrates IEC 61000-4-2 level 4 ESD Protection. These combine to maintain that the device can protect against most transient conditions regardless of length or type.

For more information on TI's test methods for Surge, ESD, and EFT testing, reference TI's IEC 61000-4-x Testing Application Note

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TVS5800 can be used to protect any power, analog, or digital signal from transient fault conditions caused by the environment or other electrical components.

8.2 Typical Application

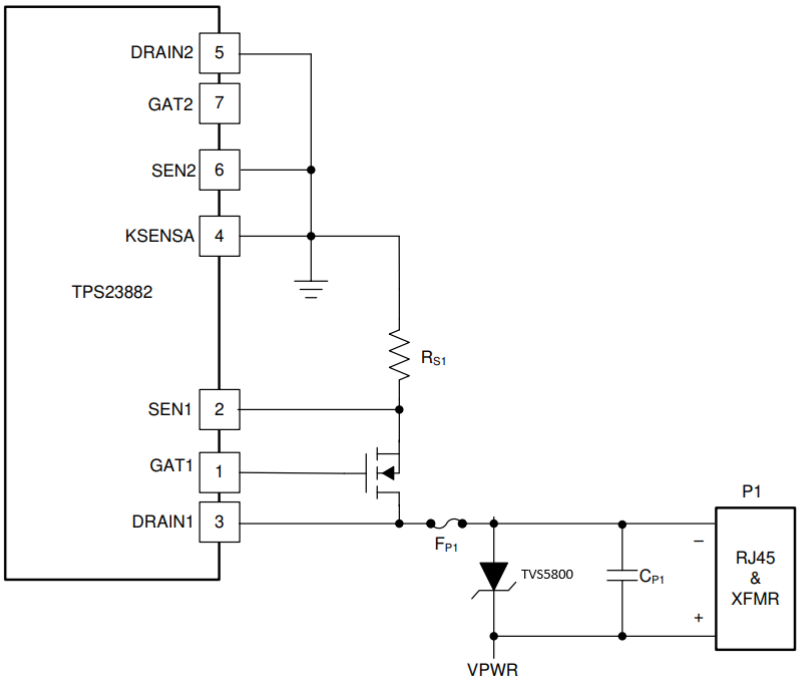


Figure 8-1. TVS5800 Application Schematic

8.2.1 Design Requirements

An application for the TVS5800 is protecting a Power over Ethernet (PoE) Power Sourcing Equipment (PSE) controller. In this example, the TVS5800 is protecting a PoE PSE controller such as the TPS23882, that has a nominal voltage of 58V and a clamping voltage requirement below 95V which is easily doable for the TVS5800 with a max clamping voltage of 75V. Most industrial interfaces such as this require protection against ±1kV surge test through a 42Ω coupling resistor and a 0.5µF capacitor, equaling roughly 24A of surge current. Without any input protection, if a surge event is caused by lightning, coupling, ringing, or any other fault condition thissd input voltage rises to hundreds of volts for multiple microseconds, violating the absolute maximum input voltage and harming the device. A desired surge protection diode maximizes the useable voltage range while still clamping at a safe level for the system, TI's Flat-Clamp technology provides the best protection design. For more information on PoE PSE controller protection, see Section 10.2 of the TPS23882 data sheet.

8.2.2 Detailed Design Procedure

If the TVS5800 is in place to protect the device, during a surge event the voltage rises to the breakdown of the diode at 69.8V, and then the TVS5800 turns on, shunting the surge current to ground. With the low dynamic resistance of the TVS5800, large amounts of surge current has minimal impact on the clamping voltage. The dynamic resistance of the TVS5800 is around 40mΩ, which means 25A of surge current causes a voltage raise of 25A × 40mΩ = 1V. Because the device turns on at 69.8V, this means the TPS23882 input is exposed to a maximum of 69.8V + 1V = 70.8V during surge pulses. This maintains robust protection of your circuit.

The small size of the device also improves fault protection by lowering the effect of fault current coupling onto neighboring traces. The small form factor of the TVS5800 allows the device to be placed extremely close to the input connector, lowering the length of the path fault current takes through the system compared to larger protection designs.

9 Power Supply Recommendations

The TVS5800 is a clamping device so there is no need to power the device. To maintain the device functions properly do not violate the recommended V_{IN} voltage range (0V to 58V) .

10 Layout

10.1 Layout Guidelines

The optimum placement is close to the connector. EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures. The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.

Route the protected traces straight. Eliminate any sharp corners on the protected traces between the TVS5800 and the connector by using rounded corners with the largest radii possible. Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Example

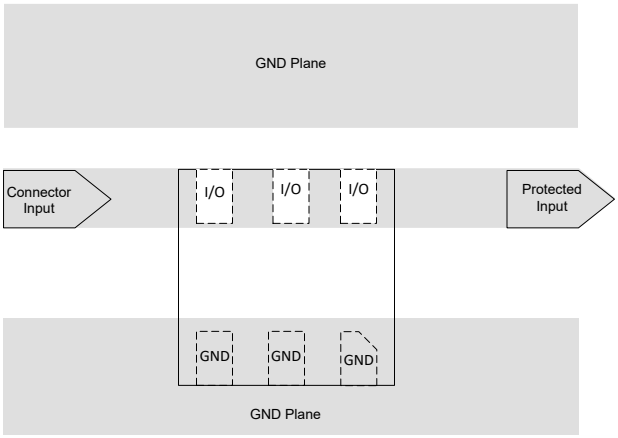


Figure 10-1. TVS5800 DFN1616 Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Flat-Clamp TVS Evaluation Kit*
- Texas Instruments, *How to select a Surge Diode*
- Texas Instruments, *Flat-Clamp surge protection technology for efficient system protection*

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
January 2026	*	Initial Release

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TVS5800VEBR	Active	Production	UQFN-HR (VEB) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	S9

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

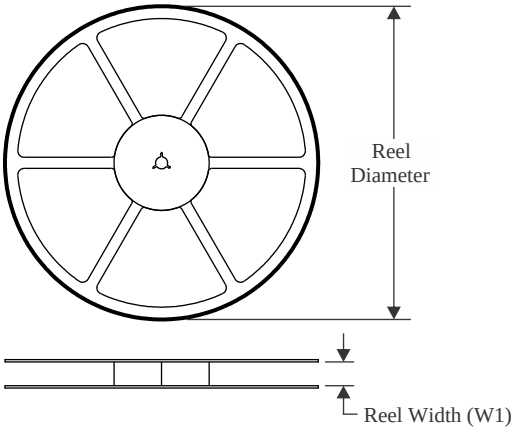
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

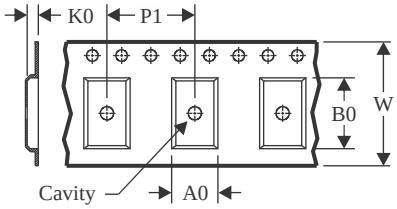
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

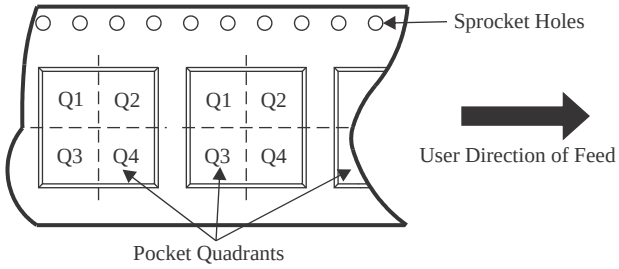


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

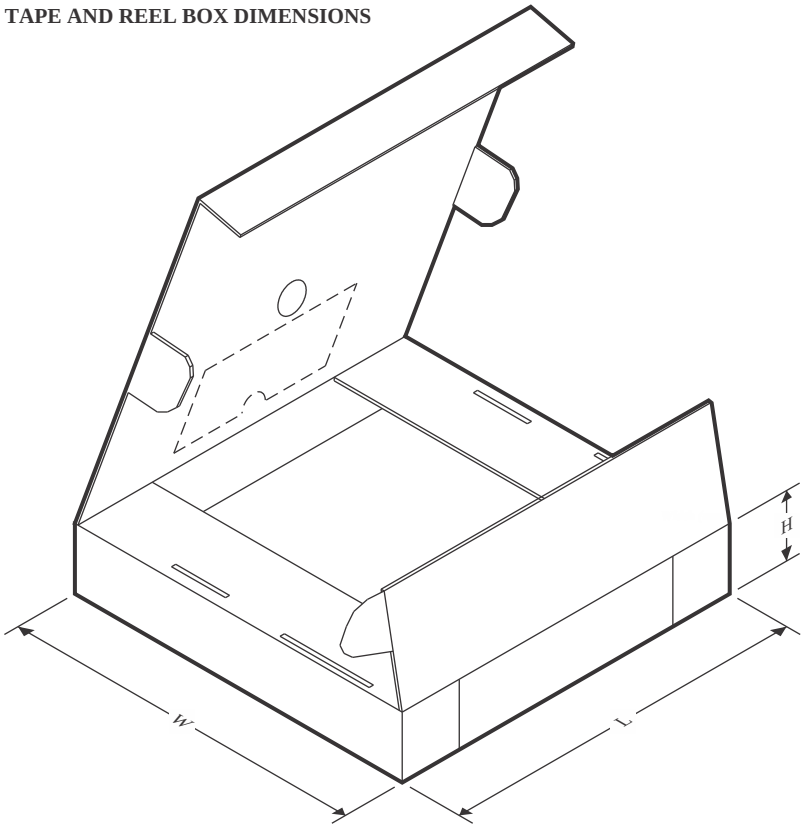
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TVS5800VEBR	UQFN-HR	VEB	6	3000	180.0	8.4	1.85	1.85	0.85	4.0	8.0	Q1

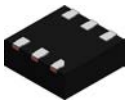
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TVS5800VEBR	UQFN-HR	VEB	6	3000	210.0	185.0	35.0

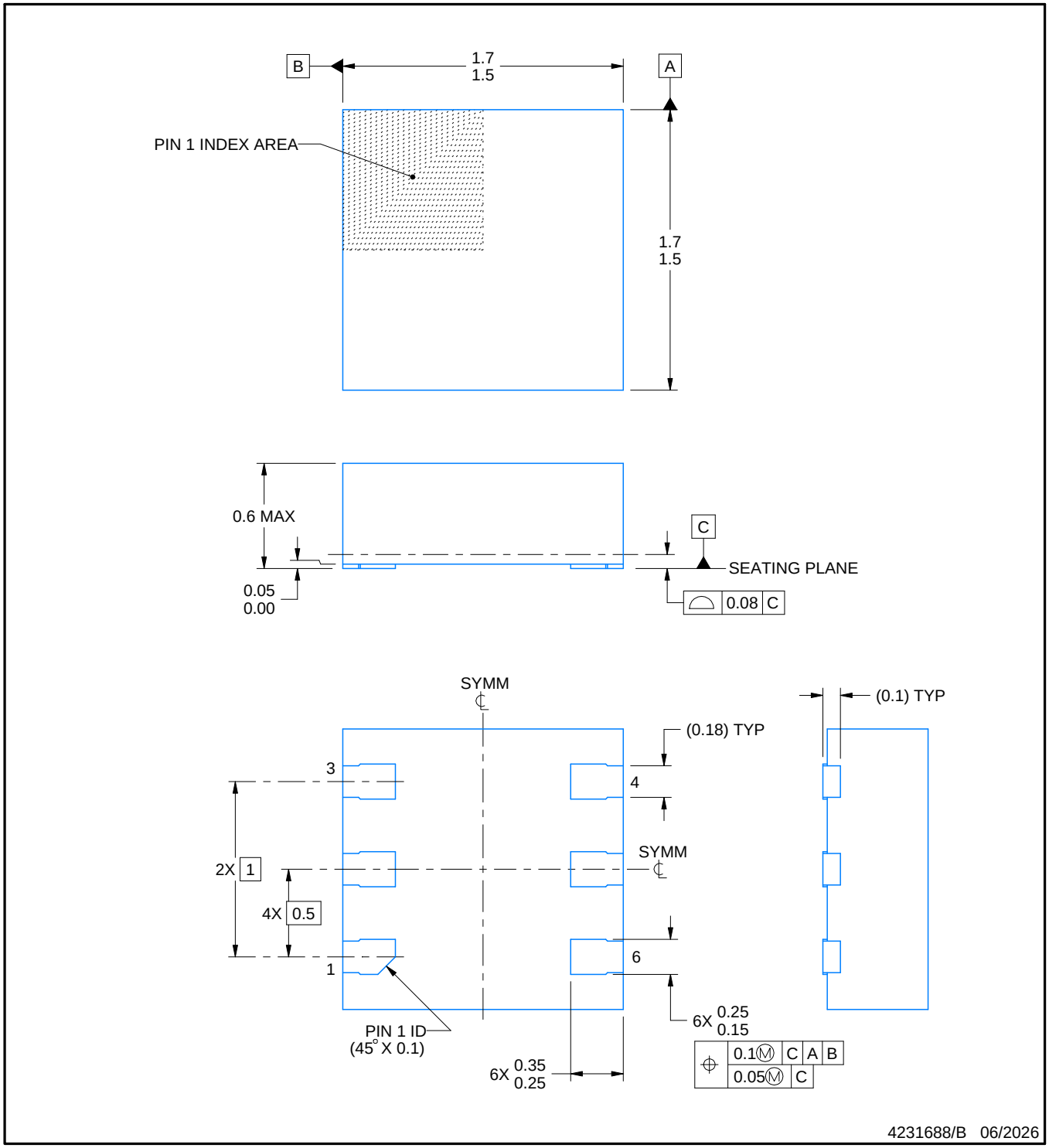
VEB0006A



PACKAGE OUTLINE

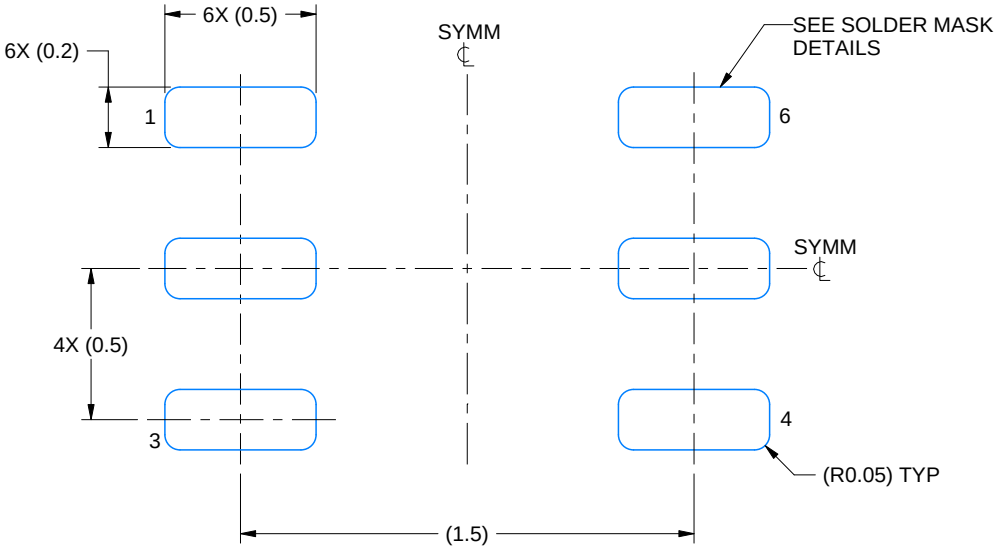
UQFN-HR - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

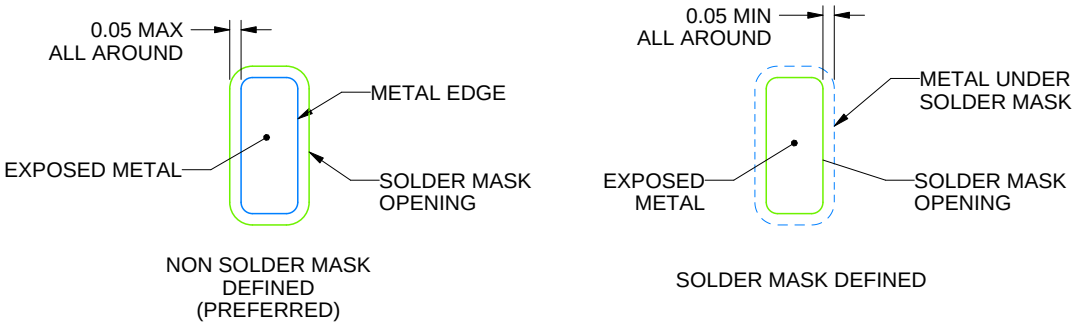


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 40X



SOLDER MASK DETAILS

4231688/B 06/2026

NOTES: (continued)

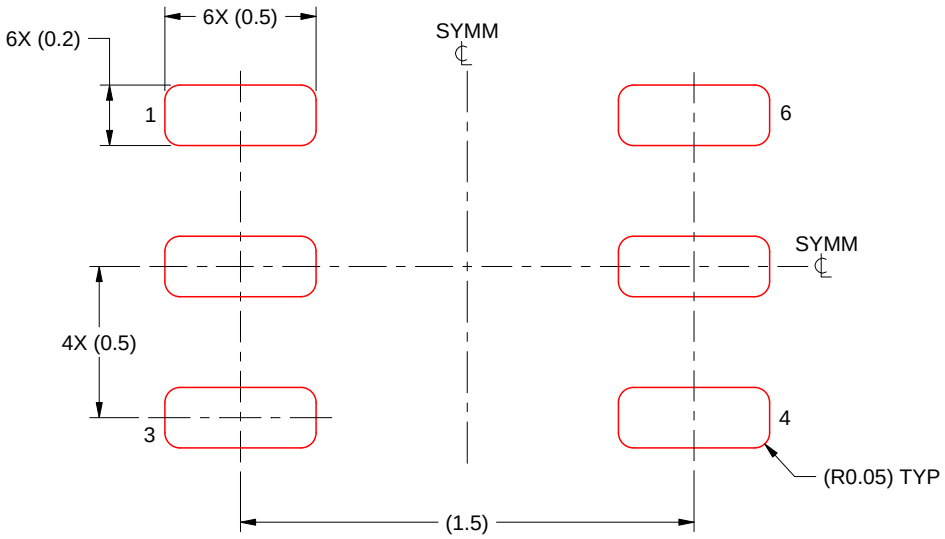
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

VEB0006A

UQFN-HR - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 40X

4231688/B 06/2026

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025