TXS0104W 4-Bit Bidirectional Voltage-Level Translator for Open-Drain and Push-Pull Applications

1 Features

- No direction-control signal needed
- Maximum data rates:
  - 50Mbps (push pull)
  - 2Mbps (open drain)
- 1.2V to 3.6V on A port and 1.65V to 5.5V on B port
- No power-supply sequencing required – either VCCA or VCCB can be ramped first
- VCCA can be >, =, < VCCB
- Latch-up performance exceeds 100mA per JESD 78, class II
- ESD protection exceeds JESD 22:
  - A port:
    - 2000V Human-Body Model (A114-B)
    - 200V Machine Model (A115-A)
    - 1000V Charged-Device Model (C101)
  - B port:
    - 8kV Human-Body Model (A114-B)
    - 200V Machine Model (A115-A)
    - 1000V Charged-Device Model (C101)

2 Applications

- Handset
- Smartphone
- Tablet
- Desktop PC

3 Description

The TXS0104W is a 4-bit non-inverting translator, which uses two separate configurable power-supply rails. The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 1.2V to 3.6V. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 1.65V to 5.5V. This allows for low-voltage bidirectional translation between any of the 1.2V, 1.8V, 2.V, 3.3V, and 5V voltage nodes.

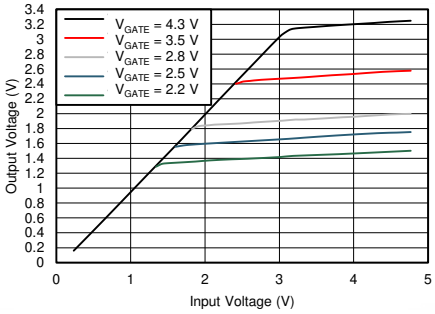
When the output-enable (OE) input is low, all outputs are placed in the high-impedance state. The TXS0104W is designed so that the OE input circuit is supplied by V_{CCA}.

For the high-impedance state during power up or power down, tie OE to GND through a pull-down resistor. The minimum value of the resistor is determined by the current-sourcing capability of the driver.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TXS0104W	D (SOIC, 14)	8.65mm x 6mm
	PW (TSSOP, 14)	5mm × 6.4mm
	RGY (VQFN, 14)	3.5mm × 3.5mm
	BQA (WQFN, 12)	3mm × 2.5mm
	RUT (UQFN, 12)	2.00mm × 1.70mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Transfer Characteristics of an N-Channel Transistor

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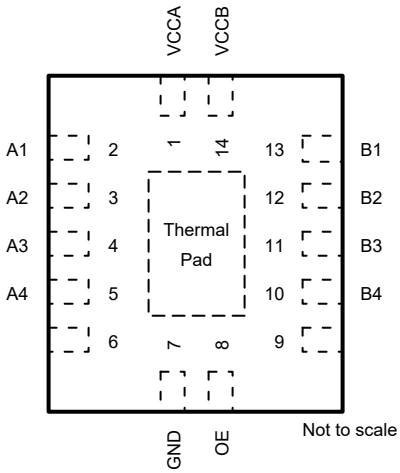
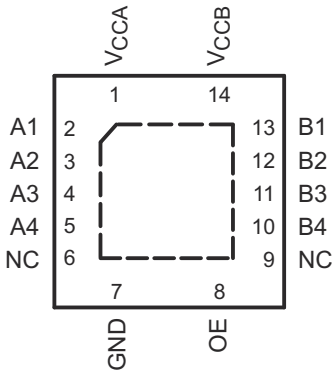


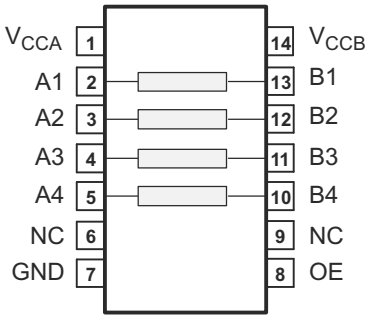
NC - No internal connection

Figure 4-1. BQA Package, 14-Pin WQFN (Top View)



NC - No internal connection

Figure 4-2. RGY Package, 14-Pin VQFN (Top View)



NC - No internal connection

Figure 4-3. D and PW Package, 14-Pin SOIC and TSSOP (Top View)

Table 4-1. Pin Functions: D, PW, or RGY

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
A1	2	I/O	Input/output A1. Referenced to V_{CCA}.
A2	3	I/O	Input/output A2. Referenced to V_{CCA}.
A3	4	I/O	Input/output A3. Referenced to V_{CCA}.
A4	5	I/O	Input/output A4. Referenced to V_{CCA}.
B1	13	I/O	Input/output B1. Referenced to V_{CCB}.
B2	12	I/O	Input/output B2. Referenced to V_{CCB}.
B3	11	I/O	Input/output B3. Referenced to V_{CCB}.
B4	10	I/O	Input/output B4. Referenced to V_{CCB}.
GND	7	—	Ground
OE	8	I	3-state output-mode enable. Pull OE low to place all outputs in 3-state mode. Referenced to V_{CCA}.
V_{CCA}	1	—	A-port supply voltage. $1.2V \le V_{CCA} \le 3.6V$ and V_{CCA} can be greater than, less than, or equal to V_{CCB}.
V_{CCB}	14	—	B-port supply voltage. $1.65V \le V_{CCB} \le 5.5V$.
Thermal Pad		—	For the RGY package, the exposed center thermal pad must be connected to ground

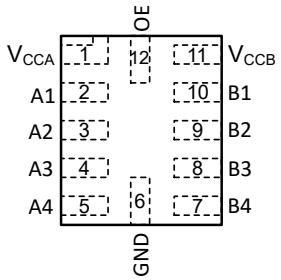


Figure 4-4. RUT Package, 12-Pin UQFN (Transparent Top View)

Table 4-2. Pin Functions: RUT

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
A1	2	I/O	Input/output A1. Referenced to V_{CCA}.
A2	3	I/O	Input/output A2. Referenced to V_{CCA}.
A3	4	I/O	Input/output A3. Referenced to V_{CCA}.
A4	5	I/O	Input/output A4. Referenced to V_{CCA}.
B1	10	I/O	Input/output B1. Referenced to V_{CCB}.
B2	9	I/O	Input/output B2. Referenced to V_{CCB}.
B3	8	I/O	Input/output B3. Referenced to V_{CCB}.
B4	7	I/O	Input/output B4. Referenced to V_{CCB}.
GND	6	—	Ground
OE	12	I	3-state output-mode enable. Pull OE low to place all outputs in 3-state mode. Referenced to V_{CCA}.
V_{CCA}	1	—	A-port supply voltage. $1.2V \le V_{CCA} \le 3.6V$ and V_{CCA} can be greater than, less than, or equal to V_{CCB}.
V_{CCB}	11	—	B-port supply voltage. $2.3V \le V_{CCB} \le 5.5V$

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage A		–0.5	4.6	V
V_{CCB}	Supply voltage B		–0.5	6.5	V
V_I	Input Voltage(2)	I/O Ports (A Port)	–0.5	4.6	V
		I/O Ports (B Port)	–0.5	6.5	
		OE	–0.5	6.5	
V_O	Voltage applied to any output in the high-impedance or power-off state(2)	A Port	–0.5	4.6	V
		B Port	–0.5	6.5	
V_O	Voltage applied to any output in the high or low state(2) (3)	A Port	–0.5	V_{CCA} + 0.5	V
		B Port	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	V_I < 0	–50		mA
I_{OK}	Output clamp current	V_O < 0	–50		mA
I_O	Continuous output current		–50	50	mA
	Continuous current through V_{CC} or GND		–100	100	mA
T_j	Junction Temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Section 5.1* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Section 5.3* Exposure beyond the limits listed in *Section 5.3* may affect device reliability.
(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 6.5 V maximum if the output current rating is observed.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	A Port	±2000	V
			B Port	±8000	
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002	A Port	±1000	
			B Port	±1000	

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			V_{CCA}	V_{CCB}	MIN	MAX	UNIT
V_{CCA}	Supply voltage A				1.2	3.6	V
V_{CCB}	Supply voltage B				1.65	5.5	V
V_{IH}	High-level input voltage	A-port I/O's	1.2 V to 1.6 V	1.65 V to 5.5 V	V_{CCA} - 0.2	V_{CCA}	V
			1.65 V to 3.6 V	2.3 V to 5.5 V	V_{CCA} - 0.4	V_{CCA}	
		B-port I/O's	1.2 V to 3.6 V	1.65 V to 5.5 V	V_{CCB} - 0.4	V_{CCB}	
		OE Input	1.2 V to 3.6 V	1.65 V to 5.5 V	V_{CCA} x 0.65	5.5	

over operating free-air temperature range (unless otherwise noted)

			V_{CCA}	V_{CCB}	MIN	MAX	UNIT
V_{IL}	Low-level input voltage	A-port I/O's	1.2 V to 3.6 V	1.65 V to 5.5 V		0.2	V
		B-port I/O's	1.2 V to 3.6 V	1.65 V to 5.5 V		0.2	
		OE Input	1.2 V to 3.6 V	1.65 V to 5.5 V		V_{CCA} x 0.35	
V_{RTA}	RTA Activation Threshold	A-port I/O's	1.2 V to 3.6 V	1.65 V to 5.5 V	V_{CCI} x 0.30		V
		B-port I/O's	1.2 V to 3.6 V	1.65 V to 5.5 V	V_{CCI} x 0.30		
Δt/Δv	Input transition rise and fall time	Push-Pull Driving	1.2 V to 3.6 V	1.65 V to 5.5 V		10	ns/V
T_A	Operating free-air temperature				–40	125	°C

5.4 Thermal Information

THERMAL METRIC(1)		TXS0104W					UNIT
		RGY (VQFN)	BQA (WQFN)	RUT (UQFN)	D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	12 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	52.9	73.5	150.4	93.7	115.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.3	76.9	68.6	53.8	46.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	28.4	43.0	76.3	52.0	70.9	°C/W
Y_{JT}	Junction-to-top characterization parameter	2.7	4.7	2.4	13.4	3.4	°C/W
Y_{JB}	Junction-to-board characterization parameter	28.3	42.9	76.2	51.6	70.2	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case (bottom) thermal resistance	12	19.6	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	Operating free-air temperature (T_A)									UNIT
					25°C			–40°C to 85°C			–40°C to 125°C			
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{OHA}	Port A output high voltage (2)	I_{OH} = –20 uA $V_{I(Bx)} \geq V_{CCB}$ - 0.4 V	1.2 V to 3.6 V	1.65 V to 5.5 V	V_{CCA} x 0.8			V_{CCA} x 0.8			V_{CCA} x 0.8			V
			1.65 V to 3.6 V	1.65 V to 5.5 V	V_{CCA} x 0.8			V_{CCA} x 0.8			V_{CCA} x 0.8			
V_{OHB}	Port B output high voltage	I_{OH} = –20 uA $V_{I(Ax)} \geq V_{CCA}$ - 0.4 V	1.2 V to 3.6 V	1.65 V to 5.5 V	V_{CCB} x 0.8			V_{CCB} x 0.8			V_{CCB} x 0.8			
			1.65 V to 3.6 V	1.65 V to 5.5 V	V_{CCB} x 0.8			V_{CCB} x 0.8			V_{CCB} x 0.8			V
V_{OLA}	Low-level output voltage (3)	I_{OL} = 1 mA $V_{I(Bx)} \leq$ 0.15 V	1.2 V to 3.6 V	1.65 V to 5.5 V			0.4			0.4			0.4	V

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	Operating free-air temperature (T_A)									UNIT
					25°C			–40°C to 85°C			–40°C to 125°C			
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{OLB}	Low-level output voltage (3)	I_{OL} = 1 mA $V_{I(Ax)}$ ≤ 0.15 V	1.2 V to 3.6 V	1.65 V to 5.5 V			0.4			0.4			0.4	V
I_I	Input leakage current	OE V_I = V_{CC} or GND	1.2 V to 3.6 V	1.65 V to 5.5 V	-2		2	-2		2	-2		2	µA
I_{OZ}	Tri-state output current	A or B Port: V_I = V_{CCI} or GND V_O = V_{CCO} or GND OE = GND	1.2 V to 3.6 V	1.65 V to 5.5 V	–1		1	–2		2	–3		3	µA
I_{CCA}	V_{CCA} supply current	V_I = V_{CCI} or GND I_O = 0	1.2 V to 3.6 V	1.65 V to 5.5 V			2.4			3.3			6.2	µA
			0 V	5.5 V	–3			–3			–3			
			3.6 V	0 V			2.2			2.2			2.2	
I_{CCB}	V_{CCB} supply current	V_I = V_{CCI} or GND I_O = 0	1.2 V to 3.6 V	1.65 V to 5.5 V			12			12			21	µA
			0 V	5.5 V			5			5			8	
			3.6 V	0 V	-1			–1			–1			
I_{CCA} + I_{CCB}	Combined supply current	V_I = V_{CCI} or GND I_O = 0	1.2 V to 3.6 V	1.65 V to 5.5 V			14.4			14.4			25	µA
C_i	Control Input Capacitance	V_I = 3.3 V or GND	3.3 V	3.3 V			6			6			6	pF
C_{io}	Data I/O Capacitance	OE = GND, V_O = 1.65V DC +1 MHz -16 dBm sine wave	3.3 V	3.3 V		5	6.5		12	16.5		12	16.5	pF

(1) V_{CCI} is the V_{CC} associated with the input port
(2) Tested at V_I = $V_{T+(MAX)}$
(3) Tested at V_I = $V_{T-(MIN)}$

5.6 Switching Characteristics, V_{CCA} = 1.2 V

PARAMETER		FROM	TO	Test Conditions		B-Port Supply Voltage (V_{CCB})								UNIT
						1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V		5.0 ± 0.5 V		
						MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PHL}	Propagation Delay (Hight-to-Low)	A	B	Push-Pull	-40°C to 125°C		6.7		7.3		8.3		9.8	ns
				Open-Drain			7.2		8.4		10		12.7	
t_{PLH}	Propagation Delay (Low-to-High)			Push-Pull			16		13.8		15.3		29.5	
				Open-Drain			58.7		53.1		49		55.2	
t_{PHL}	Propagation Delay (Hight-to-Low)	B	A	Push-Pull			3.9		3.9		4.3		5.5	ns
				Open-Drain			4.1		4.3		4.9		6.2	
t_{PLH}	Propagation Delay (Low-to-High)			Push-Pull			1.4		0.6		0.2		0.5	
				Open-Drain			0.6		0.5		0.5		0.5	
t_{en}	Enable Time	OE	A or B				260		179.5		142.5		107	ns
t_{dis}	Disable Time	OE	A or B				260		200		250		250	
t_{rA}	Ouput Rise Time	B	A	Push-Pull			22.7		18.4		16.3		14.2	ns
				Open-Drain			221.5		173.3		145.9		119.4	
t_{rB}		A	B	Push-Pull			20.6		16.8		15.9		22.1	
				Open-Drain			148.1		108.4		81.6		55.5	
t_{fA}	Output Fall Time	B	A	Push-Pull			5.6		4.8		4.7		5	ns
				Open-Drain			6.1		5.5		5.8		6.4	
t_{fB}		A	B	Push-Pull			12		13.1		15.2		19.9	
				Open-Drain			13.2		15.4		19.1		26.7	

5.7 Switching Characteristics, V_{CCA} = 1.5 ± 0.1 V

PARAMETER		FROM	TO	Test Conditions		B-Port Supply Voltage (V_{CCB})								UNIT
						1.8 ± 0.15 V			2.5 ± 0.2 V			3.3 ± 0.3 V			5.0 ± 0.5 V			
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Propagation Delay (Hight-to-Low)	A	B	Push-Pull	-40°C to 125°C		4			3.9			4.5			5.6		ns
				Open-Drain			4			4.3			5			6.4		
t_{PLH}	Propagation Delay (Low-to-High)			Push-Pull			9.1			6.8			6.2			6		
				Open-Drain			12.5			10.7			10.5			10.4		
t_{PHL}	Propagation Delay (Hight-to-Low)	B	A	Push-Pull			3			2.9			3.3			4.3		
				Open-Drain			3			3.1			3.5			4.7		
t_{PLH}	Propagation Delay (Low-to-High)			Push-Pull			1.8			1			0.3			1		
				Open-Drain			4			1			1			1		
t_{en}	Enable Time	OE	A or B				250			200			200			100		ns
t_{dis}	Disable Time	OE	A or B				250			200			250			160		
t_{rA}	Ouput Rise Time	B	A	Push-Pull			12.5			9.5			7.9			7		ns
				Open-Drain			166.3			130			102.1			73.7		
t_{rB}		A	B	Push-Pull			14.3			10.8			9.4			8.2		
				Open-Drain			150			110			79			43.1		
t_{fA}	Output Fall Time	B	A	Push-Pull			4			3.3			3.2			3.4		
				Open-Drain			4.1			3.5			3.5			3.8		
t_{fB}		A	B	Push-Pull			7			6.9			7.8			10		
				Open-Drain			7.2			7.5			8.8			11.5		

5.8 Switching Characteristics, V_{CCA} = 1.8 ± 0.15 V

PARAMETER		FROM	TO	Test Conditions		B-Port Supply Voltage (V_{CCB})								UNIT
						1.8 ± 0.15 V			2.5 ± 0.2 V			3.3 ± 0.3 V			5.0 ± 0.5 V			
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Propagation Delay (Hight-to-Low)	A	B	Push-Pull	-40°C to 125°C		6			6			5.8			5.8		ns
				Open-Drain			8.8			8.8			9.6			10		
t_{PLH}	Propagation Delay (Low-to-High)			Push-Pull			8			7.7			6.8			7		
				Open-Drain			50			50			26			33		
t_{PHL}	Propagation Delay (Hight-to-Low)	B	A	Push-Pull			4.4			4.4			4.5			4.7		
				Open-Drain			5.3			5.3			4.4			4.5		
t_{PLH}	Propagation Delay (Low-to-High)			Push-Pull			5.3			5.3			4.5			4.7		
				Open-Drain			36			36			16			20		
t_{en}	Enable Time	OE	A or B				200			200			200			200		ns
t_{dis}	Disable Time	OE	A or B				250			200			250			200		
t_{rA}	Ouput Rise Time	B	A	Push-Pull			11.4			9.5			9.3			15		ns
				Open-Drain			199			199			150			109		
		A	B	Push-Pull			13.3			10.8			9.1			7.6		
				Open-Drain			186			186			112			58		
t_{fA}	Output Fall Time	B	A	Push-Pull			5.9			5.9			6			13.3		
				Open-Drain			6.9			6.9			6.4			6.1		
		A	B	Push-Pull			7.6			7.6			7.5			8.8		
				Open-Drain			13.8			13.8			16.2			16.2		

5.9 Switching Characteristics, V_{CCA} = 2.5 ± 0.2 V

PARAMETER		FROM	TO	Test Conditions		B-Port Supply Voltage (V_{CCB})								UNIT
						1.8 ± 0.15 V			2.5 ± 0.2 V			3.3 ± 0.3 V			5.0 ± 0.5 V			
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Propagation Delay (Hight-to-Low)	A	B	Push-Pull	-40°C to 125°C		3.2			3.2			3.3			3.4		ns
				Open-Drain			6.3			6.3			6			5.8		
t_{PLH}	Propagation Delay (Low-to-High)			Push-Pull			3.8			3.8			4.1			4.4		
				Open-Drain			3.5			3.5			4.1			4.4		
t_{PHL}	Propagation Delay (Hight-to-Low)	B	A	Push-Pull			3			3			3.6			4.3		
				Open-Drain			4.7			4.7			4.2			4		
t_{PLH}	Propagation Delay (Low-to-High)			Push-Pull			8.7			2.5			1.6			0.7		
				Open-Drain			29.9			2.5			1.6			1		
t_{en}	Enable Time	OE	A or B				200			200			200			200		ns
t_{dis}	Disable Time	OE	A or B				250			200			200			200		
t_{rA}	Ouput Rise Time	B	A	Push-Pull			10.6			7.4			6.6			5.6		ns
				Open-Drain			180			180			150			105		
t_{rB}		A	B	Push-Pull			11.9			8.8			7.6			6.6		
				Open-Drain			170			170			120			64		
t_{fA}	Output Fall Time	B	A	Push-Pull			5.7			5.7			5.5			5.3		
				Open-Drain			5.8			5.8			5.8			5.8		
t_{fB}		A	B	Push-Pull			7.8			7.8			6.7			6.6		
				Open-Drain			8.8			8.8			9.4			10.4		

5.10 Switching Characteristics, V_{CCA} = 3.3 ± 0.3 V

PARAMETER		FROM	TO	Test Conditions		B-Port Supply Voltage (V_{CCB})								UNIT
						1.8 ± 0.15 V			2.5 ± 0.2 V			3.3 ± 0.3 V			5.0 ± 0.5 V			
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Propagation Delay (Hight-to-Low)	A	B	Push-Pull	-40°C to 125°C		3.5			2.8			2.4			3.1		ns
				Open-Drain			4.2			4.2			4.2			4.6		
t_{PLH}	Propagation Delay (Low-to-High)			Push-Pull			4.2			4.2			4.2			4.4		
				Open-Drain			4.2			4.2			4.2			4.4		
t_{PHL}	Propagation Delay (Hight-to-Low)	B	A	Push-Pull			2.9			2.5			2.5			3.3		
				Open-Drain			124			124			124			97		
t_{PLH}	Propagation Delay (Low-to-High)			Push-Pull			10			5			2.5			2.6		
				Open-Drain			27.5			15			2.5			3.3		
t_{en}	Enable Time	OE	A or B				200			200			200			200		ns
t_{dis}	Disable Time						250			200			250			200		
t_{rA}	Ouput Rise Time	B	A	Push-Pull			11.6			6.9			5.8			5		ns
				Open-Drain			140			140			140			102		
t_{rB}		A	B	Push-Pull			11.3			8.1			6.8			7.4		
				Open-Drain			135			130			130			75		
t_{fA}	Output Fall Time	B	A	Push-Pull			5.4			5.4			5.4			5		
				Open-Drain			6.1			6.1			6.1			5.7		
t_{fB}		A	B	Push-Pull			7.4			7.4			7.4			7.6		
				Open-Drain			7.6			7.6			7.6			8.3		

5.11 Switching Characteristics: T_{sk}, T_{MAX}

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CCA}	V_{CCB}	Operating free-air temperature (T_A) -40°C to 125°C			UNIT
					MIN	TYP	MAX	
TMAX - Maximum Data Rate	50% Duty Cycle InputOne channel switching	Push-Pull Driving	1.2 V ± 0.1 V	1.8 ± 0.15 V	24			Mbps
				2.5 V ± 0.2 V	24			
				3.3 V ± 0.3 V	24			
				5 V ± 0.5 V	24			
			1.5 V ± 0.1 V	1.8 ± 0.15 V	24			
				2.5 V ± 0.2 V	24			
				3.3 V ± 0.3 V	24			
				5 V ± 0.5 V	24			
			1.8 ± 0.15 V	1.8 ± 0.15 V	50			
				2.5 V ± 0.2 V	50			
				3.3 V ± 0.3 V	50			
				5 V ± 0.5 V	50			
			2.5 V ± 0.2 V	1.8 ± 0.15 V	50			
				2.5 V ± 0.2 V	50			
				3.3 V ± 0.3 V	50			
				5 V ± 0.5 V	50			
			3.3 V ± 0.3 V	1.8 ± 0.15 V	50			
				2.5 V ± 0.2 V	50			
				3.3 V ± 0.3 V	50			
				5 V ± 0.5 V	50			
		Open-Drain Driving	1.2 V ± 0.1 V	1.8 ± 0.15 V	1			
				2.5 V ± 0.2 V	1			
				3.3 V ± 0.3 V	1			
				5 V ± 0.5 V	1			
			1.5 V ± 0.1 V	1.8 ± 0.15 V	2			
				2.5 V ± 0.2 V	2			
				3.3 V ± 0.3 V	2			
				5 V ± 0.5 V	2			
			1.8 ± 0.15 V	1.8 ± 0.15 V	2			
				2.5 V ± 0.2 V	2			
				3.3 V ± 0.3 V	2			
				5 V ± 0.5 V	2			
			2.5 V ± 0.2 V	1.8 ± 0.15 V	2			
				2.5 V ± 0.2 V	2			
				3.3 V ± 0.3 V	2			
				5 V ± 0.5 V	2			
			3.3 V ± 0.3 V	1.8 ± 0.15 V	2			
				2.5 V ± 0.2 V	2			
				3.3 V ± 0.3 V	2			
				5 V ± 0.5 V	2			

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CCA}	V_{CCB}	Operating free-air temperature (T_A)			UNIT
					-40°C to 125°C			
					MIN	TYP	MAX	
t_w	Pulse Duration, Data Inputs	Push-Pull Driving	1.2 V ± 0.1 V to 3.3 V ± 0.3 V	1.8 V ± 0.15 V to 5.5 V ± 0.5 V	41			ns
		Open-Drain Driving	1.2 V ± 0.1 V to 3.3 V ± 0.3 V	1.8 V ± 0.15 V to 5.5 V ± 0.5 V	500			
t_{sk} - Output skew	Skew between any two outputs of the same package switching in the same direction	Push-Pull Driving	1.65 V to 3.6 V	2.3 V to 5.5 V			1	ns
		Open-Drain Driving	1.65 V to 3.6 V	2.3 V to 5.5 V			1	

5.12 Typical Characteristics

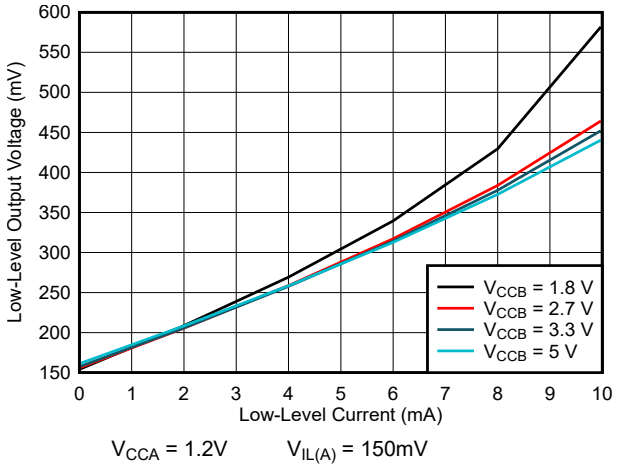


Figure 5-1. Low-Level Output Voltage ($V_{OL(Ax)}$) vs Low-Level Current ($I_{OL(Ax)}$)

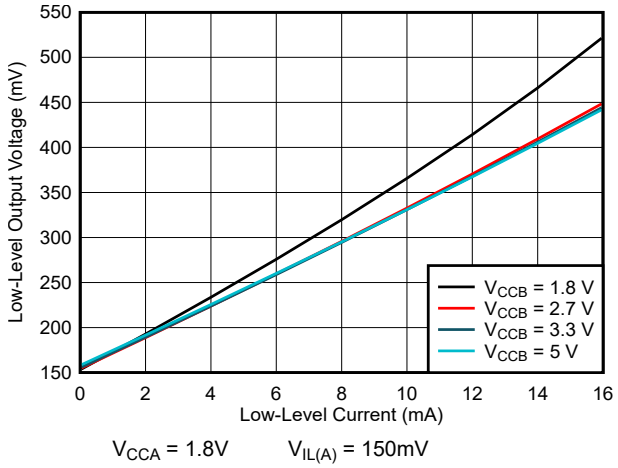


Figure 5-2. Low-Level Output Voltage ($V_{OL(Ax)}$) vs Low-Level Current ($I_{OL(Ax)}$)

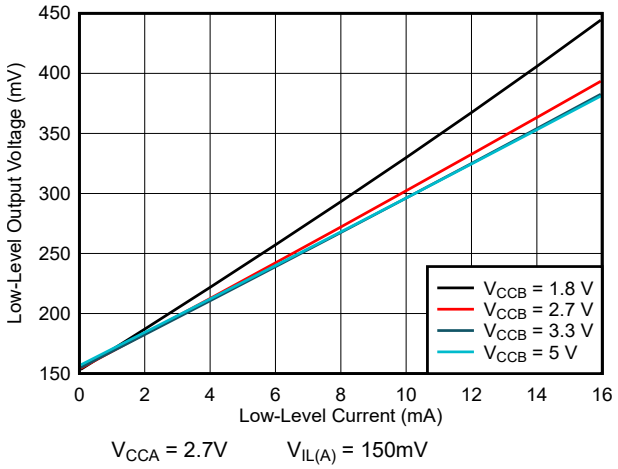


Figure 5-3. Low-Level Output Voltage ($V_{OL(Ax)}$) vs Low-Level Current ($I_{OL(Ax)}$)

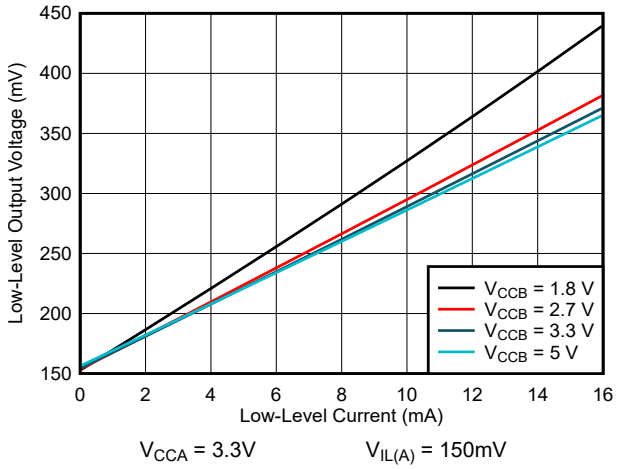


Figure 5-4. Low-Level Output Voltage ($V_{OL(Ax)}$) vs Low-Level Current ($I_{OL(Ax)}$)

6 Parameter Measurement Information

6.1 Load Circuits

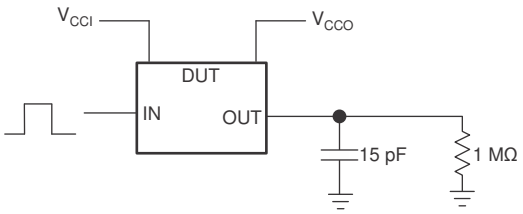


Figure 6-1. Data Rate, Pulse Duration, Propagation Delay, Output Rise-Time and Fall-Time Measurement Using a Push-Pull Driver

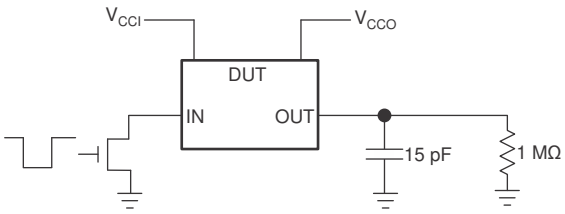
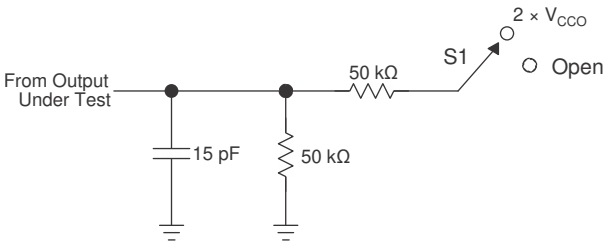


Figure 6-2. Data Rate, Pulse Duration, Propagation Delay, Output Rise-Time and Fall-Time Measurement Using an Open-Drain Driver



TEST	S1
t_{PZL} / t_{PLZ} (t_{dis})	2 × V_{CCO}
t_{PHZ} / t_{PZH} (t_{en})	Open

Figure 6-3. Load Circuit for Enable-Time and Disable-Time Measurement

1. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
2. t_{PZL} and t_{PZH} are the same as t_{en}.
3. V_{CCI} is the V_{CC} associated with the input port.
4. V_{CCO} is the V_{CC} associated with the output port.

6.2 Voltage Waveforms

The outputs are measured one at a time, with one transition per measurement. All input pulses are supplied by generators that have the following characteristics:

- PRR ≤ 10MHz
- Z_O = 50Ω
- dv/dt ≥ 1V/ns

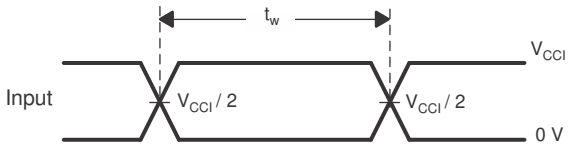


Figure 6-4. Pulse Duration

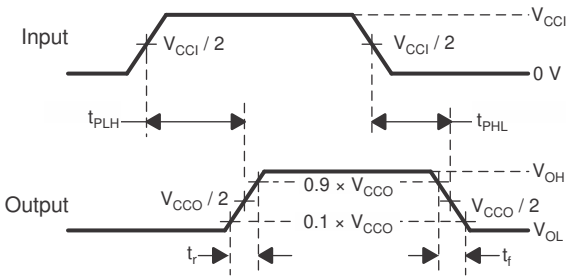
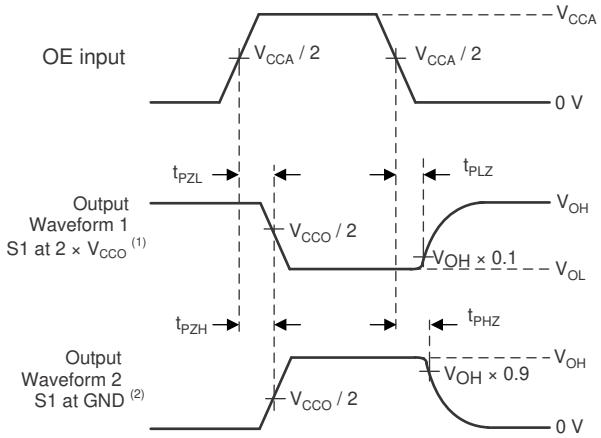


Figure 6-5. Propagation Delay Times



A. Waveform 1 is for an output with internal such that the output is high, except when OE is high (see Figure 6-3).

B. Waveform 2 is for an output with conditions such that the output is low, except when OE is high.

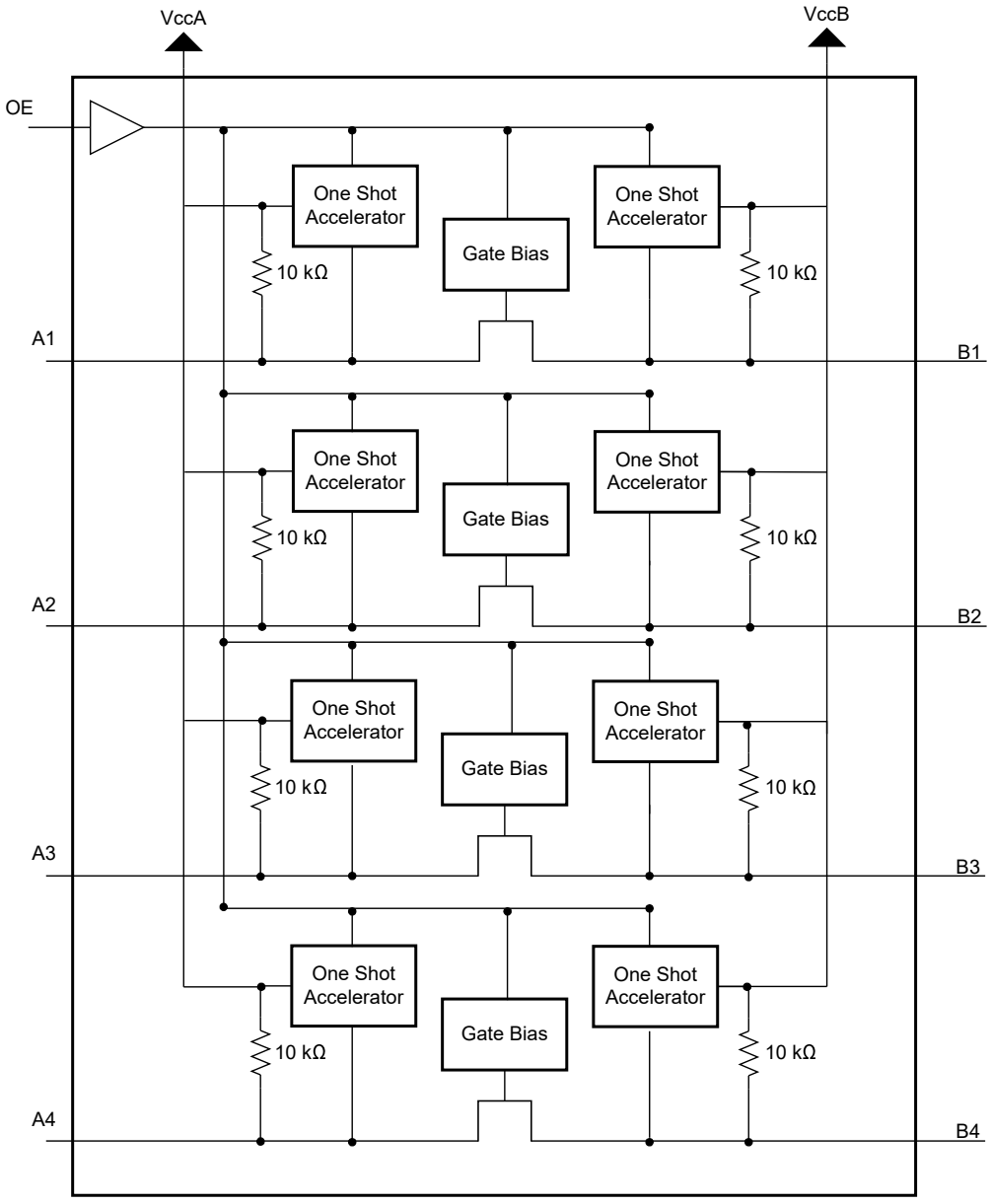
Figure 6-6. Enable and Disable Times

7 Detailed Description

7.1 Overview

The TXS0104W device is a directionless voltage-level translator specifically designed for translating logic voltage levels. The A port is able to accept I/O voltages ranging from 1.2V to 3.6V, while the B port can accept I/O voltages from 1.65V to 5.5V. The device is a pass gate architecture with edge rate accelerators (one shots) to improve the overall data rate. 10kΩ pullup resistors, commonly used in open drain applications, have been conveniently integrated so that an external resistor is not needed. While this device is designed for open drain applications, the device can also translate push-pull CMOS logic outputs.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Architecture

The TXS0104W architecture (see Figure 7-1) does not require a direction-control signal in order to control the direction of data flow from A to B or from B to A.

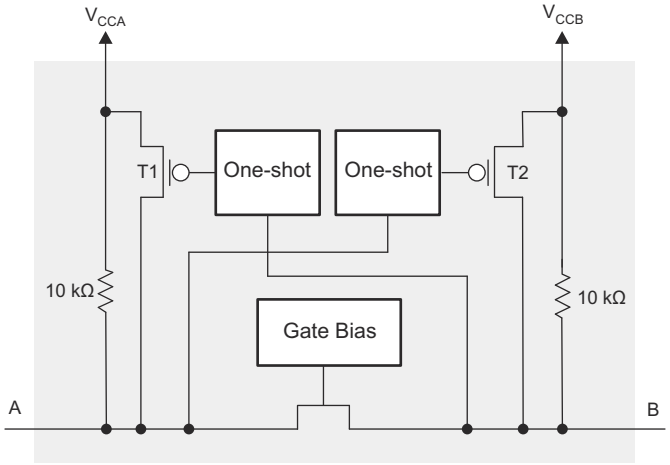


Figure 7-1. Architecture of a TXS0104W Cell

Each A-port I/O has an internal 10kΩ pullup resistor to V_{CCA}, and each B-port I/O has an internal 10kΩ pullup resistor to V_{CCB}. The output one-shots detect rising edges on the A or B ports. During a rising edge, the one-shot turns on the PMOS transistors (T1, T2) for a short duration which speeds up the low-to-high transition.

7.3.2 Input Driver Requirements

The fall time (t_{fA}, t_{fB}) of a signal depends on the output impedance of the external device driving the data I/Os of the TXS0104W device. Similarly, the t_{PHL} and maximum data rates also depend on the output impedance of the external driver. The values for t_{fA}, t_{fB}, t_{PHL}, and maximum data rates in the data sheet assume that the output impedance of the external driver is less than 50Ω.

7.3.3 Enable and Disable

The TXS0104W device has an OE input that disables the device by setting OE low, which places all I/Os in the high-impedance state. The disable time (t_{dis}) indicates the delay between the time when the OE pin goes low and when the outputs actually enter the high-impedance state. The enable time (t_{en}) indicates the amount of time the user must allow for the one-shot circuitry to become operational after the OE pin is taken high.

7.3.4 Pullup and Pulldown Resistors on I/O Lines

Each A-port I/O has an internal 10kΩ pullup resistor to V_{CCA}, and each B-port I/O has an internal 10-kΩ pullup resistor to V_{CCB}. If a smaller value of pullup resistor is required, an external resistor must be added from the I/O to V_{CCA} or V_{CCB} (in parallel with the internal 10-kΩ resistors).

7.4 Device Functional Modes

The TXS0104W device has two functional modes, enabled and disabled. To disable the device set the OE input low, which places all I/Os in a high impedance state. Setting the OE input high will enable the device.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TXS0104W device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The TXS0104W device is an excellent choice for applications where an open-drain driver is connected to the data I/Os. The TXS0104W device can also be used in applications where a push-pull driver is connected to the data I/Os, but the TXB0104 device might be a better option for such push-pull applications.

8.2 Typical Application

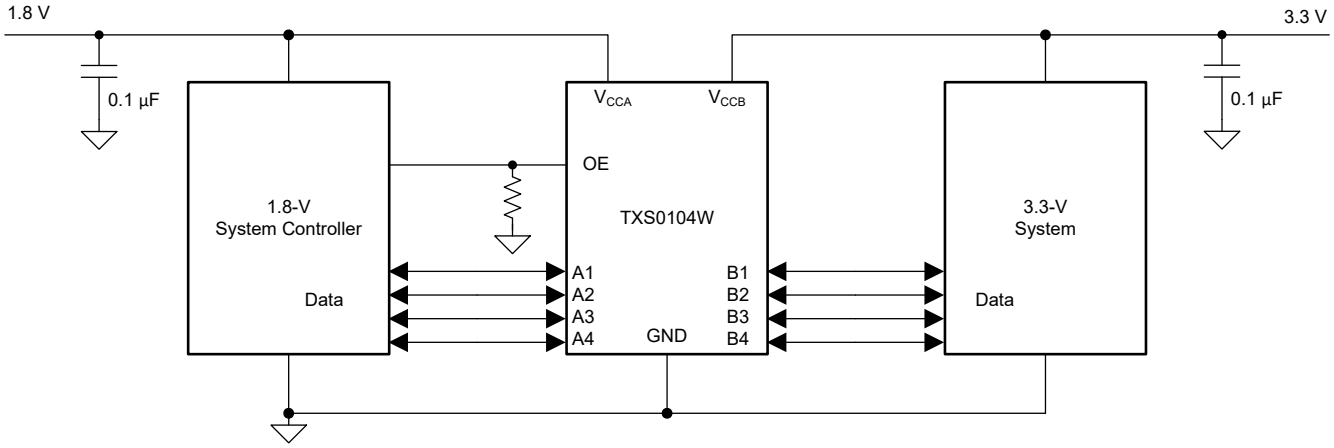


Figure 8-1. Application Schematic

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 8-1.

Table 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	1.2 to 3.6V
Output voltage range	1.65 to 5.5V

8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the TXS0104W device to determine the input voltage range. For a valid logic high the value must exceed the V_{IH} of the input port. For a valid logic low the value must be less than the V_{IL} of the input port.
- Output voltage range
  - Use the supply voltage of the device that the TXS0104W device is driving to determine the output voltage range.
  - The TXS0104W device has 10-kΩ internal pullup resistors. External pullup resistors can be added to reduce the total RC of a signal trace if necessary.
- An external pull down resistor decreases the output V_{OH} and V_{OL}. Use Equation 1 to calculate the V_{OH} as a result of an external pull down resistor.

$$V_{OH} = V_{CCx} \times R_{PD} / (R_{PD} + 10\ k\Omega) \quad (1)$$

where

V_{CCx} is the supply voltage on either V_{CCA} or V_{CCB}
R_{PD} is the value of the external pull down resistor

8.2.3 Application Curve

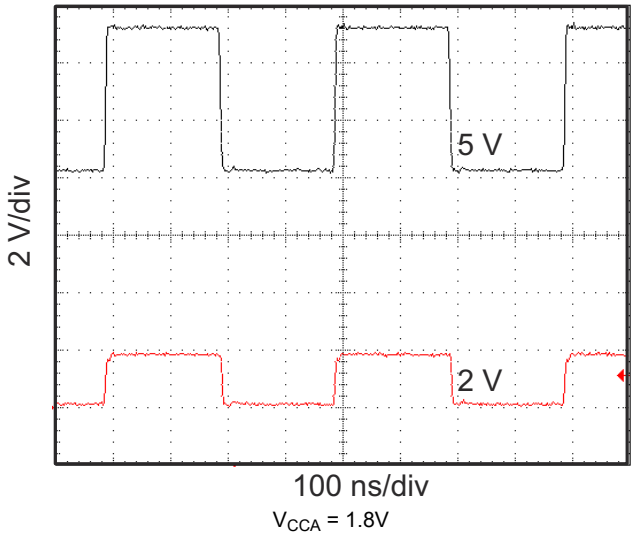


Figure 8-2. Level-Translation of a 2.5MHz Signal

8.3 Power Supply Recommendations

The TXS0104W device uses two separate configurable power-supply rails, V_{CCA} and V_{CCB}. V_{CCB} accepts any supply voltage from 1.65V to 5.5V and V_{CCA} accepts any supply voltage from 1.2V to 3.6V as long as Vs is less than or equal to V_{CCB}. The A port and B port are designed to track V_{CCA} and V_{CCB} respectively allowing for low-voltage bidirectional translation between any of the 1.8V, 2.5V, 3.3V, and 5V voltage nodes.

The TXS0104W device does not require power sequencing between V_{CCA} and V_{CCB} during power-up so the power-supply rails can be ramped in any order. A V_{CCA} value greater than or equal to V_{CCB} ($V_{CCA} \geq V_{CCB}$) does not damage the device.

The output-enable (OE) input circuit is designed so that it is supplied by V_{CCA} and when the (OE) input is low, all outputs are placed in the high-impedance state. For the high-impedance state of the outputs during power up or power down, the OE input pin must be tied to GND through a pulldown resistor and must not be enabled until V_{CCA} and V_{CCB} are fully ramped and stable. The minimum value of the pulldown resistor to ground is determined by the current-sourcing capability of the driver.

8.4 Layout

8.4.1 Layout Guidelines

For device reliability, following common printed-circuit board layout guidelines is recommended.

- Bypass capacitors should be used on power supplies.
- Short trace lengths should be used to avoid excessive loading.
- PCB signal trace-lengths must be kept short enough so that the round-trip delay of any reflection is less than the one shot duration, approximately 30ns, and encounters low impedance at the source driver.
- Placing pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals depending on the system requirements

8.4.2 Layout Example

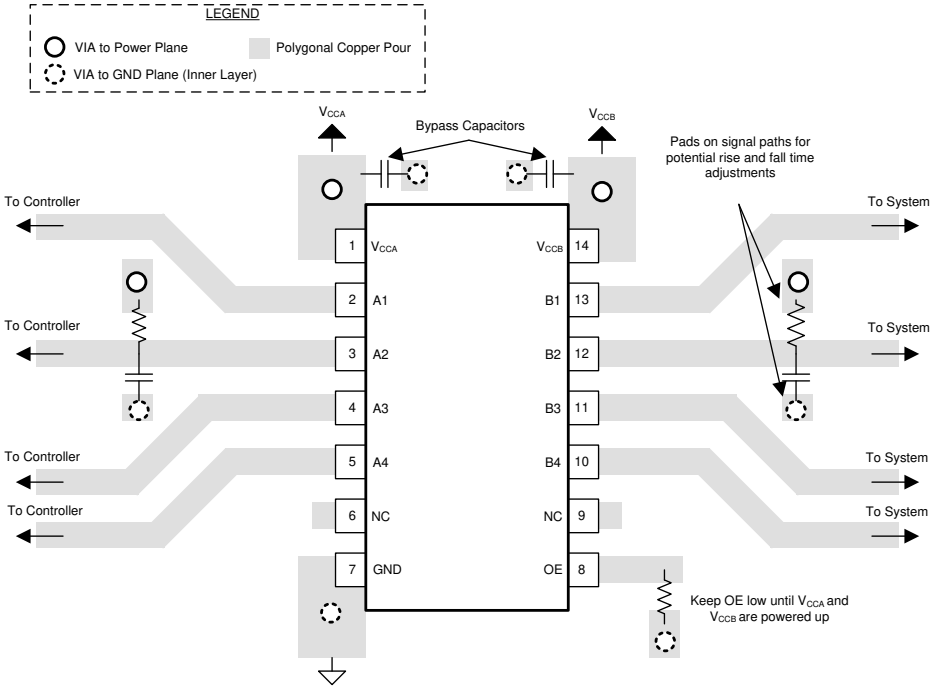


Figure 8-3. TXS0104W Layout Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Effects of External Pullup and Pulldown Resistors on TXS and TXB Devices* application report
- Texas Instruments, *Basics of Voltage Translation* application report
- Texas Instruments, *A Guide to Voltage Translation With TXS-Type Translators* application report

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2025) to Revision B (January 2026)	Page
• First public release of the data sheet	1

Changes from Revision * (June 2025) to Revision A (September 2025)	Page
• Added mechanical data and tape and reel information	25

DATE	REVISION	NOTES
June 2025	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TXS0104WRUTR	Active	Production	UQFN (RUT) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WRP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TXS0104W :

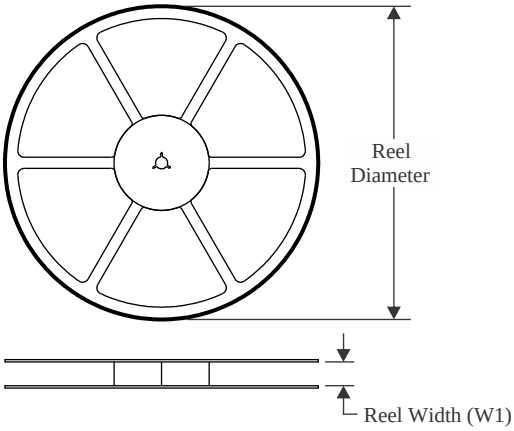
- Automotive : TXS0104W-Q1

NOTE: Qualified Version Definitions:

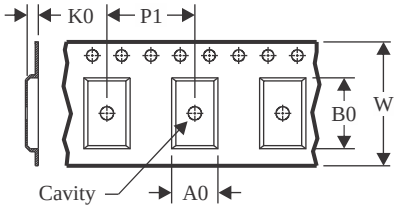
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

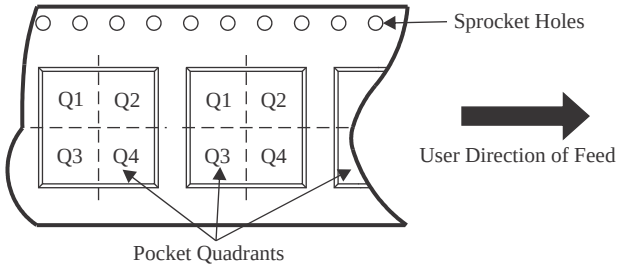


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

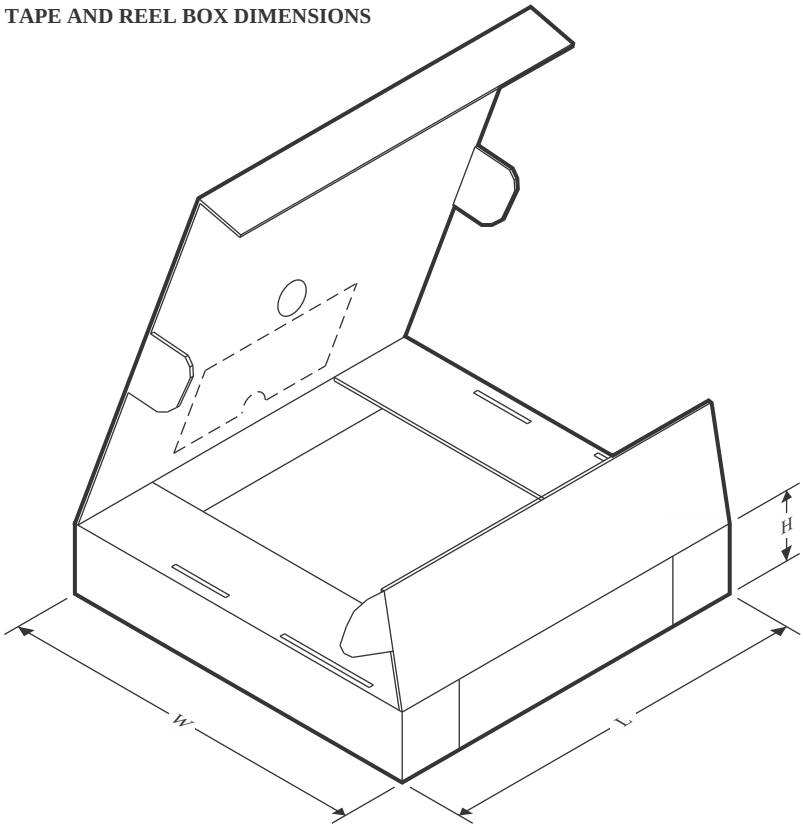
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXS0104WRUTR	UQFN	RUT	12	3000	180.0	8.4	2.0	2.3	0.75	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

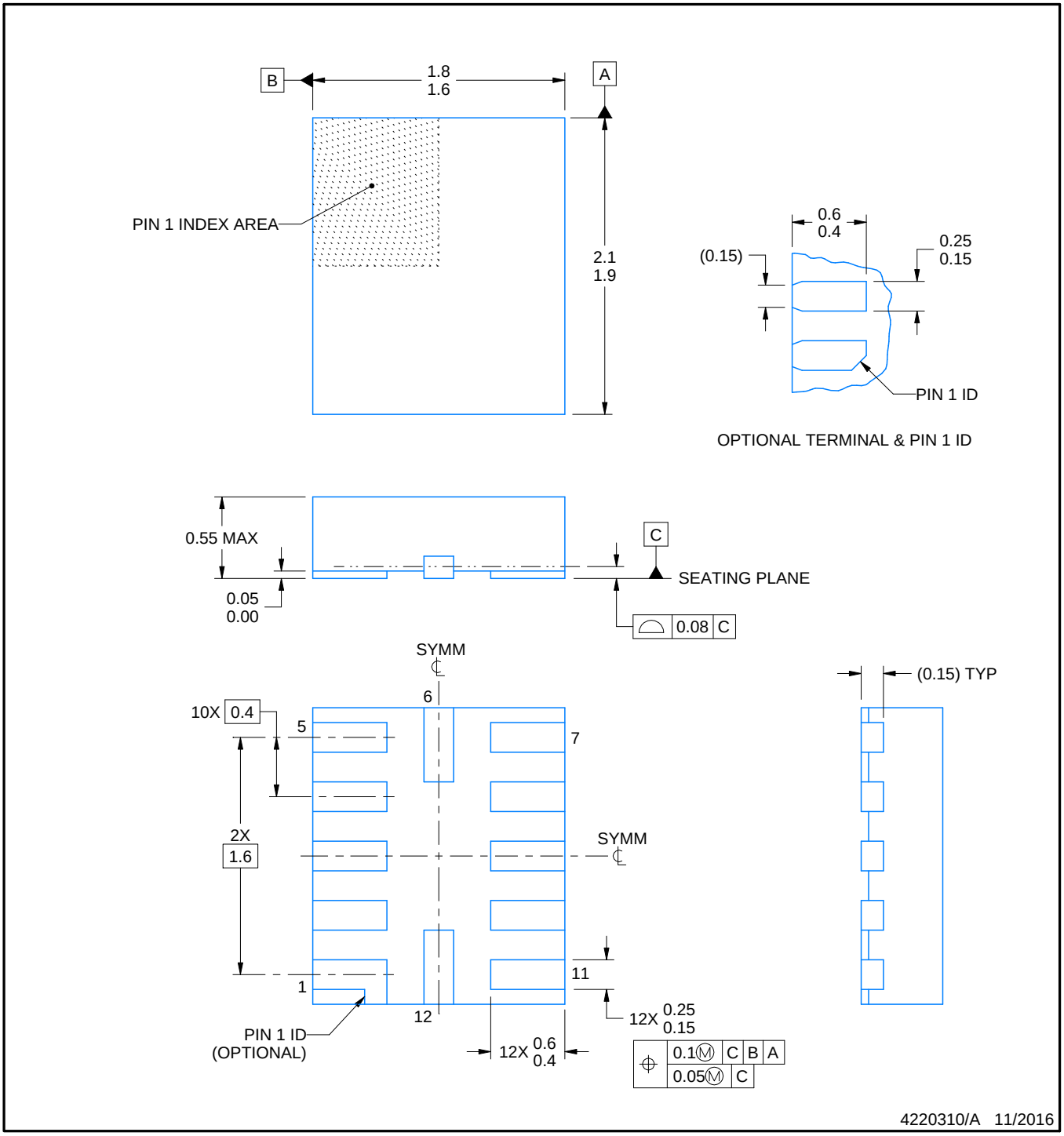
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXS0104WRUTR	UQFN	RUT	12	3000	210.0	185.0	35.0

RUT0012A

PACKAGE OUTLINE

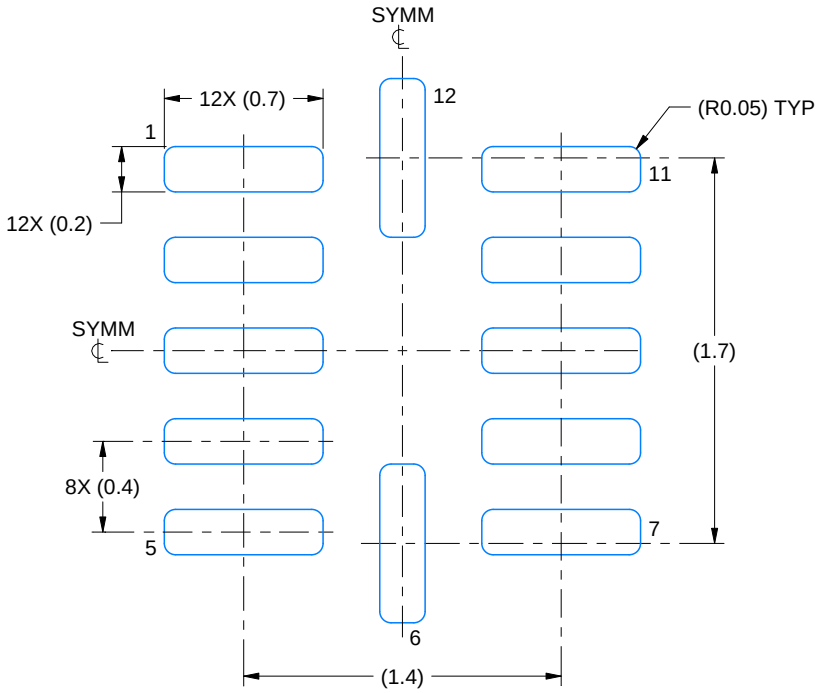
UQFN - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

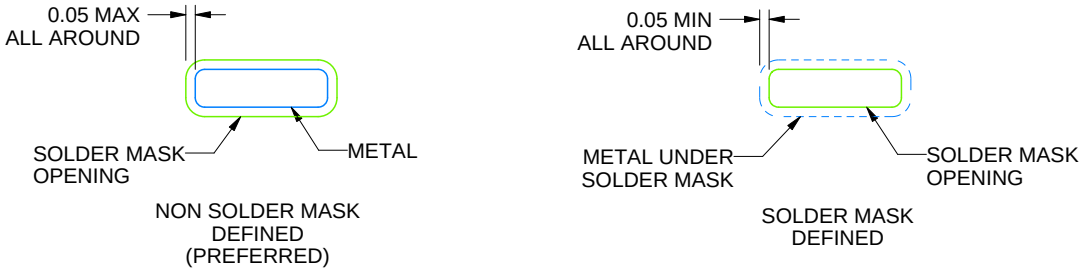


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS

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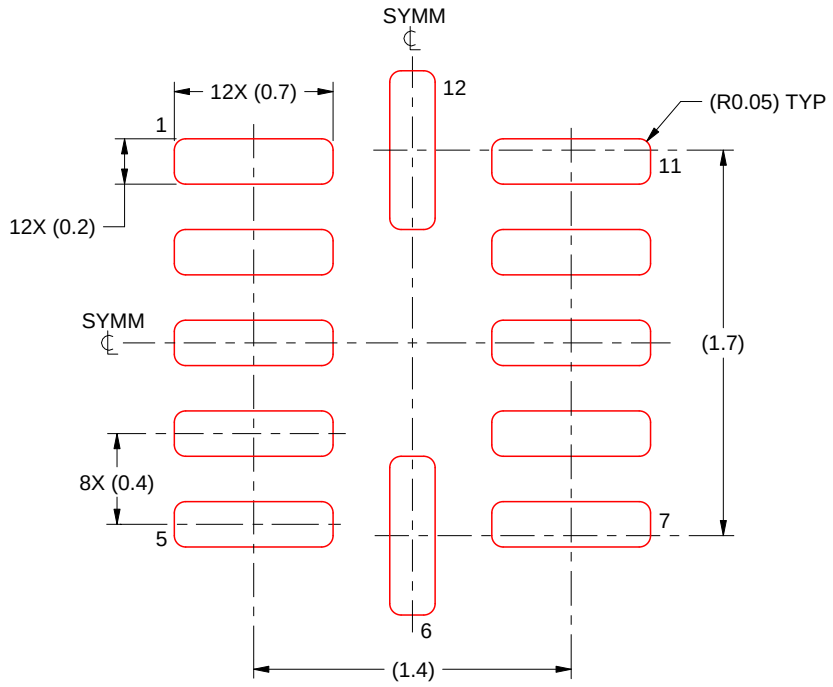
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 30X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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