TXV0108-Q1 Automotive 8-Bit Direction Controlled Low-Skew, Low-Jitter Voltage Translator or Buffer

1 Features

- Configurable design allows each port to operate with a power supply range from 1.14V to 3.6V
- Supports up to 500Mbps for 1.65V to 3.6V
- AEC-Q100 qualified for automotive applications
- Meets RGMII 2.0 timing specifications:
  - < 750ps rise and fall time
  - < ± 5 % duty cycle distortion
  - < ± 400ps channel to channel skew
  - Up to 250Mbps/channel
- Integrated 10Ω damping output resistor to minimize signal reflections
- High drive strength (up to 12mA at 3.6V)
- Fully configurable symmetric dual-rail design
- Optimal signal integrity performance with 390ps peak-to-peak jitter for 1.8V to 3.3V
- Features V_{CC} isolation and V_{CC} disconnect
- I_{off} supports partial-power-down mode operation
- Latch-up performance exceeds 100mA per JESD 78, Class II
- ESD protection exceeds JESD 22:
  - 2000-V Human-Body Model
  - 1000-V Charged-Device Model
- Low power consumption:
  - 10µA maximum (25°C)
  - 20µA maximum (–40°C to 125°C)
- Operating temperature from –40°C to +125°C
- Pin compatible with SN74AVC8T245 (VQFN)
- Available in wettable flank VQFN (RGY) package

2 Applications

- Medium or short range radar
- ADAS domain controller
- HVAC controller design
- Machine vision camera
- Rack server motherboard
- IP telephone

3 Description

The TXV0108-Q1 is an 8-bit, dual-supply direction controlled low-skew, low-jitter voltage translation device. This device can be used for redriving, voltage translation, and power isolation when implementing skew sensitive interface, such as RGMII between Ethernet® MAC and PHY devices. The Ax I/O pins and control pins (DIR, $\overline{OE}$) are referenced to V_{CCA} logic levels, and Bx I/O pins are referenced to V_{CCB} logic levels. This device has improved channel-to-channel skew, duty cycle distortion and symmetric rise and fall time for applications requiring strict timing conditions.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, thus preventing damaging current backflow through the device when it is powered down.

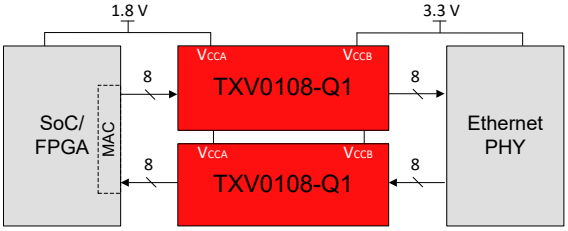
The V_{CC} isolation feature is designed so that if either V_{CC} supply is at or near 0V both ports will switch to a high-impedance state. This feature enables power isolation for communications across multiple MACs and PHYs, and is beneficial in situations where MACs and PHYs are powered up asynchronously preventing current backflow between devices.

A High on DIR allows data transmission from A to B while a Low on DIR allows data transmission from B to A when $\overline{OE}$ is set to Low. When $\overline{OE}$ is set to High, both Ax and Bx pins will be forced into a high-impedance state. See *Device Functional Modes* for a summary of the operation of the control logic.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TXV0108-Q1	RGY (VQFN, 24)	5.5mm × 3.5mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



TXV0108-Q1 in RGMII Applications

Table of Contents

4 Pin Configuration and Functions

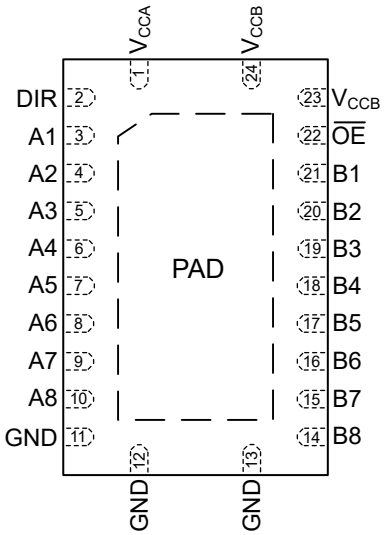


Figure 4-1. RGY Package, 24-Pin VQFN (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
V_{CCA}	1	—	A-port supply voltage.
DIR	2	I	Direction-control signal for all ports. Referenced to V_{CCA}.
A1	3	I/O	Input/Output A1. Referenced to V_{CCA}.
A2	4	I/O	Input/Output A2. Referenced to V_{CCA}.
A3	5	I/O	Input/Output A3. Referenced to V_{CCA}.
A4	6	I/O	Input/Output A4. Referenced to V_{CCA}.
A5	7	I/O	Input/Output A5. Referenced to V_{CCA}.
A6	8	I/O	Input/Output A6. Referenced to V_{CCA}.
A7	9	I/O	Input/Output A7. Referenced to V_{CCA}.
A8	10	I/O	Input/Output A8. Referenced to V_{CCA}.
GND	11, 12, 13	—	Ground.
B8	14	I/O	Input/Output B8. Referenced to V_{CCB}.
B7	15	I/O	Input/Output B7. Referenced to V_{CCB}.
B6	16	I/O	Input/Output B6. Referenced to V_{CCB}.
B5	17	I/O	Input/Output B5. Referenced to V_{CCB}.
B4	18	I/O	Input/Output B4. Referenced to V_{CCB}.
B3	19	I/O	Input/Output B3. Referenced to V_{CCB}.
B2	20	I/O	Input/Output B2. Referenced to V_{CCB}.
B1	21	I/O	Input/Output B1. Referenced to V_{CCB}.
$\overline{OE}$	22	I	Output Enable. Pull to GND to enable all outputs. Pull to V_{CCA} to place all outputs in high-impedance mode. Referenced to V_{CCA}.
V_{CCB}	23, 24	—	B-port supply voltage.
Thermal Pad		—	Thermal pad. Can be grounded (recommended) or left floating.

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage A		–0.5	4.6	V
V_{CCB}	Supply voltage B		–0.5	4.6	V
V_I	Input Voltage(2)	I/O Ports (A Port)	–0.5	4.6	V
		I/O Ports (B Port)	–0.5	4.6	
		Control Inputs	–0.5	4.6	
V_O	Voltage applied to any output in the high-impedance or power-off state(2)	A Port	–0.5	4.6	V
		B Port	–0.5	4.6	
V_O	Voltage applied to any output in the high or low state(2) (3)	A Port	–0.5	V_{CCA} + 0.5	V
		B Port	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	V_I < 0	–50		mA
I_{OK}	Output clamp current	V_O < 0	–50		mA
I_O	Continuous output current		–50	50	mA
	Continuous current through V_{CC} or GND		–100	100	mA
T_j	Junction Temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Rating* may cause permanent device damage. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Condition*. If used outside the *Recommended Operating Condition* but within the *Absolute Maximum Rating*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD classification level 2	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD classification level C3	±1000	V

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1)

				MIN	MAX	UNIT
V_{CCA}	Supply voltage A			1.14	3.6	V
V_{CCB}	Supply voltage B			1.14	3.6	V
V_{IH}	High-level input voltage	Data Inputs (Ax, Bx), $\overline{OE}$, DIR (Referenced to V_{CCI})	V_{CCI} = 1.14 V - 3.6 V	V_{CCI} x 0.7		V
V_{IL}	Low-level input voltage	Data Inputs (Ax, Bx), $\overline{OE}$, DIR (Referenced to V_{CCI})	V_{CCI} = 1.14 V - 3.6 V		V_{CCI} x 0.3	V
I_{OH}	High-level output current		V_{CCO} = 1.14 V		–3	mA
			V_{CCO} = 1.65 V - 1.95 V		–8	
			V_{CCO} = 2.3 V - 2.7 V		–9	
			V_{CCO} = 3 V - 3.6 V		–12	
I_{OL}	Low-level output current		V_{CCO} = 1.14 V		3	mA
			V_{CCO} = 1.65 V - 1.95 V		8	
			V_{CCO} = 2.3 V - 2.7 V		9	
			V_{CCO} = 3 V - 3.6 V		12	
V_I	Input voltage			0	3.6	V
V_O	Output voltage	Active State		0	V_{CCO}	V
		Tri-State		0	3.6	
Δt/Δv	Input transition rise and fall time				5	ns/V
T_A	Operating free-air temperature			–40	125	°C

(1) V_{CCI} is the V_{CC} associated with the input port. V_{CCO} is the V_{CC} associated with the output port.

5.4 Thermal Information

THERMAL METRIC (1)		TXV0108 / TXV0108-Q1 RGY (VQFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	52.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	46.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	30.2	°C/W
Y_{JT}	Junction-to-top characterization parameter	4.2	°C/W
Y_{JB}	Junction-to-board characterization parameter	30.1	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case (bottom) thermal resistance	19.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics app report.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	Operating free-air temperature (T_A)			UNIT
					–40°C to 125°C			
					MIN	TYP	MAX	
V_{IL}	Data Input_Negative threshold	Data inputs, $\overline{OE}$, DIR	1.14 V - 3.6 V	1.14 V - 3.6 V			0.3× VCCA	V
V_{IH}	Data Input_Positive threshold	Data inputs, $\overline{OE}$, DIR	1.14 V - 3.6 V	1.14 V - 3.6 V	0.7× VCCA			V
V_{OH}	High-level output voltage (3)	I_{OH} = –3 mA	1.14 V	1.14 V		0.9		V
		I_{OH} = –8 mA	1.65 V	1.65 V	1.1			
		I_{OH} = –9 mA	2.3 V	2.3 V	1.8			
		I_{OH} = –12 mA	3 V	3 V	2.4			
V_{OL}	Low-level output voltage (4)	I_{OL} = 3 mA	1.14 V	1.14 V		0.1		V
		I_{OL} = 8 mA	1.65 V	1.65 V			0.27	
		I_{OL} = 9 mA	2.3 V	2.3 V			0.23	
		I_{OL} = 12 mA	3 V	3 V			0.26	
I_I	Input leakage current	Data Inputs (Ax, Bx) $V_I = V_{CCI}$ or GND	1.14 V - 3.6 V	1.14 V - 3.6 V	–1		1	µA
I_{off}	Partial power down current	A Port or B Port V_I or V_O = 0 V - 3.6 V	0 V	0 V - 3.6 V	–5		3.6	µA
			0 V - 3.6 V	0 V	–5		3.6	
I_{OZ}	Tri-state output current (5)	A or B Port: $V_I = V_{CCI}$ or GND $V_O = V_{CCO}$ or GND $\overline{OE} = V_{IH}$	3.6 V	3.6 V	–5		5	µA
I_{CCA}	V_{CCA} supply current	$V_I = V_{CCI}$ or GND I_O = 0	1.14 V - 3.6 V	1.14 V - 3.6 V			14	µA
			3.6 V	0 V			11	
			0 V	3.6 V	-1			
I_{CCB}	V_{CCB} supply current	$V_I = V_{CCI}$ or GND I_O = 0	1.14 V - 3.6 V	1.14 V - 3.6 V			14	µA
			3.6 V	0 V	–1			
			0 V	3.6 V			11	
I_{CCA} + I_{CCB}	Combined supply current	$V_I = V_{CCI}$ or GND I_O = 0	1.14 V - 3.6 V	1.14 V - 3.6 V			22	µA
C_i	Control Input Capacitance	V_I = 3.3 V or GND	3.3 V	3.3 V			3.9	pF
C_{io}	Data I/O Capacitance	$\overline{OE} = V_{CCA}$, V_O = 1.65V DC +1 MHz -16 dBm sine wave	3.3 V	3.3 V			2.7	pF

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) Tested at $V_I = V_{IH}$.
(4) Tested at $V_I = V_{IL}$.
(5) For I/O ports, the parameter I_{OZ} includes the input leakage current.

5.6 Switching Characteristics, V_{CCA} = 1.2 ± 0.06 V

Over the recommended temperature range at C_L = 5 pF, unless otherwise indicated.

PARAMETER		FROM	TO	B-Port Supply Voltage (V_{CCB})				UNIT
				1.2V ± 0.06	1.8 ± 0.15 V	2.5 ± 0.2 V	3.3 ± 0.3 V	
				TYP	TYP	TYP	TYP	
t_{pd}	Propagation delay	A	B	4.5	3.0	2.5	2.5	ns
		B	A					
t_{dis}	Disable time	$\overline{OE}$	A	7.5	6.5	6.0	6.0	ns
		$\overline{OE}$	B					
t_{en}	Enable time	$\overline{OE}$	A	9	7	6.5	6.5	ns
		$\overline{OE}$	B					
T_R	Rise time (1)	A	B	0.75	0.40	0.30	0.25	ns
		B	B					
T_F	Fall time (1)	A	B	0.65	0.40	0.30	0.30	ns
		B	B					
Duty Cycle	Duty cycle variation	A	B	50	50	50	50	%
		B	A					

(1) Rise and fall time is measured at 20% - 80%

5.7 Switching Characteristics, V_{CCA} = 1.8 ± 0.15 V

Minimum and maximum limits apply over the recommended temperature range at C_L = 15 pF and 250 Mbps, unless otherwise indicated.

PARAMETER		FROM	TO	B-Port Supply Voltage (V_{CCB})									UNIT
				1.8 ± 0.15 V			2.5 ± 0.2 V			3.3 ± 0.3 V			
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	Propagation delay	A	B	1.2		4.8	1.2		3.5	1.1		3.1	ns
		B	A	1.6		4.8	1.5		4.2	1.4		3.9	
t_{dis}	Disable time	$\overline{OE}$	A	2.5		7.0	2.5		6.5	2.5		6.5	ns
			B	2.6		7.0	2.2		5.5	2.3		6.4	
t_{en}	Enable time	$\overline{OE}$	A	1.5		6.6	1.5		6.6	1.5		6.6	ns
			B	1.2		5.3	1.0		4.0	1.0		3.7	
t_{SKO}	Output channel-to-channel skew (1)	A	B	-450		450	-300		300	-330		330	ps
		B	A	-450		450	-330		330	-300		300	ps
T_R	Rise time (2)	A	B	0.49		1.35	0.40		0.95	0.35		0.80	ns
		B	A	0.50		1.35	0.50		1.35	0.50		1.35	
T_F	Fall time (2)	A	B	0.45		1.35	0.35		0.95	0.35		0.80	ns
		B	A	0.45		1.35	0.45		1.35	0.45		1.35	
Duty Cycle	Duty cycle variation	A	B	48	50	56	48	50	54	48	50	54	%
		B	A	48	50	56	47	50	55	46	50	54	
T_{R_5pF}	Rise time (2) (3)	A	B	0.28		0.75	0.22		0.55	0.19		0.45	ns
		B	A	0.28		0.75	0.28		0.75	0.30		0.76	
T_{F_5pF}	Fall time (2) (3)	A	B	0.27		0.75	0.20		0.55	0.18		0.40	ns
		B	A	0.28		0.75	0.28		0.76	0.30		0.77	
t_{SKO_5pF}	Output channel-to-channel skew (1) (3)	A	B	-300		300	-270		270	-310		310	ps
		B	A	-300		300	-170		170	-180		180	
Duty Cycle _5pF	Duty cycle variation (3)	A	B	49	50	54	49	50	54	48	50	54	%
		B	A	49	50	54	48	50	53	48	50	53	
$t_{jit(pp)}$	Peak-to-peak jitter (250 Mbps 2^{15}- 1 PRBS input)	A	B	160		450	130		335	120		390	ps

(1) Skew parameter also includes jitter
(2) Rise and fall time is measured at 20% - 80%
(3) Parameters tested under RGMII input transition (≤ 2 ns/V) rise and fall time. C_{LOAD} = 5pF

5.8 Switching Characteristics, V_{CCA} = 2.5 ± 0.2 V

Minimum and maximum limits apply over the recommended temperature range at C_L = 15 pF and 250 Mbps, unless otherwise indicated.

PARAMETER		FROM	TO	B-Port Supply Voltage (V_{CCB})									UNIT
				1.8 ± 0.15 V			2.5 ± 0.2 V			3.3 ± 0.3 V			
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	Propagation delay	A	B	1.5		4.2	1.2		3.0	1.1		2.5	ns
		B	A	1.3		3.5	1.2		3.0	1.2		2.7	
t_{dis}	Disable time	$\overline{OE}$	A	1.9		4.5	1.9		4.5	1.9		4.5	ns
			B	2.4		6.5	2.0		5.0	2.2		6.0	
t_{en}	Enable time	$\overline{OE}$	A	1.1		4.0	1.1		4.0	1.1		4.0	ns
			B	1.2		4.7	1.0		3.5	0.9		3.0	
t_{SKO}	Output channel-to-channel skew (1)	A	B	-370		370	-200		200	-200		200	ps
		B	A	-300		300	-210		210	-210		210	
T_R	Rise time (2)	A	B	0.50		1.4	0.40		1.0	0.35		0.90	ns
		B	A	0.40		1.0	0.40		1.0	0.40		1.0	
T_F	Fall time (2)	A	B	0.45		1.4	0.35		1.0	0.30		0.80	ns
		B	A	0.35		1.0	0.35		1.0	0.35		1.0	
Duty Cycle	Duty cycle variation	A	B	46	50	56	48	50	53	48	50	53	%
		B	A	48	50	54	48	50	53	48	50	53	
T_{R_5pF}	Rise time (2) (3)	A	B	0.25		0.75	0.20		0.55	0.15		0.45	ns
		B	A	0.20		0.55	0.20		0.55	0.20		0.55	
T_{F_5pF}	Fall time (2) (3)	A	B	0.25		0.76	0.20		0.55	0.15		0.45	ns
		B	A	0.20		0.55	0.20		0.55	0.20		0.56	
t_{SKO_5pF}	Output Channel-to-channel skew (1) (3)	A	B	-235		235	-160		160	-180		180	ps
		B	A	-270		270	-160		160	-130		130	
Duty Cycle _5pF	Duty cycle variation (3)	A	B	48	50	53	49	50	52	48	50	52	%
		B	A	49	50	54	49	50	52	49	50	52	
$t_{jit(pp)}$	Peark-to-peak jitter (250 Mbps 2^{15}- 1 PRBS input)	A or B	A or B	120		370	100		300	90		360	ps

(1) Skew parameter also includes jitter
(2) Rise and fall time is measured at 20% - 80%
(3) Parameters tested under RGMII input transition (≤ 2 ns/V) rise and fall time. C_{LOAD} = 5 pF

5.9 Switching Characteristics, V_{CCA} = 3.3 ± 0.3 V

Minimum and maximum limits apply over the recommended temperature range at C_L = 15 pF and 250 Mbps, unless otherwise indicated.

PARAMETER		FROM	TO	B-Port Supply Voltage (V_{CCB})									UNIT
				1.8 ± 0.15 V			2.5 ± 0.2 V			3.3 ± 0.3 V			
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	Propagation delay	A	B	1.2		3.8	1.2		2.7	1.1		2.3	ns
		B	A	1.2		3.0	1.1		2.5	1.1		2.3	
t_{dis}	Disable time	$\overline{OE}$	A	2.0		5.5	2.0		5.5	2.0		5.5	ns
			B	2.2		6.0	1.8		4.5	2.0		5.5	
t_{en}	Enable time	$\overline{OE}$	A	1.0		3.0	1.0		3.0	1.0		3.0	ns
			B	1.2		4.5	0.95		3.0	0.85		2.7	
t_{SKO}	Output channel-to-channel skew (1)	A	B	-380		380	-230		230	-170		170	ps
		B	A	-330		330	-190		190	-165		165	
T_R	Rise time (2)	A	B	0.50		1.3	0.40		1.0	0.35		0.90	ns
		B	A	0.35		0.80	0.35		0.80	0.35		0.80	
T_F	Fall time (2)	A	B	0.45		1.3	0.35		1.0	0.35		0.80	ns
		B	A	0.35		0.80	0.35		0.80	0.35		0.80	
Duty Cycle	Duty cycle variation	A	B	46	50	54	48	50	53	48	50	52	%
		B	A	47	50	54	47	50	53	47	50	52	
T_{R_5pF}	Rise time (2) (3)	A	B	0.30		0.80	0.20		0.55	0.15		0.45	ns
		B	A	0.15		0.45	0.15		0.45	0.15		0.45	
T_{F_5pF}	Fall time (2) (3)	A	B	0.25		0.80	0.20		0.60	0.20		0.45	ns
		B	A	0.15		0.40	0.15		0.45	0.20		0.45	
t_{SKO_5pF}	Output channel-to-channel skew (1) (3)	A	B	-265		265	-145		145	-140		140	ps
		B	A	-310		310	-170		170	-120		120	
Duty Cycle _5pF	Duty cycle variation (3)	A	B	48	50	53	49	50	52	49	50	52	%
		B	A	48	50	54	48	50	52	48	50	52	
$t_{jit(pp)}$	Peark-to-peak jitter (250 Mbps 2^{15}- 1 PRBS input)	A or B	A or B	115		390	75		330	75		330	ps

(1) Skew parameter also includes jitter
(2) Rise and fall time is measured at 20% - 80%
(3) Parameters tested under RGMII input transition (≤ 2 ns/V) rise and fall time. C_{LOAD} = 5 pF

5.10 Typical Characteristics

T_A = 25°C (unless otherwise noted)

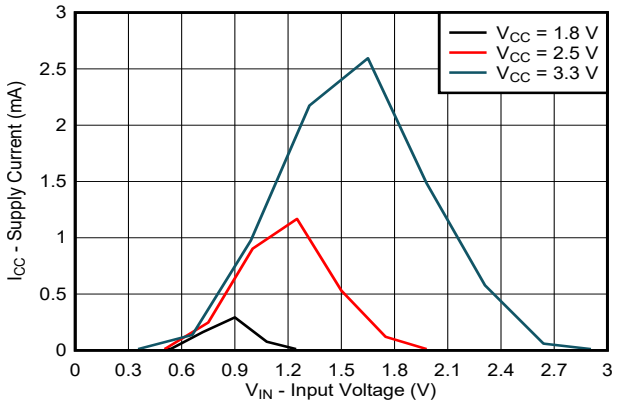


Figure 5-1. Supply Current vs Input Voltage Supply (Rising)

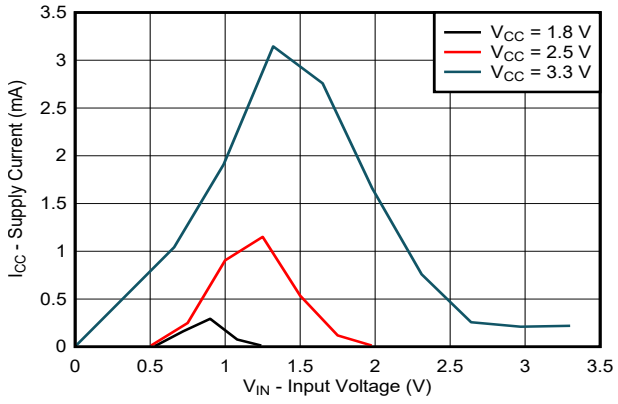


Figure 5-2. Supply Current vs Input Voltage Supply (Falling)

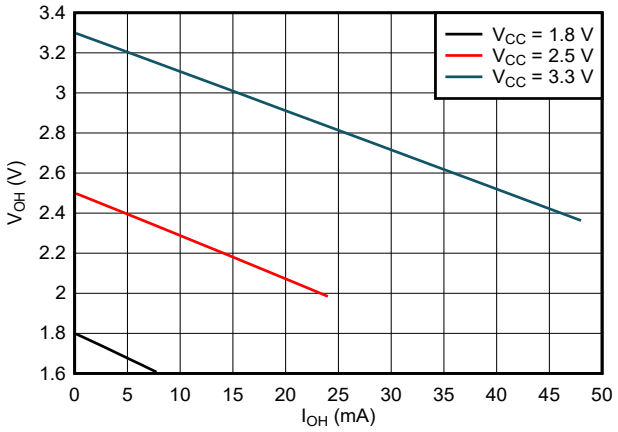


Figure 5-3. Output Voltage vs Current in HIGH State

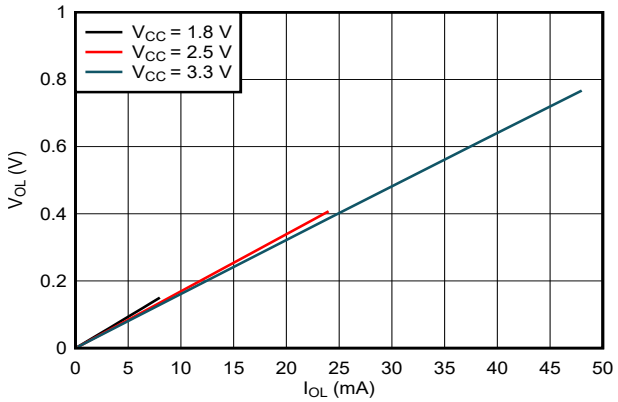


Figure 5-4. Output Voltage vs Current in LOW State

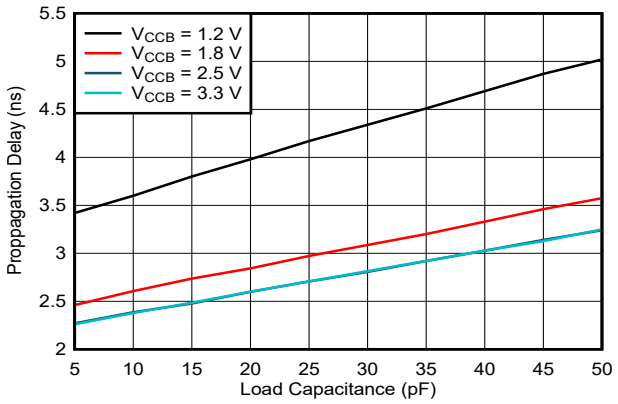


Figure 5-5. Propagation Delay vs Load Capacitance (V_{CCA} = 1.2V)

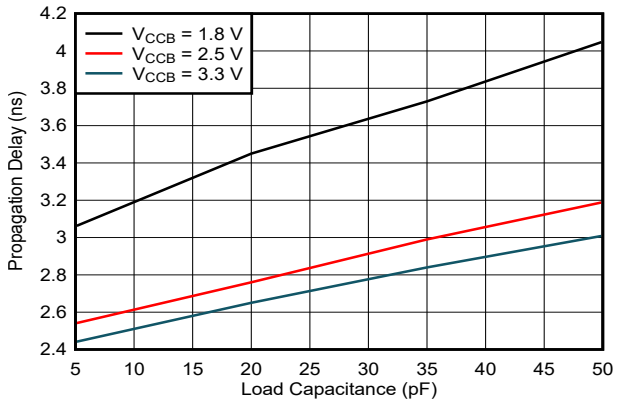


Figure 5-6. Propagation Delay, T_{PLH} vs Load Capacitance (V_{CCA} = 1.8V)

5.10 Typical Characteristics (continued)

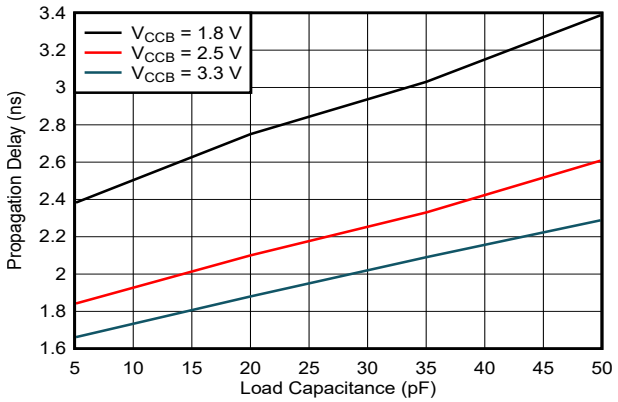


Figure 5-7. Propagation Delay, T_{PLH} vs Load Capacitance (V_{CCA} = 2.5V)

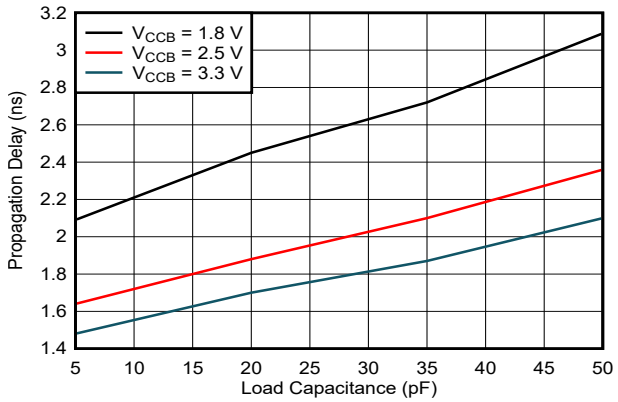


Figure 5-8. Propagation Delay, T_{PLH} vs Load Capacitance (V_{CCA} = 3.3V)

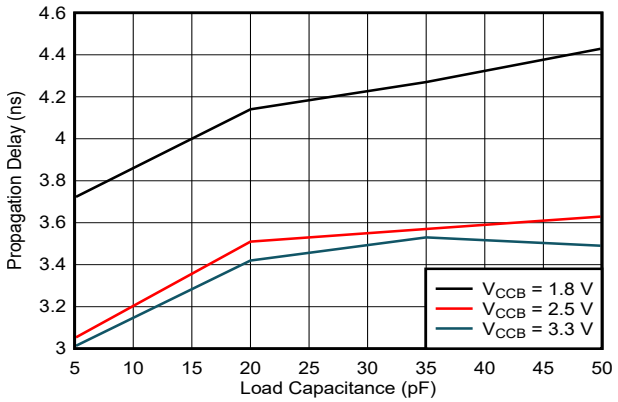


Figure 5-9. Propagation Delay, T_{PHL} vs Load Capacitance (V_{CCA} = 1.8V)

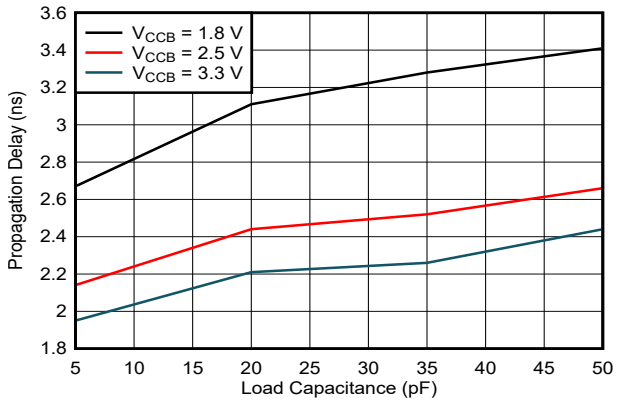


Figure 5-10. Propagation Delay, T_{PHL} vs Load Capacitance (V_{CCA} = 2.5V)

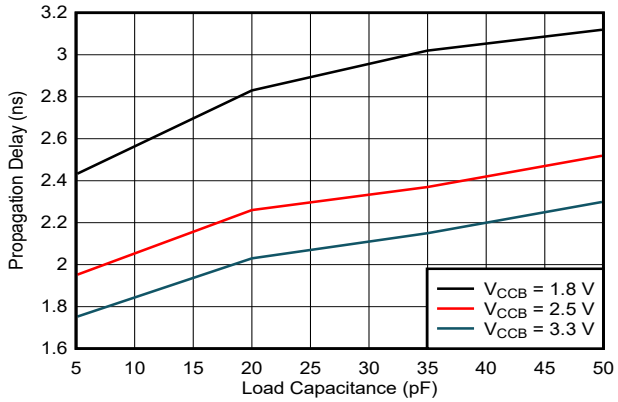


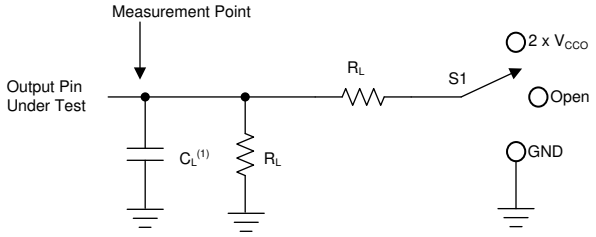
Figure 5-11. Propagation Delay, T_{PHL} vs Load Capacitance (V_{CCA} = 3.3V)

6 Parameter Measurement Information

6.1 Load Circuit and Voltage Waveforms

Unless otherwise noted, all input pulses are supplied by generators having the following characteristics:

- f = 1MHz
- Z_O = 50Ω
- Δt/ΔV ≤ 1ns/V

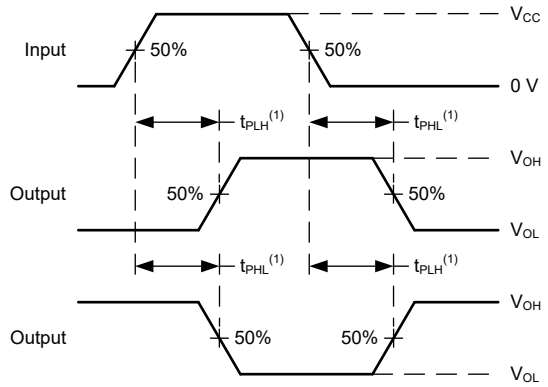


A. C_L includes probe and jig capacitance.

Figure 6-1. Load Circuit

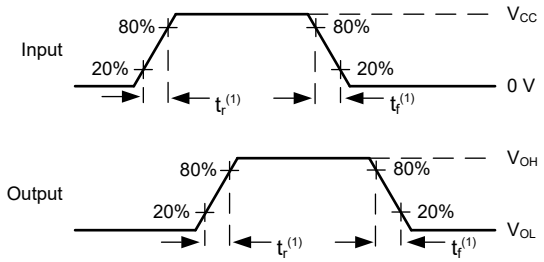
Table 6-1. Load Circuit Conditions

Parameter		V_{CCO}	R_L	C_L	S_1	V_{TP}
t_{pd}	Propagation (delay) time	1.14V – 3.6V	2kΩ	15pF	Open	N/A
t_{en}, t_{dis}	Enable time, disable time	1.14V – 3.6V	2kΩ	15pF	2 × V_{CCO}	0.15V
t_{en}, t_{dis}	Enable time, disable time	1.14V – 3.6V	2kΩ	15pF	GND	0.15V



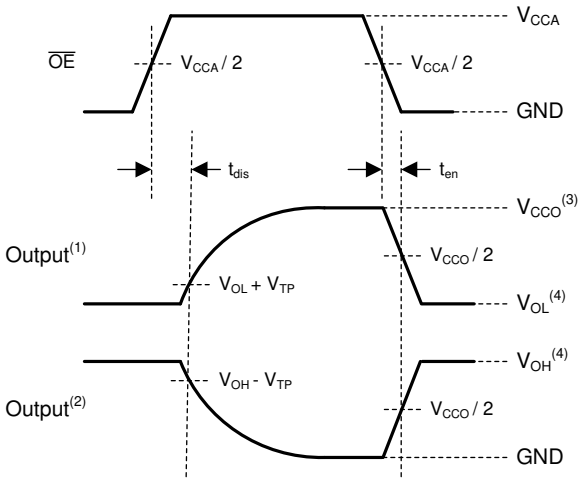
1. The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.
2. V_{OH} and V_{OL} are typical output voltage levels that occur with specified R_L, C_L, and S_1

Figure 6-2. Propagation Delay



1. V_{OH} and V_{OL} are typical output voltage levels that occur with specified R_L, C_L, and S_1

Figure 6-3. Input and Output Rise and Fall Time



A. Output waveform on the condition that input is driven to a valid Logic Low.
B. Output waveform on the condition that input is driven to a valid Logic High.
C. V_{CCO} is the supply pin associated with the output port.
D. V_{OH} and V_{OL} are typical output voltage levels with specified R_L, C_L, and S_1.

Figure 6-4. Enable Time And Disable Time

7 Detailed Description

7.1 Overview

The TXV0108-Q1 is an 8-bit translating transceiver that uses two individually configurable power-supply rails. The device is operational with both V_{CCA} and V_{CCB} supplies as low as 1.14V and as high as 3.6V. Additionally, the device can be used as a buffer with V_{CCA} = V_{CCB}. The Ax port is designed to track V_{CCA}, and the Bx port is designed to track V_{CCB}.

The TXV0108-Q1 device is designed for asynchronous communication between data buses, and transmits data from the A bus to the B bus or from the B bus to the A bus based on the logic level of the direction-control input (DIR). The output-enable input ($\overline{OE}$) is used to disable the outputs so the buses are effectively isolated. The control pins of the TXV0108-Q1 (DIR and $\overline{OE}$) are referenced to V_{CCA}. To enable the high-impedance state of the level shifter I/Os during power up or power down, the $\overline{OE}$ pin should be tied to V_{CCA} through a pullup resistor.

This device is fully specified for partial-power-down applications using the I_{off} current. The I_{off} protection circuitry prevents excessive current from being drawn from or sourced into an input, output, or I/O while the device is powered down.

7.2 Functional Block Diagram

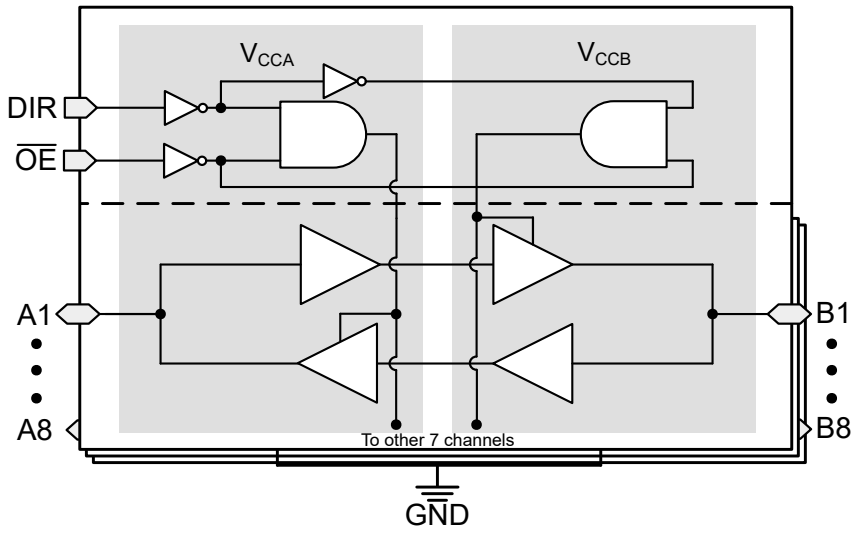


Figure 7-1. Functional Block Diagram of the TXV0108-Q1

7.3 Feature Description

7.3.1 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

7.3.2 Partial Power Down (I_{off})

The inputs and outputs for this device enter a high-impedance state when the device is powered down, inhibiting current backflow into the device. The maximum leakage into or out of any input or output pin on the device is specified by I_{off} in the *Electrical Characteristics*.

7.3.3 V_{CC} Isolation and V_{CC} Disconnect ($I_{off-float}$)

This device has 2 features (V_{CC} Isolation and V_{CC} Disconnect), which prevents current backflow in case the device is powered down unexpectedly. V_{CC} Isolation occurs when one of the supplies is kept at (or goes to) zero during normal operation, no current will be consumed by the supply that is maintained. This scenario forces all I/Os to be High-Z. V_{CC} Disconnect occurs when one of the supplies is left floating (disconnects) after ramping up, the I/Os are forced into High-Z without consuming any current from the maintained supply. In both cases, the I/Os will enter a high-impedance state when either supply (V_{CCA} or V_{CCB}) is < 100mV or left floating, while the other supply is still connected to the device. See Figure 7-2 for a visual representation.

The maximum supply current is specified by I_{CCx}, while V_{CCx} is floating, in the *Electrical Characteristics*. The maximum leakage into or out of any I/O pin on the device is specified by $I_{off(float)}$ in the *Electrical Characteristics*.

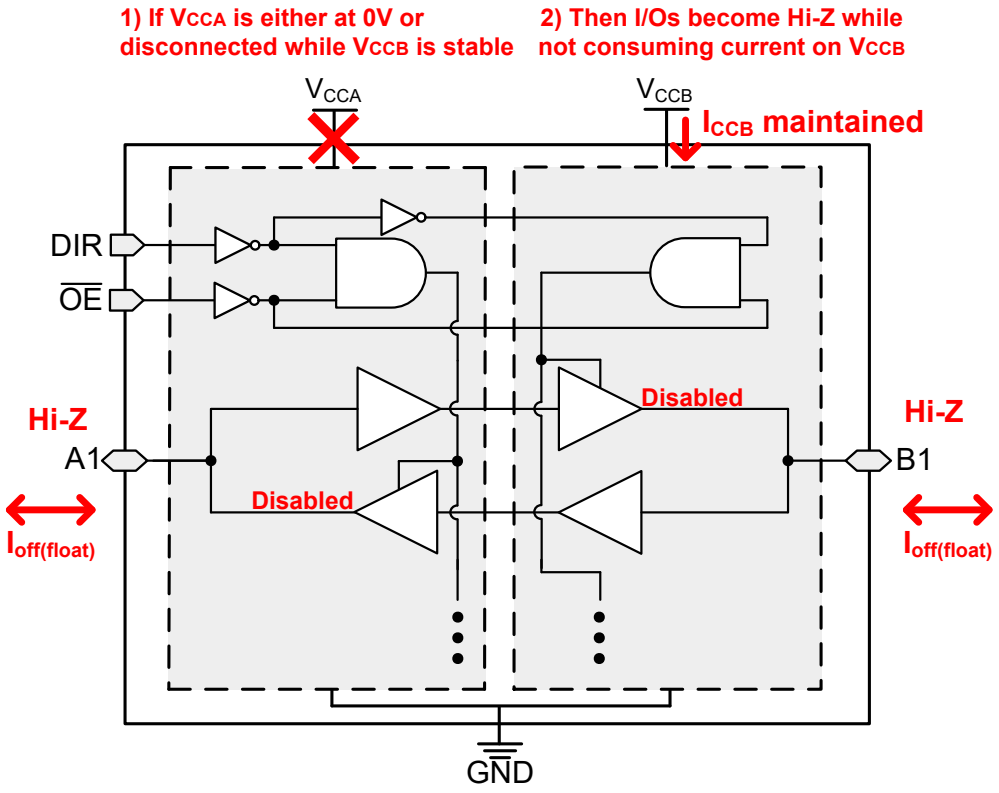


Figure 7-2. V_{CC} Disconnect and V_{CC} Isolation Feature

7.3.4 Over-Voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the *Recommended Operating Conditions*.

7.3.5 Negative Clamping Diodes

The inputs and outputs to this device have negative clamping diodes as shown in Figure 7-3

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

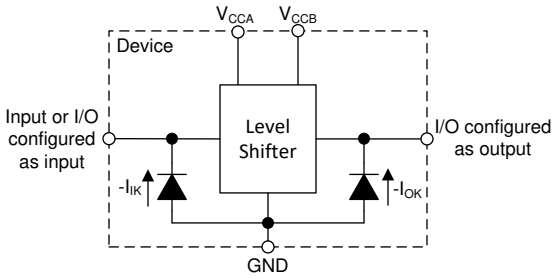


Figure 7-3. Electrical Placement of Clamping Diodes for Each Input and Output

7.3.6 Fully Configurable Dual-Rail Design

Both the V_{CCA} and V_{CCB} pins can be supplied at any voltage from 1.14V to 3.6V, making the device an excellent choice for translating between any of the voltage nodes (1.2V, 1.8V, 2.5V, and 3.3V).

7.3.7 Supports Timing Sensitive Translation

The TXV0108-Q1 can support high data rate applications. The translated signal data rate can support up to 500Mbps when the signal is translated from 1.65V to 3.6V. For the device to meet RGMII 2.0 timing specifications (rise or fall time, skew, and duty cycle distortion) the data rate will need to be lowered to 250Mbps.

7.3.8 Wettable Flanks

Wettable flanks improve side wetting after soldering which makes QFN packages easier to inspect with automatic optical inspection (AOI). A wettable flank can be dimpled or step-cut to provide additional surface area for solder adhesion which assists in reliably creating a side fillet as shown in the figure. For additional details, see the mechanical drawing.

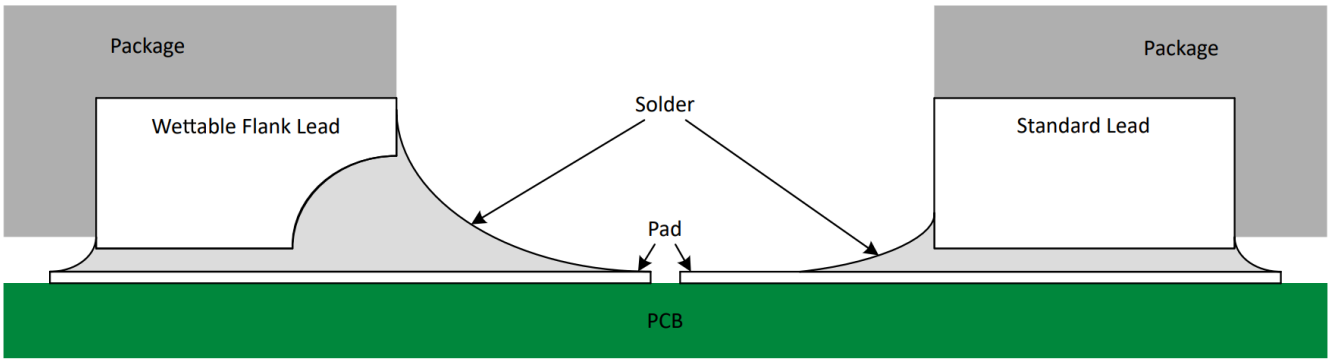


Figure 7-4. Simplified Cutaway View of Wettable-Flank QFN Package and Standard QFN Package After Soldering

7.3.9 Integrated Damping Resistor and Impedance Matching

The TXV0108-Q1 features a 10Ω integrated damping resistor to help minimize signal reflections on the rising and falling edges. If impedance matching with a 50Ω load is required, then a series resistor will be needed. Since the output impedance of the device will vary with the output voltage, (V_{CCB} when DIR = High or V_{CCA} when DIR = Low) Table 7-1 provides the recommended resistor values needed to impedance match a 50Ω load.

Table 7-1. Series Resistor Values for 50Ω Impedance Matching

Output Voltage	1.2V	1.8V	2.5V	3.3V
Series Resistor	53Ω	25Ω	30Ω	32Ω

7.4 Device Functional Modes

Table 7-2. Function Table

CONTROL INPUTS (1)		PORT STATUS		OPERATION
$\overline{OE}$	DIR	A PORT	B PORT	
L	L	Output (Enabled)	Input (Hi-Z)	B data to A bus
L	H	Input (Hi-Z)	Output (Enabled)	A data to B bus
H	X	Input (Hi-Z)	Input (Hi-Z)	Isolation

(1) Input circuits of the data I/Os are always active and should be kept at a valid logic level.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TXV0108-Q1 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The TXV0108-Q1 device is an excellent choice for use in applications where a push-pull driver is connected to the data I/Os. The maximum data rate can be up to 500Mbps when device translates a signal from 1.65V to 3.6V.

8.2 Typical Application

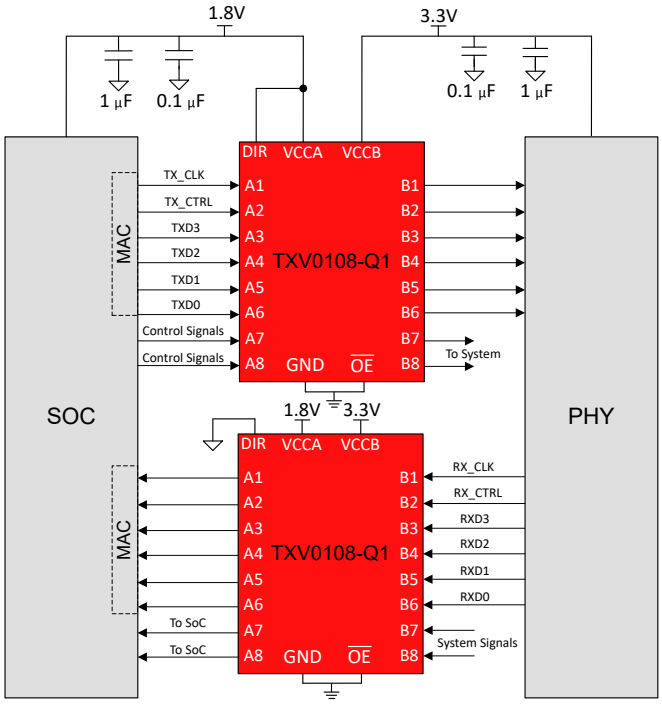


Figure 8-1. RGMII Application (Interfacing between MAC and PHY)

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 8-1.

Table 8-1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
Input voltage range	1.65V to 3.6V
Output voltage range	1.65V to 3.6V
Frequency	125MHz
Load Capacitance	5pF
Input Transition Rise/Fall Time	≤ 2ns/V

8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range:
  - Use the supply voltage of the device that is driving the TXV0108-Q1 device to determine the input voltage range. For a valid logic-high, the value must exceed the positive-going input-threshold voltage (V_{t+}) of the input port. For a valid logic low the value must be less than the negative-going input-threshold voltage (V_{t-}) of the input port.
- Output voltage range:
  - Use the supply voltage of the device that the TXV0108-Q1 device is driving to determine the output voltage range.
- RGMII timing:
  - For the TXV0108-Q1 to meet RGMII timing specifications, parameters like frequency, C_{LOAD} and input rise/fall transition have to be met. Ensure each channel does not exceed a maximum frequency of 125MHz, use a C_{LOAD} no greater than 5pF, and use an input rise/fall slew rate no greater than 2ns/V.

8.2.3 Application Curves

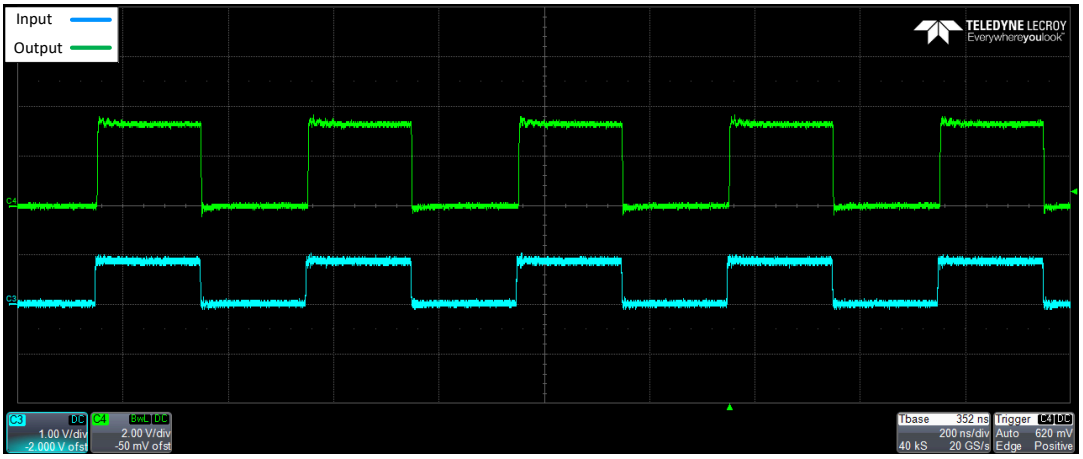


Figure 8-2. Up Translation (1.8V to 3.3V) C_{LOAD} = 15pF at 2.5MHz

8.3 System Examples

8.3.1 Solving Power Sequencing Challenges with the TXV0108-Q1

The TXV0108-Q1 not only solves voltage mismatch between interfaces but also solves power sequencing challenges. As shown in Figure 8-3, a multi-core RGMII system with an Ethernet switch may be present in some Ethernet applications. In other applications, there may be a standard Ethernet interface with one MAC and PHY. In either case, it is necessary to power up each device properly. This will prevent the I/O pins from powering up before the core blocks, which can cause in-rush current during power up or bus contention and other malfunctions.

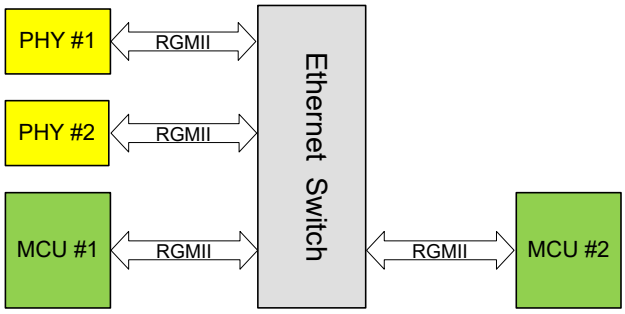


Figure 8-3. Multi-Core RGMII Communication

Low Dropout (LDO) devices are a common way to power up devices, but they do not provide any power sequencing features. As shown in Figure 8-4, before the 1.8V can be applied to the MAC, the input of the LDO will need to come up first. This will result in the PHY powering up which can lead to in-rush current flowing into the MAC I/O pins.

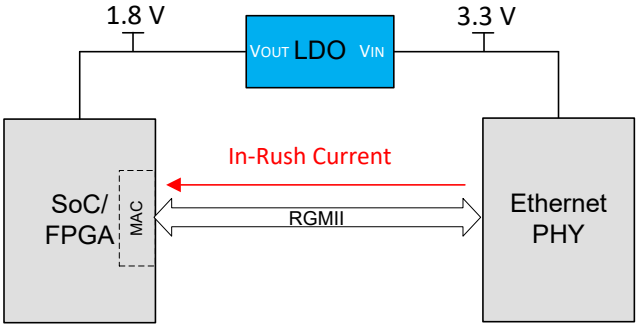


Figure 8-4. Residual Current Flowing Into MAC I/O Pins After PHY is Powered Up

With the TXV0108-Q1 supporting the $I_{off-float}$ feature, in-rush current from improper power sequencing can be prevented. When either power supply pin is at 0V or below 100mV, the I/O pins become high impedance until both pins go above 100mV. The high impedance state will prevent any in-rush current from flowing to the opposite side.

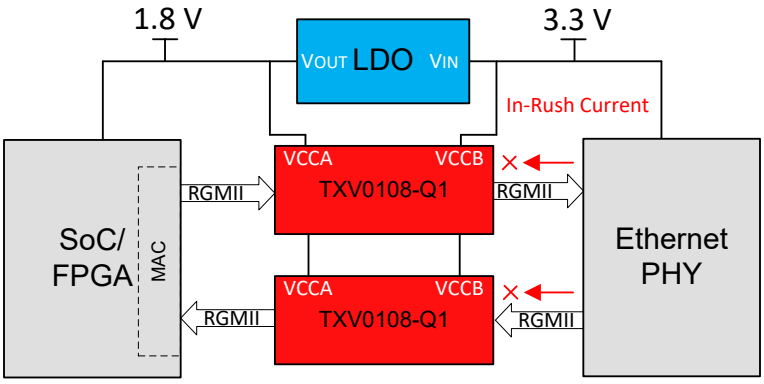


Figure 8-5. Using the TXV0108-Q1 for Power Isolation

For additional information on the TXV0108-Q1 and power isolation use cases, see the *Solving Power Sequencing Challenges for Ethernet RGMII Communications* application note.

8.4 Power Supply Recommendations

The TXV0108-Q1 uses two separate configurable power supply rails (V_{CCA} and V_{CCB}). The A port and B port are designed to track V_{CCA} and V_{CCB}, respectively, allowing for low-voltage translation between any of the 1.2V, 1.8V, 2.5V and 3.3V voltage nodes.

V_{CCA} supplies the output-enable $\overline{OE}$ input circuit in this design. When the $\overline{OE}$ input is high, all outputs are placed in the high-impedance state. To put the outputs in a high-impedance state during power up or power down, tie the $\overline{OE}$ input pin to V_{CCA} through a pullup resistor and do not be enable it until V_{CCA} and V_{CCB} are fully ramped and stable. The current-sinking capability of the driver determines the minimum value of the pullup resistor to V_{CCA}.

8.5 Layout

8.5.1 Layout Guidelines

For device reliability, following common printed-circuit board layout guidelines are recommended:

- Use short trace lengths to avoid excessive loading.
- Use bypass capacitors on the power supply pins and place them as close to the device as possible.
- A 0.1µF bypass capacitor is recommended, but transient performance can be improved by having both 1µF and 0.1µF capacitors in parallel with the smallest value capacitor placed closest to the power pin.
- The high drive capability of this device creates fast edges into light loads. Routing and load conditions should be considered to prevent ringing.

8.5.2 Layout Example

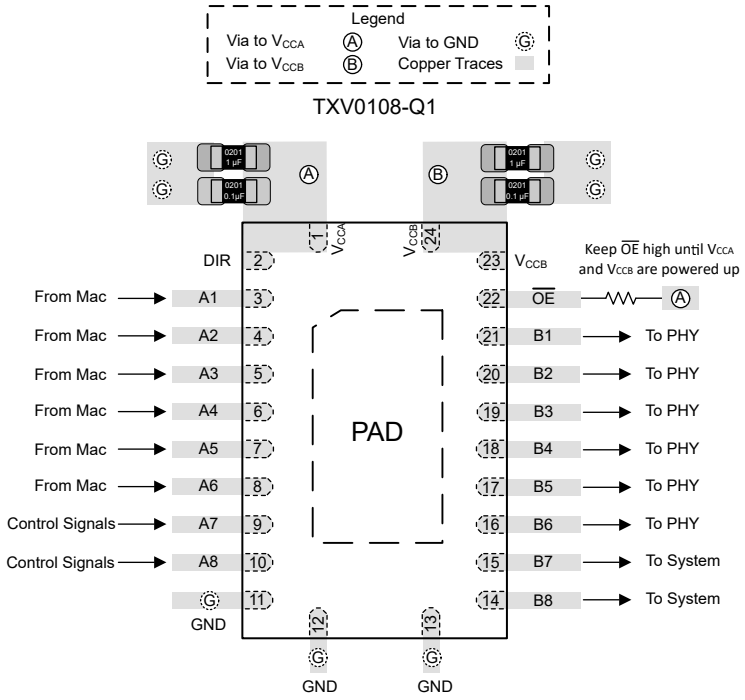


Figure 8-6. Layout Example – TXV0108-Q1

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Solving Power Sequencing Challenges for Ethernet RGMII Communications* application note

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
Ethernet® is a registered trademark of Xerox Corporation.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (December 2023) to Revision B (April 2024)	Page
• Added 1.14V Test Conditions to *Recommended Operating Conditions* Table	5
• Added 1.14V Test Conditions to *Electrical Characteristics* Table	6
• Added 1.2V Switching Characteristics Table	7

Changes from Revision * (July 2023) to Revision A (December 2023)	Page
• Changed status of data sheet from *Advanced Information* to *Production Data*	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TXV0108QWRGYRQ1	Active	Production	VQFN (RGY) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TV108Q
TXV0108QWRGYRQ1.A	Active	Production	VQFN (RGY) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TV108Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TXV0108-Q1 :

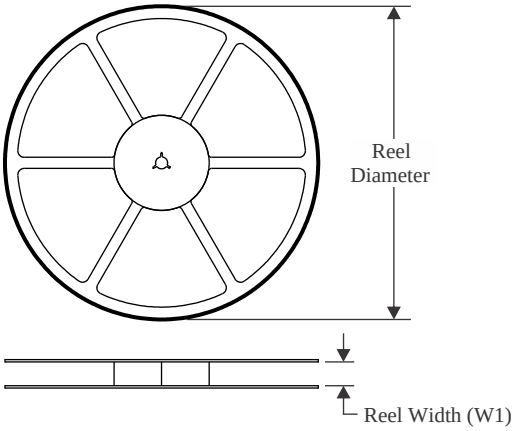
- Catalog : TXV0108

NOTE: Qualified Version Definitions:

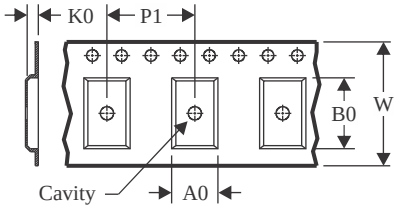
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

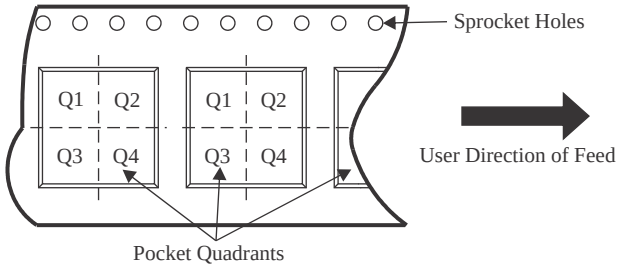


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

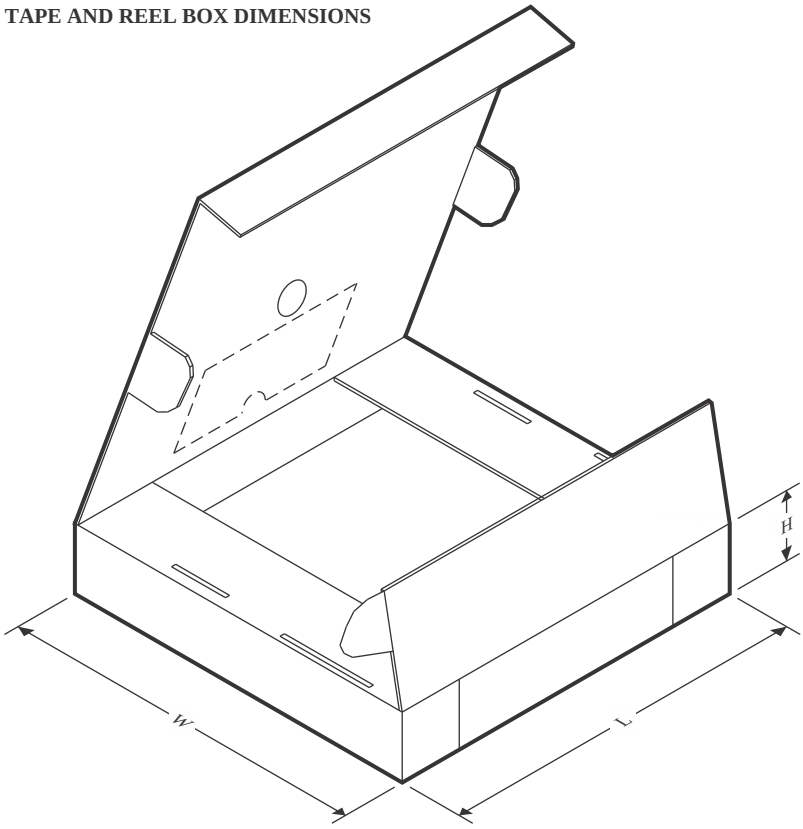
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXV0108QWRGYRQ1	VQFN	RGY	24	3000	330.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

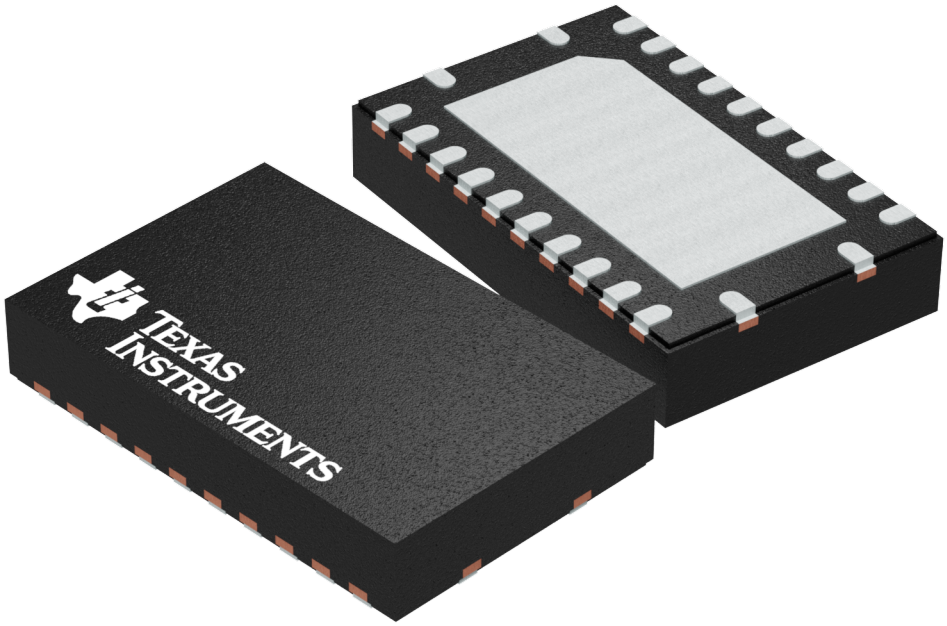
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXV0108QWRGYRQ1	VQFN	RGY	24	3000	367.0	367.0	35.0

RGY 24

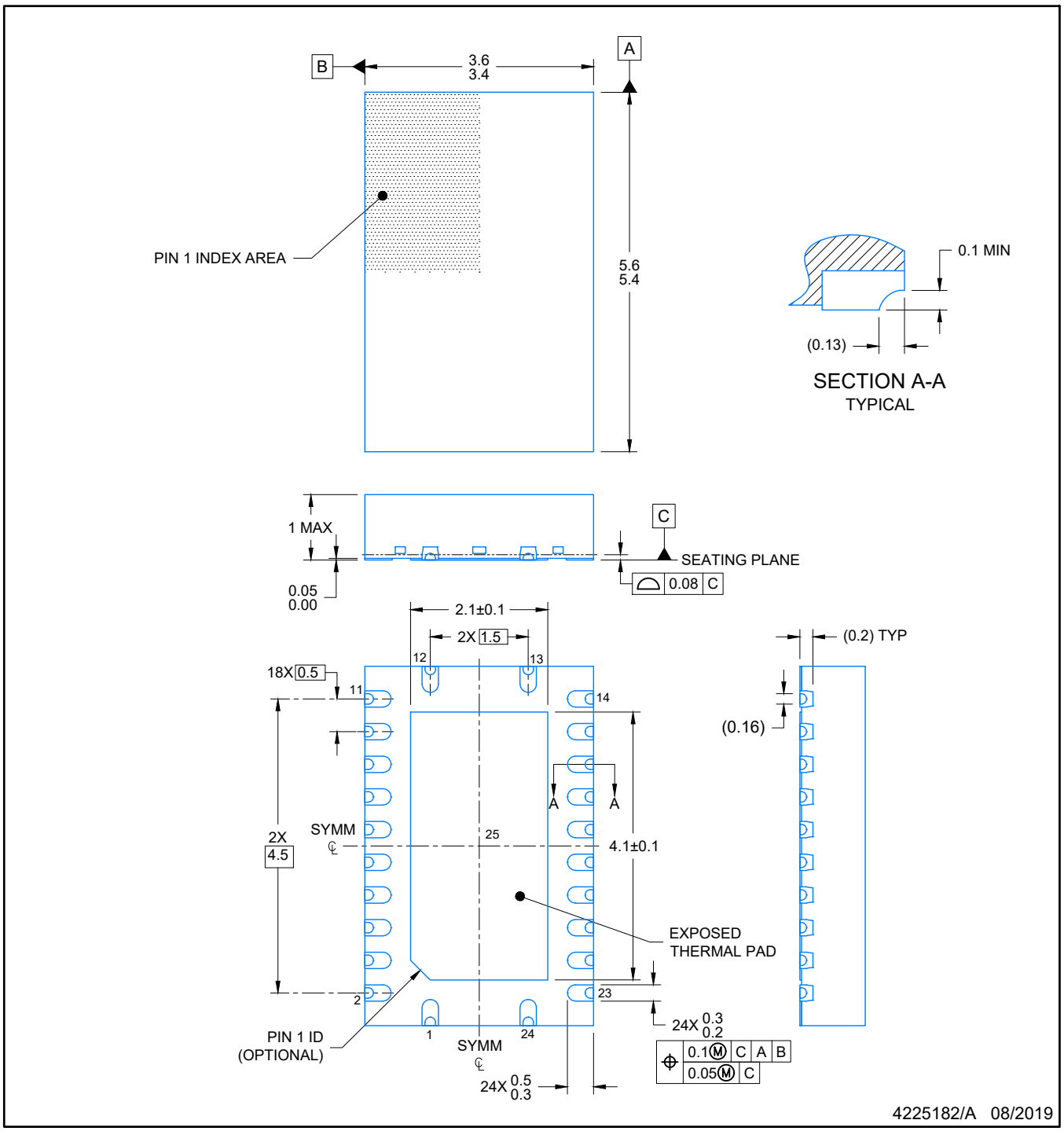
VQFN - 1 mm max height

5.5 x 3.5 mm, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

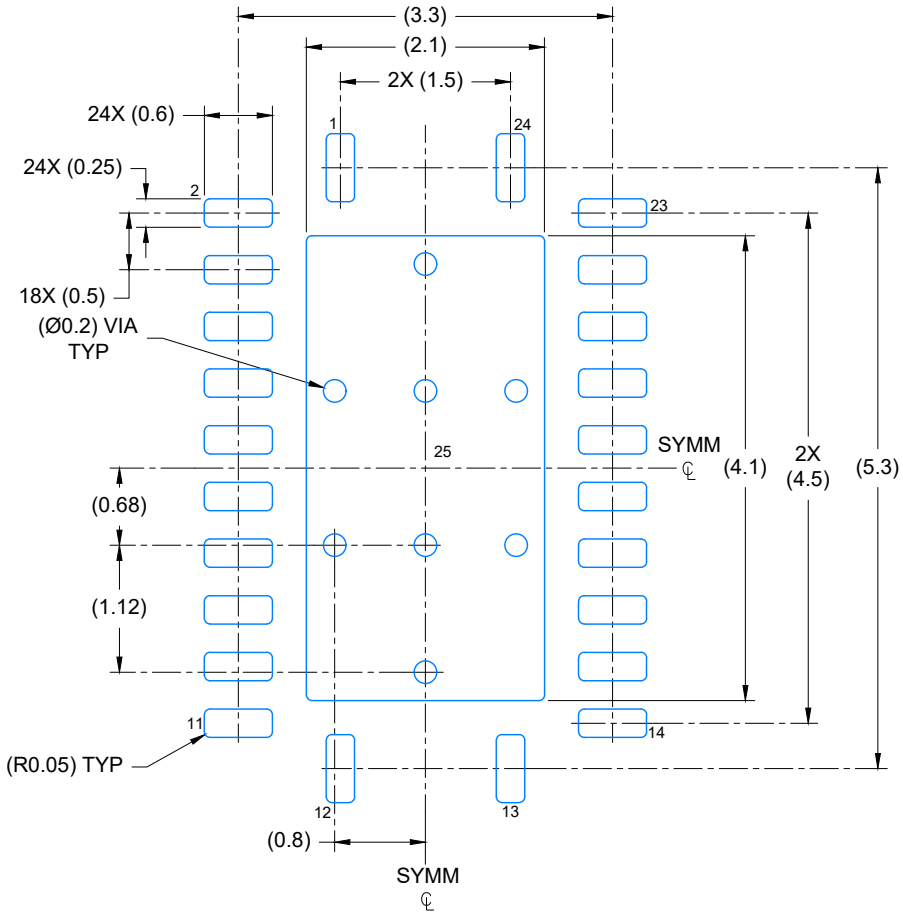


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

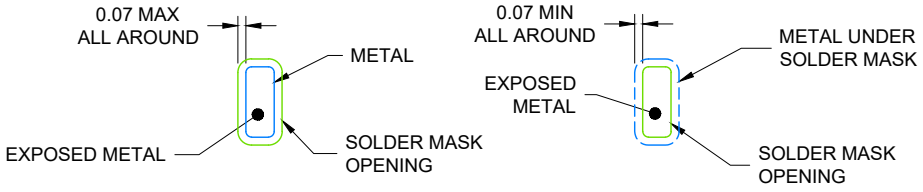


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



NON SOLDER MASK DEFINED (PREFERRED)

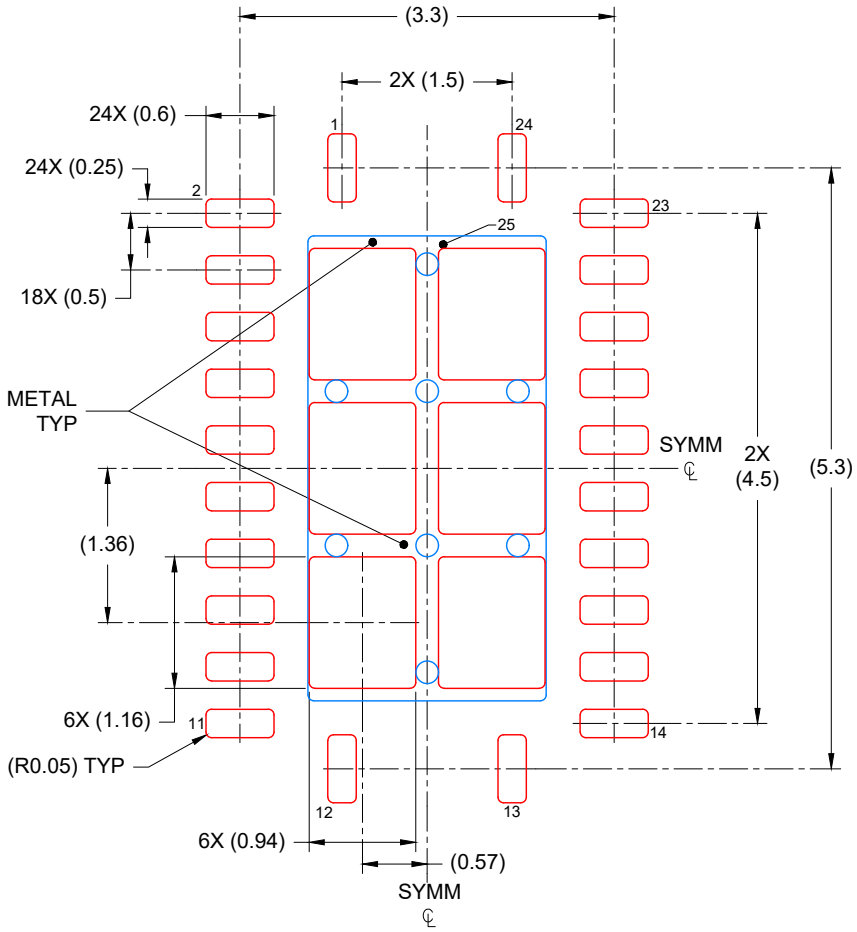
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4225182/A 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
76% PRINTED COVERAGE BY AREA
SCALE: 15X

4225182/A 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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